

To our customers,

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HAT2092R

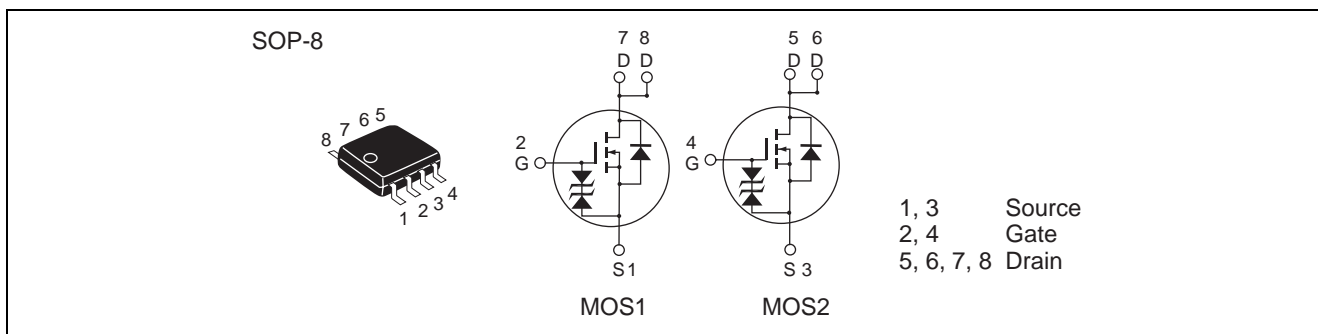
Silicon N Channel Power MOS FET High Speed Power Switching

REJ03G0511-0300
(Previous ADE-208-1236A(Z))
Rev.3.00
Jan.13.2005

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	11	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	88	A
Body-drain diode reverse drain current	I_{DR}	11	A
Channel dissipation	P_{ch} ^{Note2}	2	W
Channel dissipation	P_{ch} ^{Note3}	3	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1 \%$

2. 1 Drive operation: When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

3. 2 Drive operation: When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

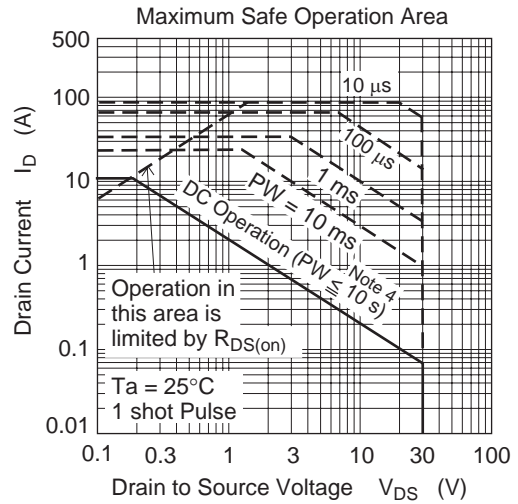
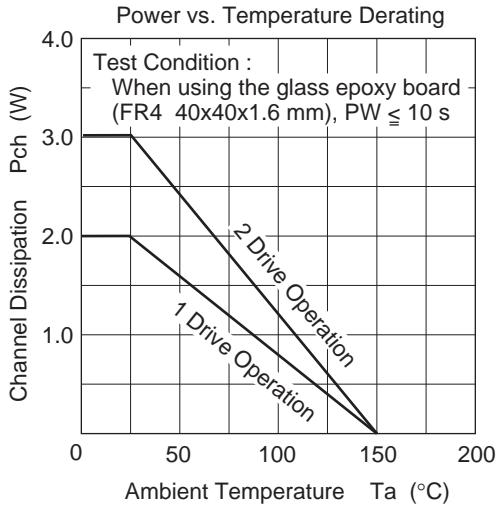
Electrical Characteristics

(Ta = 25°C)

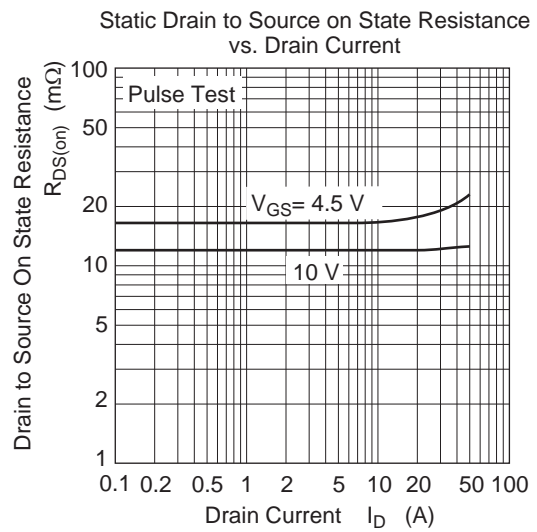
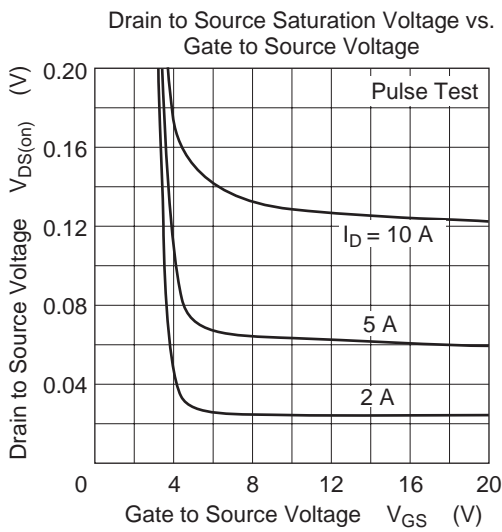
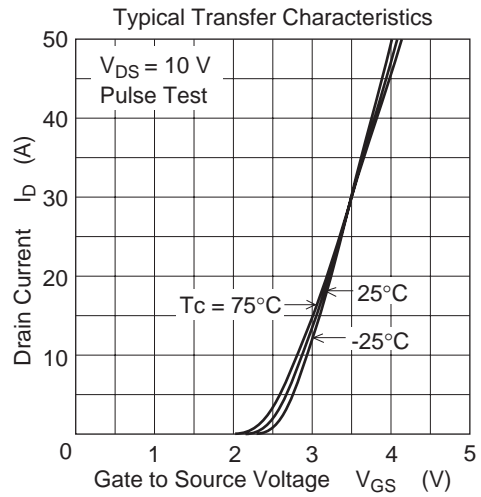
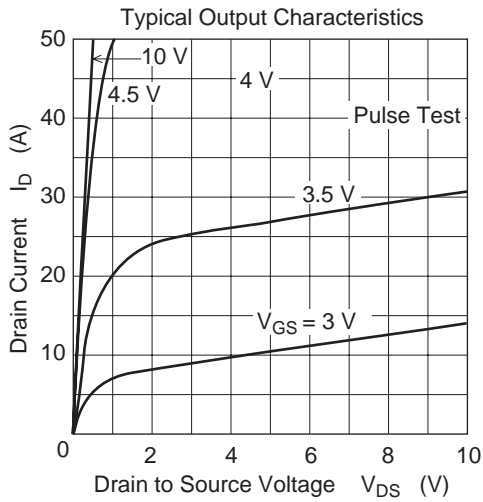
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	13	16	$\text{m}\Omega$	$I_D = 5.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	17	25	$\text{m}\Omega$	$I_D = 5.5 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	12	20	—	S	$I_D = 5.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1400	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	340	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	190	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	22	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	4	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	4	—	nc	$I_D = 11 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 5.5 \text{ A}$
Rise time	t_r	—	17	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	50	—	ns	$R_L = 1.83 \text{ }\Omega$
Fall time	t_f	—	9	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	V_{DF}	—	0.85	1.10	V	$I_F = 11 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = 11 \text{ A}$, $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

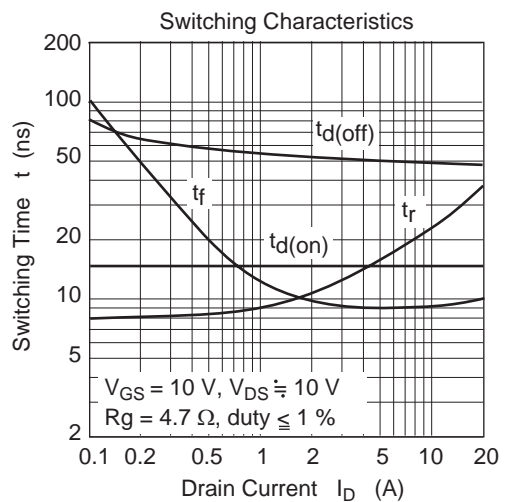
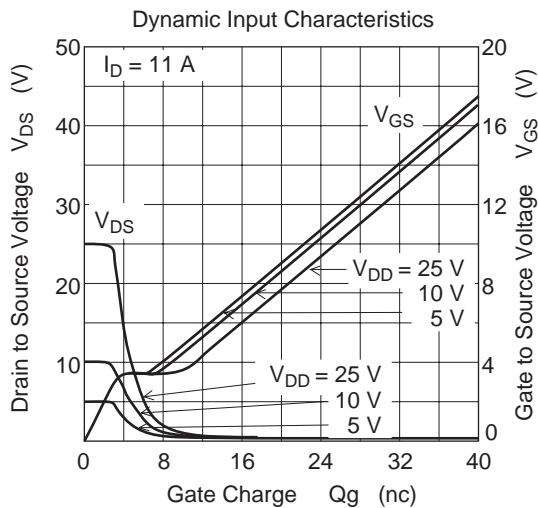
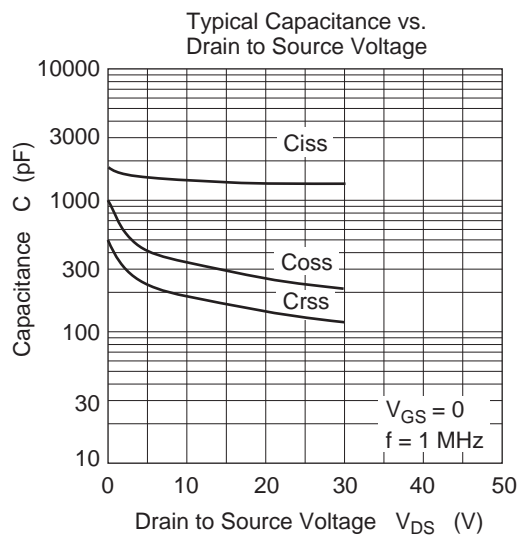
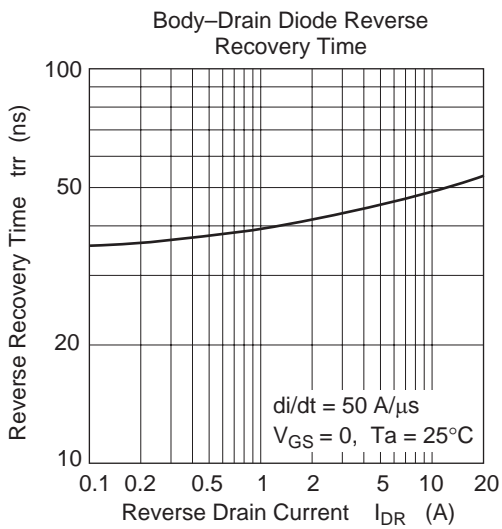
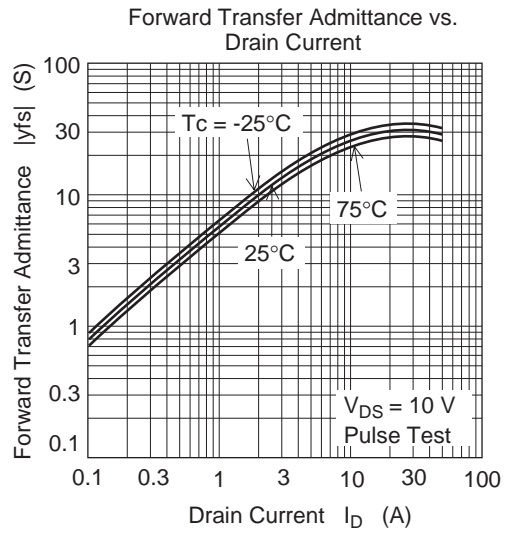
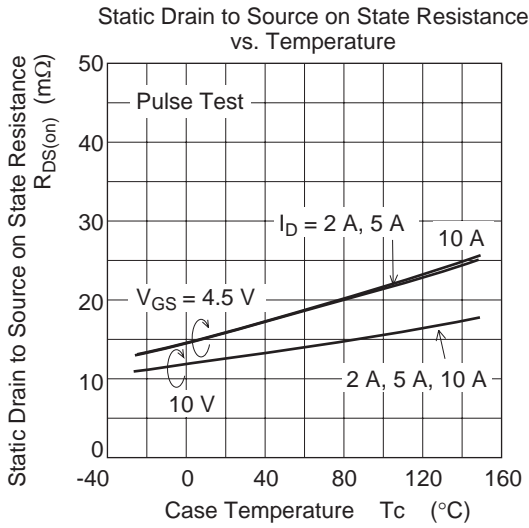
Note: 4. Pulse test

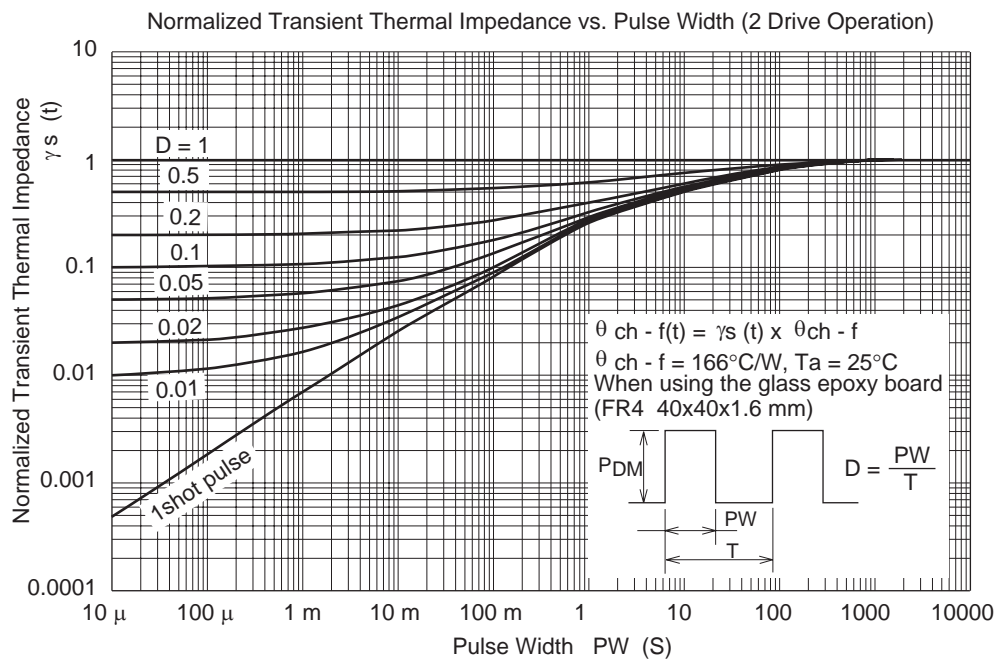
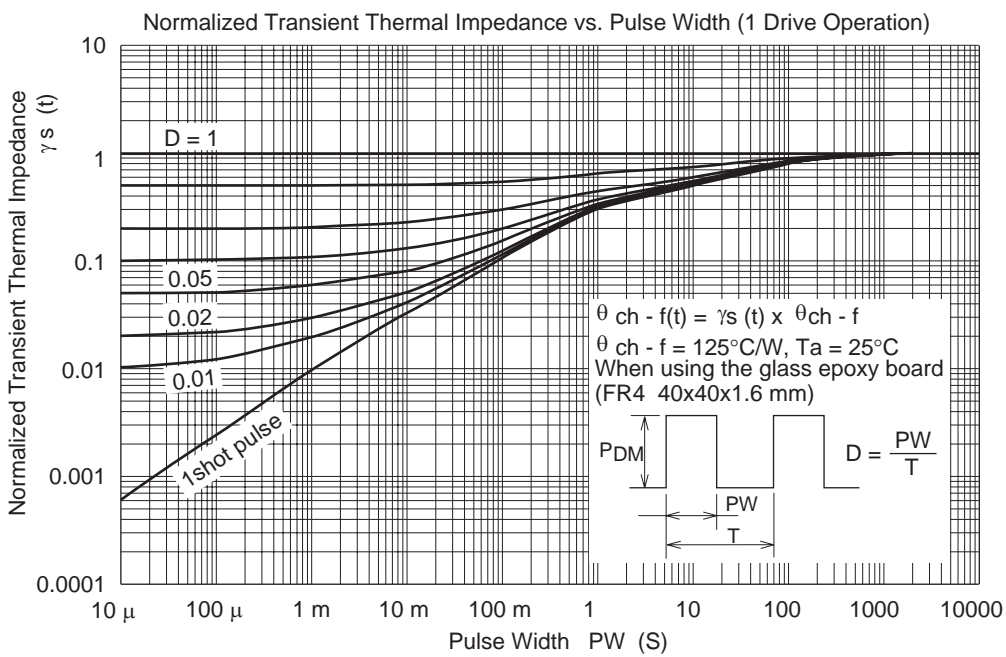
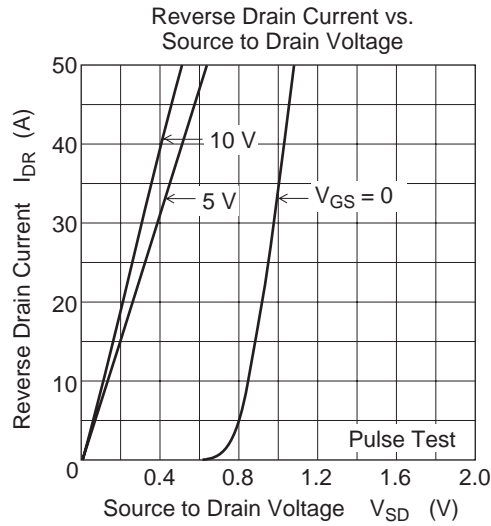
Main Characteristics

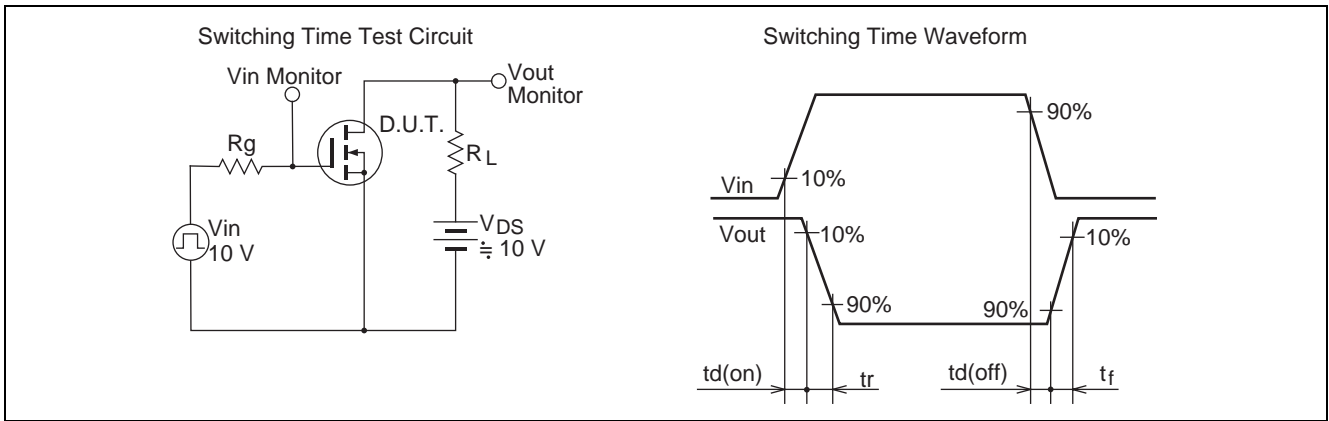


Note 4 :
When using the glass epoxy board (FR4 40x40x1.6 mm)



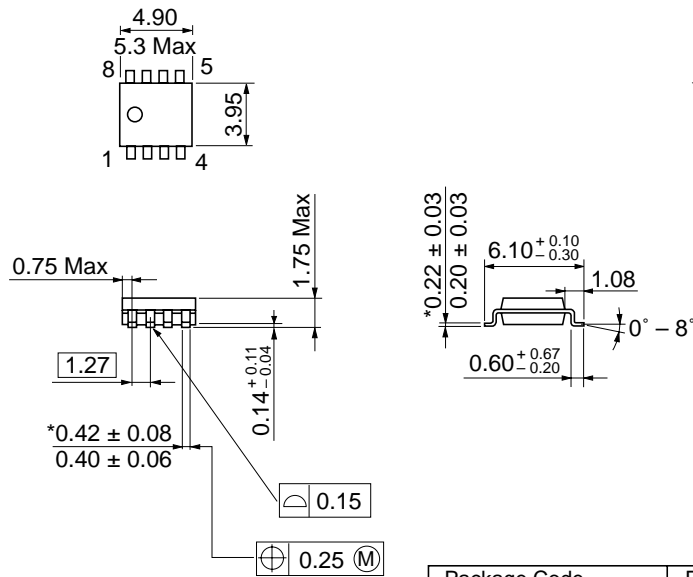






Package Dimensions

As of January, 2003
Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

Ordering Information

Part Name	Quantity	Shipping Container
HAT2092R-EL-E	2500 pcs	Taping
HAT2092RJ-EL-E	2500 pcs	Taping

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