



**THE DATASHEET OF  
HUFA75332S3ST**



**60A, 55V, 0.019 Ohm, N-Channel UltraFET Power MOSFETs**



These N-Channel power MOSFETs are manufactured using the innovative UltraFET® process. This advanced process technology

achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75332.

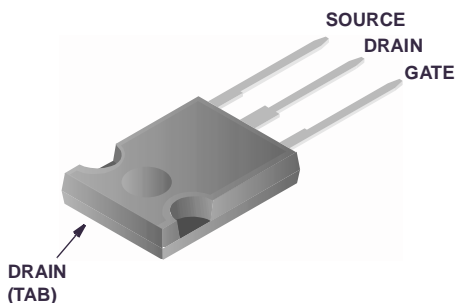
**Ordering Information**

PART NUMBER	PACKAGE	BRAND
HUFA75332G3	TO-247	75332G
HUFA75332P3	TO-220AB	75332P
HUFA75332S3S	TO-263AB	75332S

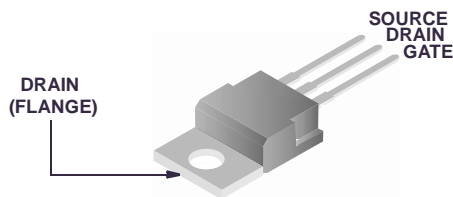
NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUFA75332S3ST.

**Packaging**

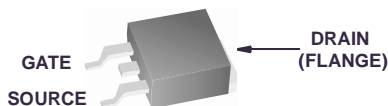
JEDEC STYLE TO-247



JEDEC TO-220AB



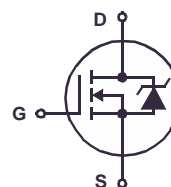
JEDEC TO-263AB



**Features**

- 60A, 55V
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Models
  - SPICE and SABER Thermal Impedance Models Available on the WEB at: [www.fairchildsemi.com](http://www.fairchildsemi.com)
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**



This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

# HUFA75332G3, HUFA75332P3, HUFA75332S3S

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$	55	V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	55	V
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20$	V
Drain Current			
Continuous (Figure 2) . . . . .	$I_D$	60	A
Pulsed Drain Current . . . . .	$I_{DM}$	Figure 4	
Pulsed Avalanche Rating . . . . .	$E_{AS}$	Figure 6	
Power Dissipation . . . . .	$P_D$	145	W
Derate Above $25^\circ\text{C}$ . . . . .		0.97	$\text{W}/^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
<b>OFF STATE SPECIFICATIONS</b>							
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 11)	55	-	-	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$	
		$V_{DS} = 45\text{V}, V_{GS} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	250	$\mu\text{A}$	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA	
<b>ON STATE SPECIFICATIONS</b>							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ (Figure 10)	2	-	4	V	
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 60\text{A}, V_{GS} = 10\text{V}$ (Figure 9)	-	0.016	0.019	$\Omega$	
<b>THERMAL SPECIFICATIONS</b>							
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	1.03	$^\circ\text{C}/\text{W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247	-	-	30	$^\circ\text{C}/\text{W}$	
		TO-220, TO-263	-	-	62	$^\circ\text{C}/\text{W}$	
<b>SWITCHING SPECIFICATIONS (<math>V_{GS} = 10\text{V}</math>)</b>							
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}, I_D \cong 60\text{A}, R_L = 0.50\Omega, V_{GS} = 10\text{V}, R_{GS} = 6.8\Omega$	-	-	100	ns	
Turn-On Delay Time	$t_{d(ON)}$		-	12	-	ns	
Rise Time	$t_r$		-	55	-	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	11	-	ns	
Fall Time	$t_f$		-	25	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	55	ns	
<b>GATE CHARGE SPECIFICATIONS</b>							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V}$ to $20\text{V}$	$V_{DD} = 30\text{V}, I_D \cong 60\text{A}, R_L = 0.50\Omega, I_{g(REF)} = 1.0\text{mA}$ (Figure 13)	-	70	85	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0\text{V}$ to $10\text{V}$		-	40	50	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to $2\text{V}$		-	2.5	3.0	nC
Gate to Source Gate Charge	$Q_{gs}$			-	6	-	nC
Reverse Transfer Capacitance	$Q_{gd}$			-	15	-	nC

# HUFA75332G3, HUFA75332P3, HUFA75332S3S

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>CAPACITANCE SPECIFICATIONS</b>						
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ (Figure 12)	-	1300	-	pF
Output Capacitance	$C_{OSS}$		-	480	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	115	-	pF

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 60\text{A}$	-	-	1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 60\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	75	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 60\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	140	nC

## Typical Performance Curves

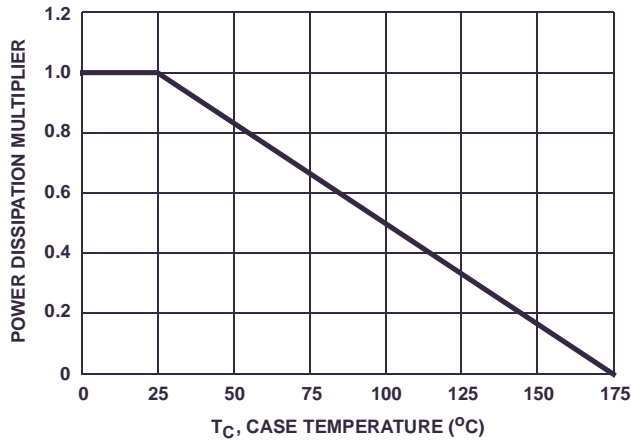


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

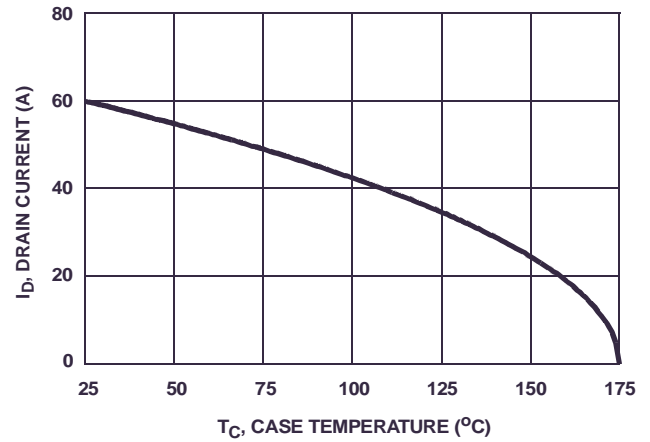


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

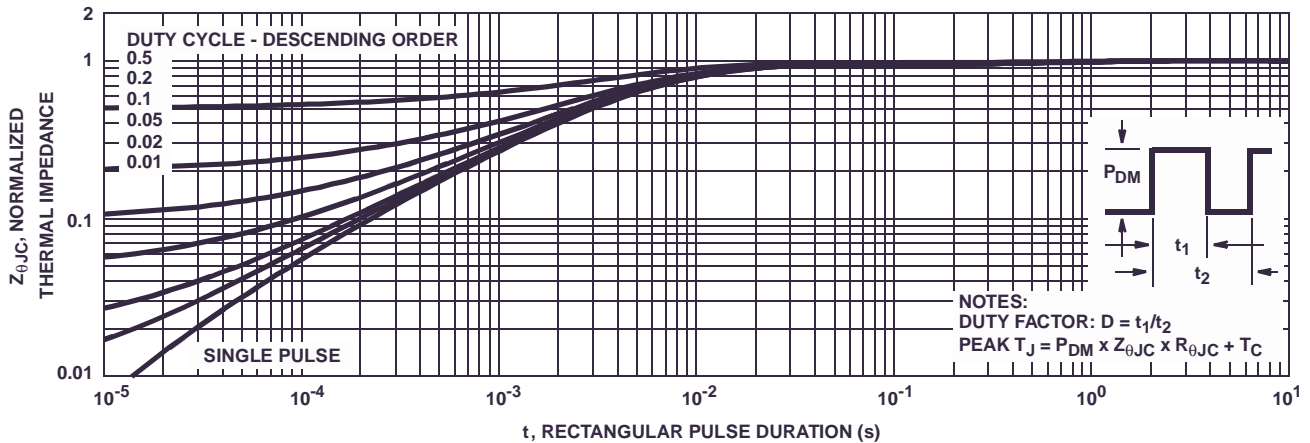


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (Continued)

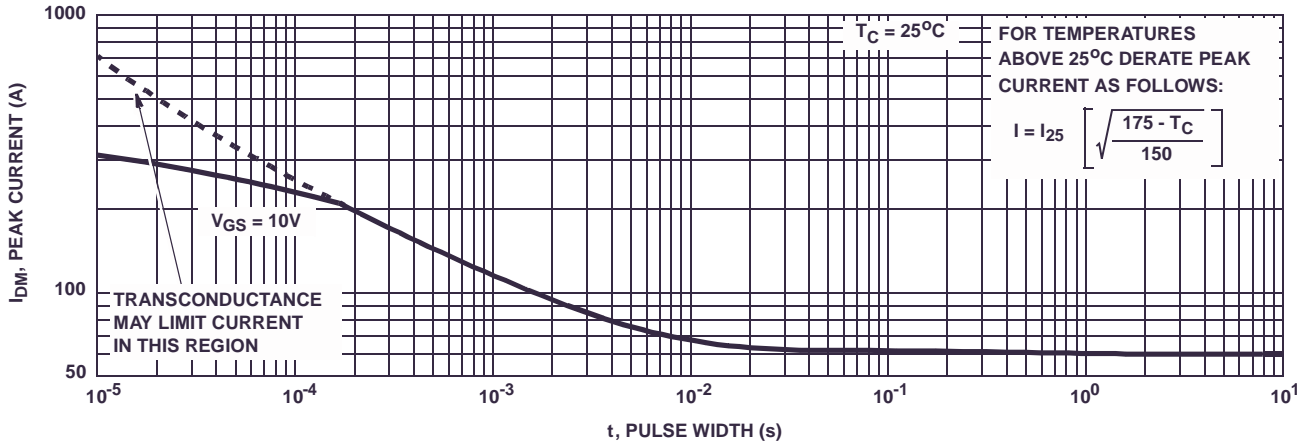


FIGURE 4. PEAK CURRENT CAPABILITY

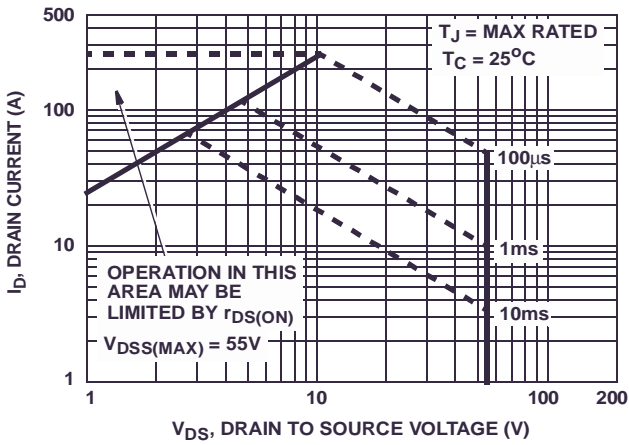
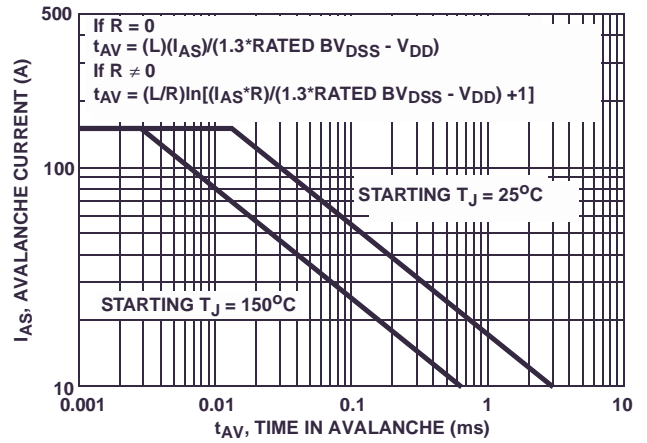


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.  
 FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

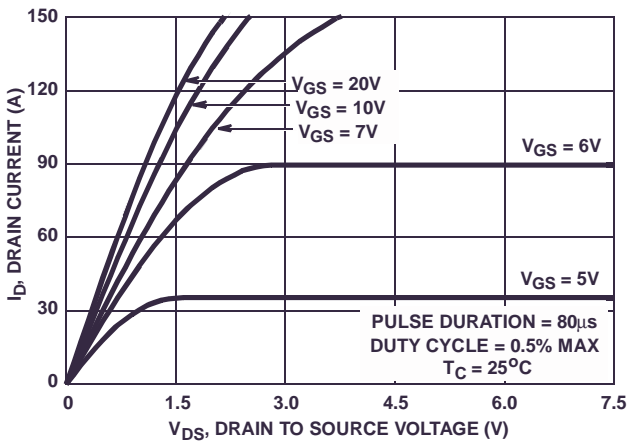


FIGURE 7. SATURATION CHARACTERISTICS

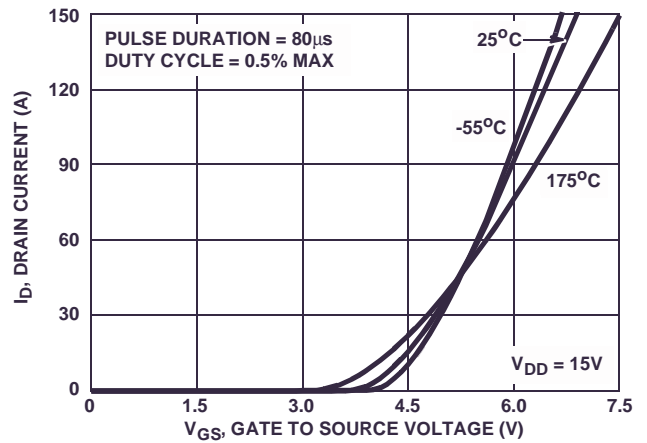


FIGURE 8. TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

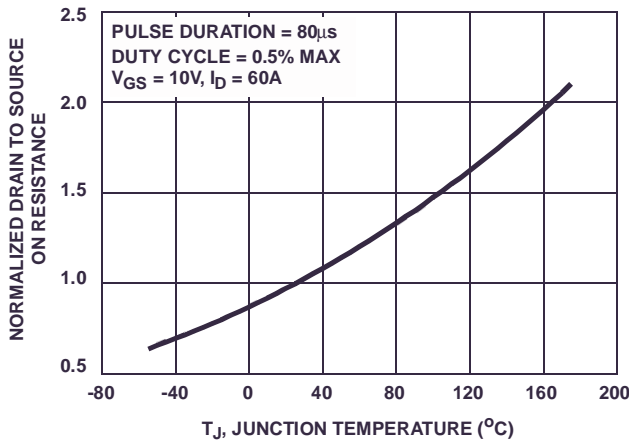


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

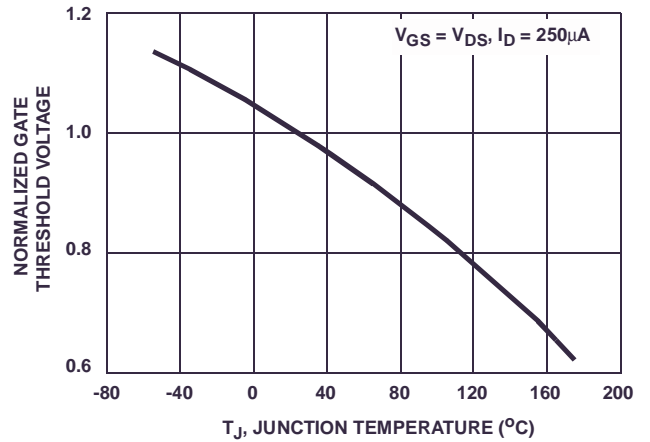


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

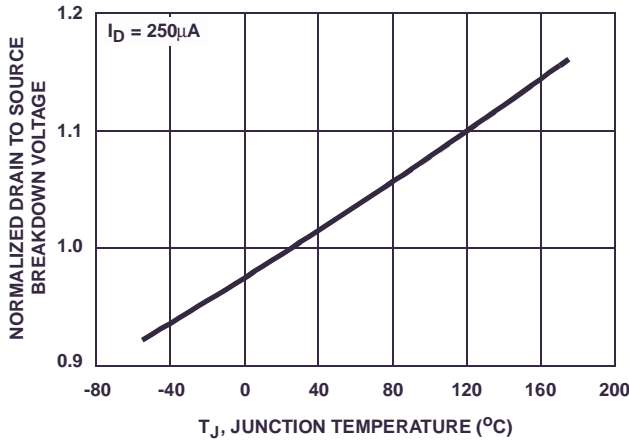


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

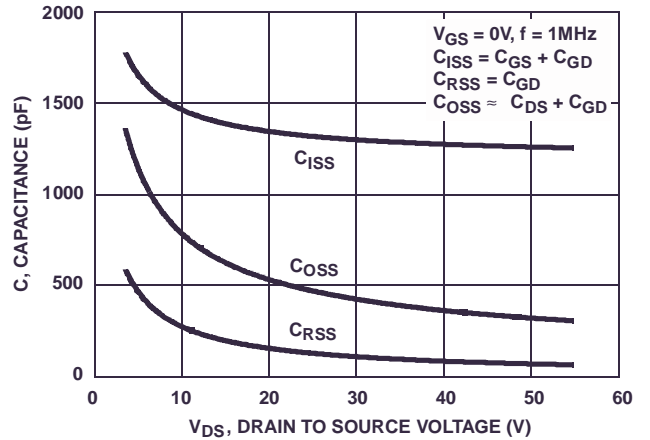
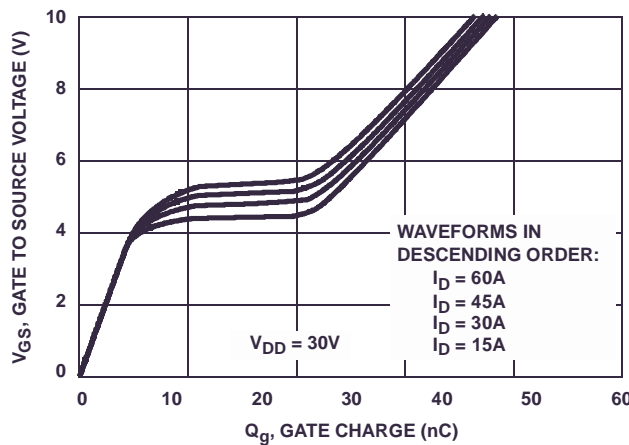


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

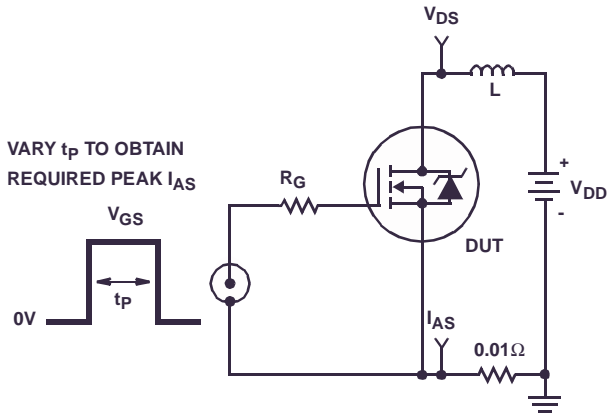


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

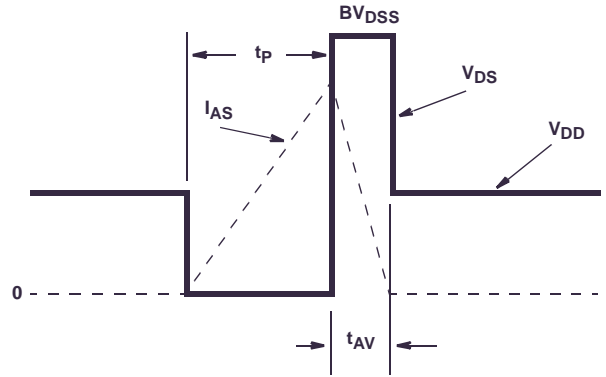


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

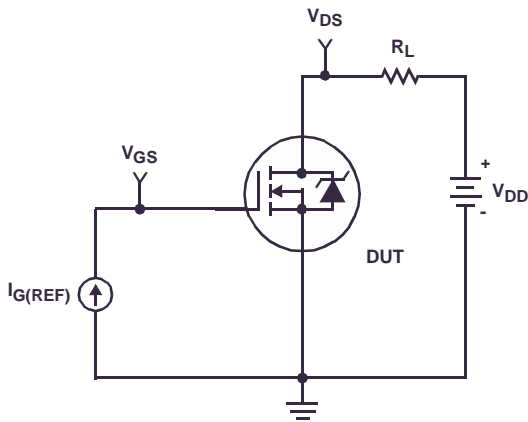


FIGURE 16. GATE CHARGE TEST CIRCUIT

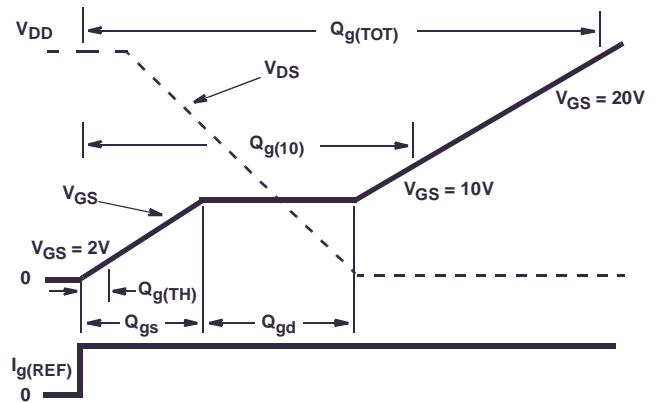


FIGURE 17. GATE CHARGE WAVEFORM

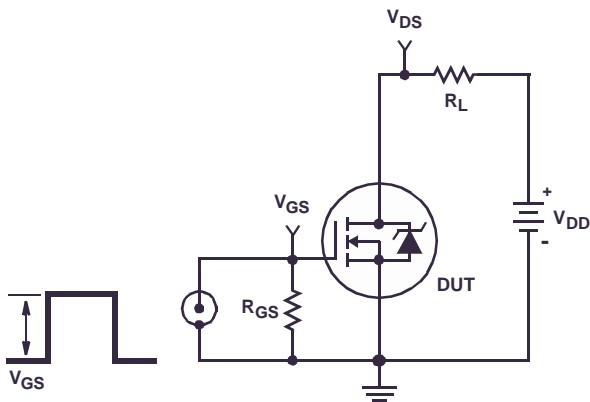


FIGURE 18. SWITCHING TIME TEST CIRCUIT

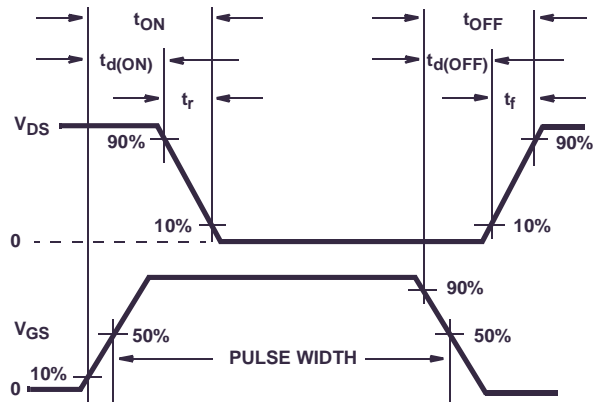


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

**PSPICE Electrical Model**

.SUBCKT HUFA75332 2 1 3 ; rev 18 June 2002

CA 12 8 1.8e-9  
 CB 15 14 1.73e-9  
 CIN 6 8 1.19e-9

DBODY 7 5 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 58.85  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 1e-9  
 LSOURCE 3 7 1e-9  
 K1 LSOURCE LGATE 0.0085

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 4.5e-3  
 RGATE 9 20 1.3  
 RLDRAIN 2 5 10  
 RLGATE 1 9 10  
 RLSOURCE 3 7 10  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 5.95e-3  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

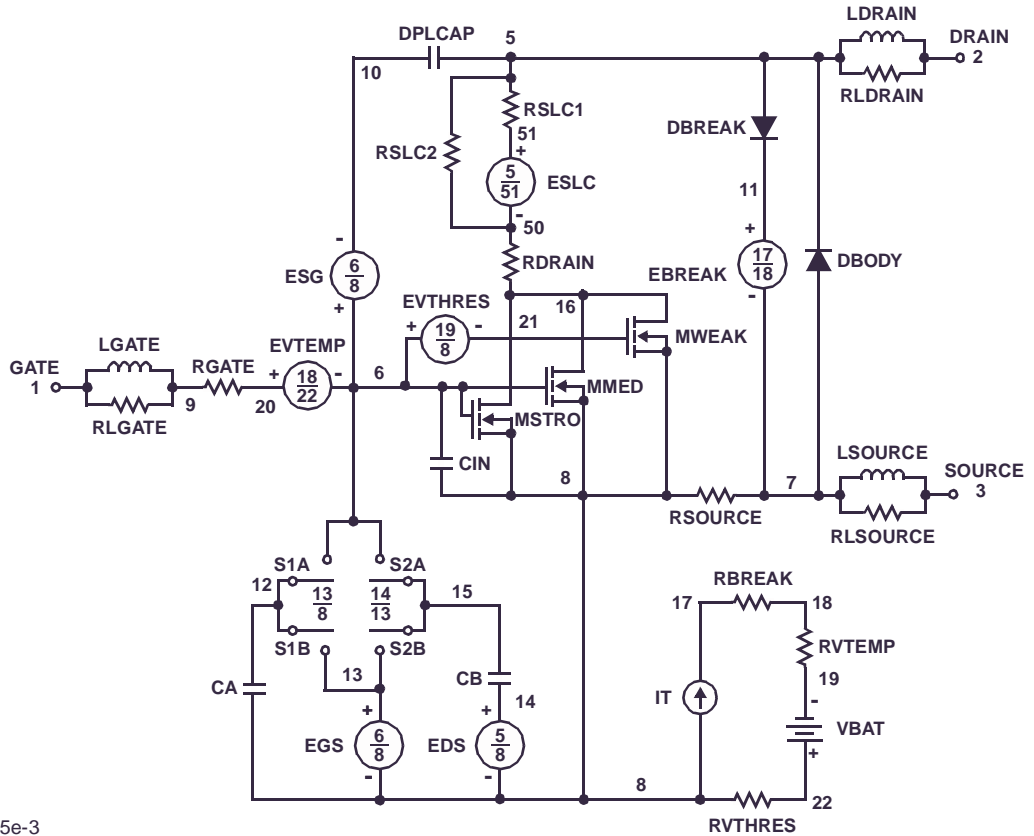
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*180),4.6))}

.MODEL DBODYMOD D (IS = 1.3e-12 RS = 3.0e-3 IKF = 20 XTI = 6 TRS1 = 2.7e-3 TRS2 = 7.0e-7 CJO = 1.7e-9 TT = 4.0e-8 M = 0.45 vj = 0.75)  
 .MODEL DBREAKMOD D (RS = 1.71e-2 IKF = 1.0e-5 TRS1 = -4.0e-4 TRS2 = -1.55e-5)  
 .MODEL DPLCAPMOD D (CJO = 1.8e-9 IS = 1e-30 N = 1 M = 0.9 vj = 1.45)  
 .MODEL MMEDMOD NMOS (VTO = 3.183 KP = 2 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.3)  
 .MODEL MSTROMOD NMOS (VTO = 3.66 KP = 51.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL MWEAKMOD NMOS (VTO = 2.703 KP = 0.008 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 13)  
 .MODEL RBREAKMOD RES (TC1 = 1.05e-3 TC2 = 4.5e-7)  
 .MODEL RDRAINMOD RES (TC1 = 1.16e-2 TC2 = 1.7e-5)  
 .MODEL RSLCMOD RES (TC1 = 3.96e-3 TC2 = 2.7e-6)  
 .MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-5)  
 .MODEL RVTHRESMOD RES (TC1 = -2.8e-3 TC2 = -1.0e-5)  
 .MODEL RVTEMPMOD RES (TC1 = -2.75e-3 TC2 = 5.0e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -8 VOFF = -3)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3 VOFF = -8)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0 VOFF = 0.5)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = 0)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.





**SPICE Thermal Model**

REV 18June 2002

HUFA75332

CTHERM1 th 6 4.00e-3  
 CHERM2 6 5 7.00e-3  
 CHERM3 5 4 7.50e-3  
 CHERM4 4 3 8.00e-3  
 CHERM5 3 2 1.85e-2  
 CHERM6 2 tl 12.55

RHERM1 th 6 7.09e-3  
 RHERM2 6 5 1.77e-2  
 RHERM3 5 4 4.97e-2  
 RHERM4 4 3 2.79e-1  
 RHERM5 3 2 4.21e-1  
 RHERM6 2 tl 5.58e-2

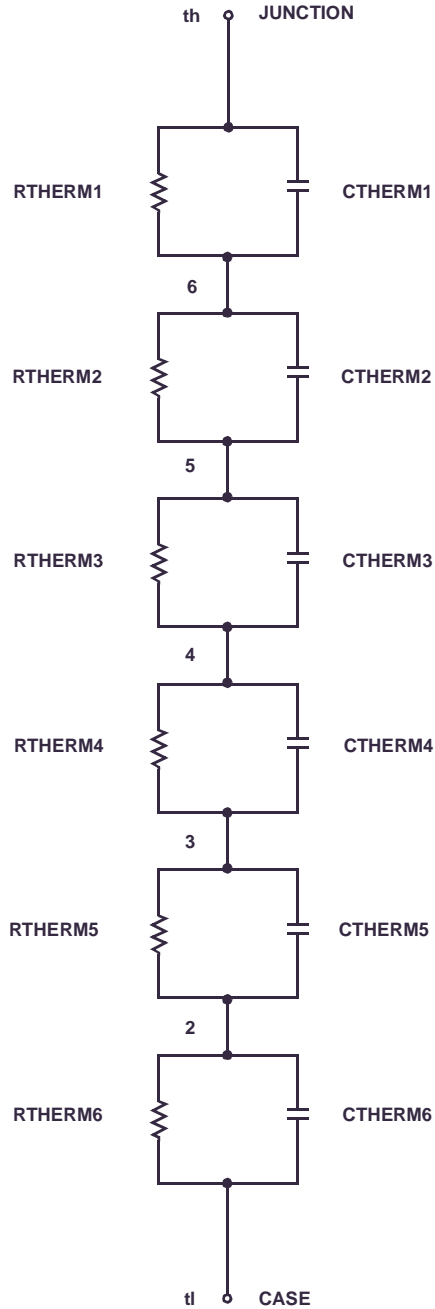
**SABER Thermal Model**

SABER thermal model HUFA75332

```

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thermal_c th, tl
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ctherm.ctherm1 th 6 = 4.00e-3
ctherm.ctherm2 6 5 = 7.00e-3
ctherm.ctherm3 5 4 = 7.50e-3
ctherm.ctherm4 4 3 = 8.00e-3
ctherm.ctherm5 3 2 = 1.85e-2
ctherm.ctherm6 2 tl = 12.55

rtherm.rtherm1 th 6 = 7.09e-3
rtherm.rtherm2 6 5 = 1.77e-2
rtherm.rtherm3 5 4 = 4.97e-2
rtherm.rtherm4 4 3 = 2.79e-1
rtherm.rtherm5 3 2 = 4.21e-1
rtherm.rtherm6 2 tl = 5.58e-2
}
    
```



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ACE <sub>x</sub> <sup>™</sup>	FAST <sub>r</sub> <sup>™</sup>	OPTOLOGIC <sup>®</sup>	SMART START <sup>™</sup>	VCX <sup>™</sup>
Bottomless <sup>™</sup>	FRFET <sup>™</sup>	OPTOPLANAR <sup>™</sup>	SPM <sup>™</sup>	
CoolFET <sup>™</sup>	GlobalOptoisolator <sup>™</sup>	PACMAN <sup>™</sup>	Stealth <sup>™</sup>	
CROSSVOLT <sup>™</sup>	GTO <sup>™</sup>	POP <sup>™</sup>	SuperSOT <sup>™</sup> -3	
DOME <sup>™</sup>	HiSeC <sup>™</sup>	Power247 <sup>™</sup>	SuperSOT <sup>™</sup> -6	
EcoSPARK <sup>™</sup>	I <sup>2</sup> C <sup>™</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>™</sup> -8	
E <sup>2</sup> CMOS <sup>™</sup>	ISOPLANAR <sup>™</sup>	QFET <sup>™</sup>	SyncFET <sup>™</sup>	
EnSigna <sup>™</sup>	LittleFET <sup>™</sup>	QST <sup>™</sup>	TinyLogic <sup>™</sup>	
FACT <sup>™</sup>	MicroFET <sup>™</sup>	QT Optoelectronics <sup>™</sup>	TruTranslation <sup>™</sup>	
FACT Quiet Series <sup>™</sup>	MicroPak <sup>™</sup>	Quiet Series <sup>™</sup>	UHC <sup>™</sup>	
FAST <sup>®</sup>	MICROWIRE <sup>™</sup>	SILENT SWITCHER <sup>®</sup>	UltraFET <sup>®</sup>	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management