THE DATASHEET OF

HVDA553QDRQ1

HVDA55x-Q1 5-V CAN Transceiver With I/O Level Adapting and Low-Power-Mode Supply Optimization

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level:
    - Level 3B for Pins 6 and 7
    - Level 3A for All Other Pins
  - Device CDM ESD Classification Level C6
- Meets or Exceeds the Requirements of ISO 11898-2 and ISO 11898-5
- GIFT/ICT Compliant
- Data Rate Up to 1 Mbps
- ESD Protection Up to ±12 kV (Human-Body Model) on Bus Pins
- I/O Voltage Level Adapting
  - HVDA551: Adaptable I/O Voltage Range (V_{IO}) From 3 V to 5.33 V
- SPLIT Voltage Source
  - HVDA553: Common-Mode Bus Stabilization
- Operating Modes:
  - Normal Mode
  - Low-Power Standby Mode With RXD Wake-Up Request
- High Electromagnetic Compliance (EMC)
- Supports CAN Flexible Data-Rate (FD)
- Protection
  - Undervoltage Protection on V_{IO} and V_{CC}
  - Bus-Fault Protection of –27 V to 40 V
  - TXD Dominant State Time-Out
  - RXD Wake-Up Request Lockout on CAN Bus Stuck Dominant Fault (HVDA551)
  - Digital Inputs Compatible With 5-V Microprocessors (HVDA553)
  - Thermal Shutdown Protection
  - Power-Up and Power-Down Glitch-Free Bus I/O
  - High Bus Input Impedance When Unpowered (No Bus Load)

2 Applications

- SAE J2284 High-Speed CAN for Automotive Applications
- SAE J1939 Standard Data Bus Interface
- GMW3122 Dual-Wire CAN Physical Layers
- ISO 11783 Standard Data Bus Interface
- NMEA 2000 Standard Data Bus Interface

3 Description

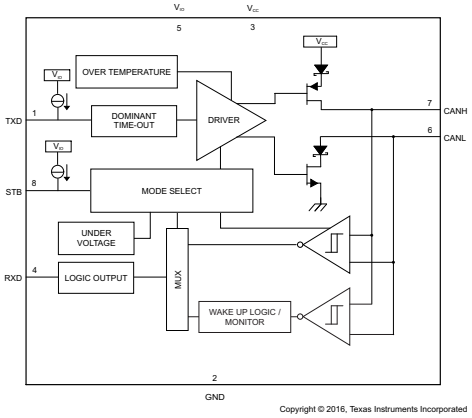
The HVDA55x-Q1 device is designed and qualified for use in automotive applications and meets or exceeds the specifications of the ISO 11898 High Speed CAN (Controller Area Network) Physical Layer standard (transceiver).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
HVDA551-Q1 HVDA553-Q1	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

HVDA551 Block Diagram



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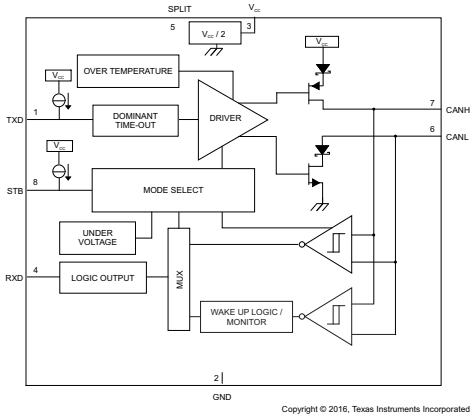
HVDA553 Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2013) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed *Ordering Information* table, see POA at the end of the data sheet ... 1

Changes from Original (June 2013) to Revision A **Page**

- In *Electrical Characteristics* rows 6.3 and 6.7, changed ® to (R) ... 6

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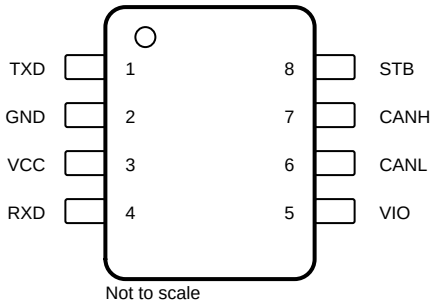
5 Pin Configuration and Functions

HVDA551 D Package
8-Pin SOIC
Top View



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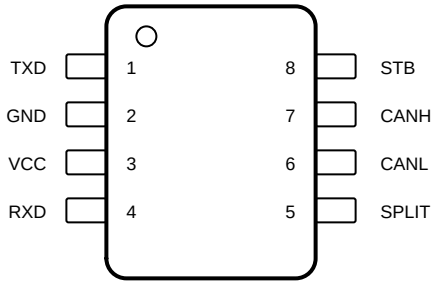
HVDA553 D Package
8-Pin SOIC
Top View



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Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	TXD	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
2	GND	G	Ground connection
3	V_{CC}	P	Transceiver 5-V supply voltage
4	RXD	O	CAN receive data output (low in dominant bus state, high in recessive bus state)
5	V_{IO} (HVDA551)	P/O	Transceiver logic level (IO) supply voltage
	SPLIT (HVDA553)	P/O	Common-mode stabilization output
6	CANL	I/O	Low level CAN bus line
7	CANH	I/O	High level CAN bus line
8	STB	I	Standby mode select pin (active high)

(1) G = Ground, I = Input, O = Output, and P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.3	6	V
V_{IO}	I/O supply voltage		–0.3	6	V
	Voltage at bus terminals (CANH, CANL)		–27	40	V
I_O	Receiver output current (RXD)			20	mA
V_I	Voltage input (TXD, STB, S)	HVDA55x	–0.3	6 and $V_I \le V_{IO} + 0.3$	V
		HVDA553	–0.3	6	
T_J	Operating virtual-junction temperature		–40	150	°C
T_{stg}	Storage temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to the ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)	All pins except 6 and 7	±4000	V
			Pins 6 and 7(2)	±12000	
		Charged-device model (CDM)(3)		±1000	
		IEC 61000-4-2 according to IBEE CAN EMC test specification(4)	Pins 6, 7 to 2	±7000	
		ISO 7637 transients according to IBEE CAN EMC test specification(5)	Pulse 1	–100	
			Pulse 2a	75	
			Pulse 3a	–150	
			Pulse 3b	100	

(1) HBM tested in accordance with AEC-Q100-002.
(2) HBM test method based on AEC-Q100-002, CANH and CANL bus pins stressed with respect to each other and GND.
(3) CDM tested in accordance with AEC-Q100-011.
(4) IEC 61000-4-2 is a system-level ESD test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system-level configurations lead to different results.
(5) ISO 7637 is a system level transient test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system level configurations lead to different results.

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6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.68	5.33	V
V_{IO}	I/O supply voltage	3	5.33	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)	–12	12	V
V_{IH}	High-level input voltage, TXD, STB (for HVD553, $V_{IO} = V_{CC}$)	0.7 × V_{IO}	V_{IO}	V
V_{IL}	Low-level input voltage, TXD, STB (for HVD553, $V_{IO} = V_{CC}$)	0	0.3 × V_{IO}	V
V_{ID}	Differential input voltage, bus (between CANH and CANL)	–6	6	V
I_{OH}	High-level output current, RXD	–2		mA
I_{OL}	Low-level output current, RXD		2	mA
T_A	Operating ambient free-air temperature (see *Thermal Information*)	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)			HVDA55x-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K thermal resistance	140	°C/W
		High-K thermal resistance	112	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		50	°C/W
ψ_{JT}	Junction-to-top characterization parameter		13	°C/W
ψ_{JB}	Junction-to-board characterization parameter		55	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, HVDA553 $V_{IO} = V_{CC}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
HVDA551 SUPPLY						
I_{CC}	5-V supply current	Standby mode (HVDA551 only), STB at V_{IO}, V_{CC} = 5.33 V, V_{IO} = 3 V, TXD at V_{IO} (2)			5	µA
		Normal mode (dominant), TXD at 0 V, 60-Ω load, STB at 0 V		50	70	mA
		Normal mode (recessive), TXD at V_{IO}, no load, STB at 0 V		6.75	10	
I_{IO}	I/O supply current	Standby mode (HVDA551 only), STB at V_{IO} , V_{CC} = 5.33 V or 0 V, RXD floating, TXD at V_{IO}, T_A = –40°C, 25°C, 125°C(3)		6.5	15	µA
		Normal mode (dominant), V_{CC} = 5.33 V, RXD floating, TXD at 0 V		85	300	
		Normal mode (recessive), V_{CC} = 5.33 V, RXD floating, TXD at V_{IO}		70	300	
UV_{VCC}	Undervoltage detection	On V_{CC} for forced standby mode	3.2	3.6	4	V
$V_{HYS(UVVCC)}$	Hysteresis voltage	For undervoltage detection on UV_{VCC} for standby mode		200		mV
UV_{VIO}	Undervoltage detection	On V_{IO} for forced standby mode	1.9	2.45	2.95	V
$V_{HYS(UVVIO)}$	Hysteresis voltage	For undervoltage detection on UV_{VIO} for forced standby mode		130		mV

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{IO} = 3.3 V.
(2) The V_{CC} supply is not required during standby mode so in the application I_{CC} in standby mode may be zero. If the V_{CC} supply remains, then I_{CC} is per specification with V_{CC}.
(3) See *I_{IO} Quiescent Current in Standby / Silent Mode*.

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Electrical Characteristics (continued)

T_J = –40°C to 150°C, HVDA553 V_{IO} = V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
HVDA553 SUPPLY						
I_{CC}	5-V supply current	Standby mode (HVDA553 only), STB at V_{CC}, V_{CC} = 5.33 V, TXD at V_{CC}(2)			12	µA
		Normal mode (dominant), TXD at 0 V, 60-Ω load, STB at 0 V		50	70	mA
		Normal mode (recessive), TXD at V_{CC}, no load, STB at 0 V		6.75	10	mA
UV_{VCC}	Undervoltage detection	On V_{CC} for forced standby mode	3.2	3.6	4	V
$V_{HYS(UVVCC)}$	Hysteresis voltage	For undervoltage detection on UV_{VCC} for standby mode		200		mV
DRIVER						
$V_{O(D)}$	Bus output voltage (dominant)	CANH, V_I = 0 V, STB at 0 V, R_L = 60 Ω, see Figure 2 and Figure 16	2.9		4.5	V
		CANL, V_I = 0 V, STB at 0 V, R_L = 60 Ω, see Figure 2 and Figure 16	0.8		1.75	V
$V_{O(R)}$	Bus output voltage (recessive)	V_I = V_{IO}, V_{IO} = 3 V, STB at 0 V, R_L = 60 Ω, see Figure 2 and Figure 16	2	2.5	3	V
$V_{O(STBY)}$	Bus output voltage	Standby mode (HVDA551 only), STB at V_{IO}, R_L = 60 Ω, see Figure 2 and Figure 16	–0.1		0.1	V
$V_{OD(D)}$	Differential output voltage (dominant)	V_I = 0 V, R_L = 60 Ω, STB at 0 V, see Figure 2, Figure 16, and Figure 3	1.5		3	V
		V_I = 0 V, R_L = 45 Ω, STB at 0 V, see Figure 2, Figure 16, and Figure 3	1.4		3	V
$V_{OD(R)}$	Differential output voltage (recessive)	V_I = 3 V, STB at 0 V, R_L = 60 Ω, see Figure 2 and Figure 16	–0.012		0.012	V
		V_I = 3 V, STB at 0 V, no load	–0.5		0.05	V
V_{SYM}	Output symmetry (dominant or recessive)	$V_{O(CANH)}$ + $V_{O(CANL)}$, STB at 0 V, R_L = 60 Ω, see Figure 12	0.9 × V_{CC}	V_{CC}	1.1 × V_{CC}	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	STB at 0 V, R_L = 60 Ω, see Figure 8	2	2.5	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	STB at 0 V, R_L = 60 Ω, see Figure 8		50		mV
$I_{OS(SS)_DOM}$	Short-circuit steady-state output current, dominant	V_{CANH} = 0 V, CANL open, TXD = low, see Figure 11	–100			mA
		V_{CANL} = 32 V, CANH open, TXD = low, see Figure 11			100	mA
$I_{OS(SS)_REC}$	Short-circuit steady-state output current, recessive	–20 V ≤ V_{CANH} ≤ 32 V, CANL open, TXD = high, see Figure 11	–10		10	mA
		–20 V ≤ V_{CANL} ≤ 32 V, CANH open, TXD = high, see Figure 11	–10		10	mA
C_O	Output capacitance	See receiver input capacitance				
RECEIVER						
V_{IT+}	Positive-going input threshold voltage	Normal mode, STB at 0 V, see Table 1		800	900	mV
$V_{IT–}$	Negative-going input threshold voltage	Normal mode, STB at 0 V, see Table 1	500	650		mV
V_{hys}	Hysteresis voltage	V_{IT+} – $V_{IT–}$		125		mV
$V_{IT(STBY)}$	Input threshold voltage	HVDA551 only, standby mode, STB at V_{IO}	400		1150	mV
$I_{I(OFF_LKG)}$	Power-off (unpowered) bus input leakage current	CANH = CANL = 5 V, V_{CC} at 0 V, V_{IO} at 0 V, TXD at 0 V			3	µA

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Electrical Characteristics (continued)

T_J = –40°C to 150°C, HVDA553 V_{IO} = V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
C_I	Input capacitance to ground (CANH or CANL)	HVDA551: TXD at V_{IO}, V_{IO} at 3.3 V; HVDA553: TXD at V_{CC}, V_I = 0.4 sin (4E6πt) + 2.5 V		13		pF
C_{ID}	Differential input capacitance	HVDA551: TXD at V_{IO}, V_{IO} at 3.3 V; HVDA553: TXD at V_{CC}, V_I = 0.4 sin(4E6πt)		5		pF
R_{ID}	Differential input resistance	HVDA551: TXD at V_{IO}, V_{IO} = 3.3 V, STB at 0 V; HVDA553: TXD at V_{CC}, STB at 0 V	29		80	kΩ
R_{IN}	Input resistance (CANH or CANL)	HVDA551: TXD at V_{IO}, V_{IO} = 3.3 V, STB at 0 V; HVDA553: TXD at V_{CC}, STB at 0 V	14.5	25	40	kΩ
$R_{I(M)}$	Input resistance matching	$[1 – R_{IN(CANH)} / R_{IN(CANL)})] \times 100\%$, $V_{(CANH)} = V_{(CANL)}$	–3%	0%	3%	
TXD PIN						
V_{IH}	High-level input voltage	HVD553: V_{IO} = V_{CC}	0.7 × V_{IO}			V
V_{IL}	Low-level input voltage	HVD553: V_{IO} = V_{CC}			0.3 × V_{IO}	V
I_{IH}	High-level input current	HVDA551: TXD at V_{IO}; HVDA553: TXD at V_{CC}	–2		2	µA
I_{IL}	Low-level input current	TXD at 0 V	–100		–7	µA
RXD PIN						
V_{OH}	High-level output voltage	HVD553: V_{IO} = V_{CC}, I_O = –2 mA, see Figure 6	0.8 × V_{IO}			V
V_{OL}	Low-level output voltage	HVD553: V_{IO} = V_{CC}, I_O = 2 mA, see Figure 6			0.2 × V_{IO}	V
STB PIN						
V_{IH}	High-level input voltage	HVD553: V_{IO} = V_{CC}	0.7 × V_{IO}			V
V_{IL}	Low-level input voltage	HVD553: V_{IO} = V_{CC}			0.3 × V_{IO}	V
I_{IH}	High-level input current	HVDA551: STB at V_{IO}; HVDA553: STB at V_{CC}	–2		2	µA
I_{IL}	Low-level input current	STB at 0 V	–20			µA
SPLIT PIN (HVDA553 ONLY)						
V_O	Output voltage	–500 µA < I_O < 500 µA	0.3 × V_{CC}	0.5 × V_{CC}	0.7 × V_{CC}	V
$I_{O(STB)}$	Leakage current	Standby mode, STB at V_{CC}, –12 V ≤ I_O ≤ 12 V	–5		5	µA
POWER DISSIPATION AND THERMAL SHUTDOWN						
P_D	Average power dissipation	V_{CC} = 5 V, V_{IO} = V_{CC}, T_J = 27°C, R_L = 60 Ω, STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF		140		mW
		V_{CC} = 5.33 V, V_{IO} = V_{CC}, T_J = 130°C, R_L = 60 Ω , STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_L at RXD = 15 pF			215	
	Thermal shutdown temperature			185		°C

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
PROPAGATION TIME (LOOP TIME TXD to RXD)						
$t_{PROP(LOOP1)}$	Total loop delay 1	Driver input (TXD) to receiver output (RXD), recessive to dominant, see Figure 9, STB at 0 V	70		230	ns
$t_{PROP(LOOP2)}$	Total loop delay 2	Driver input (TXD) to receiver output (RXD), dominant to recessive, see Figure 9, STB at 0 V	70		230	
DRIVER						
t_{PLH}	Propagation delay time, low-to-high level output	STB at 0 V, see Figure 4		65		ns
t_{PHL}	Propagation delay time, high-to-low level output	STB at 0 V, see Figure 4		50		ns
t_R	Differential output signal rise time	STB at 0 V, see Figure 4		25		ns
t_F	Differential output signal fall time	STB at 0 V, see Figure 4		55		ns
t_{EN}	Enable time from standby or silent mode to normal mode, dominant	See Figure 7			30	µs
$t_{(DOM)}$ (2)	Dominant time-out	See Figure 10	1200	2000	2800	µs
RECEIVER						
t_{PLH}	Propagation delay time, low-to-high-level output	STB at 0 V , see Figure 6		95		ns
t_{PHL}	Propagation delay time, high-to-low-level output	STB at 0 V , see Figure 6		60		ns
t_R	Output signal rise time	STB at 0 V , see Figure 6		13		ns
t_F	Output signal fall time	STB at 0 V , see Figure 6		10		ns
t_{BUS}	Dominant time	HVDA551 only, required on bus for wake-up from standby, STB at V_{IO}, see Figure 18 and Figure 19	1.5		5	µs
t_{CLEAR}	Recessive time	HVDA551 only, on the bus to clear the standby mode receiver output (RXD) if standby mode is entered while bus is dominant, STB at V_{IO}, see Figure 18 and Figure 19	1.5		5	µs

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and V_{IO} = 3.3 V.
(2) The TXD dominant time out ($t_{(DOM)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(DOM)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(DOM)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11 / $t_{(DOM)}$ = 11 bits / 300 µs = 37 kbps

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6.7 Typical Characteristic

V_{IO} = 5 V, STB = 0 V, R_I = 60 Ω, C_L= open, RCM = open, T_J = 25°C (unless otherwise noted)

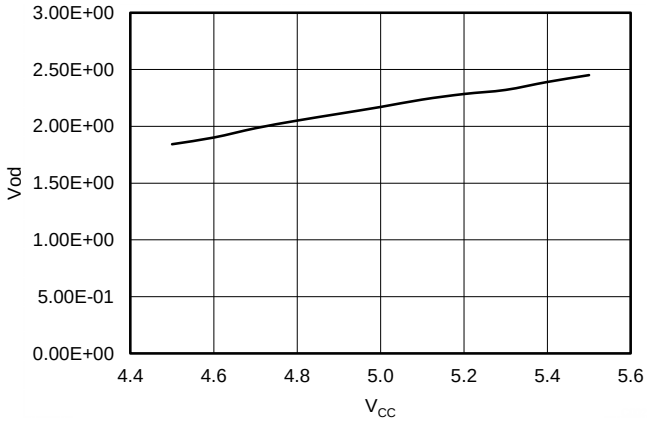


Figure 1. V_{od} vs V_{CC} for HVDA55x

7 Parameter Measurement Information

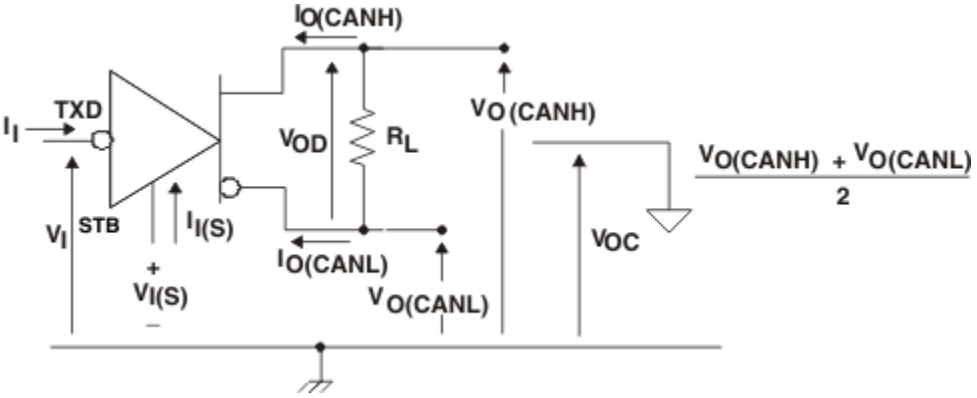


Figure 2. Driver Voltage, Current, and Test Definition

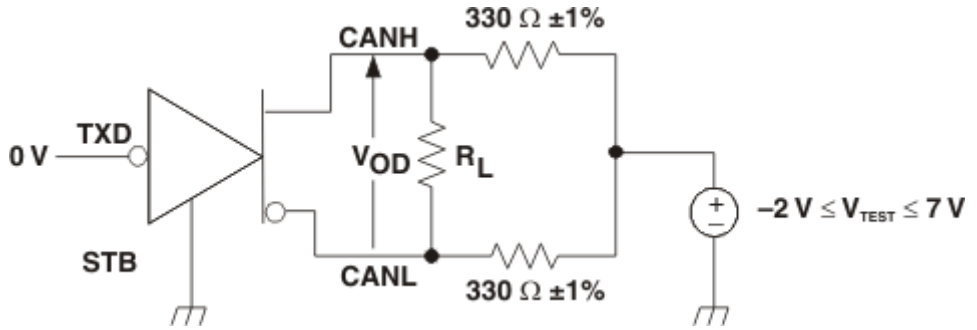
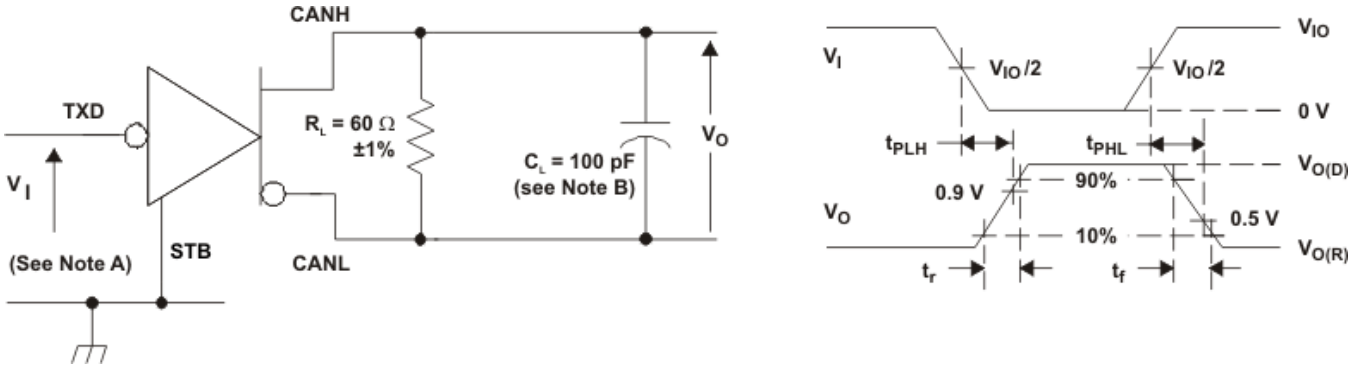


Figure 3. Driver V_{OD} Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

C. For HVDA553 device versions, $V_{IO} = V_{CC}$.

Figure 4. Driver Test Circuit and Voltage Waveforms

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Parameter Measurement Information (continued)

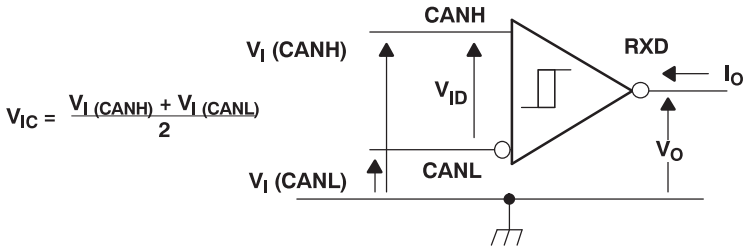
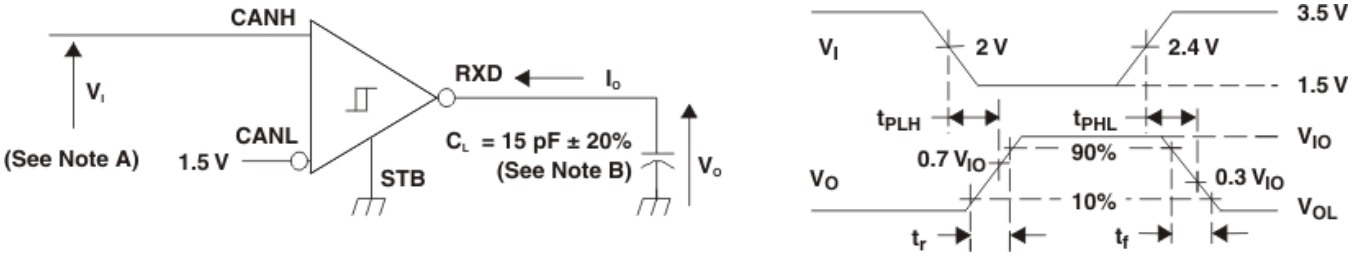


Figure 5. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

C. For HVDA553 device versions $V_{IO} = V_{CC}$.

Figure 6. Receiver Test Circuit and Voltage Waveforms

Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R	
–11.1 V	–12 V	900 mV	L	V_{OL}
12 V	11.1 V	900 mV	L	
–6 V	–12 V	6 V	L	
12 V	6 V	6 V	L	
–11.5 V	–12 V	500 mV	H	V_{OH}
12 V	11.5 V	500 mV	H	
–12 V	–6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	

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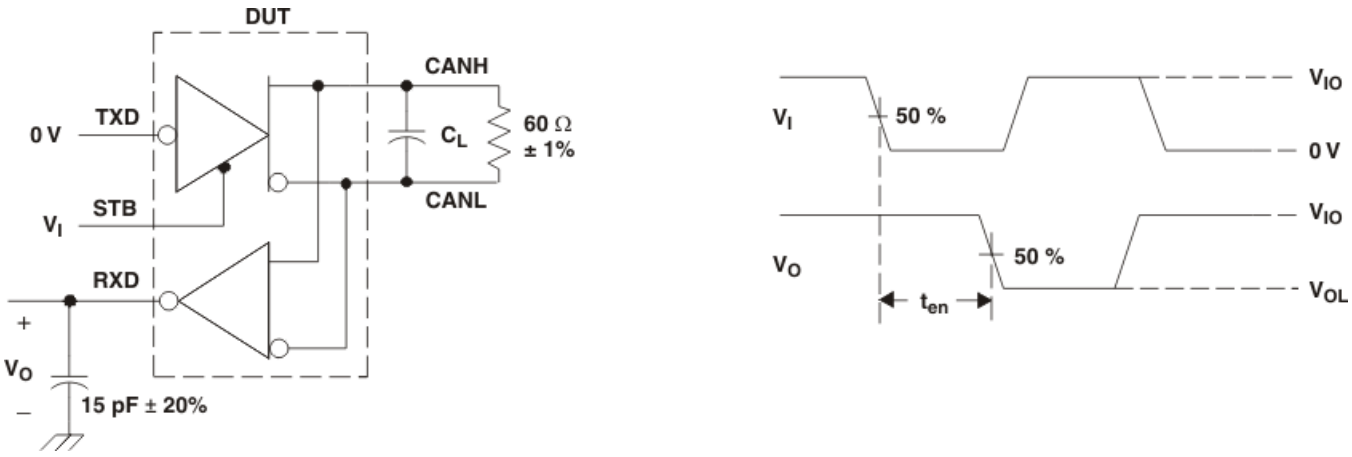
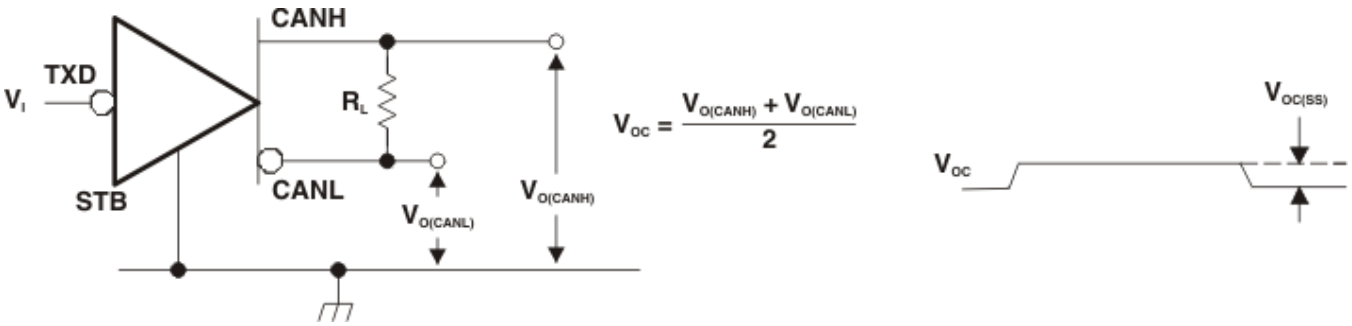


A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse repetition rate (PRR) = 25 kHz, 50% duty cycle.

C. For HVDA553 device versions, $V_{IO} = V_{CC}$.

Figure 7. t_{EN} Test Circuit and Waveforms



A. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8. Common-Mode Output Voltage Test and Waveforms

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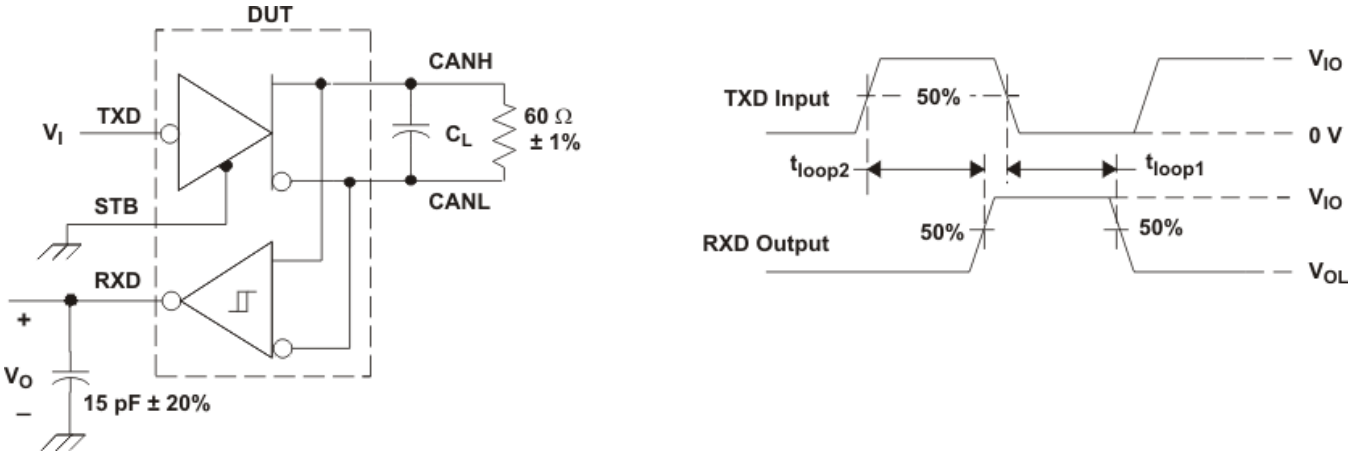
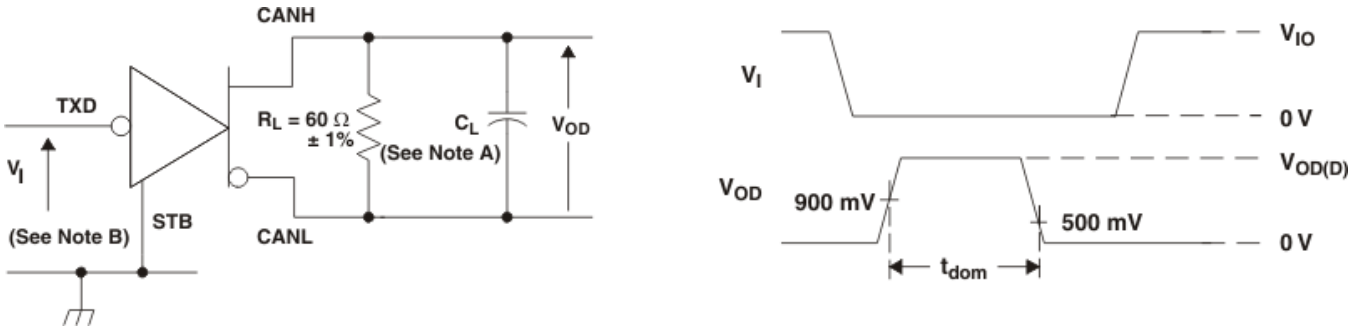


A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

C. For HVDA553 device versions, $V_{IO} = V_{CC}$.

Figure 9. $t_{PROP(LOOP)}$ Test Circuit and Waveform



A. C_L = 100 pF includes instrumentation and fixture capacitance within ±20%.

B. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r or t_f ≤ 6 ns. Pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.

C. For HVDA553 device versions, $V_{IO} = V_{CC}$.

Figure 10. TXD Dominant Time-Out Test Circuit and Waveforms

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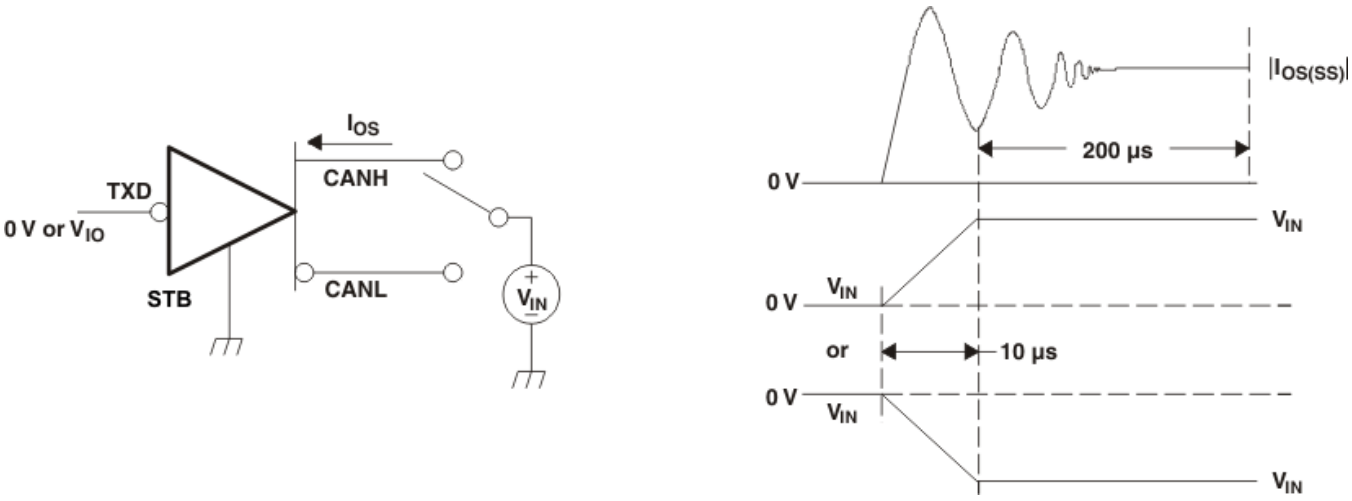
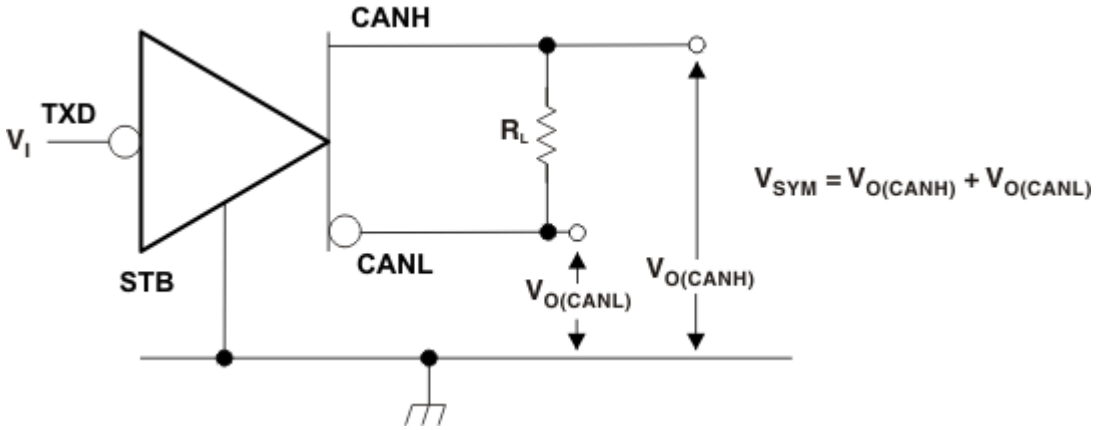


A. For HVDA553 device versions $V_{IO} = V_{CC}$.

Figure 11. Driver Short-Circuit Current Test and Waveforms



A. All V_I input pulses are from 0 V to V_{IO} and supplied by a generator having the following characteristics: t_r and $t_f \leq 6$ ns, pulse repetition rate (PRR) = 250 kHz, 50% duty cycle.

Figure 12. Driver Output Symmetry Test Circuit

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8 Detailed Description

8.1 Overview

The device meets or exceeds the specifications of the ISO 11898 High-Speed CAN (Controller Area Network) Physical Layer standard (transceiver). This device provides CAN transceiver functions: differential transmit capability to the bus and differential receive capability at data rates up to 1 megabit per second (Mbps). The device includes many protection features providing device and CAN network robustness.

8.2 Functional Block Diagrams

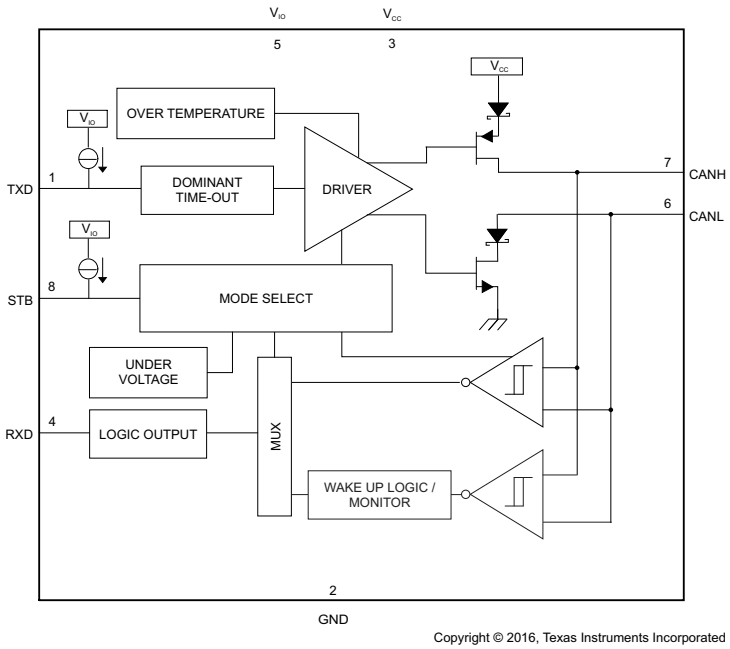

Figure 13. HVDA551 Block Diagram

Functional Block Diagrams (continued)

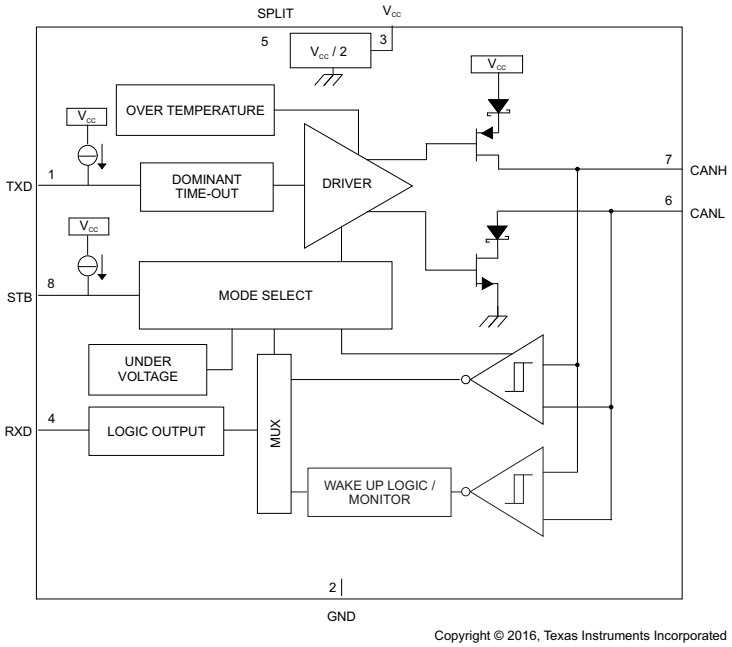

Figure 14. HVDA553 Block Diagram

8.3 Feature Description

8.3.1 Digital Inputs and Outputs

The HVDA551 device has an I/O supply voltage input pin (V_{IO}) to ratiometrically level shift the digital logic input and output levels with respect to V_{IO} for compatibility with protocol controllers having I/O supply voltages between 3 V and 5.33 V.

The HVDA553 devices have a single V_{CC} supply (5 V). The digital logic input and output levels for these devices are with respect to V_{CC} for compatibility with protocol controllers having I/O supply voltages between 4.68 V and 5.33 V.

8.3.2 Using the HVDA553 With Split Termination

The SPLIT pin voltage output provides 0.5 × V_{CC} in normal mode. The circuit may be used by the application to stabilize the common-mode voltage of the bus by connecting it to the center tap of split termination for the CAN network (see Figure 15 and Figure 23). This pin provides a stabilizing recessive voltage drive to offset leakage currents of unpowered transceivers or other bias imbalances that might bring the network common-mode voltage away from 0.5 × V_{CC}. Using this feature in a CAN network improves electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltage levels at the start of message transmissions.

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Feature Description (continued)

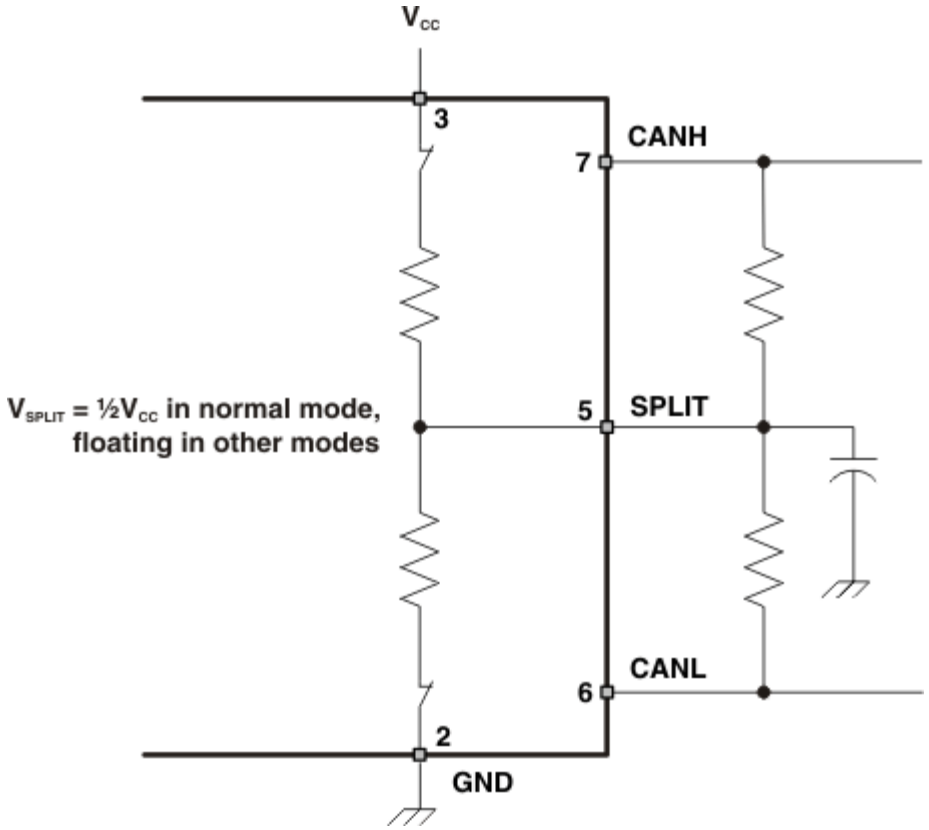

Figure 15. SPLIT Pin Circuitry and Application

8.3.3 Protection Features

8.3.3.1 TXD Dominant State Time Out

During normal mode, the only mode where the CAN driver is active, the TXD dominant time-out circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the time-out period $t_{(DOM)}$. The dominant time-out circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out constant of the circuit expires ($t_{(DOM)}$) the CAN bus driver is disabled, freeing the bus for communication between other network nodes. The CAN driver is re-activated when a recessive signal is seen on the TXD pin, thus clearing the dominant-state time-out. The CAN bus pins are biased to the recessive level during a TXD dominant-state time-out.

NOTE

The maximum dominant TXD time allowed by the TXD dominant-state time-out limits the minimum possible data rate of the devices.

The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(DOM)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by Equation 1:

$$\text{Minimum Bit Rate} = 11 / t_{(DOM)} \quad (1)$$

8.3.3.2 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold, the device turns off the CAN driver circuits. This condition is cleared once the temperature drops below the thermal shutdown temperature of the device. The CAN bus pins are biased to the recessive level during a thermal shutdown.

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Feature Description (continued)

8.3.3.3 Undervoltage Lockout or Unpowered Device

Both of the supply pins have undervoltage detection, which places the device in forced standby mode to protect the bus during an undervoltage event on either the V_{CC} or V_{IO} supply pins. If V_{IO} is undervoltage, the RXD pin is forced to the high-impedance state and the device does not pass any wake-up signals from the bus to the RXD pin. Because the device is placed into forced standby mode, the CAN bus pins have a common-mode bias to ground, protecting the CAN network; see Figure 16 and Figure 17.

The device is designed to be an *ideal passive* load to the CAN bus if it is unpowered. The bus pins (CANH, CANL) have extremely low leakage currents when the device is unpowered, so they do not load down the bus but rather be a no-load. This is critical, especially if some nodes of the network are unpowered while the rest of the network remains in operation.

NOTE

Once an undervoltage condition is cleared and V_{CC} and V_{IO} have returned to valid levels, the device typically requires 300 µs to transition to normal operation.

Table 2. Undervoltage Protection

DEVICE	V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD
Both devices	Bad	Good	Forced standby mode	Common mode bias to GND(1)	Mirrors bus state through wake-up filter(2)
	Good	Bad	Forced standby mode(3)	Common mode bias to GND(1)	High Z
	Unpowered		Unpowered	No load	High Z

(1) See Figure 16 and Figure 17 for common-mode bias information.
(2) See Figure 18 and Figure 19 for operation of the low-power wake-up receiver and bus monitor for RXD wake-up request behavior and Table 5 for the wake-up receiver threshold levels.
(3) When V_{IO} is undervoltage, the device is forced into standby mode with respect to the CAN bus, because there is not a valid digital reference to determine the digital I/O states or power the wake-up receiver.

8.3.3.4 Floating Pins

The device has integrated pullups and pulldowns on critical pins to place the device into known states if the pins float. The TXD and STB pins on the HVDA551 are pulled up to V_{IO}. This forces a recessive input level on TXD in the case of a floating TXD pin and prevents the device from entering into the low-power standby mode if the STB pin floats. In the case of the HVDA553 both the TXD and STB pins are pulled up to V_{CC}, which has the same effect.

8.3.3.5 CAN Bus Short-Circuit Current Limiting

The device has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver-current limiting (dominant and recessive) and TXD dominant-state time-out to prevent continuously driving dominant. During CAN communication, the bus switches between dominant and recessive states; thus, the short-circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in termination resistance and common-mode choke ratings, the average short-circuit current must be used. The device has TXD dominant-state time-out, which prevents permanently having the higher short-circuit current of dominant state. The CAN protocol also has forced state changes and recessive bits such as bit stuffing, control fields, and interframe space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

NOTE

The short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents.

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The average short-circuit current may be calculated with Equation 2:

$$I_{OS(AVG)} = \%Transmit \times [(\%REC_Bits \times I_{OS(SS)_REC}) + (\%DOM_Bits \times I_{OS(SS)_DOM})] + [\%Receive \times I_{OS(SS)_REC}] \quad (2)$$

where

- $I_{OS(AVG)}$ is the average short-circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)_REC}$ is the recessive steady-state, short-circuit current
- $I_{OS(SS)_DOM}$ is the dominant steady-state, short-circuit current

8.4 Device Functional Modes

These devices have two main operating modes: normal mode and standby mode. Table 3 lists these modes in detail. Operating mode selection is made through the STB input pin.

Table 3. Operating Modes

DEVICE	STB	MODE	DRIVER	RECEIVER	RXD Pin
All devices	LOW	Normal mode	Enabled (On)	Enabled (On)	Mirrors bus state (1)
	HIGH	Standby mode (RXD wake-up request)	Disabled (Off)	Low-power wake-up receiver and bus monitor enabled	Mirrors bus state through wake-up filter (2)

(1) Mirrors bus state: LOW if CAN bus is dominant, HIGH if CAN bus is recessive.
(2) See Figure 18 and Figure 19 for operation of the low-power wake-up receiver and bus monitor for RXD wake-up request behavior and Table 5 for the wake-up receiver threshold levels.

8.4.1 Bus States by Mode

The CAN bus has three valid states during powered operation, depending on the mode of the device. In normal mode, the bus may be dominant (logic LOW) where the bus lines are driven differentially apart, or or the bus may be recessive (logic HIGH) where the bus lines are biased to V_{CC} / 2 through the high-ohmic internal input resistors R_{IN} of the receiver. The third state is low-power standby mode where the bus lines are biased to GND through the high-ohmic internal input resistors R_{IN} of the receiver.

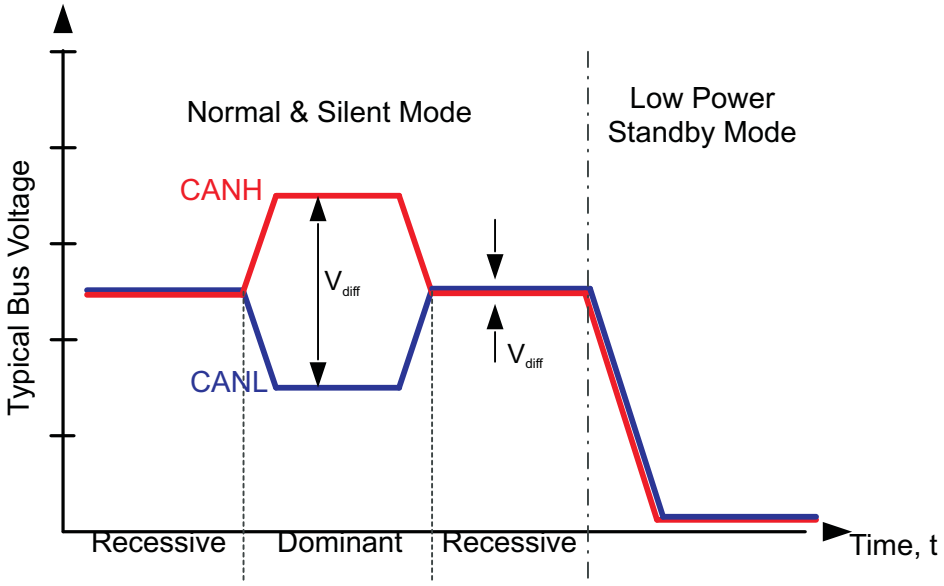

Figure 16. Bus States (Physical Bit Representation)

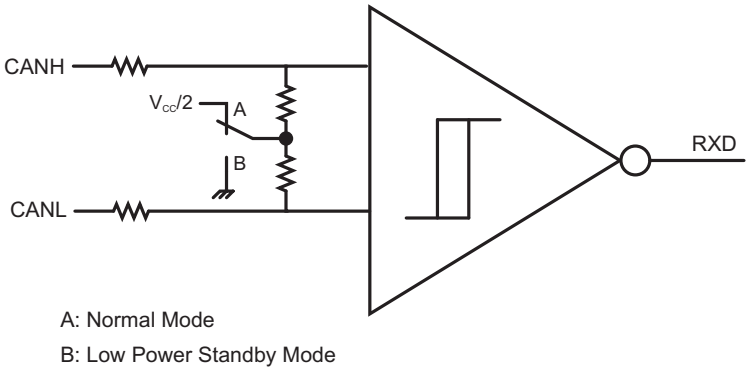

Figure 17. Simplified Common-Mode Bias and Receiver Implementation

8.4.2 Normal Mode

This is the normal operating mode of the device. Normal mode is selected by setting STB low. The CAN driver and receiver are fully operational and CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. In recessive state, the CAN bus pins (CANH and CANL) are biased to 0.5 × V_{CC}. In dominant state, the bus pins are driven differentially apart. Logic high is equivalent to recessive on the bus, and logic low is equivalent to a dominant (differential) signal on the bus.

8.4.3 Standby Mode With RXD Wake-Up Request

This is the low-power mode of the device. Standby mode is selected by setting STB high. The CAN driver and main receiver are turned off and bidirectional CAN communication is not possible. The low-power receiver and bus monitor, both supplied through the V_{IO} supply, are enabled to allow for RXD wake-up requests through the CAN bus. The V_{CC} (5-V) supply may be turned off for additional power savings at the system level. A wake-up request is output to RXD (driven low) for any dominant bus transmissions longer than the filter time t_{BUS}. The local protocol controller (MCU) must monitor RXD for transitions and then reactivate the device to normal mode based on the wake-up request. The 5-V (V_{CC}) supply must be reactivated by the local protocol controller to resume normal mode if it has been turned off for low-power standby operation. The CAN bus pins are weakly pulled to GND, see Figure 16 and Figure 17.

8.4.3.1 RXD Wake-Up Request Lockout for Bus-Stuck Dominant Fault (HVDA551)

If the bus has a fault condition where it is stuck dominant while the HVDA551 is placed into standby mode through the STB pin, the device locks out the RXD wake-up request until the fault has been removed to prevent false wake-up signals in the system.

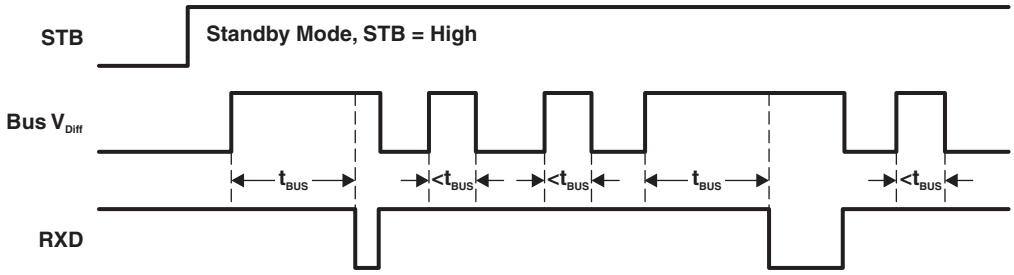

Figure 18. HVDA551 RXD Wake-Up Request With No Bus Fault Condition

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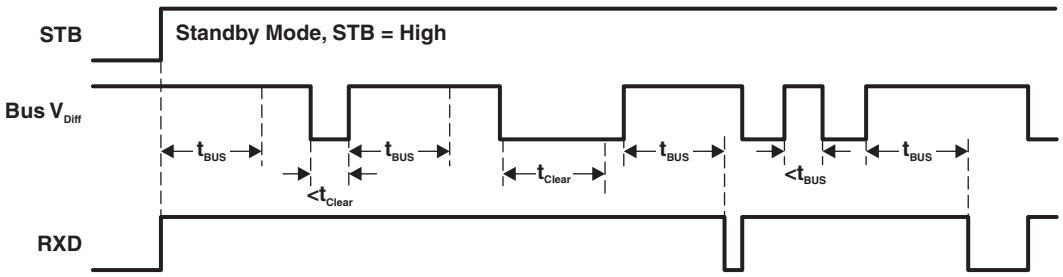

Figure 19. HVDA551 RXD Wake-Up Request Lockout During Bus Dominant Fault Condition

8.4.4 Driver and Receiver Function Tables

Table 4 shows the behavior of devices when in driver mode.

Table 4. Driver Function Table

DEVICE	INPUTS		OUTPUTS		DRIVEN BUS STATE
	STB / S(1)	TXD(1)	CANH(1)	CANL(1)	
Both devices	L	L	H	L	Dominant
	L	H	Z	Z	Recessive
	L	Open	Z	Z	Recessive
HVDA551, HVDA553(2)	H	X	Y	Y	Recessive

(1) H = high level, L = low level, X = irrelevant, Y = common-mode bias to GND, Z = common-mode bias to V_{CC} / 2. See Figure 16 and Figure 17 for common-mode bias information.
(2) HVDA551 and HVDA553 have internal pullup to V_{IO} on the STB pin. If the STB pin is open, the pin is pulled high and the device is in standby mode.

Table 5. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS V_{ID} = V(CANH) – V(CANL)	BUS STATE	RXD PIN(1)
Standby with RXD wake-up request (HVDA551, HVDA553)(2)	$V_{ID} \geq 1.15$ V	DOMINANT	L
	0.4 V < V_{ID} < 1.15 V	?	?
	$V_{ID} \leq 0.4$ V	RECESSIVE	H
NORMAL	$V_{ID} \geq 0.9$ V	DOMINANT	L
	0.5 V < V_{ID} < 0.9 V	?	?
	$V_{ID} \leq 0.5$ V	RECESSIVE	H
ANY	Open	N/A	H

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate.
(2) While STB is high (standby mode) the RXD output of the HVDA551 functions according to the levels above and the wake-up conditions shown in Figure 18 and Figure 19.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

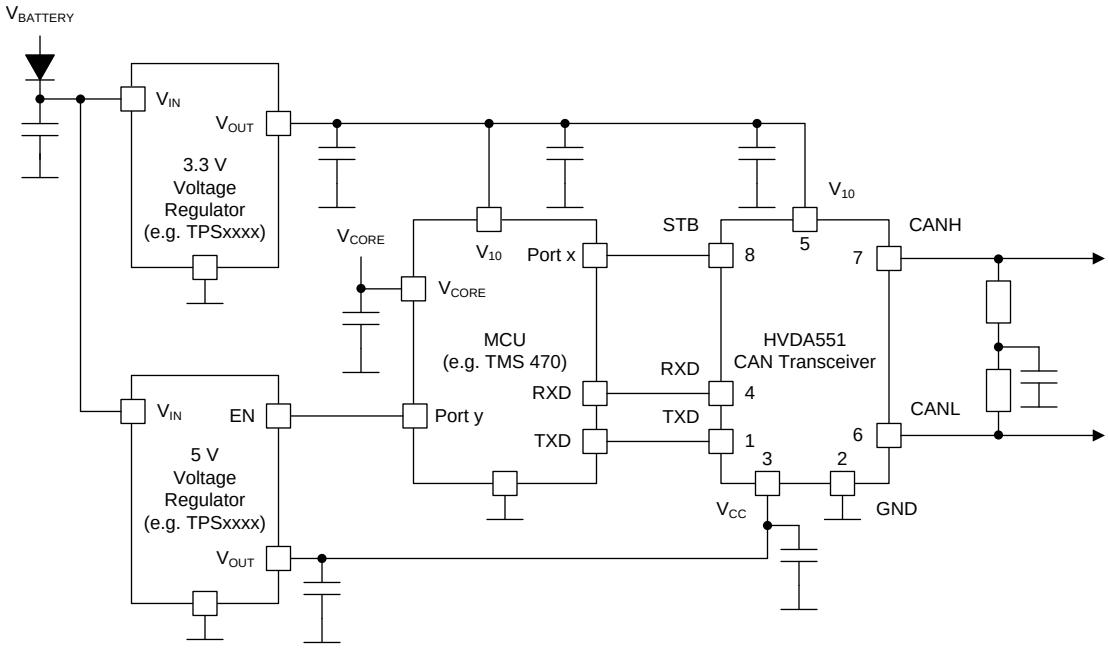
9.1 Application Information

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. The following typical application configurations are for both 5-V and 3.3-V microprocessor applications. The bus termination is shown for illustrative purposes.

9.2 Typical Applications

Some typical applications for the HVDA55x family are shown in the following sections.

9.2.1 3.3-V I/O Voltage Level in Low-Power Mode



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5-V V_{CC} Not Required in Low-Power Mode

Figure 20. Typical Application Using the HVDA551 With 3.3-V I/O Voltage Level in Low-Power Mode

9.2.1.1 Design Requirements

The ISO 11898-2 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the HVDA55x family of transceivers.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet, and NMEA2000.

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Typical Applications (continued)

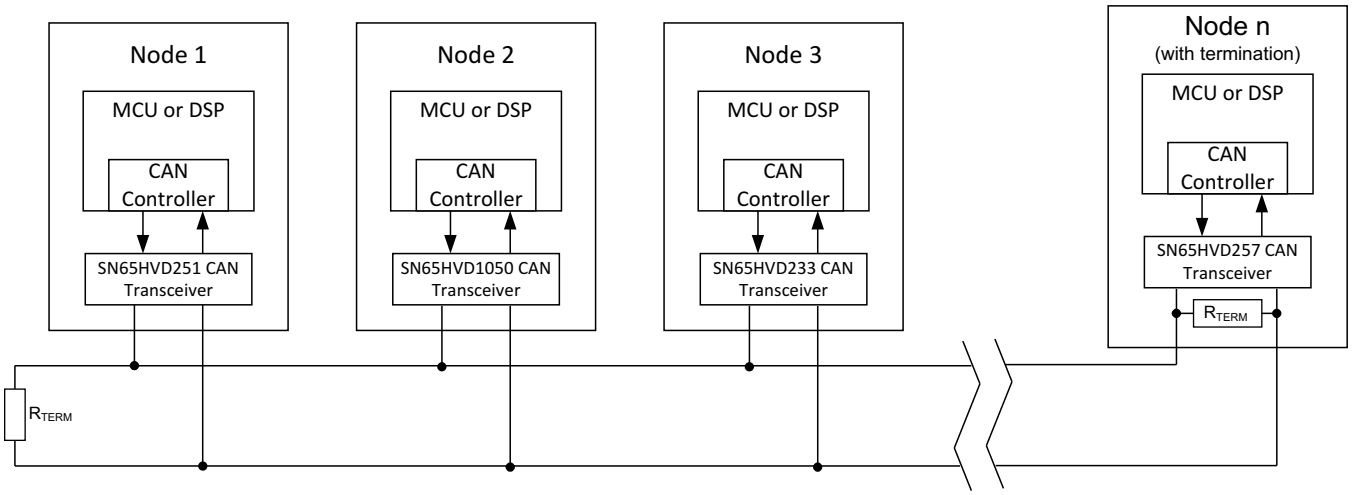

Figure 21. Typical CAN Bus

9.2.1.2 Detailed Design Procedure

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line must be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus must be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that two terminations always exist on the network.

Termination may be a single 120-Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination may be used (see Figure 22). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

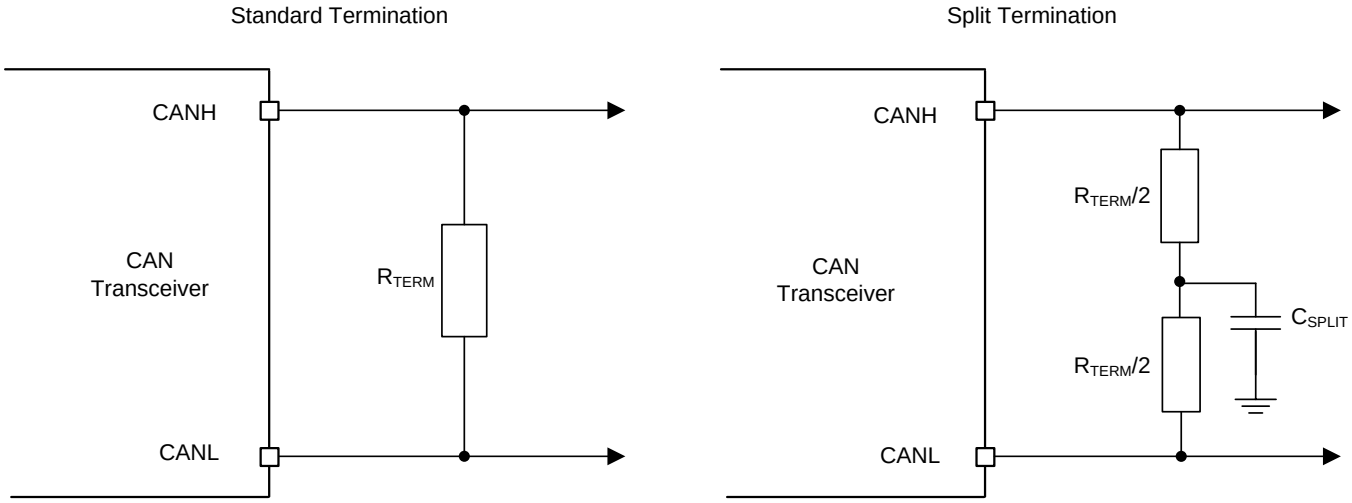

Figure 22. CAN Bus Termination Concepts

The family of transceivers have variants for both 5-V-only applications, and applications where level shifting is needed for a 3.3-V micrcontroller.

Typical Applications (continued)

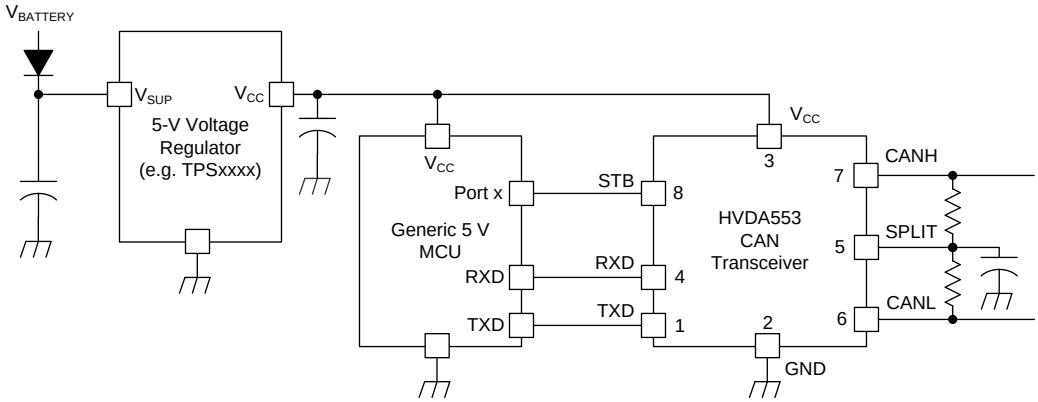

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Figure 23. Typical Application Using the HVDA553 With SPLIT Termination Diagram

9.2.1.2.1 Loop Propagation Delay

Transceiver loop delay is a measure of the overall device propagation delay and consists of the delay from driver input (TXD pin) to differential outputs (CANH and CANL), plus the delay from the receiver inputs (CANH and CANL) to the RXD output pin.

In Figure 24 is displayed the loop delay at 1 Mbps with V_{IO} equal to 3.3 V

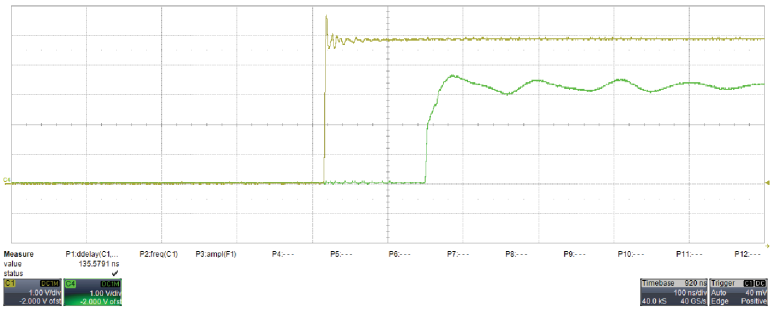

Figure 24. t_LOOP Delay

9.2.1.3 Application Curves

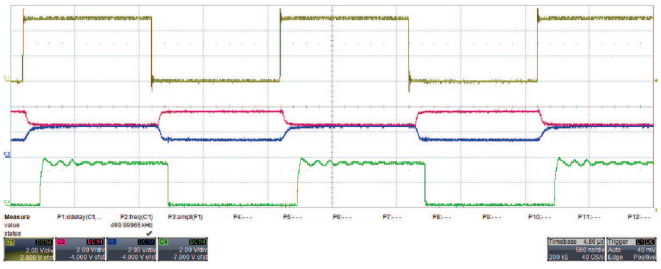

Figure 25. TXD, CANH, CANL, and RXD Waveforms 1 Mbps

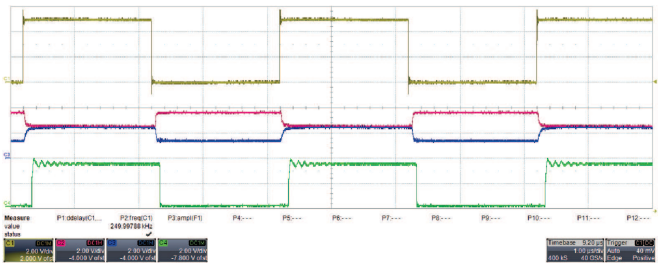

Figure 26. TXD, CANH, CANL, and RXD Waveforms 500 Kbps

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10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be decoupled with a 100-nF ceramic capacitor placed as close to the V_{CC} supply pins as possible. Either a linear regulator or switched-mode power supply may be used. Power and ground nets must be routed on the PCB using planes or wide traces so that series resistance and inductance are minimized.

11 Layout

11.1 Layout Guidelines

HVDA551 and HVDA553 families come with high on-chip IEC ESD protection, but if higher levels are desired, external TVS diodes can be used. TVS diodes and bus-filtering capacitors must be placed as close as possible to board connectors to prevent noisy transient events into PCB. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system. Use V_{CC} and ground planes to provide low inductances. High frequency current follows the path of least impedance and not the path of least resistance. TI recommends designing the bus protection components in the direction of the signal path. Do not force transient current to divert from signal path to reach protection device.

- Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. In this layout example, a transient voltage suppression (TVS) device, D1, has been used for added protection. The production solution can be either bidirectional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C4 and C5. Additionally (not shown) a series common mode choke (CMC) can be placed on the CANH and CANL lines between the transceiver U1 and connector J1.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use supply (V_{CC}) and ground planes to provide low inductance.

NOTE

High-frequency currents follows the path of least impedance and not the path of least resistance.

- Use at least two vias for supply (V_{CC}) and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- Bypass and bulk capacitors must be placed as close as possible to the supply terminals of transceiver, examples are C1 and C2 on the V_{CC} supply and C6 and C7 on the V_{IO} supply.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R6 and R7, with the center or split tap of the termination connected to ground through capacitor C3. Split termination provides common-mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, take additional care to ensure the terminating node is not removed from the bus thus also removing the termination.
- To limit current of digital lines, serial resistors may be used. Examples are R2, R3, and R4. These are not required.
- Terminal 1: R1 is shown optionally for the TXD input of the device. If an open-drain host processor is used, this is mandatory to ensure the bit timing into the device is met.
- Terminal 5: For devices with a VIO input, bypass capacitors must be placed as close to the pin as possible (example C6 and C7). In devices without a VIO input, this pin is not internally connected and can be left floating or tied to any existing net (for example, a split pin connection).
- Terminal 8 is shown assuming the mode terminal, STB, will be used. If the device is only used in normal mode, R4 is not needed and R5 could be used for the pulldown resistor to GND.

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11.2 Layout Example

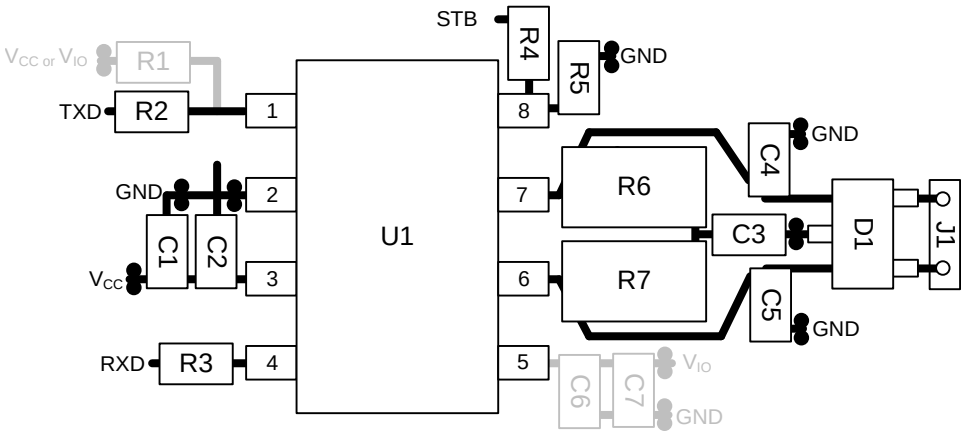

Figure 27. HVDA551 Layout Example Recommendation

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

I_{IO} Quiescent Current in Standby / Silent Mode (SLLZ073)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
HVDA551-Q1	Click here	Click here	Click here	Click here	Click here
HVDA553-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HVDA551QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	H551Q	Samples
HVDA553QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	H553Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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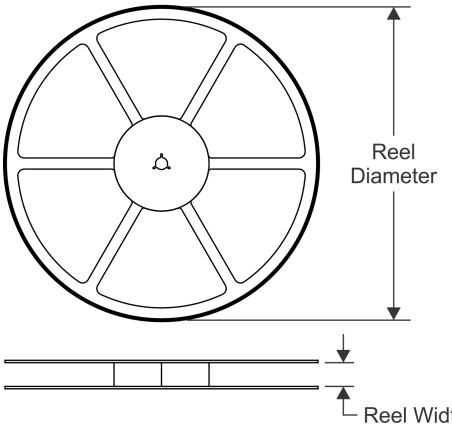
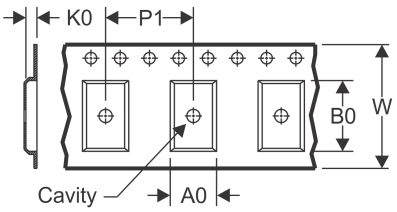
TAPE AND REEL INFORMATION

REEL DIMENSIONS

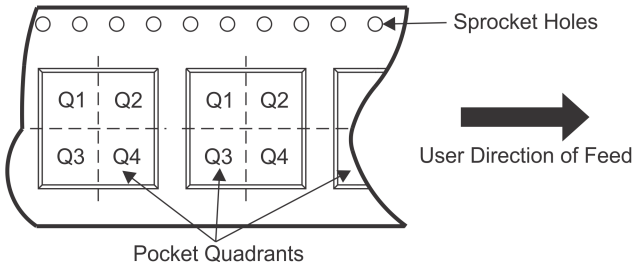


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

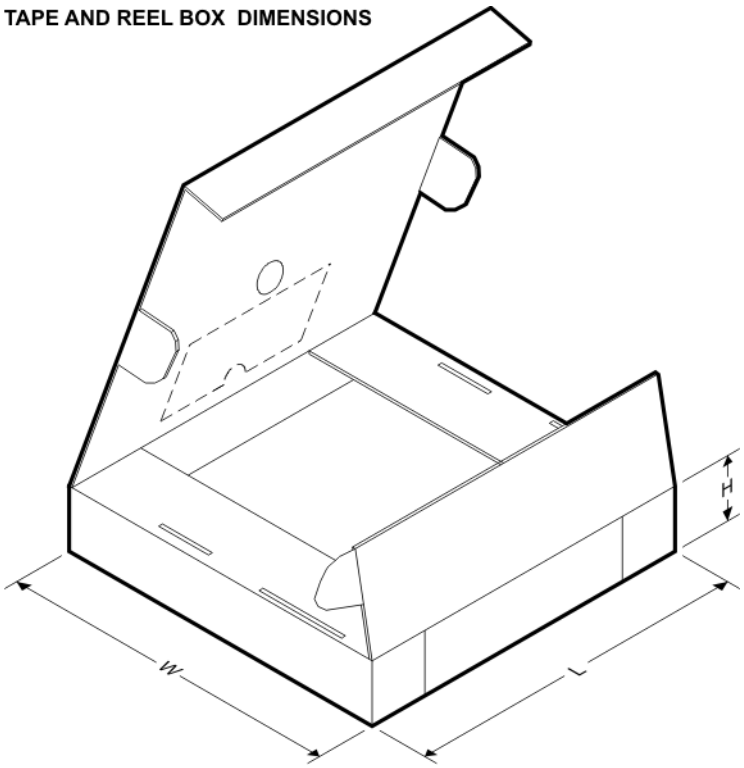
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

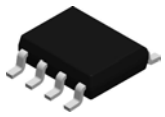
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HVDA551QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
HVDA553QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HVDA551QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
HVDA553QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

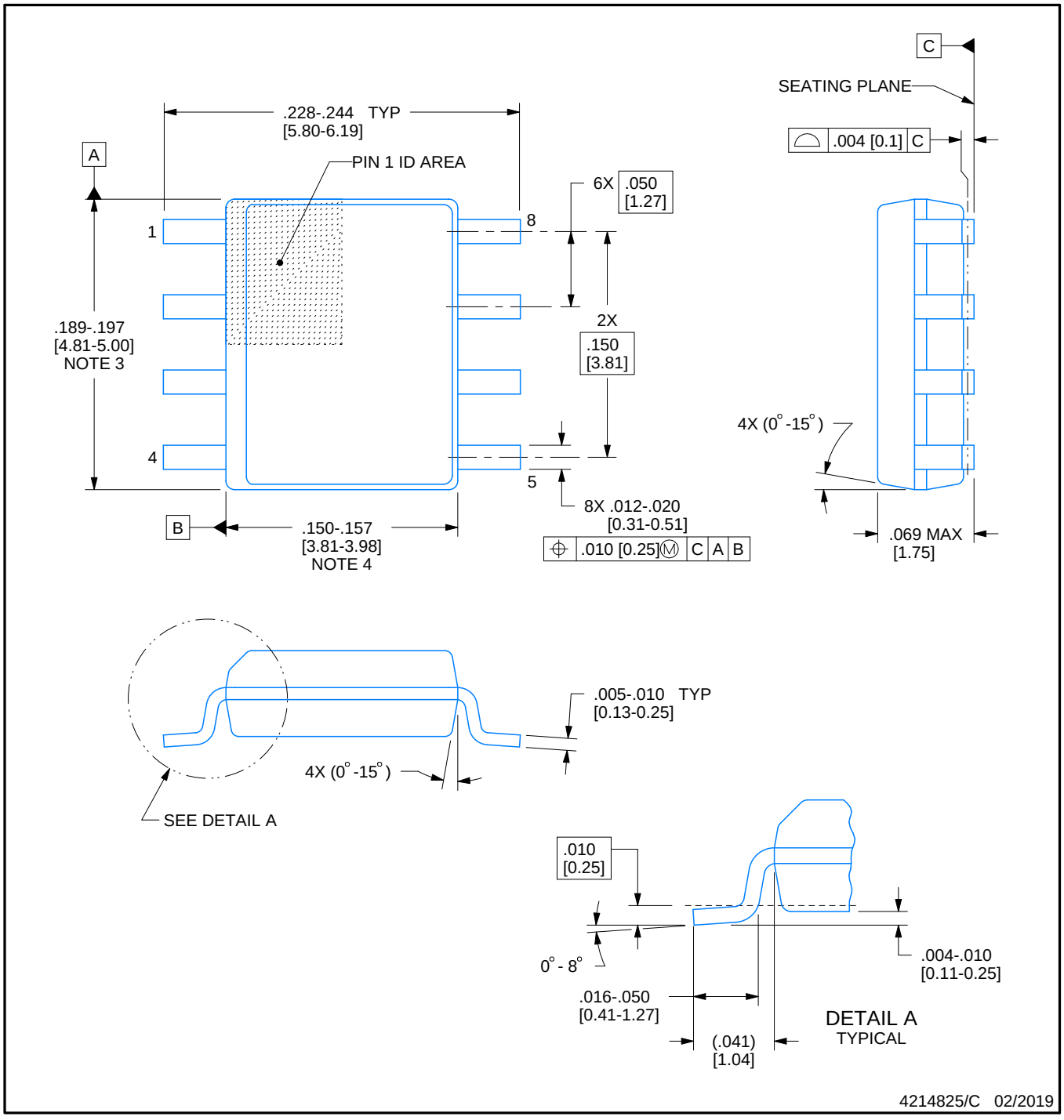


PACKAGE OUTLINE

D0008A

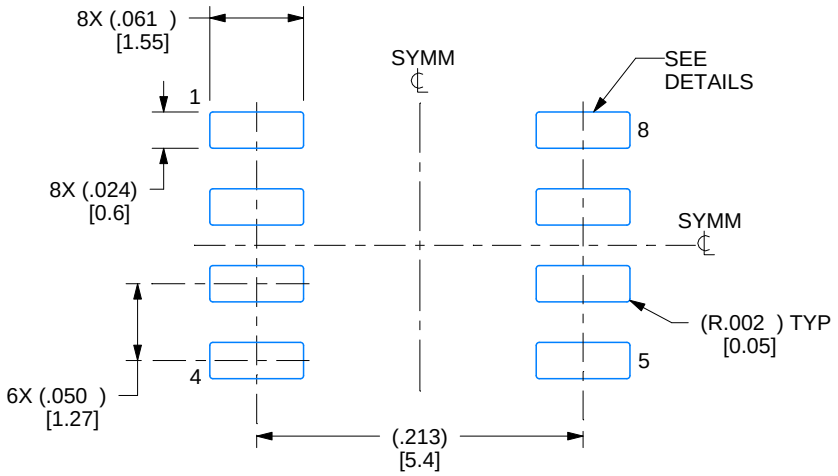
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

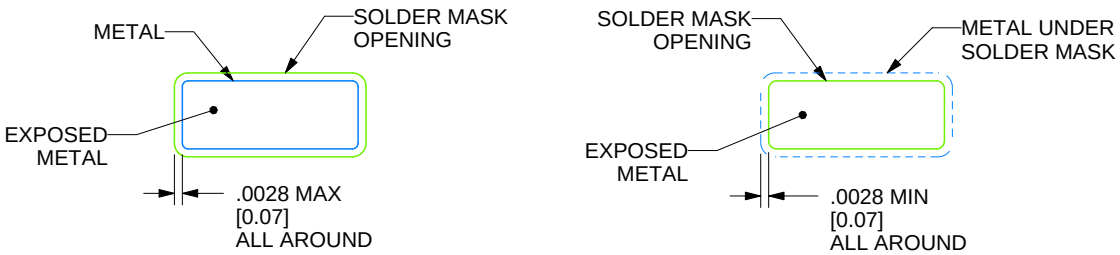


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

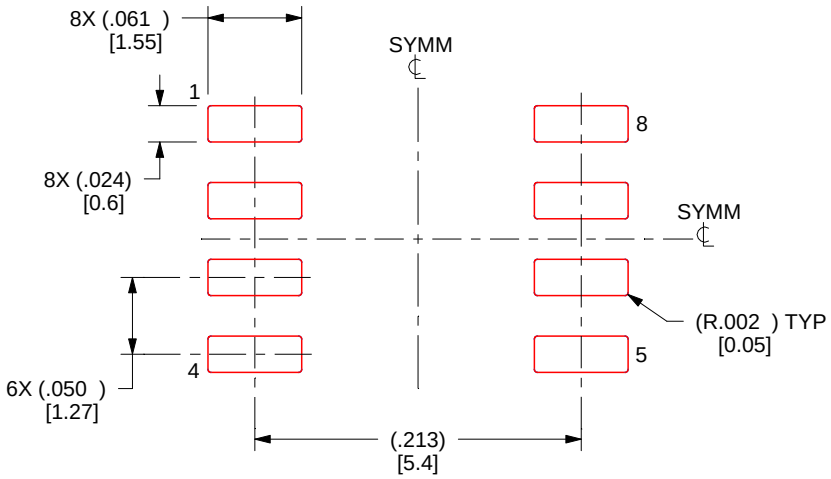
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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