THE DATASHEET OF

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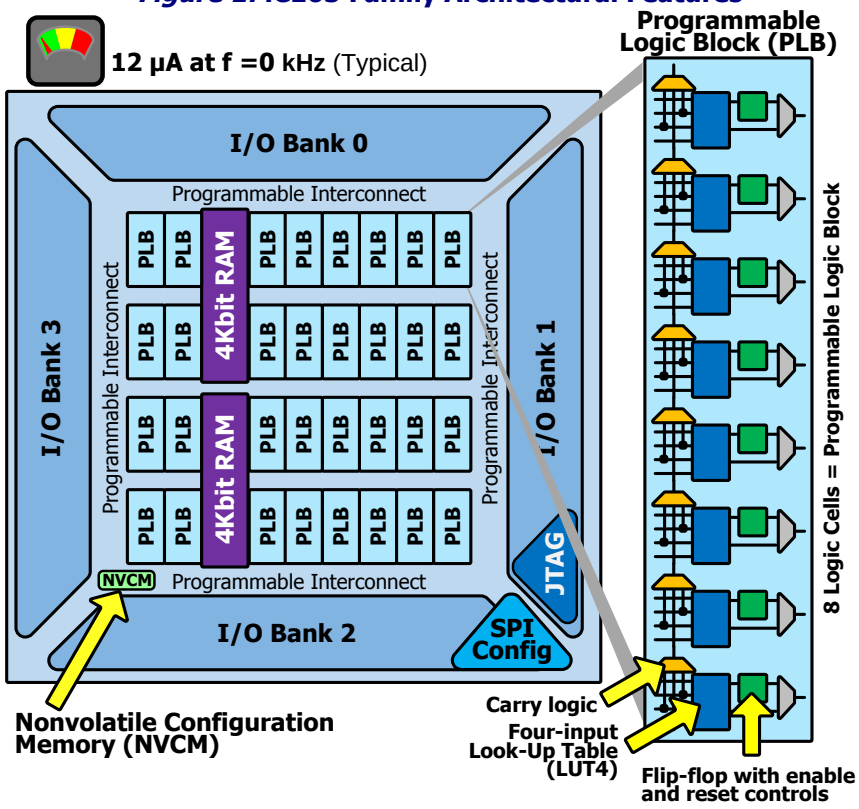
iCE65™ Ultra Low-Power mobileFPGA™ Family

March 30, 2012 (2.42) Data Sheet

- **First high-density, ultra low-power single-chip, SRAM mobileFPGA family specifically designed for hand-held applications and long battery life**
  - 12 µA in static mode
  - Two power/speed options
    - –L: Low Power
    - –T: High speed
- **Up to 256 MHz internal performance**
- **Reprogrammable from a variety of sources and methods**
  - Processor-like mode self-configures from external, commodity SPI serial Flash PROM
  - Downloaded by processor using SPI-like serial interface in as little as 20 µs
  - In-system programmable, ASIC-like mode loads from secure, internal Nonvolatile Configuration Memory (NVCM)
    - Ideal for volume production
    - Superior design and intellectual property protection; no exposed data
- **Proven, high-volume 65 nm, low-power CMOS technology**
  - Low leakage, µW static power
  - Lower core voltage, lowest dynamic power
- **Flexible programmable logic and programmable interconnect fabric**
  - Over 7,600 look-up tables (LUT4) and flip-flops
  - Low-power logic and interconnect
- **Flexible I/O pins to simplify system interfaces**
  - Up to 222 programmable I/O pins
  - Four independently-powered I/O banks; support for 3.3V, 2.5V, 1.8V, and 1.5V voltage standards
  - LVCMOS, MDDR, LVDS, and SubLVDS I/O standards

Figure 1: **iCE65 Family Architectural Features**



- **Plentiful, fast, on-chip 4Kbit RAM blocks**
- **Low-cost, space-efficient packaging options**
  - Known-good die (KGD) options available
- **Complete iCEcube™ development system**
  - Windows® and Linux® support
  - VHDL and Verilog logic synthesis
  - Place and route software
  - Design and IP core libraries
  - Low-cost iCEman65 development board

Table 1: **iCE65 Ultra Low-Power Programmable Logic Family Summary**

	iCE65L01	iCE65L04	iCE65L08
Logic Cells (LUT + Flip-Flop)	1,280	3,520	7,680
RAM4K Memory Blocks	16	20	32
RAM4K RAM bits	64K	80K	128K
Configuration bits (maximum)	245 Kb	533 Kb	1,057 Kb
Typical Current at 0 kHz, 1.0 V	**12 µA**	**26 µA**	**54 µA**
Maximum Programmable I/O Pins	95	176	222
Maximum Differential Input Pairs	0	20	25

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Overview

The Lattice Semiconductor iCE65 programmable logic family is specifically designed to deliver the lowest static and dynamic power consumption of any comparable CPLD or FPGA device. iCE65 devices are designed for cost-sensitive, high-volume applications and provide on-chip, nonvolatile configuration memory (NVCM) to customize for a specific application. iCE65 devices can self-configure from a configuration image stored in an external commodity SPI serial Flash PROM or be downloaded from an external processor over an SPI-like serial port.

The three iCE65 components, highlighted in Table 1, deliver from approximately 1K to nearly 8K logic cells and flip-flops while consuming a fraction of the power of comparable programmable logic devices. Each iCE65 device includes between 16 to 32 RAM blocks, each with 4Kbits of storage, for on-chip data storage and data buffering.

As pictured in Figure 1, each iCE65 device consists of four primary architectural elements.

- An array of Programmable Logic Blocks (PLBs)
  - Each PLB contains eight Logic Cells (LCs); each Logic Cell consists of ...
    - A fast, four-input look-up table (LUT4) capable of implementing any combinational logic function of up to four inputs, regardless of complexity
    - A 'D'-type flip-flop with an optional clock-enable and set/reset control
    - Fast carry logic to accelerate arithmetic functions such as adders, subtracters, comparators, and counters.
  - Common clock input with polarity control, clock-enable input, and optional set/reset control input to the PLB is shared among all eight Logic Cells
- Two-port, 4Kbit RAM blocks (RAM4K)
  - 256x16 default configuration; selectable data width using programmable logic resources
  - Simultaneous read and write access; ideal for FIFO memory and data buffering applications
  - RAM contents pre-loadable during configuration
- Four I/O banks with independent supply voltage, each with multiple Programmable Input/Output (PIO) blocks
  - LVCMOS I/O standards and LVDS outputs supported in all banks
  - I/O Bank 3 supports additional SSTL, MDDR, LVDS, and SubLVDS I/O standards
- Programmable interconnections between the blocks
  - Flexible connections between all programmable logic functions
  - Eight dedicated low-skew, high-fanout clock distribution networks

Packaging Options

iCE65 components are available in a variety of package options to support specific application requirements. The available options, including the number of available user-programmable I/O pins (PIOs), are listed in Table 2. Fully-tested Known-Good Die (KGD) DiePlus™ are available for die stacking and highly space-conscious applications. All iCE65 devices are provided exclusively in Pb-free, RoHS-compliant packages.

Table 2: **iCE65 Family Packaging Options, Maximum I/O per Package**

Package	Package Body (mm)	Package Code	Ball/Lead Pitch (mm)	65L01	65L04	65L08
81-ball chip-scale BGA	5 x 5	CB81	0.5	63 *(0)*	—	—
84-pin quad flat no-lead package	7 x 7	QN84	0.5	67 *(0)*	—	—
100-pin very thin quad flat package	14 x 14	VQ100	0.5	72 *(0)* ⟺	72 *(9)*	—
121-ball chip-scale BGA	6 x 6	CB121	0.5	92 *(0)*	—	—
132-ball chip-scale BGA	8 x 8	CB132		93 *(0)* ⇔	95 *(11)* ⇔	95 *(12)*
196-ball chip-scale BGA	8 x 8	CB196		—	150 *(18)* ⇔	150 *(18)*
284-ball chip-scale BGA	12 x 12	CB284		—	176 *(20)* ⟺	222 *(25)*
Known Good Die	See DiePlus data sheet	DI	—	95 *(0)*	176 *(20)*	222 *(25)*

⟺ = Common footprint allows each density migration on the same printed circuit board. *(Differential input count)*.

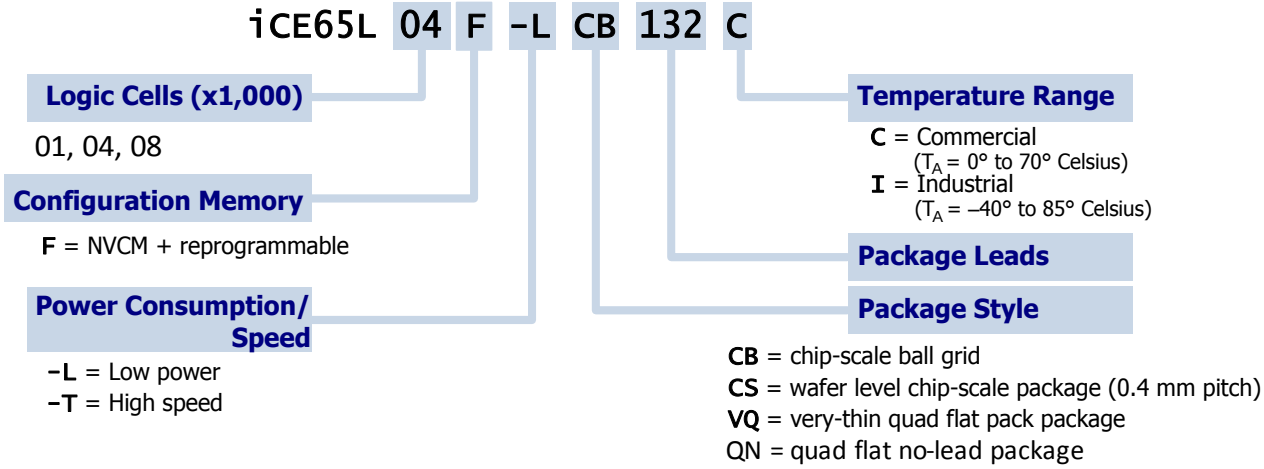
The iCE65L04 and the iCE65L08 are both available in the CB196 package and have similar footprints but are not completely pin compatible. See "Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package" on page 73 for more information.

When iCE65 components are supplied in the same package style, devices of different gate densities share a common footprint. The common footprint improves manufacturing flexibility. Different models of the same product can share a common circuit board. Feature-rich versions of the end application mount a larger iCE65 device on the circuit board. Low-end versions mount a smaller iCE65 device.

Ordering Information

Figure 2 describes the iCE65 ordering codes for all packaged, non-NVCM Programed components. See the separate DiePlus data sheets when ordering die-based products.

Figure 2: **iCE65 Ordering Codes Standard Device**

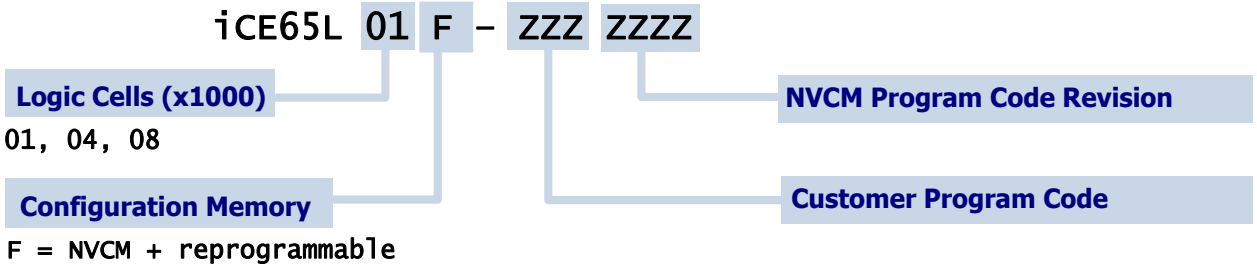


iCE65 devices offer two power consumption, speed options. Standard products ("-L" ordering code) have low standby and dynamic power consumption. The "-T" provides higher-speed logic.

Similarly, iCE65 devices are available in two operating temperature ranges, one for typical commercial applications, the other with an extended temperature range for industrial and telecommunications applications. The ordering code also specifies the device package option, as described further in Table 2.

Figure 3 describes the iCE65 ordering codes for all packaged, NVCM Programmed components.

Figure 3: **iCE65 Ordering Codes NVCM Programmed Device**



Programmable Logic Block (PLB)

Generally, a logic design for an iCE65 component is created using a high-level hardware description language such as Verilog or VHDL. The Lattice Semiconductor development software then synthesizes the high-level description into equivalent functions built using the programmable logic resources within each iCE65 device. Both sequential and combinational functions are constructed from an array of Programmable Logic Blocks (PLBs). Each PLB contains eight Logic Cells (LCs), as pictured in Figure 4, and share common control inputs, such as clocks, reset, and enable controls.

PLBs are connected to one another and other logic functions using the rich Programmable Interconnect resources.

Logic Cell (LC)

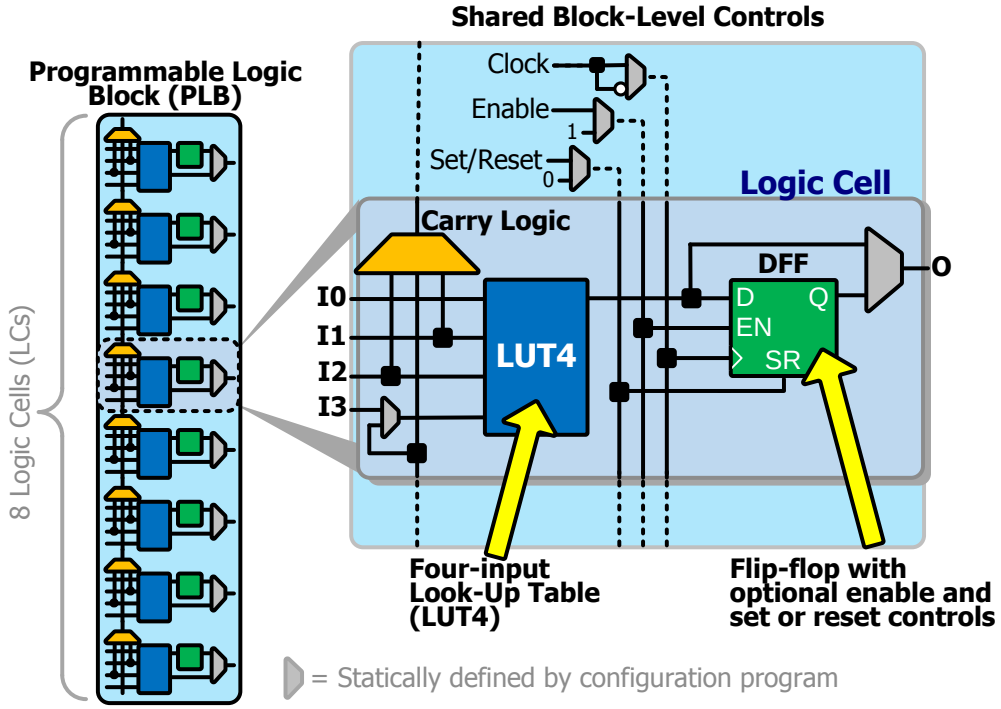
Each iCE65 device contains thousands of Logic Cells (LCs), as listed in Table 1. Each Logic Cell includes three primary logic elements, shown in Figure 4.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, of up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.

Figure 4: **Programmable Logic Block and Logic Cell**

- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

The output from a Logic Cell is available to all inputs to all eight Logic Cells within the Programmable Logic Block. Similarly, the Logic Cell output feeds into fabric to connect to other features on the iCE65 device.



Look-Up Table (LUT4)

The four-input Look-Up Table (LUT4) function implements any and all combinational logic functions, regardless of complexity, of between zero and four inputs. Zero-input functions include "High" (1) and "Low" (0). The LUT4 function has four inputs, labeled I0, I1, I2, and I3. Three of the four inputs are shared with the Carry Logic function, as shown in Figure 4. The bottom-most LUT4 input connects either to the I3 input or to the Carry Logic output from the previous Logic Cell.

The output from the LUT4 function connects to the flip-flop within the same Logic Cell. The LUT4 output or the flip-flop output then connects to the programmable interconnect.

For detailed LUT4 internal timing, see Table 54.

'D'-style Flip-Flop (DFF)

The 'D'-style flip-flop (DFF) optionally stores state information for the application.

The flip-flop has a data input, 'D', and a data output, 'Q'. Additionally, each flip-flop has up to three control signals that are shared among all flip-flops in all Logic Cells within the PLB, as shown in Figure 4. Table 3 describes the behavior of the flip-flop based on inputs and upon the specific DFF design primitive used or synthesized.

Table 3: 'D'-Style Flip-Flop Behavior

DFF Primitive	Operation	Flip-Flop Mode	Inputs				Output
			D	**EN**	**SR**	**CLK**	**Q**
All	Cleared Immediately after Configuration	X	X	X	X	X	0
	Hold Present Value (Disabled)		X	0	X	X	Q
	Hold Present Value (Static Clock)		X	X	X	1 or 0	Q
	Load with Input Data		D	1*	0*	↑	D
SB_DFFR	Asynchronous Reset	Asynchronous Reset	X	X	1	X	0
SB_DFFS	Asynchronous Set	Asynchronous Set	X	X	1	X	1
SB_DFFSR	Synchronous Reset	Synchronous Reset	X	1*	1	↑	0
SB_DFFSS	Synchronous Set	Synchronous Set	X	1*	1	↑	1

X = don't care, ↑ = rising clock edge (default polarity), 1* = High or unused, 0* = Low or unused

The CLK clock signal is not optional and is shared among all flip-flops in a Programmable Logic Block. By default, flip-flops are clocked by the rising edge of the PLB clock input, although the clock polarity can be inverted for all the flip-flops in the PLB.

The CLK input optionally connects to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The EN clock-enable signal is common to all Logic Cells in a Programmable Logic Block. If the enable signal is not used, then the flip-flop is always enabled. This condition is indicated as "1*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

Similarly, the SR set/reset signal is common to all Logic Cells in a Programmable Logic Block. If not used, then the flip-flop is never set/reset, except when cleared immediately after configuration or by the Global Reset signal. This condition is indicated as "0*" in Table 3. The asterisk indicates that this is the default state if the control signal is not connected in the application.

Each flip-flop has an additional control that defines its set or reset behavior. As defined in the configuration image, the control defines whether the set or reset operation is synchronized to the active CLK clock edge or whether it is completely asynchronous.

- The SB_DFFR and SB_DFFS primitives are asynchronously controlled, solely by the SR input. If the SR input is High, then an SB_DFFR primitive is asynchronously reset and an SB_DFFS primitive is asynchronously set.
- The SB_DFFSR and SB_DFFRSS primitives are synchronously controlled by both the SR input and the clock input. If the SR input is High at a rising edge of the clock input, then an SB_DFFSR primitive is synchronously reset and an SB_DFFSS primitive is synchronously set.

The LUT4 output or the flip-flop output then connects to the programmable interconnect.

Because of the shared control signals, the design software can pack flip-flops with common control inputs into a single PLB block, as described by Table 4. There are eight total packing options.

Table 4: **Flip-flop Packing/Sharing within a PLB**

Group	Active Clock Edge	Clock Enable	Set or Reset Control (Sync. or Async)
1	↑	None (always enabled)	None
2	↓		
3	↑		PLB set/reset control
4	↓		
5	↑	Selective (controlled by PLB clock enable)	None
6	↓		
7	↑		PLB set/reset control
8	↓		

For detailed flip-flop internal timing, see Table 54.

Carry Logic

The dedicated Carry Logic within each Logic Cell primarily accelerates and improves the efficiency of arithmetic logic such as adders, accumulators, subtracters, incrementers, decrementers, counters, ALUs, and comparators. The Carry Logic also supports wide combinational logic functions.

$$COUT = I1 \bullet I2 + CIN \bullet I1 + CIN \bullet I2 \qquad \text{[Equation 1]}$$

Equation 1 and Figure 5 describe the Carry Logic structure within a Logic Cell. The Carry Logic shares inputs with the associated Look-Up Table (LUT4). The LUT4's I1 and I2 inputs directly feed the Carry Logic; inputs I0 and I3 do not. A signal cascades between Logic Cells within the Programmable Logic Block. The carry input from the previous adjacent Logic Cell optionally provides an alternate input to the LUT4 function, supplanting the I3 input.

Low-Power Disable

To save power and prevent unnecessary signal switching, the Carry Logic function within a Logic Cell is disabled if not used. The output of a Logic Cell's Carry Logic is forced High.

PLB Carry Input and Carry Output Connections

As shown in Figure 5, each Programmable Logic Block has a carry input signal that can be initialized High, Low, or come from the carry output signal from PLB immediately below.

Similarly, the Carry Logic output from the Programmable Logic Block connects to the PLB immediately above, which allows the Carry Logic to span across multiple PLBs in a column. As shown in Figure 6, the Carry Logic chain can be tapped mid-way through a chain or a PLB by feeding the value through a LUT4 function.

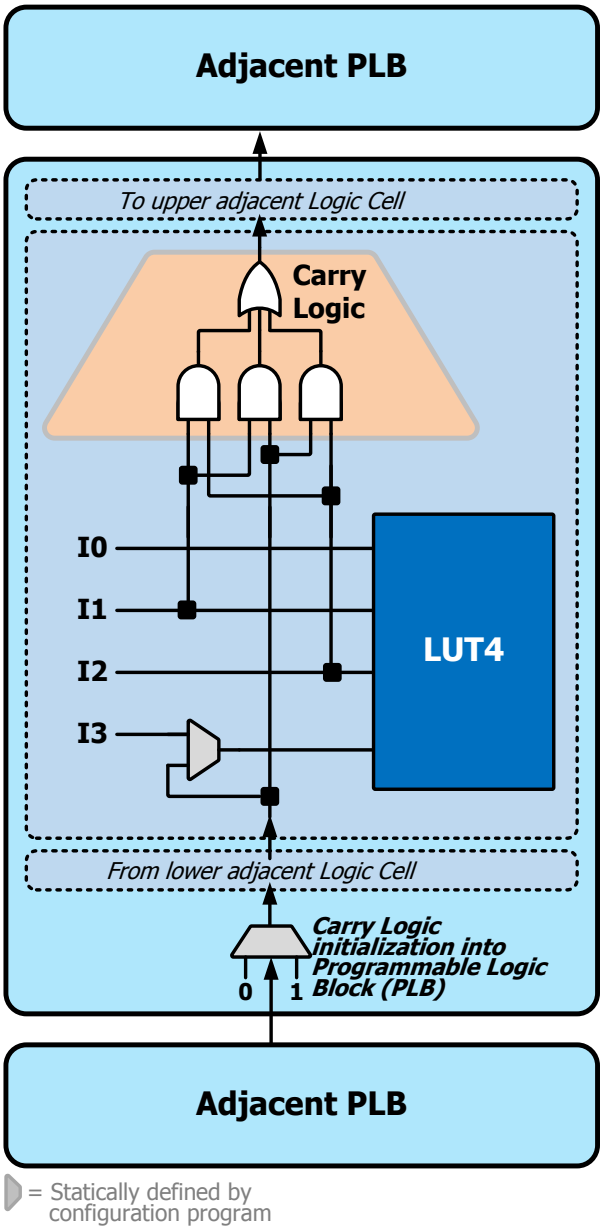
Adder Example

Figure 6 shows an example design that uses the Carry Logic. The example is a 2-bit adder, which can be expanded into an adder of arbitrary size. The LUT4 function within a Logic Cell is programmed to calculate the sum of the two input values and the carry input, `A[i] + B[i] + CARRY_IN[i-1] = SUM[i]`.

The Carry Logic generates the carry value to feed the next bit in the adder. The calculated carry value replaces the I3 input to the next LUT4 in the upper Logic Cell.

If required by the application, the carry output from the final stage of the adder is available by passing it through the final LUT4.

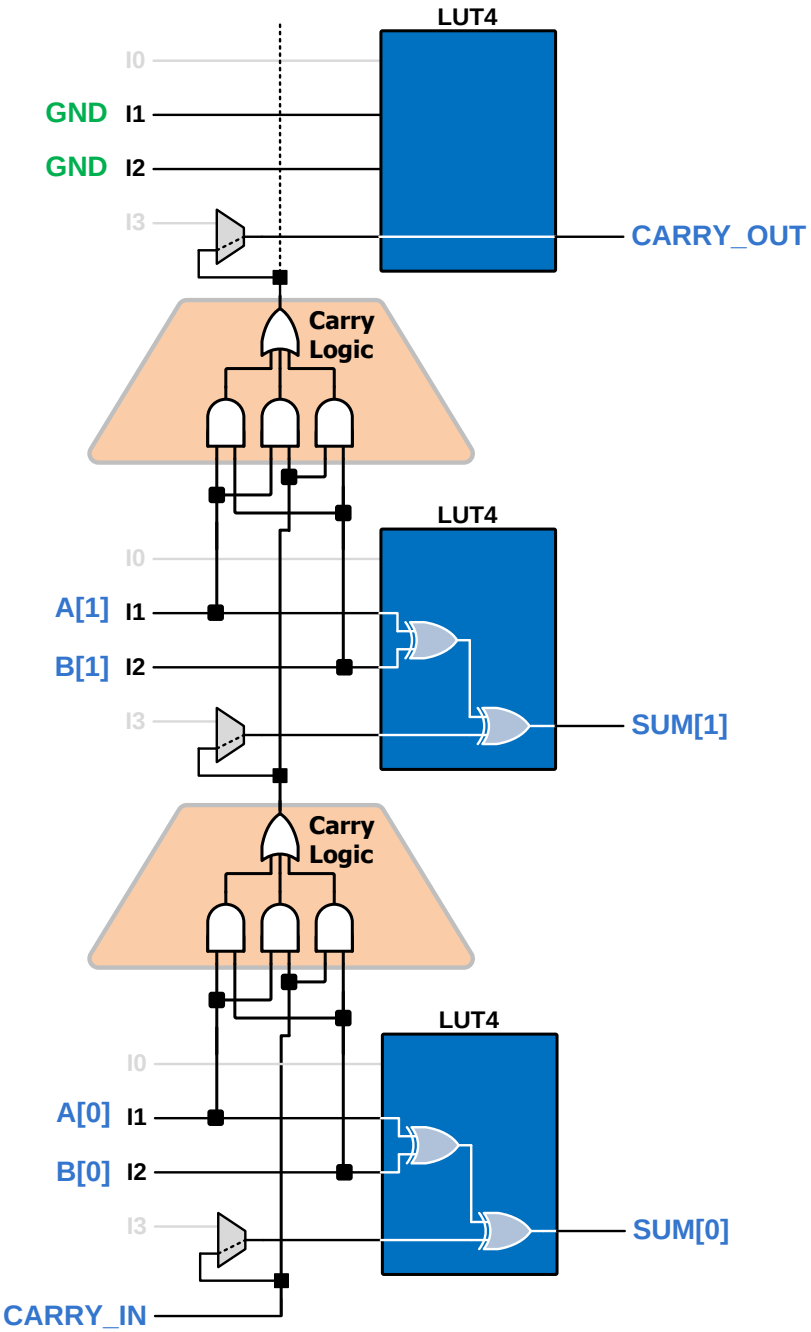
Figure 5: **Carry Logic Structure within a Logic Cell and between PLBs**



Implementing Subtracters, Decrementers

As mentioned earlier, the Carry Logic generates a High output whenever the sum of `I1 + I2 + CARRY_IN` generates a carry. The Carry Logic does not specifically have a subtract mode. To implement a subtract function or decrement function, logically invert either the I1 or I2 input and invert the initial carry input. This performs a 2s complement subtract operation.

Figure 6: Two-bit Adder Example

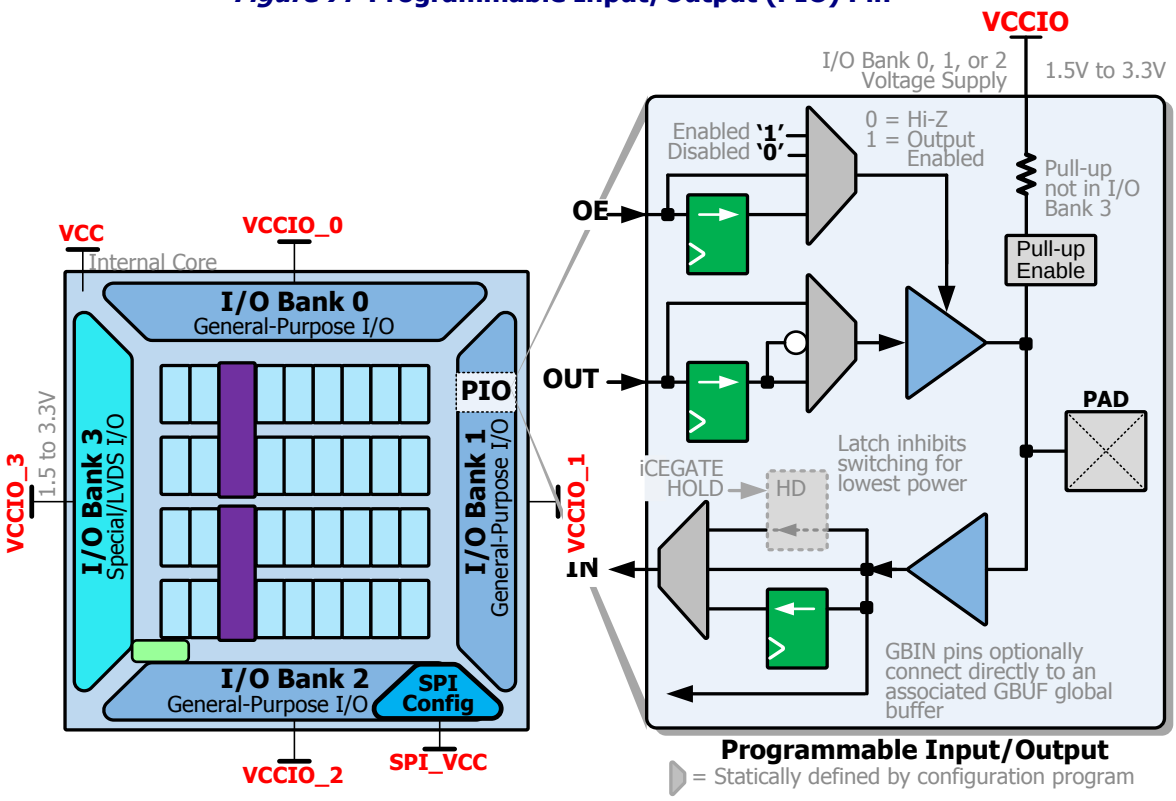


Programmable Input/Output Block (PIO)

Programmable Input/Output (PIO) blocks surround the periphery of the device and connect external components to the Programmable Logic Blocks (PLBs) and RAM4K blocks via programmable interconnect. Individual PIO pins are grouped into one of four I/O banks, as shown in Figure 7. I/O Bank 3 has additional capabilities, including LVDS differential I/O and the ability to interface to Mobile DDR memories.

Figure 7 also shows the logic within a PIO pin. When used in an application, a PIO pin becomes a signal input, an output, or a bidirectional I/O pin with a separate direction control input.

Figure 7: **Programmable Input/Output (PIO) Pin**



I/O Banks

PIO blocks are organized into four separate I/O banks, each with its own voltage supply input, as shown in Table 5. The voltage applied to the VCCIO pin on a bank defines the I/O standard used within the bank. Table 50 and Table 51 describe the I/O drive capabilities and switching thresholds by I/O standard. On iCE65L04 and iCE65L08 devices, I/O Bank 3, along the left edge of the die, is different than the others and supports specialized I/O standards.

I/O Bank Voltage Supply Inputs Support Different I/O Standards

Because each I/O bank has its own voltage supply, iCE65 components become the ideal bridging device between different interface standards. For example, the iCE65 device allows a 1.8V-only processor to interface cleanly with a 3.3V bus interface. The iCE65 device replaces external voltage translators.

Table 5: Supported Voltages by I/O Bank

Bank	Device Edge	Supply Input	3.3V	2.5V	1.8V	1.5V
0	Top	VCCIO_0	Yes	Yes	Yes	Outputs only
1	Right	VCCIO_1	Yes	Yes	Yes	Outputs only
2	Bottom	VCCIO_2	Yes	Yes	Yes	Outputs only
3	Left	VCCIO_3	Yes	Yes	Yes	iCE65L01: Outputs only iCE65L04/08: Yes
SPI	Bottom Right	SPI_VCC	Yes	Yes	Yes	No

If not connected to an external SPI PROM, the four pins associated with the SPI Master Configuration Interface can be used as PIO pins, supplied by the SPI_VCC input, essentially forming a fifth "mini" I/O bank. If using an SPI Flash PROM, then connect SPI_VCC to 3.3V.

I/O Banks 0, 1, 2, SPI and Bank 3 of iCE65L01

Table 6 highlights the available I/O standards when using an iCE65 device, indicating the drive current options, and in which bank(s) the standard is supported. I/O Banks 0, 1, 2 and SPI interface support the same standards. I/O Bank 3 has additional capabilities in iCE65L04 and iCE65L08, including support for MDDR memory standards and LVDS differential I/O.

***Table 6:* I/O Standards for I/O Banks 0, 1, 2, SPI Interface Bank, and Bank 3 of iCE65L01**

I/O Standard	Supply Voltage	Drive Current (mA)	Attribute Name
5V Input Tolerance	3.3V	N/A	N/A
LVCMOS33	3.3V	±11	SB_LVCMOS
LVCMOS25	2.5V	±8	
LVCMOS18	1.8V	±5	
LVCMOS15 outputs	1.5V	±4	

IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank

The IBIS (I/O Buffer Information Specification) file that describes the output buffers used in I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01 is available from the following link.

- IBIS Models for I/O Banks 0, 1, 2, SPI Bank and Bank 3 of iCE65L01

I/O Bank 3 of iCE65L04 and iCE65L08

I/O Bank 3, located along the left edge of the die, has additional special I/O capabilities to support memory components and differential I/O signaling (LVDS). Table 7 lists the various I/O standards supported by I/O Bank 3. The SSTL2 and SSTL18 I/O standards require the VREF voltage reference input pin which is only available on the CB284 package. Also see Table 51 for electrical characteristics.

***Table 7:* I/O Standards for I/O Bank 3 Only of iCE65L04 and iCE65L08**

I/O Standard	Supply Voltage	VREF Pin (CB284 or DiePlus) Required?	Target Drive Current (mA)	Attribute Name
LVCMOS33	3.3V	No	±8	SB_LVCMOS33_8
LVCMOS25	2.5V	No	±16	SB_LVCMOS25_16
			±12	SB_LVCMOS25_12
			±8	SB_LVCMOS25_8
			±4	SB_LVCMOS25_4
LVCMOS18	1.8V	No	±10	SB_LVCMOS18_10
			±8	SB_LVCMOS18_8
			±4	SB_LVCMOS18_4
			±2	SB_LVCMOS18_2
LVCMOS15	1.5V	No	±4	SB_LVCMOS15_4
			±2	SB_LVCMOS15_2
SSTL2_II	2.5V	Yes	±16.2	SB_SSTL2_CLASS_2
SSTL2_I			±8.1	SB_SSTL2_CLASS_1
SSTL18_II	1.8V	Yes	±13.4	SB_SSTL18_FULL
SSTL18_I			±6.7	SB_SSTL18_HALF
MDDR	1.8V	No	±10	SB_MDDR10
			±8	SB_MDDR8
			±4	SB_MDDR4
			±2	SB_MDDR2
LVDS	2.5V	No	N/A	SB_LVDS_INPUT

Table 8 lists the I/O standards that can co-exist in I/O Bank 3, depending on the VCCIO_3 voltage.

***Table 8:* Compatible I/O Standards in I/O Bank 3 of iCE65L04 and iCE65L08**

VCCIO_3 Voltage	3.3V	2.5V	1.8V	1.5V
Compatible I/O Standards	SB_LVCMOS33_8	Any SB_LVCMOS25 SB_SSTL2_Class_2 SB_SSTL2_Class_1 SB_LVDS_INPUT	Any SB_LVCMOS18 SB_SSTL18_FULL SB_SSTL18_HALF SB_MDDR10 SB_MDDR8 SB_MDDR4 SB_MDDR2 SB_LVDS_INPUT	Any SB_LVCMOS15

Programmable Output Drive Strength

Each PIO in I/O Bank 3 offers programmable output drive strength, as listed in Table 8. For the LVCMOS and MDDR I/O standards, the output driver has settings for static drive currents ranging from 2 mA to 16 mA output drive current, depending on the I/O standard and supply voltage.

The SSTL18 and SSTL2 I/O standards offer full- and half-strength drive current options

Differential Inputs and Outputs

All PIO pins support "single-ended" I/O standards, such as LVCMOS. However, iCE65 FPGAs also support differential I/O standards where a single data value is represented by two complementary signals transmitted or received using a pair of PIO pins. The PIO pins in I/O Bank 3 of iCE65L04 and iCE65L08L08 support Low-Voltage Differential Swing (LVDS) and SubLVDS inputs as shown in Figure 8. Differential outputs are available in all four I/O banks.

Differential Inputs Only on I/O Bank 3 of iCE65L04 and iCE65L08

Differential receivers are required for popular applications such as LVDS and LVPECL clock inputs, camera interfaces, and for various telecommunications standards.

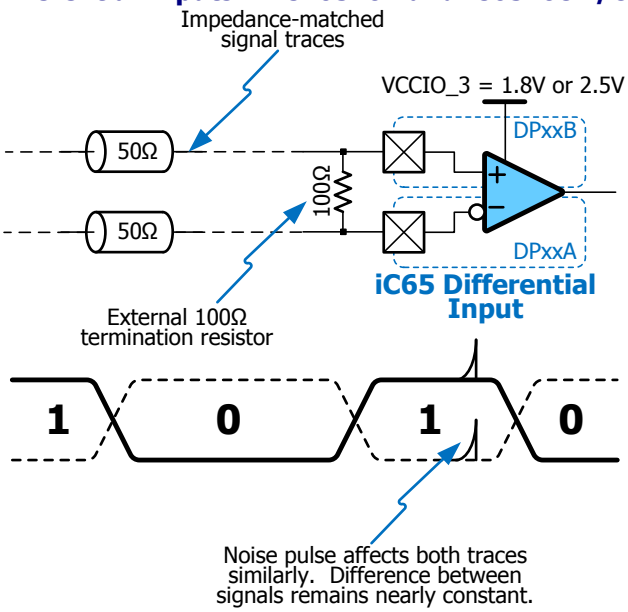
Specific pairs of PIO pins in I/O Bank 3 form a differential input. Each pair consists of a DPxxA and DPxxB pin, where "xx" represents the pair number. The DPxxB receives the true version of the signal while the DPxxA receives the complement of the signal. Typically, the resulting signal pair is routed on the printed circuit board (PCB) with matched 50Ω signal impedance. The differential signaling, the low voltage swing, and the matched signal routing are ideal for communicating very-high frequency signals. Differential signals are generally also more tolerant of system noise and generate little EMI themselves.

The LVDS input circuitry requires 2.5V on the VCCIO_3 voltage supply. Similarly, the SubLVDS input circuitry requires 1.8V on the VCCIO_3 voltage supply. For electrical specifications, see "Differential Inputs" on page 100.

Each differential input pair requires an external 100 Ω termination resistor, as shown in Figure 8.

The PIO pins that make up a differential input pair are indicated with a blue bounding box in the footprint diagrams and in the pinout tables.

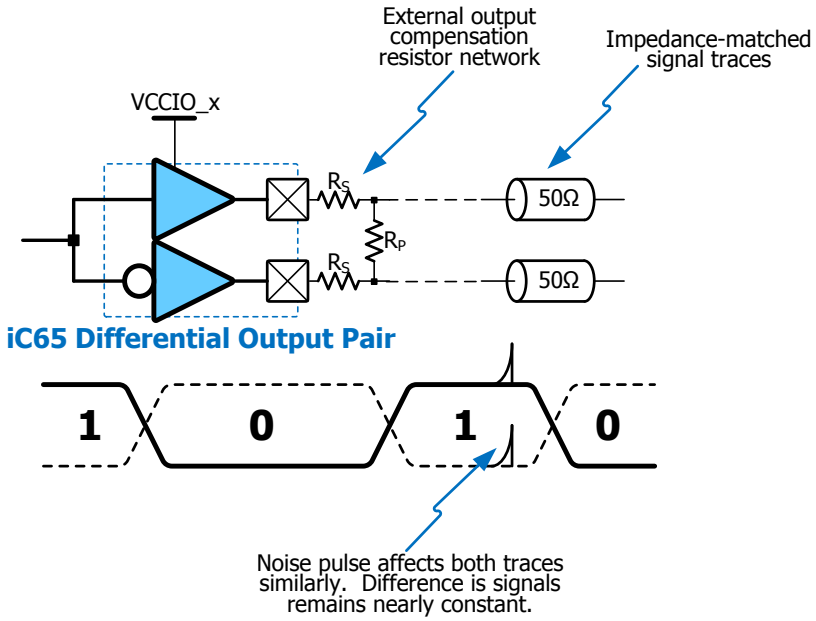
Figure 8: **Differential Inputs in iCE65L04 and iC65L08 I/O Bank 3**



Differential Outputs in Any Bank

Differential outputs are built using a pair of single-ended PIO pins as shown in Figure 9. Each differential I/O pair requires a three-resistor termination network to adjust output characteristic to match those for the specific differential I/O standard. The output characteristics depend on the values of the parallel resistors (RP) and series resistor (RS). Differential outputs must be located in the same I/O tile.

Figure 9: Differential Output Pair



For electrical characteristics, see "Differential Outputs" on page 100.

The PIO pins that make up a differential output pair are indicated with a blue bounding box in the in the tables in "Die Cross Reference" starting on page 84.

Input Signal Path

As shown in Figure 7, a signal from a package pin optionally feeds directly into the device, or is held in an input register. The input signal connects to the programmable interconnect resources through the IN signal. Table 9 describes the input behavior, assuming that the output path is not used or if a bidirectional I/O, that the output driver is in its high-impedance state (Hi-Z). Table 9 also indicates the effect of the Power-Saving I/O Bank iCEgate Latch and the Input Pull-Up Resistors on I/O Banks 0, 1, and 2.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Power-Saving I/O Bank iCEgate Latch

To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control. As shown in Figure 10, the iCEgate HOLD control signal captures the external value from the associated asynchronous input. The HOLD signal prevents switching activity on the PIO pad from affecting internal logic or programmable interconnect. Minimum power consumption occurs when there is no switching. However, individual pins within the I/O bank can bypass the iCEgate latch and directly feed into the programmable interconnect, remaining active during low-power operation. This behavior is described in Table 9. The decision on which asynchronous inputs use the iCEgate feature and which inputs bypass it is determined during system design. In other words, the iCEgate function is part of the source design used to create the iCE65 configuration image.

Figure 10: Power-Saving iCEgate Latch

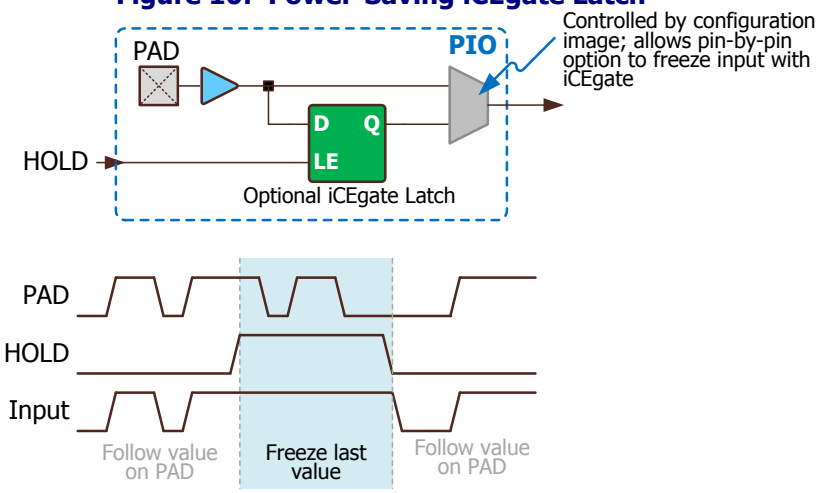


***Table 9:* PIO Non-Registered Input Operations**

Operation	HOLD	Bitstream Setting		PAD	IN
	iCEgate Latch	Controlled by iCEgate?	Input Pull-Up Enabled?	Pin Value	Input Value to Interconnect
Data Input	0	X	X	PAD	PAD Value
Pad Floating, No Pull-up	0	X	No	Z	(Undefined)
Pad Floating, Pull-up	0	X	Yes	Z	1
Data Input, Latch Bypassed	X	No	X	PAD	PAD Value
Pad Floating, No Pull-up, Latch Bypassed	X	No	No	Z	(Undefined)
Pad Floating, Pull-up, Latch Bypassed	X	No	Yes	Z	1
Low Power Mode, Hold Last Value	1	Yes	X	X	Last Captured PAD Value

There are four iCEgate HOLD controls, one per each I/O bank. The iCEgate HOLD control input originates within the interconnect fabric, near the middle of the I/O edge. Consequently, the HOLD signal is optionally controlled externally through a PIO pin or from other logic within the iCE65 device.

For best possible performance, the global buffer inputs (GBIN[7:0]) connect directly to the their associated global buffers (GBUF[7:0]), bypassing the PIO logic and iCEgate circuitry as shown in Figure 7. Consequently, the direct GBIN-to-GBUF connection cannot be blocked by the iCEgate circuitry. However, it is possible to use iCEgate to block PIO-to-GBUF clock connections.

For additional information on using the iCEgate feature, please refer to the following application note.

AN002: Using iCEgate Blocking for Ultra-Low Power

Input Pull-Up Resistors on I/O Banks 0, 1, and 2

The PIO pins in I/O Banks 0, 1, and 2 have an optional input pull-up resistor. Pull-up resistors are not provided in iCE65L04 and iCE65L08 I/O Bank 3. During the iCE65 configuration process, the input pull-up resistor is unconditionally enabled and pulls the input to within a diode drop of the associated I/O bank supply voltage (VCCIO_#). This prevents any signals from floating on the circuit board during configuration.

After iCE65 configuration is complete, the input pull-up resistor is optional, defined by a configuration bit. The pull-up resistor is also useful to tie off unused PIO pins. The Lattice iCEcube development software defines all unused PIO pins in I/O Banks 0, 1 and 2 as inputs with the pull-up resistor turned on. The pull-up resistor value depends on the VCCIO voltage applied to the bank, as shown in Table 49.

Note: JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, else VCCIO_1 draws current.

No Input Pull-up Resistors on I/O Bank 3 of iCE65L04 and iCE65L08

The PIO pins in I/O Bank 3 do not have an internal pull-up resistor. To minimize power consumption, tie unused PIO pins in Bank 3 to a known logic level or drive them as a disabled high-impedance output.

Input Hysteresis

Inputs typically have about 50 mV of hysteresis, as indicated in Table 49.

Output and Output Enable Signal Path

As shown in Figure 7, a signal from programmable interconnect feeds the OUT signal on a Programmable I/O pad. This output connects either directly to the associated package pin or is held in an optional output flip-flop. Because all flip-flops are automatically reset after configuration, the output from the output flip-flop can be optionally inverted so that an active-Low output signal is held in the disabled (High) state immediately after configuration.

Similarly, each Programmable I/O pin has an output enable or three-state control called OE. When OE = High, the OUT output signal drives the associated pad, as described in Table 10. When OE = Low, the output driver is in the high-impedance (Hi-Z) state. The OE output enable control signal itself connects either directly to the output buffer or is held in an optional register. The output buffer is optionally permanently enabled or permanently disabled, either to unconditionally drive output signals, or to allow input-only signals.

Table 10: **PIO Output Operations (non-registered operation, no inversions)**

Operation	OUT Data Output	OE Enable	PAD
Three-State	X	0	Hi-Z
Drive Output Data	OUT	1*	OUT

X = don't care, 1* = High or unused, Hi-Z = high-impedance, three-stated, floating.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Input and Output Register Control per PIO Pair

PIO pins are grouped into pairs for synchronous control. Registers within pairs of PIO pins share common input clock, output clock, and I/O clock enable control signals, as illustrated in Figure 11. The combinational logic paths are removed from the drawing for clarity.

The INCLK clock signal only controls the input flip-flops within the PIO pair.

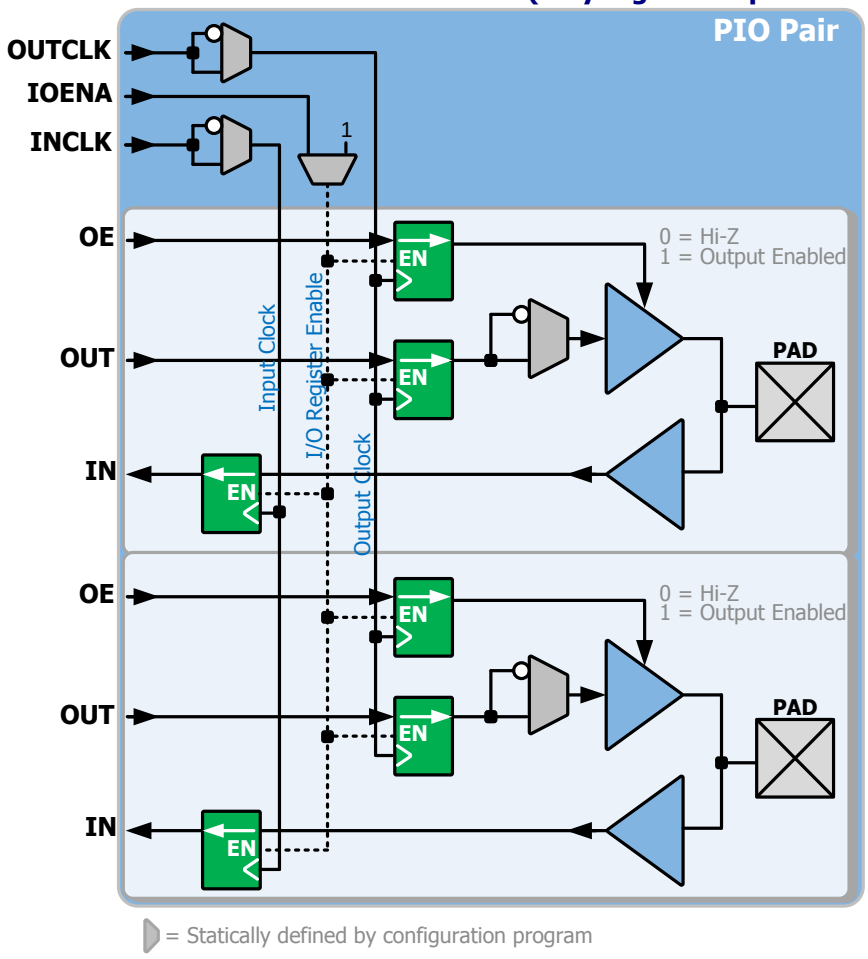
The OUTCLK clock signal controls the output flip-flops and the output-enable flip-flops within the PIO pair.

If desired in the iCE65 application, the INCLK and OUTCLK signals can be connected together.

The IOENA clock-enable input, if used, enables all registers in the PIO pair, as shown in Figure 11. By default, the registers are always enabled.

Before laying out your printed-circuit board, run the design through the iCEcube development software to verify that your selected pinout complies with these I/O register pairing requirements. See tables in "Die Cross Reference" starting on page 84.

Figure 11: **PIO Pairs Share Clock and Clock Enable Controls (only registered paths shown for clarity)**

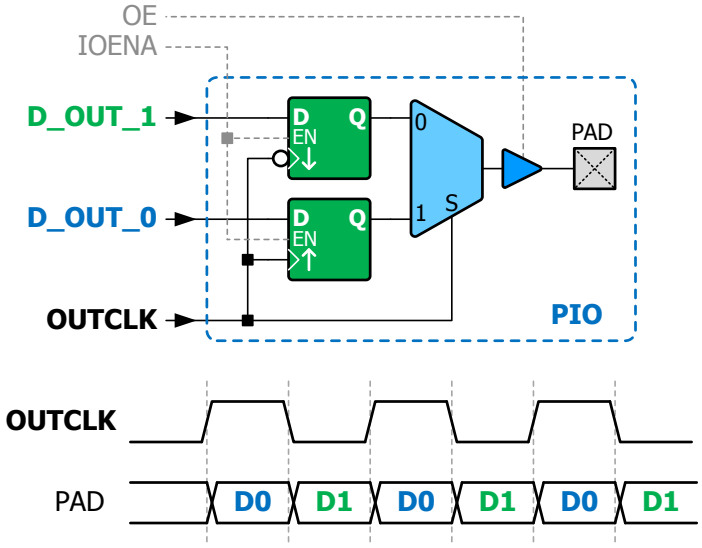


The pairing of PIO pairs is most evident in the tables in "Die Cross Reference" starting on page 84.

Double Data Rate (DDR) Flip-Flops

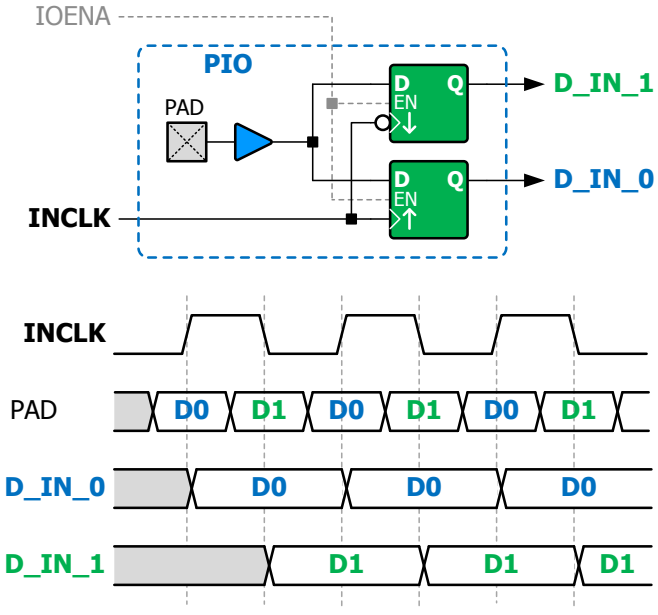
Each individual PIO pin optionally has two sets of double data rate (DDR) flip-flops; one input pair and one output pair. Figure 12 demonstrates the functionality of the output DDR flip-flop. Two signals from within the iCE65 device drive the DDR output flip-flop. The D_OUT_0 signal is clocked by the rising edge of the OUTCLK signal while the D_OUT_1 signal is clocked by the falling edge of the OUTCLK signal, assuming no optional clock polarity inversion. Internally, the two individual flip-flops are multiplexed together before the data appears at the pad, effectively doubling the output data rate.

Figure 12: DDR Output Flip-Flop



Similarly, Figure 13 demonstrates the DDR input flip-flop functionality. A double data rate (DDR) signal arrives at the pad. Internally, one value is clocked by the rising edge of the INCLK signal and another value is clocked by the falling edge of the INCLK signal. The DDR data stream is effectively de-multiplexed within the PIO pin and presented to the programmable interconnect on D_IN_0 and D_IN_1.

Figure 13: DDR Input Flip-Flop



The DDR flip-flops provide several design advantages. Internally within the iCE65 device, the clock frequency is half the effective external data rate. The lower clock frequency eases internal timing, doubling the clock period, and slashes the clock-related power in half.

Global Routing Resources

Global Buffers

Each iCE65 component has eight global buffer routing connections, illustrated in Figure 14. There are eight high-drive buffers, connected to the eight low-skew, global lines. These lines are designed primarily for clock distribution but are also useful for other high-fanout signals such as set/reset and enable signals. The global buffers originate either from the Global Buffer Inputs (GBINx) or from programmable interconnect. The associated GBINx pin represents the best pin to drive a global buffer from an external source. However, the application with an iCE65 FPGA can also drive a global buffer via any other PIO pin or from internal logic using the programmable interconnect.

If not used in an application, individual global buffers are turned off to save power.

Figure 14: **High-drive, Low-skew, High-fanout Global Buffer Routing Resources**

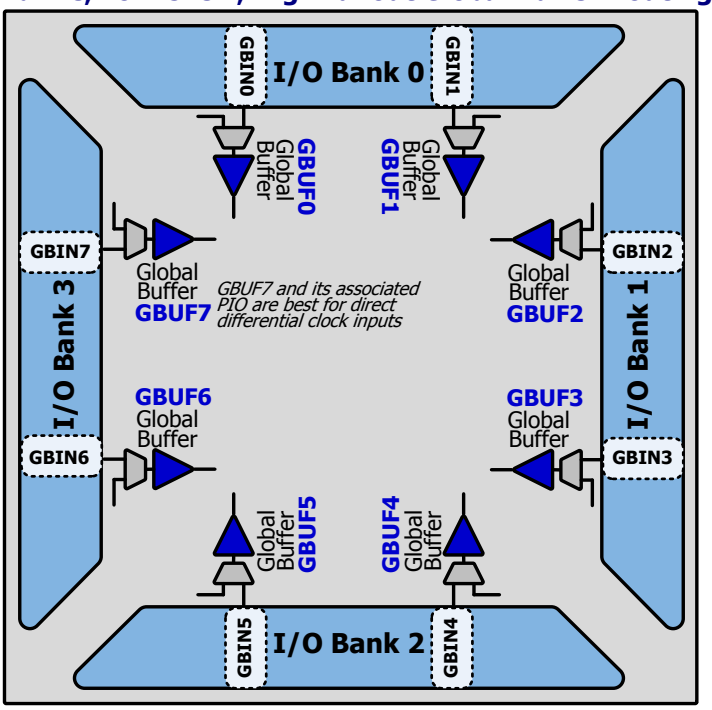


Table 11 lists the connections between a specific global buffer and the inputs on a Programmable Logic Block (PLB). All global buffers optionally connect to all clock inputs. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

Table 11: **Global Buffer (GBUF) Connections to Programmable Logic Block (PLB)**

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF buffers	Yes	Yes	No
GBUF1		Yes	No	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	No	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	No	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	No	Yes

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

The PIO clock enable connect is different between the iCE65L01/iCE65L04 and iCE65L08.

Table 12: **iCE65L01 & iCE65L04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	No
GBUF1		Yes	Yes	Yes
GBUF2		Yes	Yes	No
GBUF3		Yes	Yes	Yes
GBUF4		Yes	Yes	No
GBUF5		Yes	Yes	Yes
GBUF6		Yes	Yes	No
GBUF7		Yes	Yes	Yes

Table 13: **iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

Global Buffer	Output Connections	Input Clock	Output Clock	Clock Enable
GBUF0	No (connect through PLB LUT)	Yes	Yes	Yes
GBUF1		Yes	Yes	No
GBUF2		Yes	Yes	Yes
GBUF3		Yes	Yes	No
GBUF4		Yes	Yes	Yes
GBUF5		Yes	Yes	No
GBUF6		Yes	Yes	Yes
GBUF7		Yes	Yes	No

Global Buffer Inputs

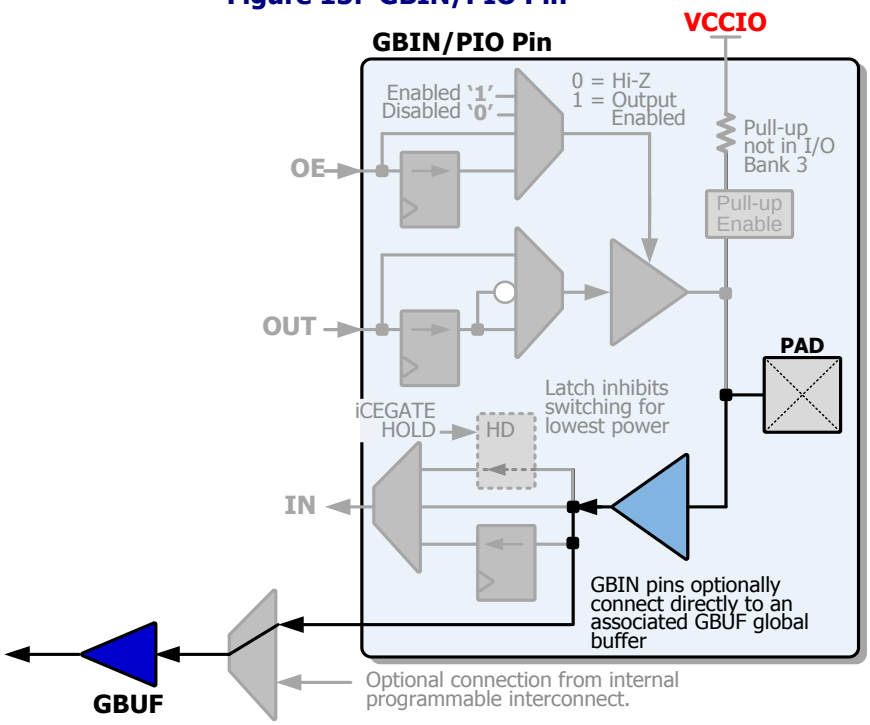
The iCE65 component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 15, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 14 and the pin locations for each GBIN input appear in Table 14.

Table 14: **Global Buffer Input Ball/Pin Number by Package**

Global Buffer Input (GBIN)	I/O Bank	VQ100	CB132	`L04 CB196	`L08 CB196	CB284
GBIN0	0	90	A6	A7	A7	E10
GBIN1		89	A7	E7	E7	E11
GBIN2	1	63	G14	F10	F10	L18
GBIN3		62	F14	G12	G12	K18
GBIN4	2	34	P8	L7	N8	V12
GBIN5		33	P7	P5	M7	V11
GBIN6	3	15	H1	H1	H1	M5
GBIN7		13	G1	G1	H3	L5

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

Figure 15: GBIN/PIO Pin



Differential Global Buffer Input

All eight global buffer inputs support single-ended I/O standards such as LVCMOS. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct SubLVDS, LVDS, or LVPECL differential clock input, as shown in Figure 16. The GBIN7 and its associated differential I/O pad accept a differential clock signal. A 100 Ω termination resistor is required across the two pads. Optionally, swap the outputs from the LVDS or LVPECL clock driver to invert the clock as it enters the iCE65 device.

Figure 16: LVDS or LVPECL Clock Input

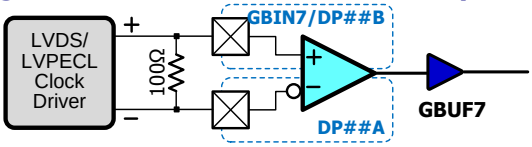


Table 15 lists the pin or ball numbers for the differential global buffer input by package style. Although this differential input is the only one that connects directly to a global buffer, other differential inputs can connect to a global buffer using general-purpose interconnect, with slightly more signal delay.

***Table 15:* Differential Global Buffer Input Ball/Pin Number by Package**

Differential Global Buffer Input (GBIN)	I/O Bank	VQ100	CB132	'L04 CB196	'L08 CB196	CB284
GBIN7/DPxxB	3	13	N/A	G1	H3	L5
DPxxA		12	N/A	G2	H4	L3

The differential global buffer input is not available for iCE65 devices in the CB132 package. This restriction is an artifact of the pin compatibility between the CB132 and CB284 package.

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

Automatic Global Buffer Insertion, Manual Insertion

The iCEcube development software automatically assigns high-fanout signals to a global buffer. However, to manual insert a global buffer input/global buffer (GBIN/GBUF) combination, use the **SB_IO_GB** primitive. To insert just a global buffer (GBUF), use the **SB_GB** primitive.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE65 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user-I/O pins into their high-impedance state. Similarly, the PIO pins can be forced into their high-impedance state via the JTAG controller.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE65 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application. See Table 3 for more information.

The PIO flip-flops are always reset during configuration, although the output flip-flop can be inverted before leaving the iCE65 device, as shown in Figure 11.

RAM

Each iCE65 device includes multiple high-speed synchronous RAM blocks (RAM4K), each 4Kbit in size. As shown in Table 16 a single iCE65 integrates between 16 to 96 such blocks. Each RAM4K block is generically a 256-word deep by 16-bit wide, two-port register file, as illustrated in Figure 17. The input and output connections, to and from a RAM4K block, feed into the programmable interconnect resources.

Figure 17: RAM4K Memory Block

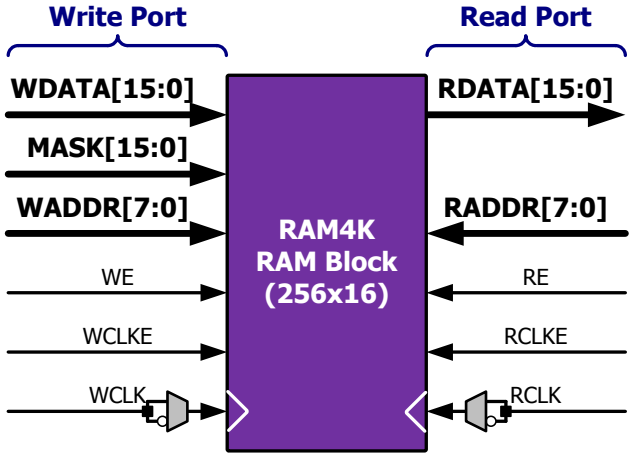


Table 16: RAM4K Blocks per Device

Device	RAM4K Blocks	Default Configuration	RAM Bits per Block	Block RAM Bits
iCE65L01	16	256 x 16	4K (4,096)	64K
iCE65L04	20			80K
iCE65L08	32			128K

Using programmable logic resources, a RAM4K block implements a variety of logic functions, each with configurable input and output data width.

- Random-access memory (RAM)
  - Single-port RAM with a common address, enable, and clock control lines
  - Two-port RAM with separate read and write control lines, address inputs, and enable

- Register file and scratchpad RAM
- First-In, First-Out (FIFO) memory for data buffering applications
- Circuit buffer
- A 256-deep by 16-wide ROM with registered outputs, contents loaded during configuration
  - Sixteen different 8-input look-up tables
  - Function or waveform tables such as sine, cosine, etc.
  - Correlators or pattern matching operations
- Counters, sequencers

As pictured in Figure 17, a RAM4K block has separate write and read ports, each with independent control signals. Table 17 lists the signals for both ports. Additionally, the write port has an active-Low bit-line write-enable control; optionally mask write operations on individual bits. By default, input and output data is 16 bits wide, although the data width is configurable using programmable logic and, if needed, multiple RAM4K blocks.

The WCLK and RCLK inputs optionally connect to one of the following clock sources.

- The output from any one of the eight Global Buffers, or
- A connection from the general-purpose interconnect fabric

The data contents of the RAM4K block are optionally pre-loaded during iCE65 device configuration. If the RAM4K blocks are not pre-loaded during configuration, then the resulting configuration bitstream image is smaller. However, if an uninitialized RAM4K block is used in the application, then the application must initialize the RAM contents to guarantee the data value.

See Table 56 for detailed timing information.

Signals

Table 17 lists the signal names, direction, and function of each connection to the RAM4K block. See also Figure 17.

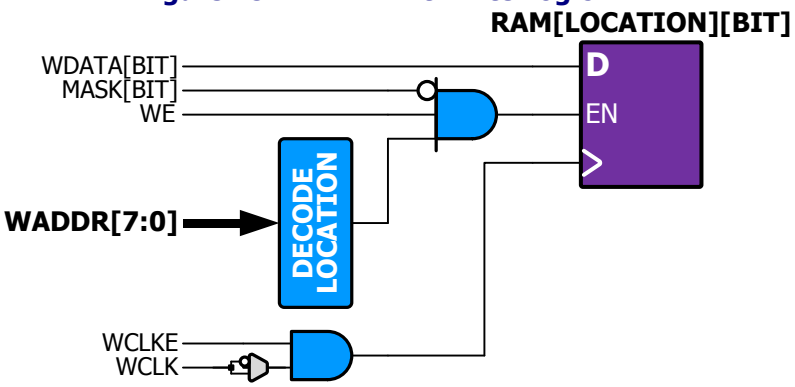
Table 17: RAM4K Block RAM Signals

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = Write bit; 1 = Don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

Write Operations

Figure 18 shows the logic involved in writing a data bit to a RAM location. Table 18 describes various write operations for a RAM4K block. By default, all RAM4K write operations are synchronized to the rising edge of WCLK although the clock is invertible as shown in Figure 18.

Figure 18: RAM4K Bit Write Logic



When the WCLKE signal is Low, the clock to the RAM4K block is disabled, keeping the RAM in its lowest power mode.

Table 18: RAM4K Write Operations

Operation	WDATA[15:0] Data	MASK[15:0] Mask Bit	WADDR[7:0] Address	WE Write Enable	WCLKE Clock Enable	WCLK Clock	RAM Location
Disabled	X	X	X	X	X	0	No change
Disabled					0	X	No change
Disabled	X	X	X	0	X	X	No change
Write Data	WDATA[i]	MASK[i] = 0	WADDR	1	1	↑	RAM[WADDR][i] = WDATA[i]
Masked Write	X	MASK[i] = 1	WADDR	1	1	↑	RAM[WADDR][i] = No change

To write data into the RAM4K block, perform the following operations.

- Supply a valid address on the WADDR[7:0] address input port
- Supply valid data on the WDATA[15:0] data input port
- To write or mask selected data bits, set the associated MASK input port accordingly. For example, write operations on data bit D[i] are controlled by the associated MASK[i] input.
  - MASK[i] = 0: Write operations are enabled for data line WDATA[i]
  - MASK[i] = 1: Mask write operations are disabled for data line WDATA[i]
- Enable the RAM4K write port (WE = 1)
- Enable the RAM4K write clock (WCLKE = 1)
- Apply a rising clock edge on WCLK (assuming that the clock is not inverted)

Read Operations

Figure 19 shows the logic involved in reading a location from RAM. Table 19 describes various read operations for a RAM4K block. By default, all RAM4K read operations are synchronized to the rising edge of RCLK although the clock is invertible as shown in Figure 19.

Figure 19: RAM4K Read Logic

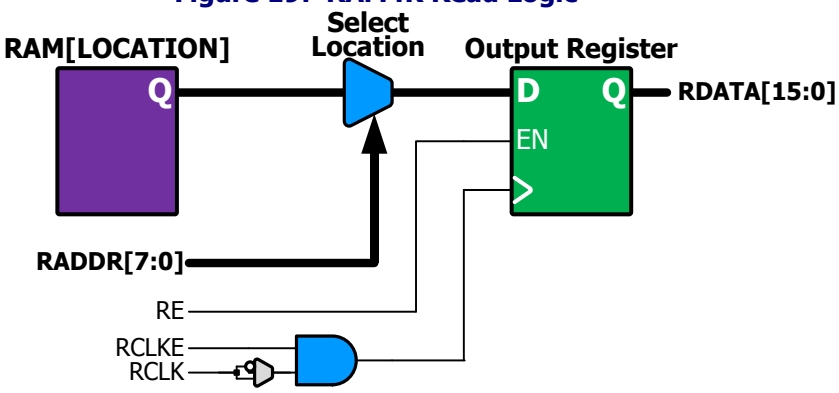


Table 19: RAM4K Read Operations

Operation	RADDR[7:0] Address	RE Read Enable	RCLKE Clock Enabe	RCLK Clock	RDATA[15:0]
After configuration, before first valid Read Data operation	X	X	X	X	Undefined
Disabled	X	X	X	0	No Change
Disabled		X	0	X	No Change
Disabled	X	0	X	X	No change
Read Data	RADDR	1	1	↑	RAM[RADDR]

To read data from the RAM4K block, perform the following operations.

- Supply a valid address on the RADDR[7:0] address input port
- Enable the RAM4K read port (RE = 1)
- Enable the RAM4K read clock (RCLKE = 1)
- Apply a rising clock edge on RCLK
- After the clock edge, the RAM contents located at the specified address (RADDR) appear on the RDATA output port

Read Data Register Undefined Immediately after Configuration

Unlike the flip-flops in the Programmable Logic Blocks and Programmable I/O pins, the RDATA[15:0] read data output register is not automatically reset after configuration. Consequently, immediately following configuration and before the first valid Read Data operation, the initial RDATA[15:0] read value is undefined.

Pre-loading RAM Data

The data contents for a RAM4K block can be optionally pre-loaded during iCE65 configuration. If not pre-loaded during configuration, then the RAM contents must be initialized by the iCE65 application before the RAM contents are valid.

Pre-loading the RAM data in the configuration bitstream increases the size of the configuration image accordingly.

RAM Contents Preserved during Configuration

RAM contents are preserved (write protected) during configuration, assuming that voltage supplies are maintained throughout. Consequently, data can be passed between multiple iCE65 configurations by leaving it in a RAM4K block and then skipping pre-loading during the subsequent reconfiguration. See "Cold Boot Configuration Option" and "Warm Boot Configuration Option" for more information.

Low-Power Setting

To place a RAM4K block in its lowest power mode, keep WCLKE = 0 and RCLKE = 0. In other words, when not actively using a RAM4K block, disable the clock inputs.

Device Configuration

As described in Table 20, iCE65 components are configured for a specific application by loading a binary configuration bitstream image, generated by the Lattice development system. For high-volume applications, the bitstream image is usually permanently programmed in the on-chip NVCM, However, the bitstream image can also be stored external in a standard, low-cost commodity SPI serial Flash PROM. The iCE65 component can automatically load the image using the SPI Master Configuration Interface. Similarly, the iCE65 configuration data can be downloaded from an external processor, microcontroller, or DSP processor using an SPI-like serial interface or an IEEE 1149 JTAG interface.

Table 20: **iCE65 Device Configuration Modes**

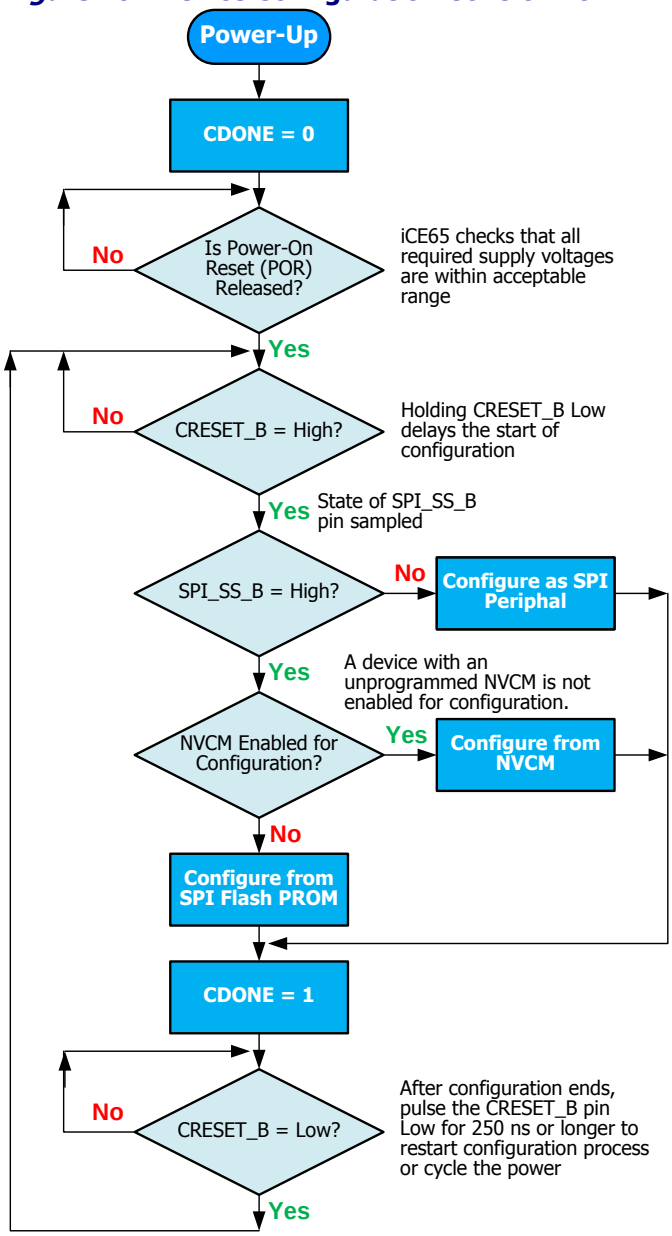
Mode	Analogy	Configuration Data Source
NVCM	ASIC	Internal, lowest-cost, secure, one-time programmable Nonvolatile Configuration Memory (NVCM)
SPI Flash	Microprocessor	External, low-cost, commodity, SPI serial Flash PROM
SPI Peripheral	Processor Peripheral	Configured by external device, such as a processor, microcontroller, or DSP using practically any data source, such as system Flash, a disk image, or over a network connection.
JTAG	JTAG	JTAG configuration requires sending a special command sequence on the SPI interface to enable JTAG configuration. Configuration is controlled by and external device.

Configuration Mode Selection

The iCE65 configuration mode is selected according to the following priority described below and illustrated in Figure 20.

- After exiting the Power-On Reset (POR) state or when CRESET_B returns High after being held Low for 250 ns or more, the iCE65 FPGA samples the logical value on its SPI_SS_B pin. Like other programmable I/O pins, the SPI_SS_B pin has an internal pull-up resistor (see Input Pull-Up Resistors on I/O Banks 0, 1, and 2).
- If the SPI_SS_B pin is sampled as a logic '1' (High), then …
  - Check if the iCE65 is enabled to configure from the Nonvolatile Configuration Memory (NVCM). If the iCE65 device has NVCM memory ('**F**' ordering code) but the NVCM is yet unprogrammed, then the iCE65 device is not enabled to configure from NVCM. Conversely, if the NVCM is programmed, the iCE65 device will configure from NVCM.
    - If enabled to configure from NVCM, the iCE65 device configures itself using NVCM.
    - If not enabled to configure from NVCM, then the iCE65 FPGA configures using the SPI Master Configuration Interface.
- If the SPI_SS_B pin is sampled as a logic '0' (Low), then the iCE65 device waits to be configured from an external controller or from another iCE65 device in SPI Master Configuration Mode using an SPI-like interface.

Figure 20: **Device Configuration Control Flow**



Configuration Image Size

Table 23 shows the number of memory bits required to configure an iCE65 device. Two values are provided for each device. The "Logic Only" value indicates the minimum configuration size, the number of bits required to configure only the logic fabric, leaving the RAM4K blocks uninitialized. The "Logic + RAM4K" column indicates the maximum configuration size, the number of bits to configure the logic fabric and to pre-initialize all the RAM4K blocks.

Table 21: **iCE65 Configuration Image Size (Kbits)**

Device	MINIMUM Logic Only (RAM4K not initialized)	MAXIUM Logic + RAM4K (RAM4K pre-initialized)
iCE65L01	181 Kbits	245 Kbits*
iCE65L04	453 Kbits	533 Kbits
iCE65L08	929 Kbits	1,057 Kbits

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM)

All standard iCE65 devices have an internal, nonvolatile configuration memory (NVCM). The NVCM is large enough to program a complete iCE65 device, including initializing all RAM4K block locations (MAXIMUM column in Table 23. The NVCM memory also has very high programming yield due to extensive error checking and correction (ECC) circuitry.

The NVCM is ideal for cost-sensitive, high-volume production applications, saving the cost and board space associated with an external configuration PROM. Furthermore, the NVCM provides exceptional design security, protecting critical intellectual property (IP). The NVCM contents are entirely contained within the iCE65 device and are not readable once protected by the one-time programmable Security bits. Furthermore, there is no observable difference between a programmed or un-programmed memory cell using optical or electron microscopy.

The NVCM memory has a programming interface similar to a 25-series SPI serial Flash PROM. Consequently, it can be programmed using standard device programmers before or after circuit board assembly or programmed in-system from a microprocessor or other intelligent controller. NVCM programming requires VCCIO_1, Bank 1 voltage to be applied on power-up, at the same time as other voltage supplies.

Configuration Control Signals

The iCE65 configuration process is self-timed and controlled by a few internal signals and device I/O pins, as described in Table 22.

Table 22: **iCE65 Configuration Control Signals**

Signal Name	Direction	Description
POR	Internal control	Internal Power-On Reset (POR) circuit.
OSC	Internal control	Internal configuration oscillator.
CRESET_B	Input	Configuration Reset input. Active-Low. No internal pull-up resistor.
CDONE	Open-drain Output	Configuration Done output. Permanent, weak pull-up resistor to VCCIO_2.

The Power-On Reset circuit, POR, automatically resets the iCE65 component to a known state during power-up (cold boot). The POR circuit monitors the relevant voltage supply inputs, as shown in Figure 22. Once all supplies exceed their minimum thresholds, the configuration controller can start the configuration process.

The configuration controller begins configuring the iCE65 device, clocked by the Internal Oscillator, OSC. The OSC oscillator continues controlling configuration unless the iCE65 device is configured using the SPI Peripheral Configuration Interface.

Figure 21: iCE65 Configuration Control Pins

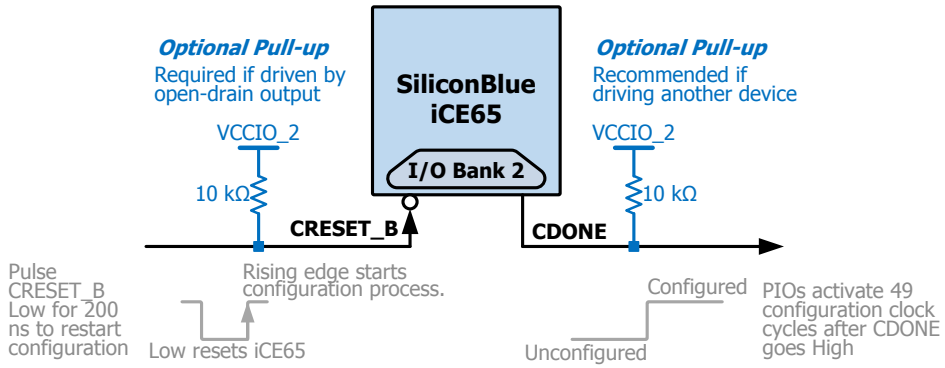


Figure 21 shows the two iCE65 configuration control pins, CRESET_B and CDONE. Table 23 lists the ball/pin numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65 device. When CRESET_B returns High, the iCE65 FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

***Table 23:* Configuration Control Ball/Pin Numbers by Package**

Configuration Control Pins	CB81	QN84	VQ100	CB132	CB196	CB284
CRESET_B	J6	A21	44	L10	L10	R14
CDONE	H6	B16	43	M10	M10	T14

The iCE65 device signals the end of the configuration process by actively turning off the internal pull-down transistor on the Configuration Done output pin, CDONE. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. If the iCE65 device drives other devices, then optionally connect the CDONE pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

The PIO pins activate according to their configured function after 49 configuration clock cycles. The internal oscillator is the configuration clock source for the SPI Master Configuration Interface and when configuring from

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM). When using the SPI Peripheral Configuration Interface, the configuration clock source is the SPI_SCK clock input pin.

Internal Oscillator

During SPI Master or NVCM configuration mode, the controlling clock signal is generated from an internal oscillator. The oscillator starts operating at the Default frequency. During the configuration process, however, bit settings within the configuration bitstream can specify a higher-frequency mode in order to maximize SPI bandwidth and reduce overall configuration time. See Table 57: Internal Oscillator Frequency on page 105 for the specified oscillator frequency range.

Using the SPI Master Configuration Interface, internal oscillator controls all the interface timing and clocks the SPI serial Flash PROM via the SPI_SCK clock output pin.

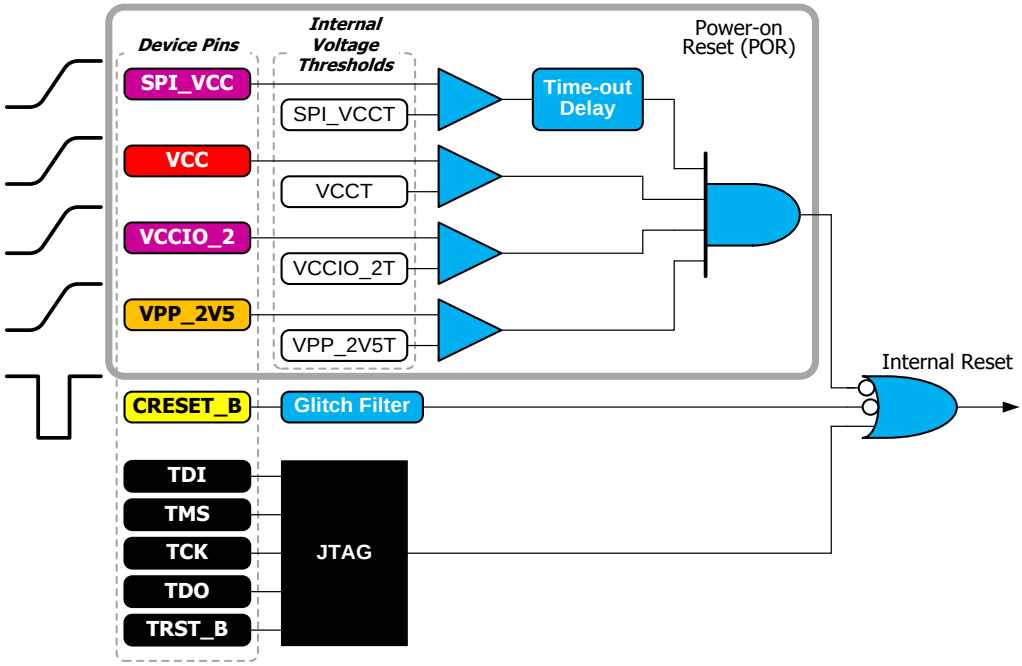
The oscillator output, which also supplies the SPI SCK clock output during the SPI Flash configuration process, has a 50% duty cycle.

Internal Device Reset

Figure 22 presents the various signals that internally reset the iCE65 internal logic.

- Power-On Reset (POR)
- CRESET_B Pin
- JTAG Interface

Figure 22: iCE65 Internal Reset Circuitry



Power-On Reset (POR)

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 24 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

***Table 24:* Power-on Reset (POR) Voltage Resources**

Supply Rail	iCE65 Production Devices
VCC	Yes
SPI_VCC	Yes
VCCIO_1	No
VCCIO_2	Yes
VPP_2V5	Yes

CRESET_B Pin

The CRESET_B pin resets the iCE65 internal logic when Low.

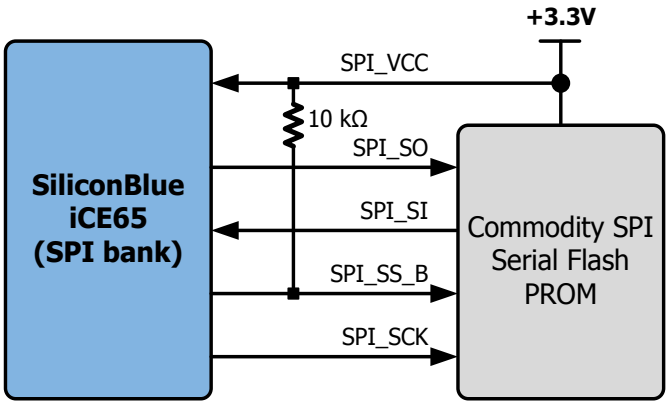
JTAG Interface

Specific command sequences also reset the iCE65 internal logic.

SPI Master Configuration Interface

All iCE65 devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 23. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

Figure 23: **iCE65 SPI Master Configuration Interface**



The SPI configuration interface is used primarily during development before mass production, where the configuration is then permanently programmed in the NVCM configuration memory. However, the SPI interface can also be the primary configuration interface allowing easy in-system upgrades and support for multiple configuration images.

The SPI control signals are defined in Table 25. Table 26 lists the SPI interface ball or pins numbers by package.

Table 25: **SPI Master Configuration Interface Pins (SPI_SS_B High before Configuration)**

Signal Name	Direction	Description
SPI_VCC	Supply	SPI Flash PROM voltage supply input.
SPI_SO	Output	SPI Serial Output from the iCE65 device.
SPI_SI	Input	SPI Serial Input to the iCE65 device, driven by the select SPI serial Flash PROM.
SPI_SS_B	Output	SPI Slave Select output from the iCE65 device. Active Low.
SPI_SCK	Output	SPI Slave Clock output from the iCE65 device.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Table 26: **SPI Interface Ball/Pin Numbers by Package**

SPI Interface	VQ100	CB132	CB196	CB284
SPI_VCC	50	L11	L11	R15
PIOS/SPI_SO	45	M11	M11	T15
PIOS/SPI_SI	46	P11	P11	V15
PIOS/SPI_SS_B	49	P13	P13	V17
PIOS/SPI_SCK	48	P12	P12	V16

SPI PROM Requirements

The iCE65 mobileFPGA SPI Flash configuration interface supports a variety of SPI Flash memory vendors and product families. However, Lattice Semiconductor does not specifically test, qualify, or otherwise endorse any specific SPI Flash vendor or product family. The iCE65 SPI interface supports SPI PROMs that they meet the following requirements.

- The PROM must operate at 3.3V or 2.5V in order to trigger the iCE65 FPGA's power-on reset circuit.
- The PROM must support the `0x0B` Fast Read command, using a 24-bit start address and has 8 dummy bits before the PROM provides first data (see Figure 25: SPI Fast Read Command).
- The PROM must have enough bits to program the iCE65 device (see Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images).
- The PROM must support data operations at the upper frequency range for the selected iCE65 internal oscillator frequency (see Table 57). The oscillator frequency is selectable when creating the FPGA bitstream image.

- For lowest possible power consumption after configuration, the PROM should also support the 0xB9 Deep Power Down command and the 0xAB Release from Deep Power-down Command (see Figure 24 and Figure 26). The low-power mode is optional.
- The PROM must be ready to accept commands 10 µs after meeting its power-on conditions. In the PROM data sheet, this may be specified as t_{VSL} or t_{VCSL}. It is possible to use slower PROMs by holding the CRESET_B input Low until the PROM is ready, then releasing CRESET_B, either under program control or using an external power-on reset circuit.

The Lattice iCEman65 development board and associated programming software uses an ST Micro/Numonyx M25Pxx SPI serial Flash PROM.

SPI PROM Size Requirements

Table 27 lists the minimum SPI PROM size required to configure an iCE65 device. Larger PROM sizes are allowed, but not required unless the end application uses the additional space. SPI serial PROM sizes are specified in bits. For each device size, the table shows the required minimum PROM size for "Logic Only" (no BRAM initialization) and "Logic + RAM4K" (RAM4K blocks pre-initialized). Furthermore, the table shows the PROM size for varying numbers of configuration images. Most applications will use a single image. Applications that use the Cold Boot or Warm Boot features may use more than one image.

Table 27: Smallest SPI PROM Size (bits), by Device, by Number of Images

Device	1 Image		2 Images		3 Images		4 Images	
	Logic Only	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**	**Logic Only**	**Logic + RAM4K**
iCE65L01	256K	256K	512K	512K	1M	1M	1M	1M
iCE65L04	512K	1M	1M	2M	2M	2M	2M	4M
iCE65L08	1M	2M	2M	4M	4M	4M	4M	8M

Enabling SPI Configuration Interface

To enable the SPI configuration mode, the SPI_SS_B pin must be allowed to float High. The SPI_SS_B pin has an internal pull-up resistor. If SPI_SS_B is Low, then the iCE65 component defaults to the SPI Slave configuration mode.

SPI Master Configuration Process

The iCE65 SPI Master Configuration Interface supports a variety of modern, high-density, low-cost SPI serial Flash PROMs. Most modern SPI PROMs include a power-saving Deep Power-down mode. The iCE65 component exploits this mode for additional system power savings.

The iCE65 SPI interface starts by driving SPI_SS_B Low, and then sends a Release from Power-down command to the SPI PROM, hexadecimal command code 0xAB. Figure 24 provides an example waveform. This initial command wakes up the SPI PROM if it is already in Deep Power-down mode. If the PROM is not in Deep Power-down mode, the extra command has no adverse affect other than that it requires a few additional microseconds during the configuration process. The iCE65 device transmits data on the SPI_SO output, on the falling edge of the SPI_SCK output. The SPI PROM does not provide any data to the iCE65 device's SPI_SI input. After sending the last command bit, the iCE65 device de-asserts SPI_SS_B High, completing the command. The iCE65 device then waits a minimum of 10 µS before sending the next SPI PROM command.

Figure 24: **SPI Release from Deep Power-down Command**

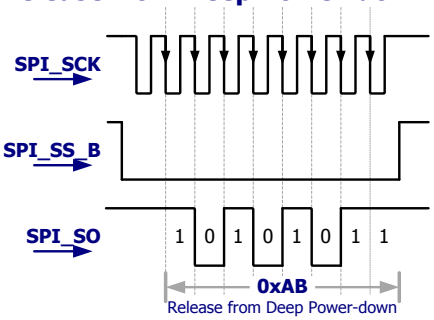
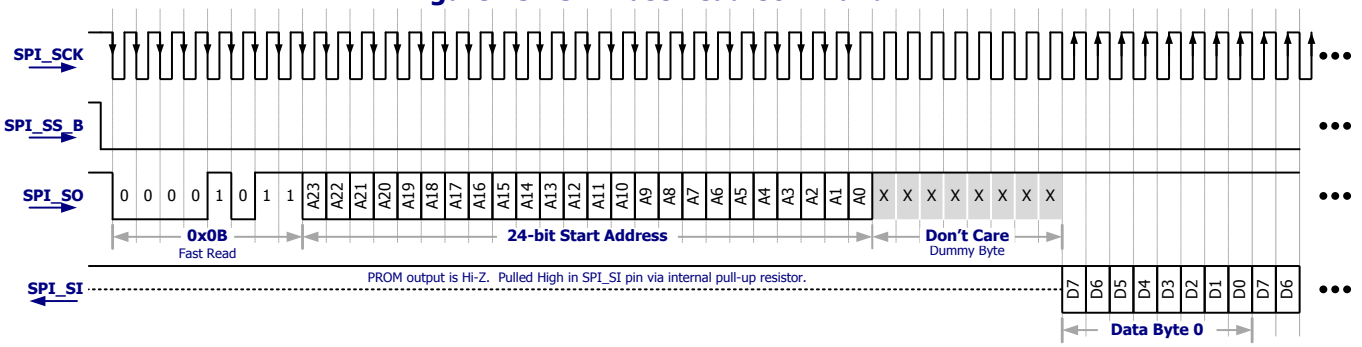


Figure 25 illustrates the next command issued by the iCE65 device. The iCE65 SPI interface again drives SPI_SS_B Low, followed by a Fast Read command, hexadecimal command code 0x0B, followed by a 24-bit start address, transmitted on the SPI_SO output. The iCE65 device provides data on the falling edge of SPI_SS_B. Upon initial power-up, the start address is always 0x00_0000. After waiting eight additional clock cycles, the iCE65 device begins reading serial data from the SPI PROM. Before presenting data, the SPI PROM's serial data output is high-impedance. The SPI_SI input pin has an internal pull-up resistor and sees high-impedance as logic '1'.

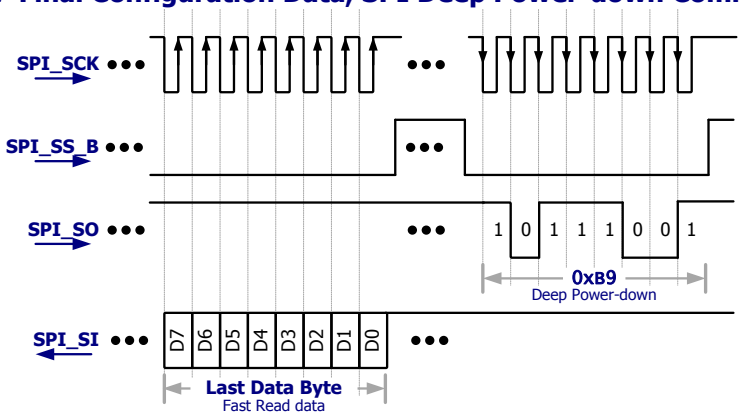
Figure 25: SPI Fast Read Command



The external SPI PROM supplies data on the falling edge of the iCE65 device's SPI_SCK clock output. The iCE65 device captures each PROM data value on the SPI_SI input, using the rising edge of the SPI_SCK clock signal. The SPI PROM data starts at the 24-bit address presented by the iCE65 device. PROM data is serially output, byte by byte, with most-significant bit, D7, presented first. The PROM automatically increments an internal byte counter as long as the PROM is selected and clocked.

After transferring the required number configuration data bits, the iCE65 device ends the Fast Read command by de-asserting its SPI_SS_B PROM select output, as shown in Figure 26. To conserve power, the iCE65 device then optionally issues a final Deep Power-down command, hexadecimal command code 0xB9. After de-asserting the SPI_SS_B output, the SPI PROM enters its Deep Power-down mode. The final power-down step is optional; the application may use the SPI PROM and can skip this step, controlled by a configuration option.

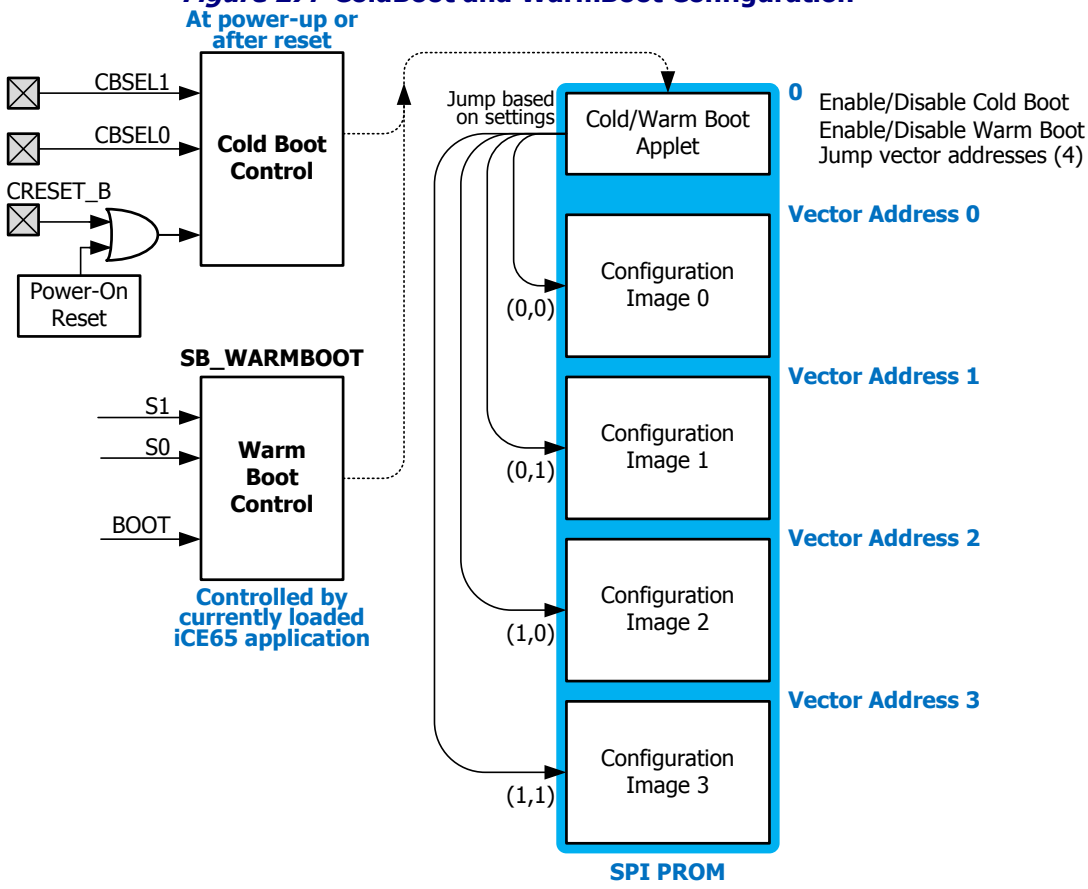
Figure 26: **Final Configuration Data, SPI Deep Power-down Command**



Cold Boot Configuration Option

By default, the iCE65 FPGA is programmed with a single configuration image, either from internal NVCM memory, from an external SPI Flash PROM, or externally from a processor or microcontroller.

Figure 27: **ColdBoot and WarmBoot Configuration**



When self loading from NVCM or from an SPI Flash PROM, there is an additional configuration option called Cold Boot mode. When this option is enabled in the configuration bitstream, the iCE65 FPGA boots normally from power-on or a master reset (CRESET_B = Low pulse), but monitors the value on two PIO pins that are borrowed during configuration, as shown in Figure 27. These pins, labeled PIO2/CBSEL0 and PIO2/CBSEL1, tell the FPGA which of the four possible SPI configurations to load into the device. Table 30 provides the pin or ball locations for these pins.

- Load from initial location, either from NVCM or from address 0 in SPI Flash PROM. For Cold Boot or Warm Boot applications, the initial configuration image contains the cold boot/warm boot applet.
- Check if Cold Boot configuration feature is enabled in the bitstream.
  - If not enabled, FPGA configures normally.
  - If Cold Boot is enabled, then the FPGA reads the logic values on pins CBSEL[1:0]. The FPGA uses the value as a vector and then reads from the indicated vector address.
  - At the selected CBSEL[1:0] vector address, there is a starting address for the selected configuration image.
    - For SPI Flash PROMs, the new address is a 24-bit start address in Flash.
    - If the selected bitstream is in NVCM, then the address points to the internal NVCM.
- Using the new start address, the FPGA restarts reading configuration memory from the new location.

Table 28: **ColdBoot Select Ball/Pin Numbers by Package**

ColdBoot Select	CB81	QN84	VQ100	CB132	CB196	CB284
PIO2/CBSEL0	G5	B15	41	L9	L9	R13
PIO2/CBSEL1	H5	A20	42	P10	P10	V14

When creating the initial configuration image, the Lattice development software loads the start address for up to four configuration images in the bitstream. The value on the CBSEL[1:0] pins tell the configuration controller to read a specific start address, then to load the configuration image stored at the selected address. The multiple bitstreams are stored either in the SPI Flash or in the internal NVCM.

After configuration, the CBSEL[1:0] pins become normal PIO pins available to the application.

The Cold Boot feature allows the iCE65 to be reprogrammed for special application requirements such as the following.

- A normal operating mode and a self-test or diagnostics mode.
- Different applications based on switch settings.
- Different applications based on a card-slot ID number.

Warm Boot Configuration Option

The Warm Boot configuration is similar to the Cold Boot feature, but is completely under the control of the FPGA application.

A special design primitive, SB_WARMBOOT, allows an FPGA application to choose between four configuration images using two internal signal ports, S1 and S0, as shown in Figure 27. These internal signal ports connect to programmable interconnect, which in turn can connect to PLB logic and/or PIO pins.

After selecting the desired configuration image, the application then asserts the internal signal BOOT port High to force the FPGA to restart the configuration process from the specified vector address stored in PROM.

A Warm Boot application can only jump to another configuration image that DOES NOT have Warm Boot enabled. There is no such restriction for Cold Boot applications.

Time-Out and Retry

When configuring from external SPI Flash, the iCE65 device looks for a synchronization word. If the device does not find a synchronization word within its timeout period, the device automatically attempts to restart the configuration process from the very beginning. This feature is designed to address any potential power-sequencing issues that may occur between the iCE65 device and the external PROM.

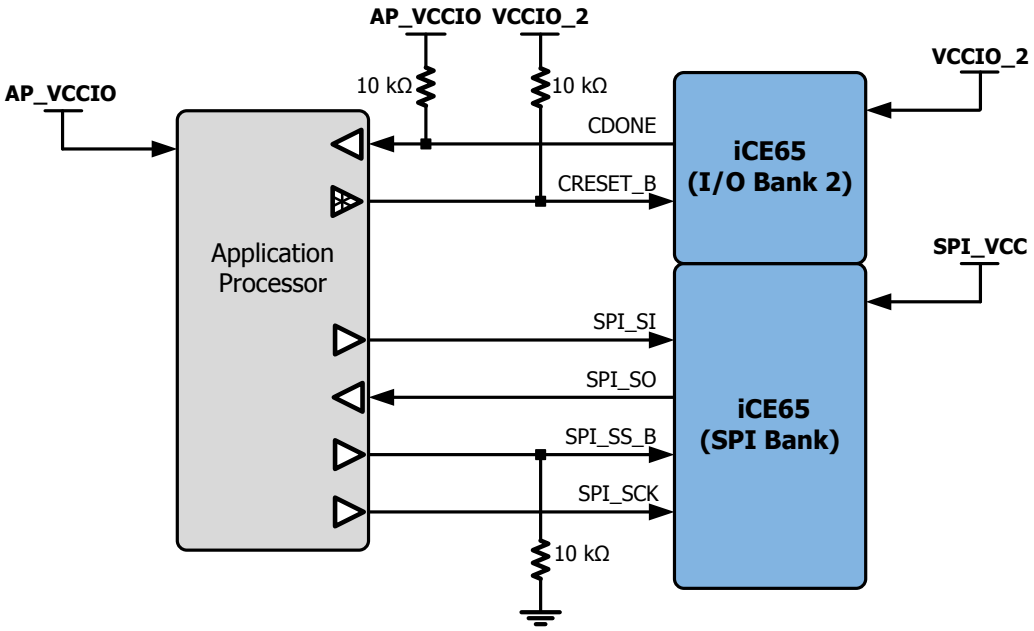
The iCE65 device attempts to reconfigure six times. If not successful after six attempts, the iCE65 FPGA automatically goes into low-power mode.

SPI Peripheral Configuration Interface

Using the SPI peripheral configuration interface, an application processor (AP) serially writes a configuration image to an iCE65 FPGA using the iCE65's SPI interface, as shown in Figure 23. The iCE65's SPI configuration interface is a separate, independent I/O bank, powered by the VCC_SPI supply input. Typically, VCC_SPI is the same voltage as the application processor's I/O. The configuration control signals, CDONE and CRESET_B, are supplied by the separate I/O Bank 2 voltage input, VCCIO_2.

This same SPI peripheral interface supports programming for the iCE65's Nonvolatile Configuration Memory (NVCM).

Figure 28: **iCE65 SPI Peripheral Configuration Interface**



The SPI control signals are defined in Table 25.

Table 29: **SPI Peripheral Configuration Interface Pins (SPI_SS_B Low when CRESET_B Released)**

Signal Name	Direction	iCE65 I/O Supply	Description
CDONE	AP ← iCE65	VCCIO_2	Configuration Done output from iCE65. Connect to a 10kΩ pull-up resistor to the application processor I/O voltage, AP_VCC.
CRESET_B	AP → iCE65		Configuration Reset input on iCE65. Typically driven by AP using an open-drain driver, which also requires a 10kΩ pull-up resistor to VCCIO_2.
SPI_VCC	Supply	SPI_VCC	SPI Flash PROM voltage supply input.
SPI_SI	AP → iCE65		SPI Serial Input to the iCE65 FPGA, driven by the application processor.
SPI_SO	AP ← iCE65		SPI Serial Output from CE65 device to the application processor. Not actually used during SPI peripheral mode configuration but required if the SPI interface is also used to program the NVCM.
SPI_SS_B	AP → iCE65		SPI Slave Select output from the application processor. Active Low. Optionally hold Low prior to configuration using a 10kΩ pull-down resistor to ground.
SPI_SCK	AP → iCE65		SPI Slave Clock output from the application processor.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Enabling SPI Configuration Interface

The optional 10 kΩ pull-down resistor on the SPI_SS_B signal ensures that the iCE65 FPGA powers up in the SPI peripheral mode. Optionally, the application processor drives the SPI_SS_B pin Low when CRESET_B is released, forcing the iCE65 FPGA into SPI peripheral mode.

SPI Peripheral Configuration Process

Figure 29 illustrates the interface timing for the SPI peripheral mode and Figure 30 outlines the resulting configuration process. The actual timing specifications appear in Table 60. The application processor (AP) begins by driving the iCE65 CRESET_B pin Low, resetting the iCE65 FPGA. Similarly, the AP holds the iCE65's SPI_SS_B pin Low. The AP must hold the CRESET_B pin Low for at least 200 ns. Ultimately, the AP either releases the CRESET_B pin and allows it to float High via the 10 kΩ pull-up resistor to VCCIO_2 or drives CRESET_B High. The iCE65 FPGA enters SPI peripheral mode when the CRESET_B pin returns High while the SPI_SS_B pin is Low.

After driving CRESET_B High or allowing it to float High, the AP must wait a minimum of t_{CR_SCK} µs, (see Table 60) allowing the iCE65 FPGA to clear its internal configuration memory.

After waiting for the configuration memory to clear, the AP sends the configuration image generated by the iCEcube development system. An SPI peripheral mode configuration image must not use the ColdBoot or WarmBoot options. Send the entire configuration image, without interruption, serially to the iCE65's SPI_SI input on the falling edge of the SPI_SCK clock input. Once the AP sends the 0x7EAA997E synchronization pattern, the generated SPI_SCK clock frequency must be within the specified 1 MHz to 25 MHz range (40 ns to 1 µs clock period) while sending the configuration image. Send each byte of the configuration image with most-significant bit (msb) first. The AP sends data to the iCE65 FPGA on the falling edge of the SPI_SCK clock. The iCE65 FPGA internally captures each incoming SPI_SI data bit on the rising edge of the SPI_SCK clock. The iCE65's SPI_SO output pin is not used during SPI peripheral mode but must connect to the AP if the AP also programs the iCE65's Nonvolatile Configuration Memory (NVCM).

Prior to sending the iCE65 configuration image , an SPI NVCM shut-off sequence must be sent. See AN014 for details.
The iCE65 configuration image must be sent as one contiguous stream without interruption.
The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

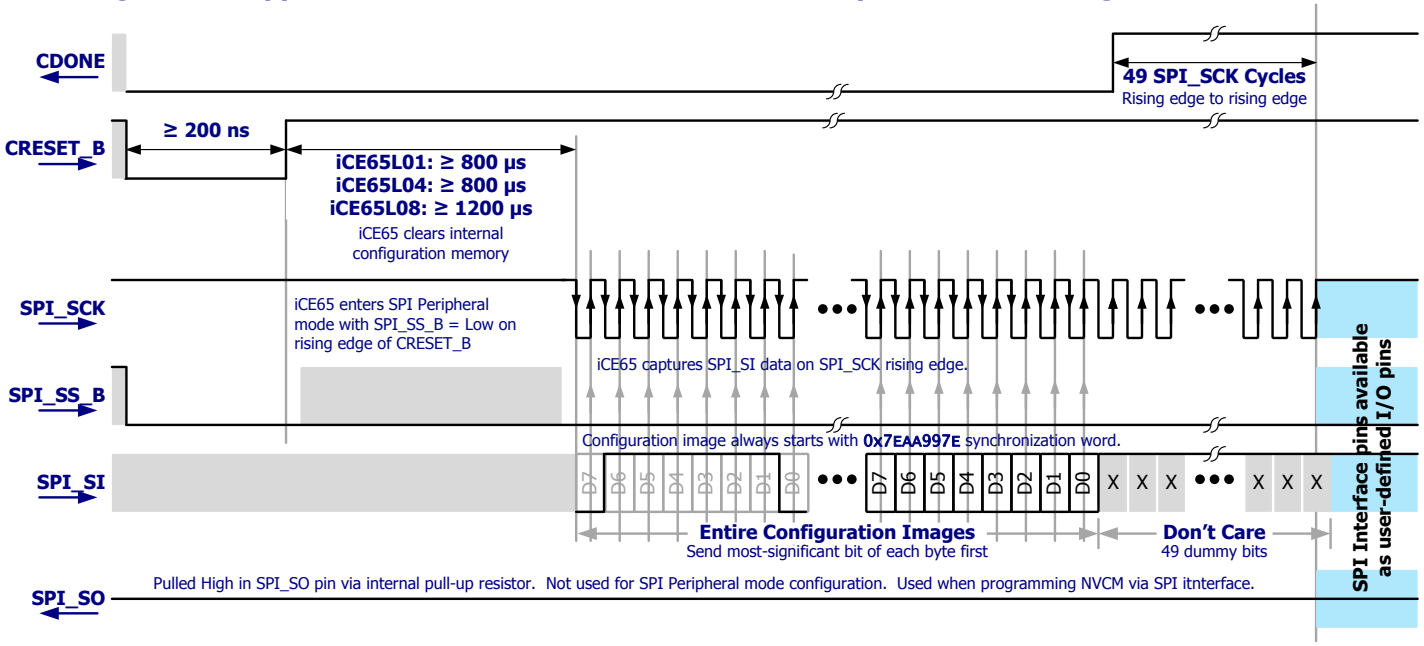
After sending the entire image, the iCE65 FPGA releases the CDONE output allowing it to float High via the 10 kΩ pull-up resistor to AP_VCC. If the CDONE pin remains Low, then an error occurred during configuration and the AP should handle the error accordingly for the application.

After the CDONE output pin goes High, send at least 49 additional dummy bits, effectively 49 additional SPI_SCK clock cycles measured from rising-edge to rising-edge.

After the additional SPI_CLK cycles, the SPI interface pins then become available to the user application loaded in FPGA.

To reconfigure the iCE65 FPGA or to load a different configuration image, merely restart the configuration process by pulsing CRESET_B Low or power-cycling the FPGA.

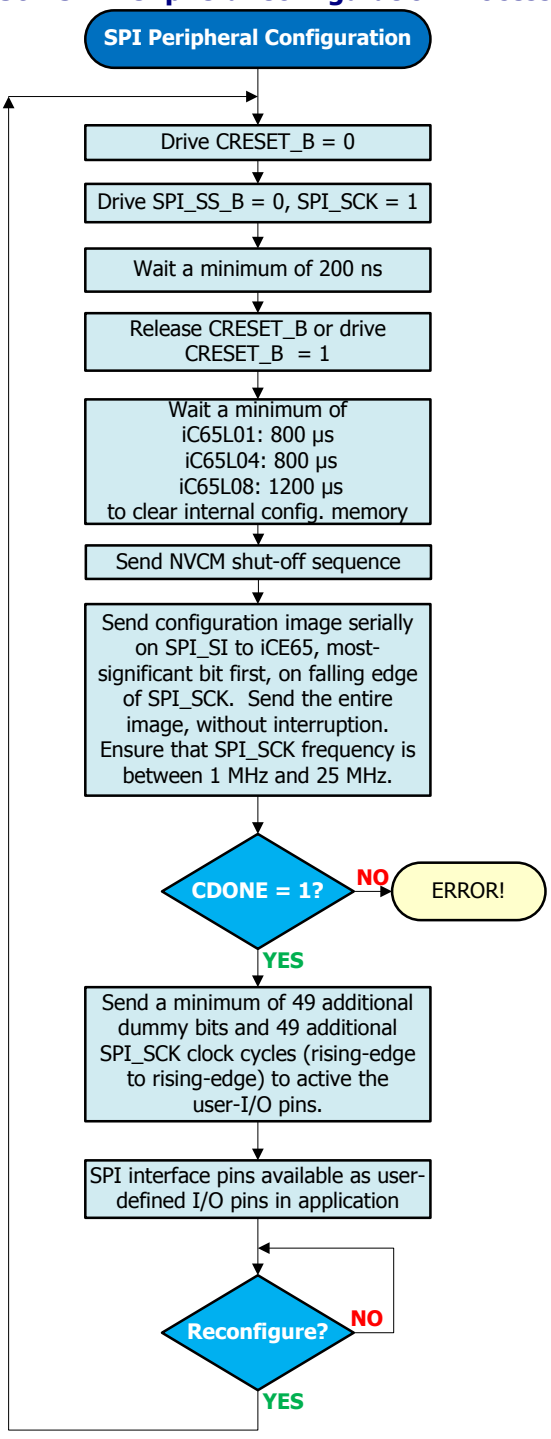
Figure 29: **Application Processor Waveforms for SPI Peripheral Mode Configuration Process**



The iCE65 configuration image must be sent as one contiguous stream without interruption.

The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

Figure 30: **SPI Peripheral Configuration Process**



Voltage Compatibility

As shown in Figure 23, there are potentially three different supply voltages involved in the SPI Peripheral interface, described in Table 30.

Table 30: **SPI Peripheral Mode Supply Voltages**

Supply Voltage	Description
AP_VCCIO	I/O supply to the Application Processor (AP)
VCC_SPI	Voltage supply for the iCE65 SPI interface.
VCCIO_2	Supply voltage for the iCE65 I/O Bank 2.

Table 31 describes how to maintain voltage compatibility for two interface scenarios. The easiest interface is when the Application Processor's (AP) I/O supply rail and the iCE65's SPI and VCCIO_2 bank supply rails all connect to the same voltage. The second scenario is when the AP's I/O supply voltage is greater than the iCE65's VCCIO_2 supply voltage.

***Table 31:* CRESET_B and CDONE Voltage Compatibility**

Condition	CRESET_B			CDONE Pull-up	Requirement
	Direct	**Open-Drain**	**Pull-up**		
VCCIO_AP = VCC_SPI **VCCIO_AP = VCCIO_2**	OK	OK with pull-up	Required if using open-drain output	Recommended	AP can directly drive CRESET_B High and Low although an open-drain output recommended is if multiple devices control CRESET_B. If using an open-drain driver, the CRESET_B input must include a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is also recommended.
AP_VCCIO > VCCIO_2	N/A	Required, requires pull-up	Required	Required	The AP must control CRESET_B with an open-drain output, which requires a 10 kΩ pull-up resistor to VCCIO_2. The 10 kΩ pull-up resistor to AP_VCCIO is required.

JTAG Boundary Scan Port

Overview

Each iCE65 device includes an IEEE 1149.1-compatible JTAG boundary-scan port. The port supports printed-circuit board (PCB) testing and debugging. It also provides an alternate means to configure the iCE65 device.

Signal Connections

The JTAG port connections are listed in Table 32.

***Table 32:* iCE65 JTAG Boundary Scan Signals**

Signal Name	Direction	Description
TDI	Input	Test Data Input. Must be tied off to GND when unused. (no pull-up resistor)*
TMS	Input	Test Mode Select. Must be tied off to GND when unused. (no pull-up resistor)*
TCK	Input	Test Clock. Must be tied off to GND when unused. (no pull-up resistor)*
TDO	Output	Test Data Output.
TRST_B	Input	Test Reset, active Low. Must be Low during normal device operation. Must be High to enable JTAG operations.*

* Must be tied off to GND or VCCIO_1, else VCCIO_1 draws current.

Table 33 lists the ball/pin numbers for the JTAG interface by package code. The JTAG interface is available in select package types. The JTAG port is located in I/O Bank 1 along the right edge of the iCE65 device and powered by the VCCIO_1 supply inputs. Consequently, the JTAG interface uses the associated I/O standards for I/O Bank 1.

***Table 33:* JTAG Interface Ball/Pin Numbers by Package**

JTAG Interface	VQ100	CB132	CB196	CB284
TDI	N/A	M12	M12	T16
TMS		P14	P14	V18
TCK		L12	L12	R16
TDO		N14	N14	U18
TRST_B		M14	M14	T18

Supported JTAG Commands

The JTAG interface supports the IEEE 1149.1 mandatory instructions, including EXTEST, SAMPLE/PRELOAD, and BYPASS.

Package and Pinout Information

Maximum User I/O Pins by Package and by I/O Bank

Table 34 lists the maximum number of user-programmable I/O pins by package, with additional detail showing user I/O pins by I/O bank. In some cases, a smaller iCE65 device is packaged in a larger package with unconnected (N.C.) pins or balls, resulting in fewer overall I/O pins. See Table 35 for device-specific I/O counts by package.

Table 34: **User I/O by Package, by I/O Bank**

	CB81	QN84	VQ100	CB132	CB196	CB284
Package Leads	81	84	100	132	196	284
Package Body (mm)	5 x 5	7 x 7	14 x 14	8 x 8	8 x 8	12 x 12
Ball Array (balls)	9 x 9	N/A	N/A	14 x 14	14 x 14	22 x 22
Ball/Lead Pitch (mm)	0.5	0.5	0.5	0.5	0.5	0.5
Maximum user I/O, all I/O banks	63	67	72	95	150	222
PIO Pins in Bank 0	17	17	19	26	37	60
PIO Pins in Bank 1	16	17	19	21	38	55
PIO Pins in Bank 2	12	11	12	20	35	53
PIO Pins in Bank 3	18	18	18	24	36	50
PIO Pins in SPI Interface	4	4	4	4	4	4

Printed Circuit Board Layout Information

For information on how to use the iCE65 packages on a printed circuit board (PCB) design, consult the following application note.

- AN010: iCE65 Printed Circuit Board (PCB Layout) Guidelines

Maximum User I/O by Device and Package

Table 35 lists the maximum available user I/O by device and by and package type. Not all devices are available in all packages. Similarly, smaller iCE65 devices may have unconnected balls in some packages. Devices sharing a common package have similar footprints.

Table 35: **Maximum User I/O by Device and Package**

Package	Device		
	iCE65L01	**iCE65L04**	**iCE65L08**
CB81	63	—	—
QN84	67	—	—
VQ100	72	72	
CB132	93	95	—
CB196	—	150	150
CB284	—	176	222

iCE65 Pin Descriptions

Table 36 lists the various iCE65 pins, alphabetically by name. The table indicates the directionality of the signal and the associated I/O bank. The table also indicates if the signal has an internal pull-up resistor enabled during configuration. Finally, the table describes the function of the pin.

Table 36: iCE65 Pin Description

Signal Name	Direction	I/O Bank	Pull-up during Config	Description
CDONE	Output	2	Yes	Configuration Done. Dedicated output. Includes a permanent weak pull-up resistor to VCCIO_2.. If driving external devices with CDONE output, connect a 10 kΩ pull-up resistor to VCCIO_2.
CRESET_B	Input	2	No	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 kΩ pull-up resistor to VCCIO_2.
GBIN0/PIO0 GBIN1/PIO0	Input/IO	0	Yes	Global buffer input from I/O Bank 0. Optionally, a full-featured PIO pin.
GBIN2/PIO1 GBIN3/PIO1	Input/IO	1	Yes	Global buffer input from I/O Bank 1. Optionally, a full-featured PIO pin.
GBIN4/PIO2 GBIN5/PIO2	Input/IO	2	Yes	Global buffer input from I/O Bank 2. Optionally, a full-featured PIO pin.
GBIN6/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin.
GBIN7/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin. Optionally, a differential clock input using the associated differential input pin.
GND	Supply	All	N/A	Ground. All must be connected.
PIOx_yy	I/O	0,1,2	Yes	Programmable I/O pin defined by the iCE65 configuration bitstream. The 'x' number specifies the I/O bank number in which the I/O pin resides. The "yy' number specifies the I/O number in that bank.
PIO2/CBSEL0	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO2/CBSEL1	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO3_yy/ DPwwz	I/O	3	No	Programmable I/O pin that is also half of a differential I/O pair. Only available in I/O Bank 3. The "yy" number specifies the I/O number in that bank. The "ww" number indicates the differential I/O pair. The 'z' indicates the polarity of the pin in the differential pair. 'A'=negative input. 'B'=positive input.
PIOS/SPI_SO	I/O	SPI	Yes	SPI Serial Output. A full-featured PIO pin after configuration.
PIOS /SPI_SI	I/O	SPI	Yes	SPI Serial Input. A full-featured PIO pin after configuration.
PIOS / SPI_SS_B	I/O	SPI	Yes	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to SPI_VCC during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE65 device, as shown in Figure 20. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
PIOS/ SPI_SCK	I/O	SPI	Yes	SPI Slave Clock. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1. Tie off to GND when unused.

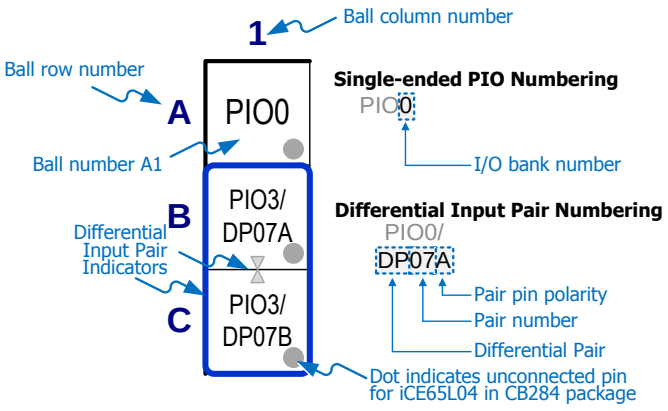
Signal Name	Direction	I/O Bank	Pull-up during Config	Description
TMS	Input	1	No	JTAG Test Mode Select. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1. Tie off to GND when unused.
TCK	Input	1	No	JTAG Test Clock. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1. Tie off to GND when unused.
TDO	Output	1	No	JTAG Test Data Output.
TRST_B	Input	1	No	JTAG Test Reset, active Low. Keep Low during normal operation; High for JTAG operation.
VCC	Supply	All	N/A	Internal core voltage supply. All must be connected.
VCCIO_0	Supply	0	N/A	Voltage supply to I/O Bank 0. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
VCCIO_1	Supply	1	N/A	Voltage supply to I/O Bank 1. All such pins or balls on the package must be connected. Required to guarantee a valid input voltage on TRST_B JTAG pin.
VCCIO_2	Supply	2	N/A	Voltage supply to I/O Bank 2. All such pins or balls on the package must be connected. Required input to the Power-On Reset (POR) circuit.
VCCIO_3	Supply	3	N/A	Voltage supply to I/O Bank 3. All such pins or balls on the package must be connected. Can be disconnected or turned off without affecting the Power-On Reset (POR) circuit.
SPI_VCC	Supply	SPI	N/A	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM. Required input to the Power-On Reset (POR) circuit.
VPP_FAST	Supply	All	N/A	Direct programming voltage supply. If unused, leave floating or unconnected during normal operation.
VPP_2V5	Supply	All	N/A	Programming supply voltage. When the iCE65 device is active, VPP_2V5 must be in the valid range between 2.3 V to 3.47 V to release the Power-On Reset circuit, even if the application is not using the NVCM.
VREF	Voltage Reference	3	N/A	Input reference voltage in I/O Bank 3 for the SSTL I/O standard. This pin only appears on the CB284 package and for die-based products.

N/A = Not Applicable

iCE65 Package Footprint Diagram Conventions

Figure 31 illustrates the naming conventions used in the following footprint diagrams. Each PIO pin is associated with an I/O Bank. PIO pins in I/O Bank 3 that support differential inputs are also numbered by differential input pair.

Figure 31: **CB Package Footprint Diagram Conventions**



CB81 Chip-Scale Ball-Grid Array

The CB81 package is a full ball grid array with 0.5 mm ball pitch. The iCE65L01 device is available in this package.

Footprint Diagram

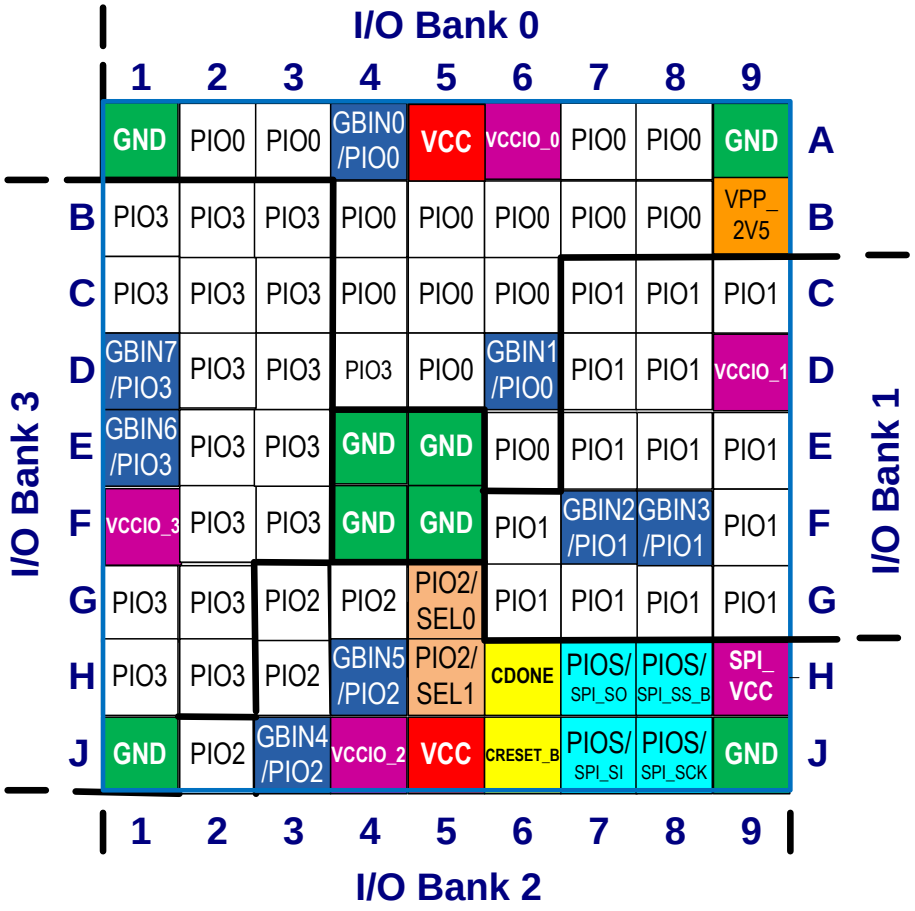
Figure 32 shows the iCE65 footprint diagram for the CB81 package.

Figure 31 shows the conventions used in the diagram.

Also see Table 37 for a complete, detailed pinout for the 81-ball BGA package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

***Figure 32*: iCE65L01 CB81 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 37 provides a detailed pinout table for the CB81 package. Pins are generally arranged by I/O bank, then by ball function.

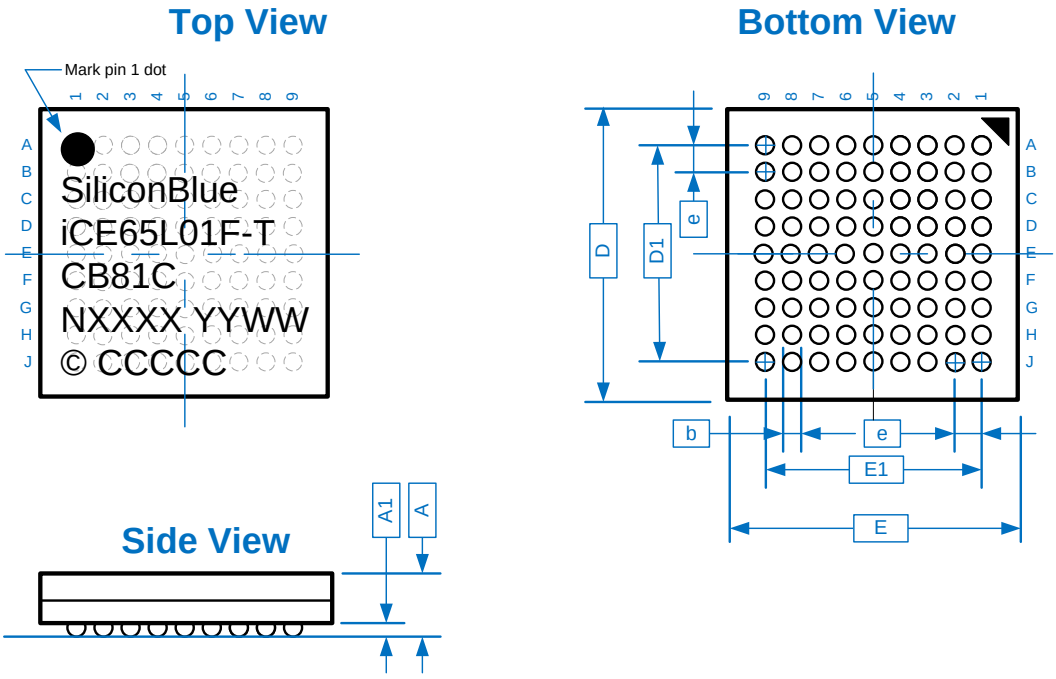
Table 37: **iCE65 CB81 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
PIO0	A2	PIO	0
PIO0	A3	PIO	0
GBIN0/PIO0	A4	GBIN	0
PIO0	A7	PIO	0
PIO0	A8	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B6	PIO	0
PIO0	B7	PIO	0
PIO0	B8	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	D4	PIO	0
PIO0	D5	PIO	0
GBIN1/PIO0	D6	GBIN	0
PIO0	E6	PIO	0
VCCIO_0	A6	VCCIO	0
PIO1	C7	PIO	1
PIO1	C8	PIO	1
PIO1	C9	PIO	1
PIO1	D7	PIO	1
PIO1	D8	PIO	1
PIO1	E7	PIO	1
PIO1	E8	PIO	1
PIO1	E9	PIO	1
PIO1	F6	PIO	1
GBIN2/PIO1	F7	GBIN	1
GBIN3/PIO1	F8	GBIN	1
PIO1	F9	PIO	1
PIO1	G6	PIO	1
PIO1	G7	PIO	1
PIO1	G8	PIO	1
PIO1	G9	PIO	1
VCCIO_1	D9	VCCIO	1
CDONE	H6	CONFIG	2
CRESET_B	J6	CONFIG	2
PIO2	G3	PIO	2
PIO2	G4	PIO	2
PIO2/CBSEL0	G5	PIO	2
PIO2	H3	PIO	2
GBIN5/PIO2	H4	PIO	2
PIO2/CBSEL1	H5	PIO	2
PIO2	J2	PIO	2
GBIN4/PIO2	J3	PIO	2
VCCIO_2	J4	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	C1	PIO	3
PIO3	C2	PIO	3
PIO3	C3	PIO	3
GBIN7/PIO3	D1	GBIN	3
PIO3	D2	PIO	3
PIO3	D3	PIO	3
GBIN6/PIO3	E1	GBIN	3
PIO3	E2	PIO	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	F3	PIO	3
PIO3	G1	PIO	3
PIO3	G2	PIO	3
PIO3	H1	PIO	3
PIO3	H2	PIO	3
VCCIO_3	F1	VCCIO	3
PIOS/SPI_SO	H7	SPI	SPI
PIOS/SPI_SI	J7	SPI	SPI
PIOS/SPI_SCK	J8	SPI	SPI
PIOS/SPI_SS_B	H8	SPI	SPI
SPI_VCC	H9	SPI	SPI
GND	A1	GND	GND
GND	A9	GND	GND
GND	J9	GND	GND
GND	J1	GND	GND
GND	E4	GND	GND
GND	E5	GND	GND
GND	F4	GND	GND
GND	F5	GND	GND
VCC	A5	VCC	VCC
VCC	J5	VCC	VCC
VPP_2V5	B9	VPP	VPP

***Figure 33:* CB81 Package Mechanical Drawing**

CB81: 5 x 5 mm, 81-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			9		Columns
Number of Ball Rows	Y			9		Rows
Number of Signal Balls		n		81		Balls
Body Size	X	E	4.90	5.00	5.10	mm
	Y	D	4.90	5.00	5.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	4.00	—	
	Y	D1	—	4.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.15	—	0.25	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65P01F	Part number
	-T	Power/Speed
3	CB81C	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
67	57

QN84 Quad Flat Pack No-Lead

The QN84 is a Quad Flat Pack No-Lead package with a 0.5 mm pad pitch.

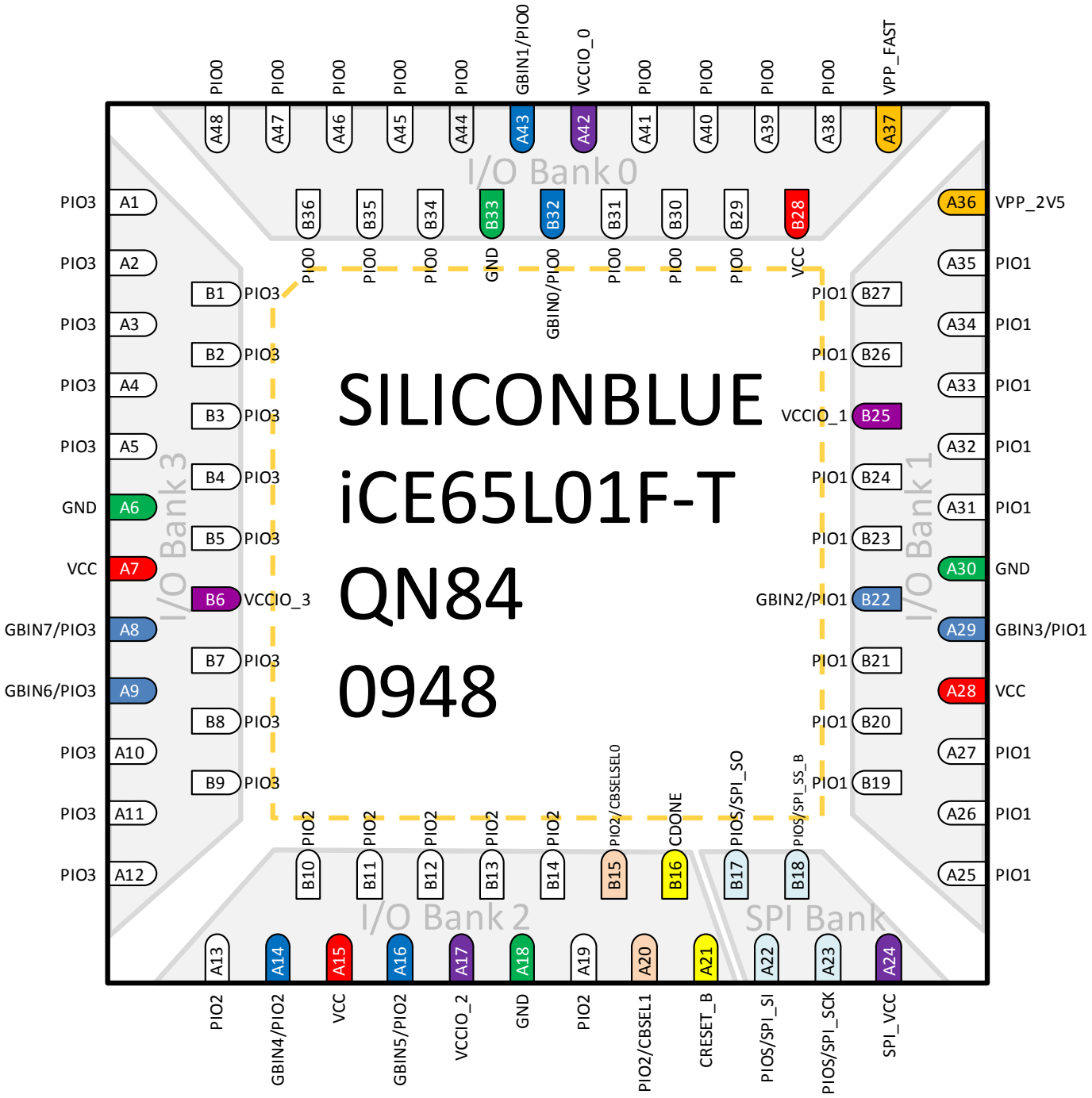
Footprint Diagram

Figure 34 shows the iCE65 footprint diagram for the QN84 package.

Also see Table 38 for a complete, detailed pinout for the QN84 package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 34: **iCE65 QN84 Quad Flat Pack No-Lead Footprint (Top View)**



Pinout Table

Table 38 provides a detailed pinout table for the QN84 package. Pins are generally arranged by I/O bank, then by ball function. The QN84 package has no JTAG pins.

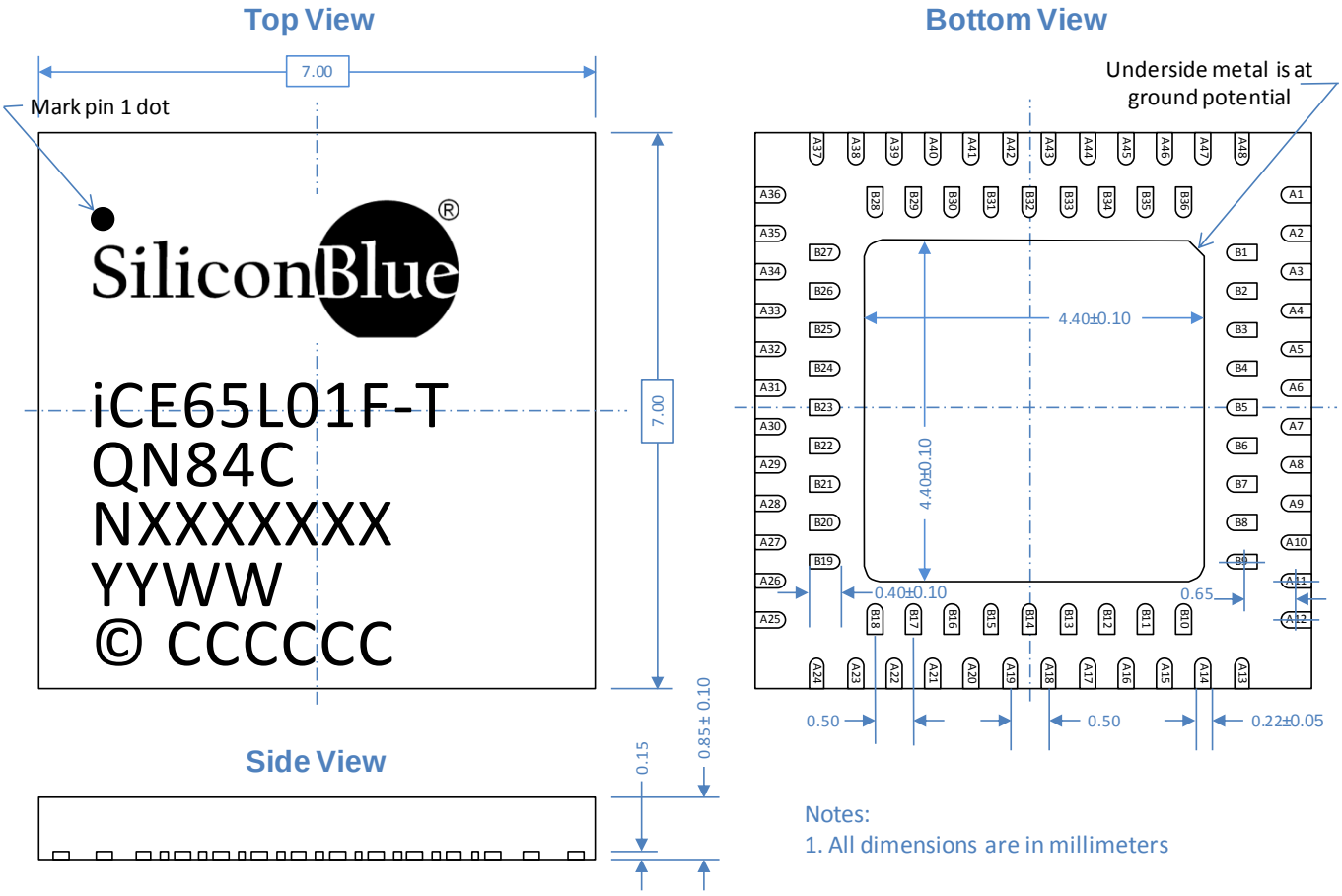
Table 38: **iCE65 QN84 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	B32	GBIN	0
GBIN1/PIO0	A43	GBIN	0
PIO0	A38	PIO	0
PIO0	A39	PIO	0
PIO0	A40	PIO	0
PIO0	A41	PIO	0
PIO0	A44	PIO	0
PIO0	A45	PIO	0
PIO0	A46	PIO	0
PIO0	A47	PIO	0
PIO0	A48	PIO	0
PIO0	B29	PIO	0
PIO0	B30	PIO	0
PIO0	B31	PIO	0
PIO0	B34	PIO	0
PIO0	B35	PIO	0
PIO0	B36	PIO	0
VCCIO_0	A42	VCCIO	0
GBIN2/PIO1	B22	GBIN	1
GBIN3/PIO1	A29	GBIN	1
PIO1	A25	PIO	1
PIO1	A26	PIO	1
PIO1	A27	PIO	1
PIO1	A31	PIO	1
PIO1	A32	PIO	1
PIO1	A33	PIO	1
PIO1	A34	PIO	1
PIO1	A35	PIO	1
PIO1	B19	PIO	1
PIO1	B20	PIO	1
PIO1	B21	PIO	1
PIO1	B23	PIO	1
PIO1	B24	PIO	1
PIO1	B26	PIO	1
PIO1	B27	PIO	1
VCCIO_1	B25	VCCIO	1
CDONE	B16	CONFIG	2
CRESET_B	A21	CONFIG	2
GBIN4/PIO2	A14	GBIN	2
GBIN5/PIO2	A16	GBIN	2
PIO2	A13	PIO	2
PIO2	B12	PIO	2
PIO2	A19	PIO	2
PIO2	B10	PIO	2
PIO2	B11	PIO	2
PIO2	B13	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO2	B14	PIO	2
PIO2/CBSEL0	B15	PIO	2
PIO2/CBSEL1	A20	PIO	2
VCCIO_2	A17	PIO	2
GBIN6/PIO3	A9	GBIN	3
GBIN7/PIO3	A8	GBIN	3
PIO3	A1	PIO	3
PIO3	A2	PIO	3
PIO3	A3	PIO	3
PIO3	A4	PIO	3
PIO3	A5	PIO	3
PIO3	A10	PIO	3
PIO3	A11	PIO	3
PIO3	A12	PIO	3
PIO3	B1	PIO	3
PIO3	B2	PIO	3
PIO3	B3	PIO	3
PIO3	B4	PIO	3
PIO3	B5	PIO	3
PIO3	B7	PIO	3
PIO3	B8	PIO	3
PIO3	B9	PIO	3
VCCIO_3	B6	VCCIO	3
PIOS/SPI_SO	B17	SPI	SPI
PIOS/SPI_SI	A22	SPI	SPI
PIOS/SPI_SCK	A23	SPI	SPI
PIOS/SPI_SS_B	B18	SPI	SPI
SPI_VCC	A24	SPI	SPI
GND	A6	GND	GND
GND	A18	GND	GND
GND	A30	GND	GND
GND	B33	GND	GND
VCC	A7	VCC	VCC
VCC	A15	VCC	VCC
VCC	A28	VCC	VCC
VCC	B28	VCC	VCC
VPP_2V5	A36	VPP	VPP
VPP_FAST	A37	VPP	VPP

Package Mechanical Drawing

Figure 35: QN84 Package Mechanical Drawing



Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
3	QN84C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient * θ_{JA} (°C/W)	
0 LFM	200 LFM
45	44

* With PCB thermal vias

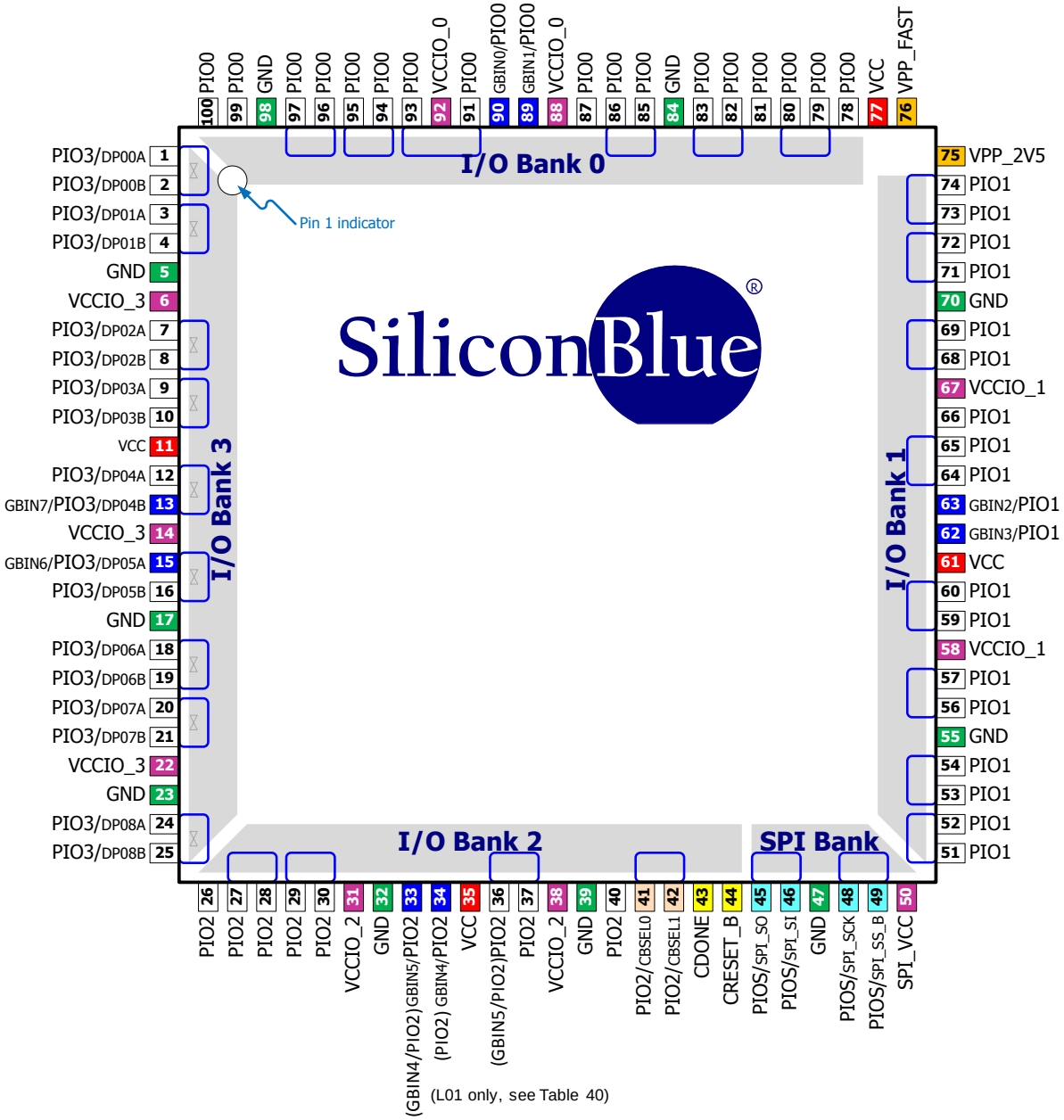
VQ100 Very-thin Quad Flat Package

The VQ100 package is a very-thin quad-flat package with 0.5 mm lead pitch. The iCE65L01 and iCE65L04 devices are available in this package.

Footprint Diagram

Figure 36 shows the footprint diagram for the 100-lead very-thin quad-flat package (VQ100). See Table 40 for a complete, detailed pinout for the 100-lead very-thin quad-flat package. The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 36: iCE65 VQ100 Footprint (Top View)



Pinout Table

Table 39 provides a detailed pinout table for the VQ100 package. Pins are generally arranged by I/O bank, then by pin function. The table also highlights the differential I/O pairs in I/O Bank 3. The VQ100 package has no JTAG pins.

Table 39: iCE65 VQ100 Pinout Table

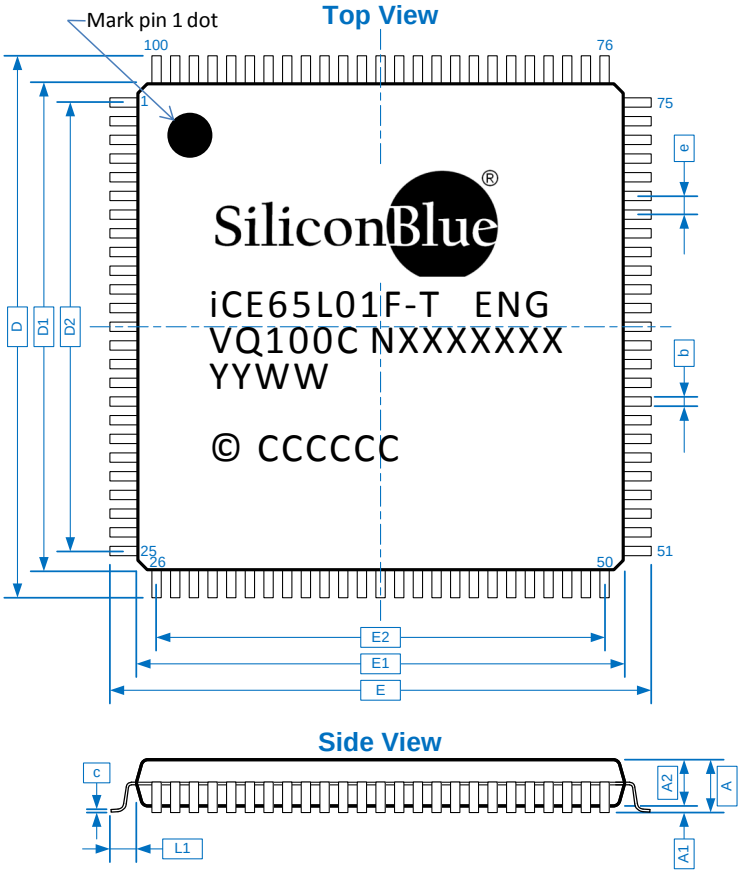
Pin Function	Pin Number	Type	Bank
GBIN0/PIO0	90	GBIN	0
GBIN1/PIO0	89	GBIN	0
PIO0	78	PIO	0
PIO0	79	PIO	0
PIO0	80	PIO	0
PIO0	81	PIO	0
PIO0	82	PIO	0
PIO0	83	PIO	0
PIO0	85	PIO	0
PIO0	86	PIO	0
PIO0	87	PIO	0
PIO0	91	PIO	0
PIO0	93	PIO	0
PIO0	94	PIO	0
PIO0	95	PIO	0
PIO0	96	PIO	0
PIO0	97	PIO	0
PIO0	99	PIO	0
PIO0	100	PIO	0
VCCIO_0	88	VCCIO	0
VCCIO_0	92	VCCIO	0
GBIN2/PIO1	63	GBIN	1
GBIN3/PIO1	62	GBIN	1
PIO1	51	PIO	1
PIO1	52	PIO	1
PIO1	53	PIO	1
PIO1	54	PIO	1
PIO1	56	PIO	1
PIO1	57	PIO	1
PIO1	59	PIO	1
PIO1	60	PIO	1
PIO1	64	PIO	1
PIO1	65	PIO	1
PIO1	66	PIO	1
PIO1	68	PIO	1
PIO1	69	PIO	1
PIO1	71	PIO	1
PIO1	72	PIO	1
PIO1	73	PIO	1
PIO1	74	PIO	1
VCCIO_1	58	VCCIO	1
VCCIO_1	67	VCCIO	1
CDONE	43	CONFIG	2
CRESET_B	44	CONFIG	2
GBIN4/PIO2	iCE65L01: 33 iCE65L04: 34	GBIN	2
GBIN5/PIO2	iCE65L01: 36 iCE65L04: 33	GBIN	2
PIO2	26	PIO	2
PIO2	27	PIO	2

Pin Function	Pin Number	Type	Bank
PIO2	28	PIO	2
PIO2	29	PIO	2
PIO2	30	PIO	2
PIO2	iCE65L01: 34 iCE65L04: 36	PIO	2
PIO2	37	PIO	2
PIO2	40	PIO	2
PIO2/CBSEL0	41	PIO	2
PIO2/CBSEL1	42	PIO	2
VCCIO_2	31	VCCIO	2
VCCIO_2	38	VCCIO	2
PIO3/DP00A	1	PIO/DPIO	3
PIO3/DP00B	2	PIO/DPIO	3
PIO3/DP01A	3	PIO/DPIO	3
PIO3/DP01B	4	PIO/DPIO	3
PIO3/DP02A	7	PIO/DPIO	3
PIO3/DP02B	8	PIO/DPIO	3
PIO3/DP03A	9	PIO/DPIO	3
PIO3/DP03B	10	PIO/DPIO	3
PIO3/DP04A	12	PIO/DPIO	3
GBIN7/PIO3/DP04B	13	GBIN/DPIO	3
GBIN6/PIO3/DP05A	15	GBIN/DPIO	3
PIO3/DP05B	16	PIO/DPIO	3
PIO3/DP06A	18	PIO/DPIO	3
PIO3/DP06B	19	PIO/DPIO	3
PIO3/DP07A	20	PIO/DPIO	3
PIO3/DP07B	21	PIO/DPIO	3
PIO3/DP08A	24	PIO/DPIO	3
PIO3/DP08B	25	PIO/DPIO	3
VCCIO_3	6	VCCIO	3
VCCIO_3	14	VCCIO	3
VCCIO_3	22	VCCIO	3
PIOS/SPI_SO	45	SPI	SPI
PIOS/SPI_SI	46	SPI	SPI
PIOS/SPI_SCK	48	SPI	SPI
PIOS/SPI_SS_B	49	SPI	SPI
SPI_VCC	50	SPI	SPI
GND	5	GND	GND
GND	17	GND	GND
GND	23	GND	GND
GND	32	GND	GND
GND	39	GND	GND
GND	47	GND	GND
GND	55	GND	GND
GND	70	GND	GND
GND	84	GND	GND
GND	98	GND	GND
VCC	11	VCC	VCC
VCC	35	VCC	VCC

Pin Function	Pin Number	Type	Bank
VCC	61	VCC	VCC
VCC	77	VCC	VCC
VPP_2V5	75	VPP	VPP
VPP_FAST	76	VPP	VPP

Package Mechanical Drawing

Figure 37: VQ100 Package Mechanical Drawing: Standard Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

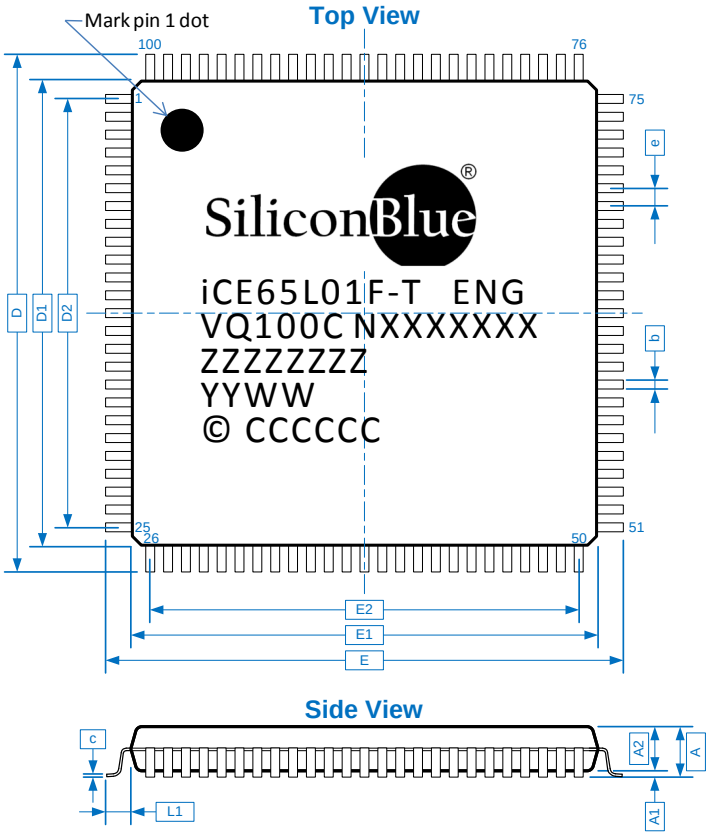
Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	YYWW	Date Code
5	N/A	Blank
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θJA (°C/W)	
0 LFM	200 LFM
38	32

Figure 38: VQ100 Package Mechanical Drawing: NVCM Programmed Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	ZZZZZZZZ	NVCM Program. code
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θJA (°C/W)	
0 LFM	200 LFM
38	32

CB121 Chip-Scale Ball-Grid Array

The CB121 package is a chip-scale, fully-populated, ball-grid array with 0.5 mm ball pitch.

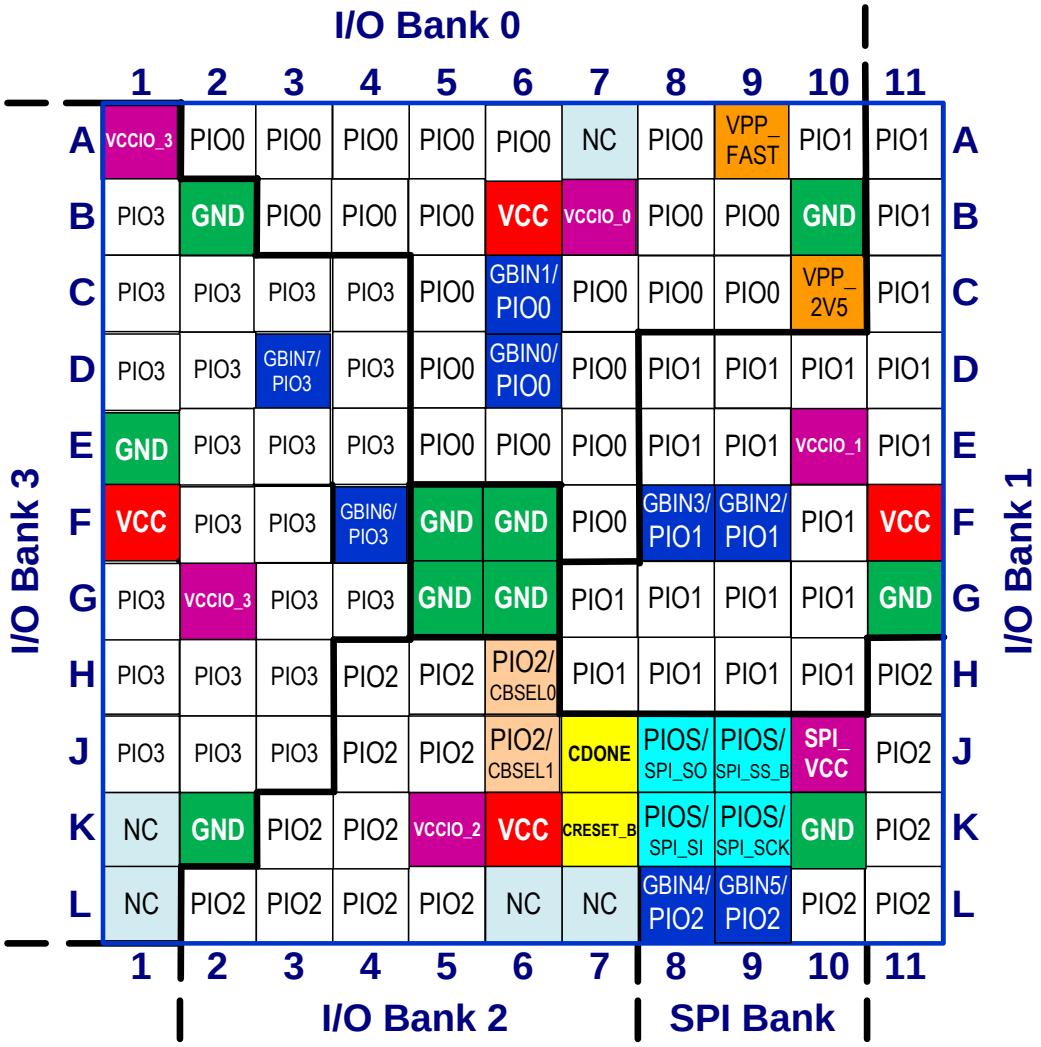
Footprint Diagram

Figure 39 shows the iCE65L01 chip-scale BGA footprint for the 6 x 6 mm CB121 package.

Also see Table 40 for a complete, detailed pinout for the 121-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 39: **iCE65L01 CB121 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 40 provides a detailed pinout table for the iCE65L01 in the CB121 chip-scale BGA package. Pins are generally arranged by I/O bank, then by ball function.

Table 40: **iCE65L01 CB121 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	D6	GBIN	0
GBIN1/PIO0	C6	GBIN	0
PIO0	A2	PIO	0
PIO0	A3	PIO	0
PIO0	A4	PIO	0

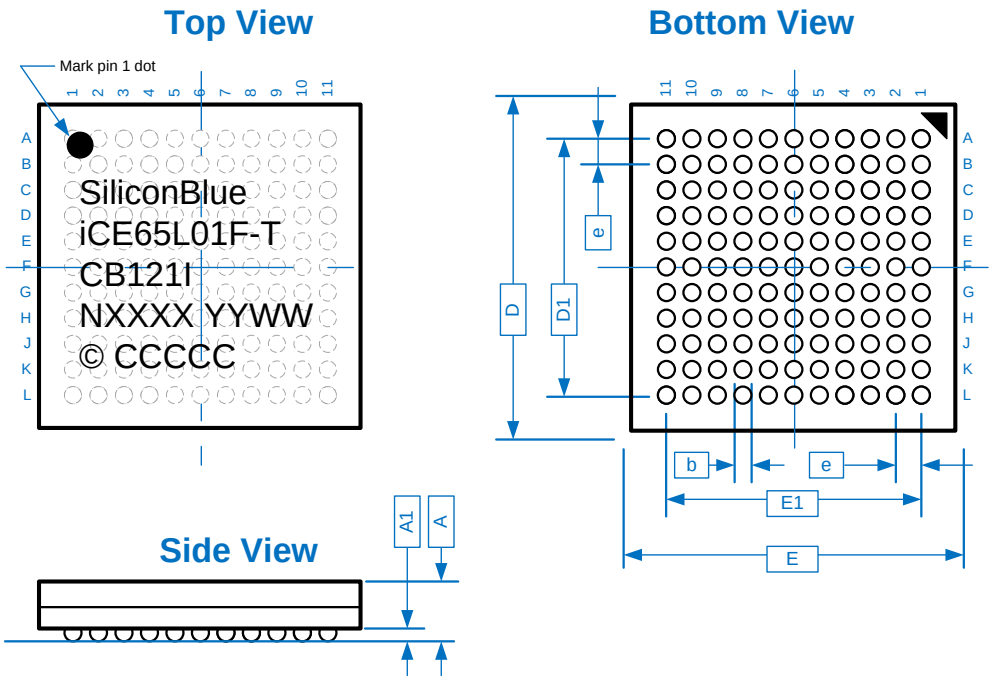
Ball Function	Ball Number	Pin Type	Bank
PIO0	A5	PIO	0
PIO0	A6	PIO	0
PIO0	A8	PIO	0
PIO0	A10	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	C5	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D7	PIO	0
PIO0	E5	PIO	0
PIO0	E6	PIO	0
PIO0	E7	PIO	0
PIO0	F7	PIO	0
VCCIO_0	B7	VCCIO	0
GBIN2/PIO1	F9	GBIN	1
GBIN3/PIO1	F8	GBIN	1
PIO1	A11	PIO	1
PIO1	B11	PIO	1
PIO1	C11	PIO	1
PIO1	D8	PIO	1
PIO1	D9	PIO	1
PIO1	D10	PIO	1
PIO1	D11	PIO	1
PIO1	E8	PIO	1
PIO1	E9	PIO	1
PIO1	E11	PIO	1
PIO1	F10	PIO	1
PIO1	G7	PIO	1
PIO1	G8	PIO	1
PIO1	G9	PIO	1
PIO1	G10	PIO	1
PIO1	H7	PIO	1
PIO1	H8	PIO	1
PIO1	H9	PIO	1
PIO1	H10	PIO	1
VCCIO_1	E10	VCCIO	1
CDONE	J7	CONFIG	2
CRESET_B	K7	CONFIG	2
GBIN4/PIO2	L8	GBIN	2
GBIN5/PIO2	L9	GBIN	2
PIO2	H4	PIO	2
PIO2	H5	PIO	2
PIO2	H11	PIO	2
PIO2	J4	PIO	2
PIO2	J5	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO2	J11	PIO	2
PIO2	K3	PIO	2
PIO2	K4	PIO	2
PIO2	K11	PIO	2
PIO2	L2	PIO	2
PIO2	L3	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L10	PIO	2
PIO2	L11	PIO	2
PIO2/CBSEL0	H6	PIO	2
PIO2/CBSEL1	J6	PIO	2
VCCIO_2	K5	VCCIO	2
PIO3	C1	PIO	3
PIO3	B1	PIO	3
PIO3	D1	PIO	3
PIO3	E2	PIO	3
PIO3	C2	PIO	3
PIO3	D2	PIO	3
PIO3	C3	PIO	3
PIO3	C4	PIO	3
PIO3	E4	PIO	3
PIO3	D4	PIO	3
PIO3	F3	PIO	3
PIO3	G3	PIO	3
PIO3	G4	PIO	3
GBIN6/PIO3	F4	GBIN	3
GBIN7/PIO3	D3	GBIN	3
PIO3	E3	PIO	3
PIO3	F2	PIO	3
PIO3	G1	PIO	3
PIO3	H1	PIO	3
PIO3	J1	PIO	3
PIO3	H2	PIO	3
PIO3	H3	PIO	3
PIO3	J3	PIO	3
PIO3	J2	PIO	3
VCCIO_3	A1	VCCIO	3
VCCIO_3	G2	VCCIO	3
PIOS/SPI_SO	J8	SPI	SPI
PIOS/SPI_SI	K8	SPI	SPI
PIOS/SPI_SCK	K9	SPI	SPI
PIOS/SPI_SS_B	J9	SPI	SPI
SPI_VCC	J10	SPI	SPI
GND	B2	GND	GND
GND	B10	GND	GND
GND	E1	GND	GND
GND	F5	GND	GND
GND	F6	GND	GND
GND	G5	GND	GND
GND	G6	GND	GND
GND	G11	GND	GND

Ball Function	Ball Number	Pin Type	Bank
GND	K2	GND	GND
GND	K10	GND	GND
VCC	B6	VCC	VCC
VCC	F1	VCC	VCC
VCC	F11	VCC	VCC
VCC	K6	VCC	VCC
VPP_2V5	C10	VPP	VPP
VPP_FAST	A9	VPP	VPP

***Figure 40:* CB121 Package Mechanical Drawing**

CB121: 6 x 6 mm, 121-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			11		Columns
Number of Ball Rows	Y			11		Rows
Number of Signal Balls		n		121		Balls
Body Size	X	E	5.90	6.00	6.10	mm
	Y	D	5.90	6.00	6.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.2	—	0.3	
Edge Ball Center to Center	X	E1	—	5.00	—	
	Y	D1	—	5.00	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.12	—	0.20	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
3	CB121I	Package type
	ENG	Engineering
4	NXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
64	55

CB132 Chip-Scale Ball-Grid Array

The CB132 package is a partially-populated ball grid array with 0.5 mm ball pitch. The empty ball rings simplify PCB layout. The iCE65L01, iCE65L04 and iCE65L08 devices are available in this package.

Footprint Diagram

Figure 41, Figure 42 and

Figure 43 show the iCE65 footprint diagrams for the CB132 package in iCE65L01, iCE65L04 and iCE65L08 devices. See Figure 48 for the "universal" chip-scale BGA footprint for the CB132 and CB284 packages. The 8 x 8 mm CB132 package fits within the same ball pattern as the 12 x 12 mm CB284 package.

Figure 31 shows the conventions used in the diagram.

Also see Table 41 for a complete, detailed pinout for the 132-ball BGA package.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

***Figure 41*: iCE65L01 CB132 Chip-Scale BGA Footprint (Top View)**

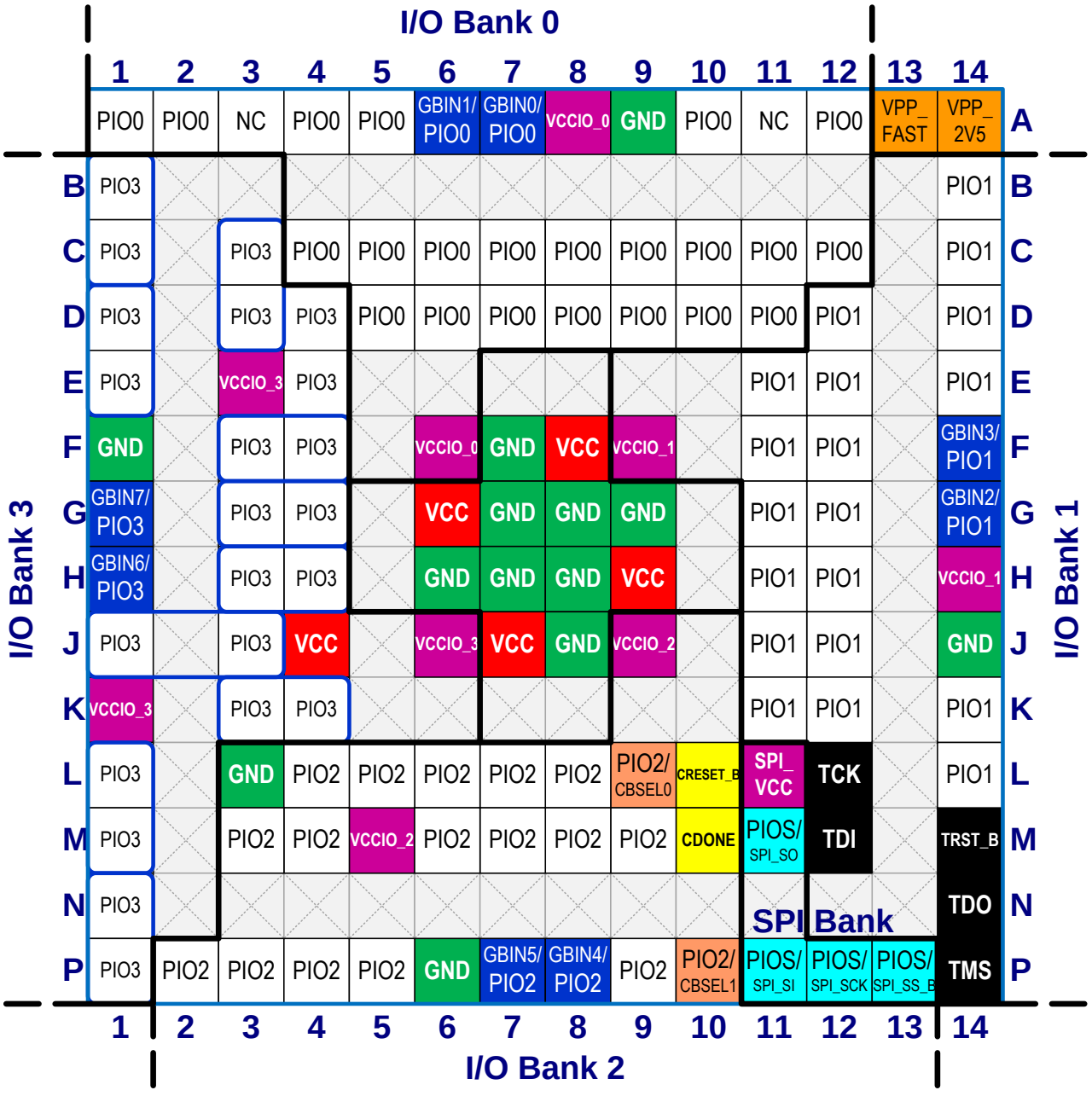


Figure 42: **iCE65L04 CB132 Chip-Scale BGA Footprint (Top View)**

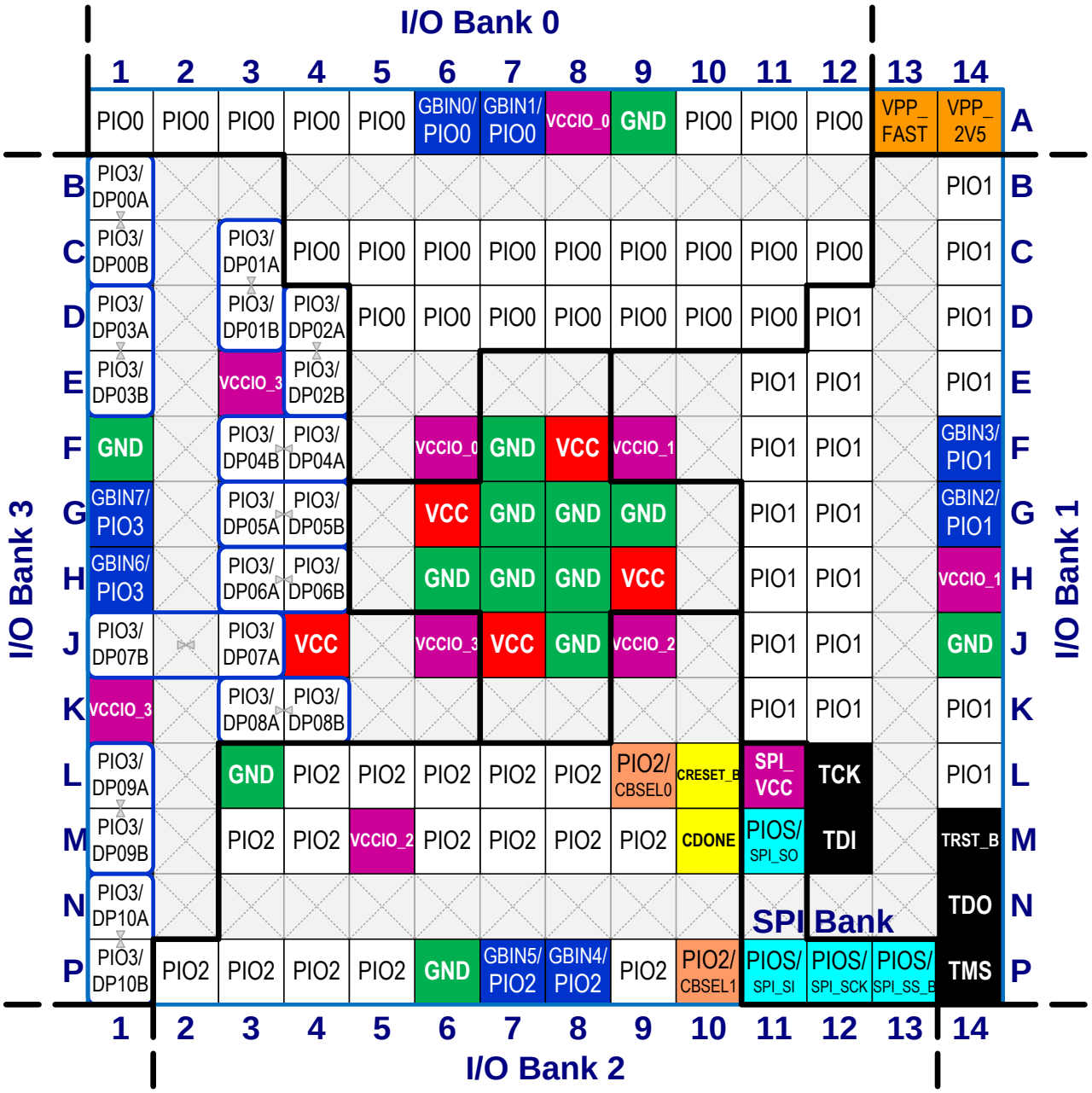
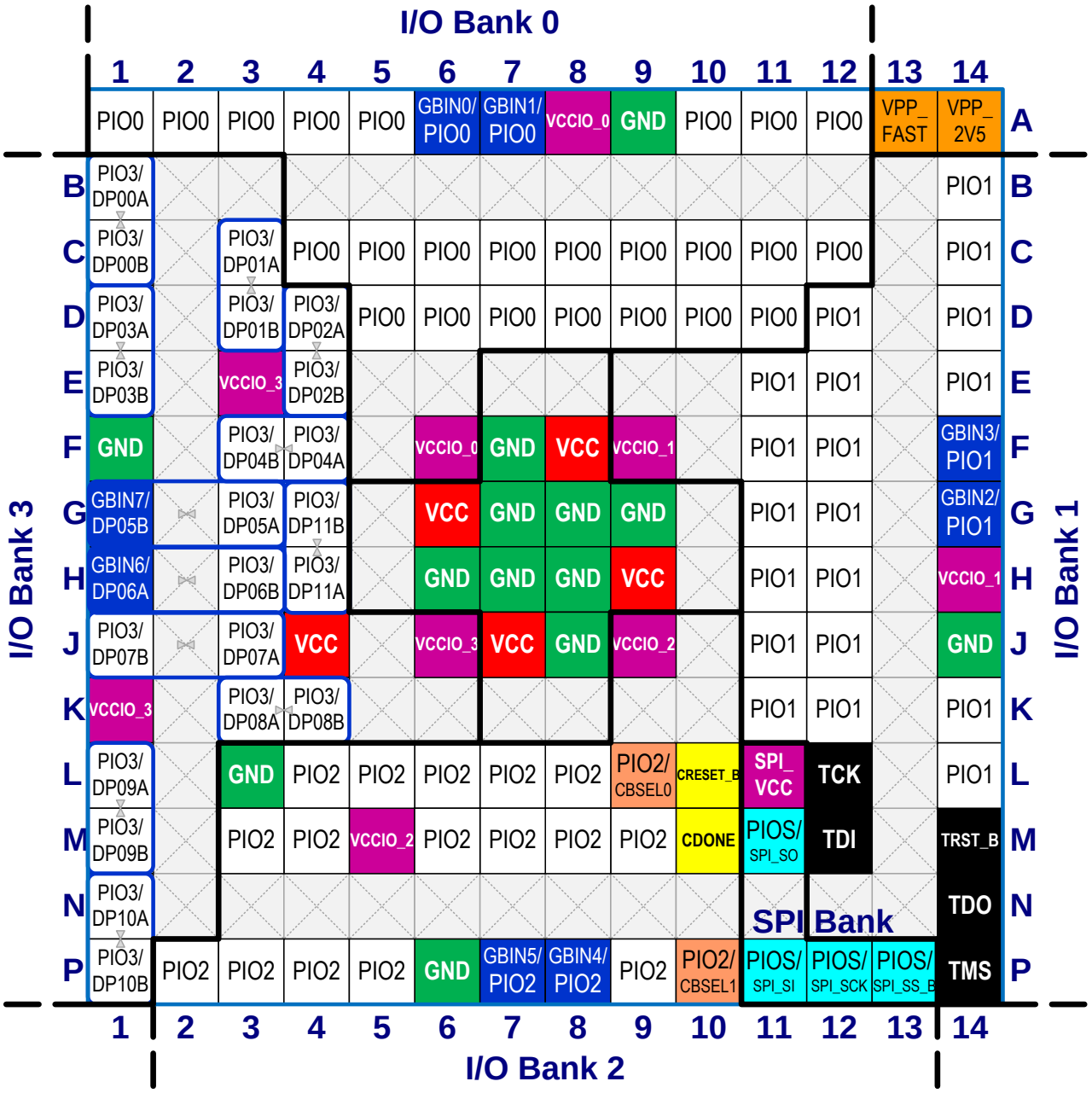


Figure 43: **iCE65L08 CB132 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 41 provides a detailed pinout table for the CB132 package. Pins are generally arranged by I/O bank, then by ball function. The table also highlights the differential I/O pairs in I/O Bank 3.

Table 41: iCE65 CB132 Chip-scale BGA Pinout Table

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	iCE65L01: A7 iCE65L04/L08: A6	GBIN	0
GBIN1/PIO0	iCE65L01: A6 iCE65L04/08: A7	GBIN	0
PIO0	A1	PIO	0
PIO0	A2	PIO	0
iCE65L01: (NC) iCE65L04/L08: PIO0	A3	iCE65L01: (NC) iCE65L04: PIO0	0
PIO0	A4	PIO	0
PIO0	A5	PIO	0
PIO0	A10	PIO	0
iCE65L01: (NC) iCE65L04/L08: PIO0	A11	iCE65L01: (NC) iCE65L04: PIO0	0
PIO0	A12	PIO	0
PIO0	C10	PIO	0
PIO0	C11	PIO	0
PIO0	C12	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	D5	PIO	0
PIO0	D6	PIO	0
PIO0	D7	PIO	0
PIO0	D8	PIO	0
PIO0	D9	PIO	0
PIO0	D10	PIO	0
PIO0	D11	PIO	0
VCCIO_0	A8	VCCIO	0
VCCIO_0	F6	VCCIO	0
GBIN2/PIO1	G14	GBIN	1
GBIN3/PIO1	F14	GBIN	1
PIO1	B14	PIO	1
PIO1	C14	PIO	1
PIO1	D12	PIO	1
PIO1	D14	PIO	1
PIO1	E11	PIO	1
PIO1	E12	PIO	1
PIO1	E14	PIO	1
PIO1	F11	PIO	1
PIO1	F12	PIO	1
PIO1	G11	PIO	1
PIO1	G12	PIO	1
PIO1	H11	PIO	1

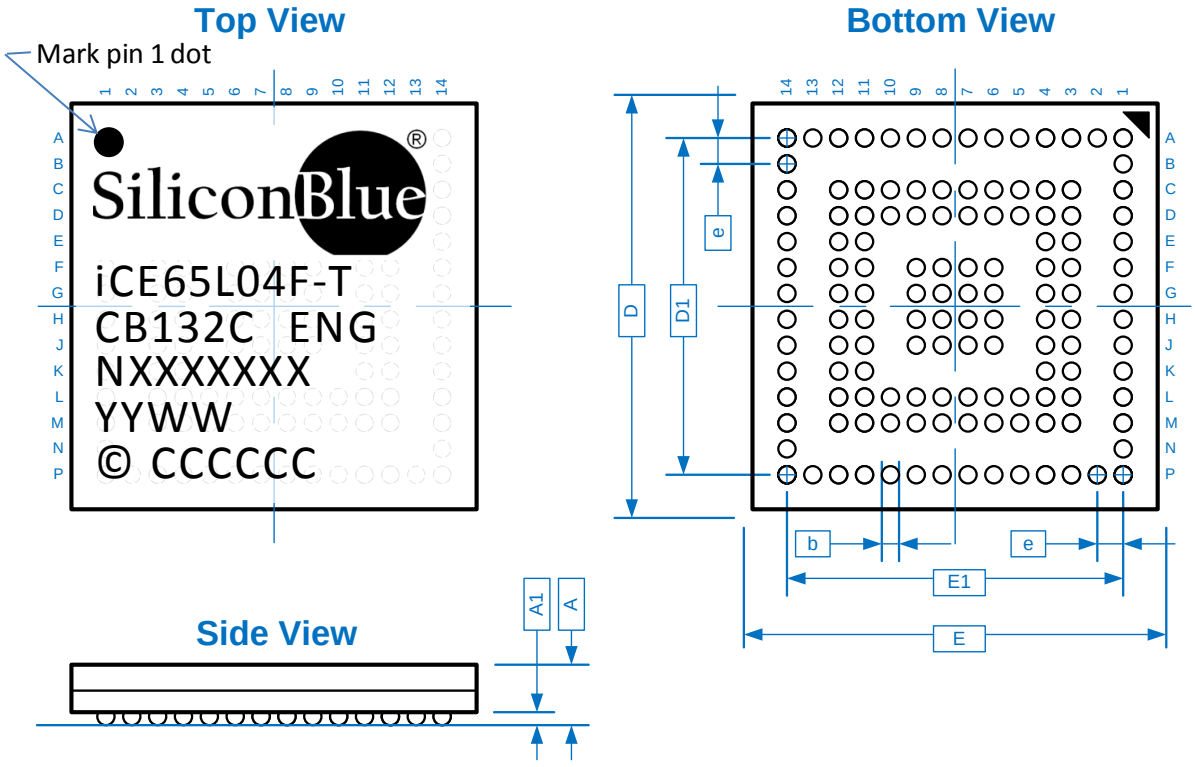
Ball Function	Ball Number	Pin Type	Bank
PIO1	H12	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L14	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2	P8	GBIN	2
GBIN5/PIO2	P7	GBIN	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L7	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2	M6	PIO	2
PIO2	M7	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	P2	PIO	2
PIO2	P3	PIO	2
PIO2	P4	PIO	2
PIO2	P5	PIO	2
PIO2	P9	PIO	2
PIO2/CBSEL0	L9	PIO	2
PIO2/CBSEL1	P10	PIO	2
VCCIO_2	J9	PIO	2
VCCIO_2	M5	PIO	2
PIO3/DP00A	B1	DPIO	3
PIO3/DP00B	C1	DPIO	3
PIO3/DP01A	C3	DPIO	3
PIO3/DP01B	D3	DPIO	3
PIO3/DP02A	D4	DPIO	3
PIO3/DP02B	E4	DPIO	3
PIO3/DP03A	D1	DPIO	3
PIO3/DP03B	E1	DPIO	3
PIO3/DP04A	F4	DPIO	3
PIO3/DP04B	F3	DPIO	3
L01/L04: GBIN6/PIO3 L08: GBIN6/DP06A	H1	GBIN	3

Ball Function	Ball Number	Pin Type	Bank
L01/L04: GBIN7/PIO3 L08: GBIN7/DP05B	G1	GBIN	3
L01/L04: PIO3/DP05A L08: PIO3/DP05A	G3	DPIO	3
L01/L04: PIO3/DP05B L08: PIO3/DP11B	G4	DPIO	3
L01/L04: PIO3/DP06A L08: PIO3/DP06B	H3	DPIO	3
L01/L04: PIO3/DP06B L08: PIO3/DP11A	H4	DPIO	3
PIO3/DP07A	J3	DPIO	3
PIO3/DP07B	J1	DPIO	3
PIO3/DP08A	K3	DPIO	3
PIO3/DP08B	K4	DPIO	3
PIO3/DP09A	L1	DPIO	3
PIO3/DP09B	M1	DPIO	3
PIO3/DP10A	N1	DPIO	3
PIO3/DP10B	P1	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
GND	A9	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

Package Mechanical Drawing

Figure 44: **CB132 Package Mechanical Drawing**

CB132: 8 x 8 mm, 132-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		132		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L04F	Part number
	-T	Power/Speed
3	CB132C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

CB196 Chip-Scale Ball-Grid Array

The CB196 package is a chip-scale, fully-populated, ball-grid array with 0.5 mm ball pitch.

Footprint Diagram

Figure 45 shows the iCE65L04 chip-scale BGA footprint for the 8 x 8 mm CB196 package. The footprint for the iCE65L08 is different than the iCE64L04 footprint, as shown in Figure 46. The pinout differences are highlighted by warning diamonds (◆) in the footprint diagrams and summarized in Table 43.

Although both the iCE65L04 and iCE65L08 are both available in the CB196 package and ***almost*** completely pin compatible, there are differences as shown in Table 43.

Figure 31 shows the conventions used in the diagram. Also see Table 42 for a complete, detailed pinout for the 196-ball chip-scale BGA packages. The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 45: **iCE65L04 CB196 Chip-Scale BGA Footprint (Top View)**

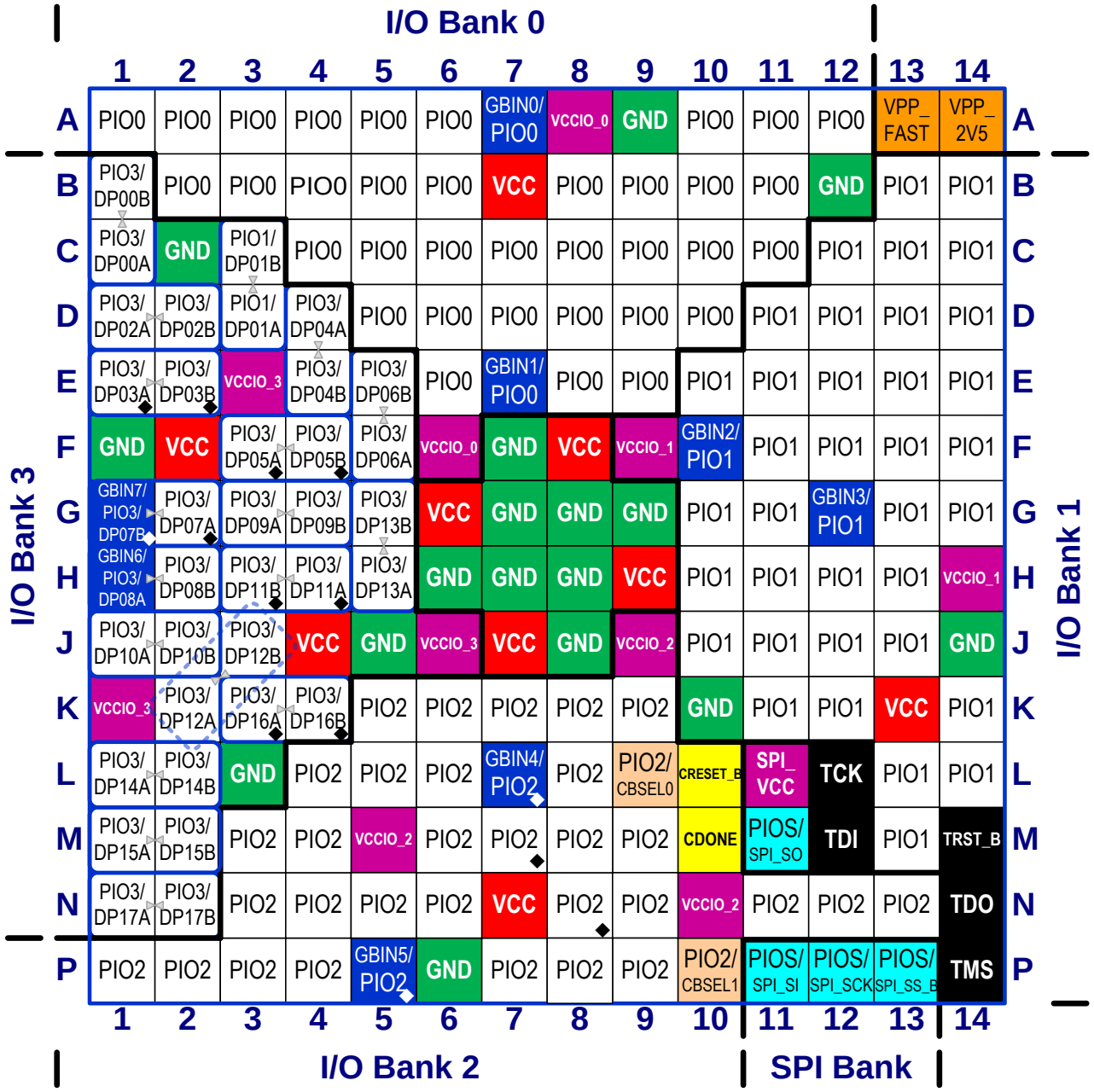
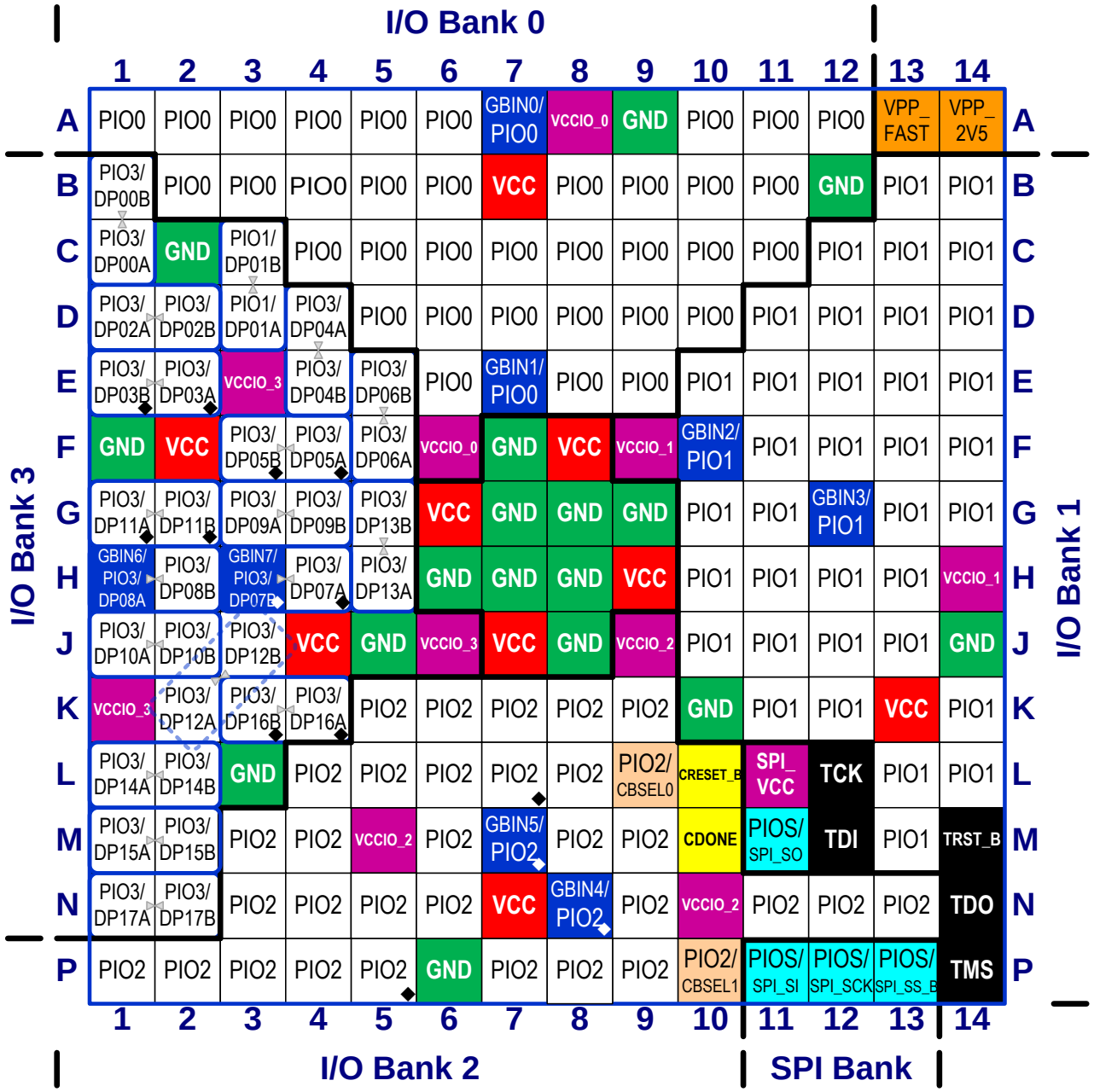


Figure 46: **iCE65L08 CB196 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 42 provides a detailed pinout table for the iCE65L04 in the CB196 chip-scale BGA package. Pins are generally arranged by I/O bank, then by ball function. The pinout for the iCE65L08 is different than the iCE64L04 pinout.

Although both the iCE65L04 and iCE65L08 are both available in the CB196 package and *almost* completely pin compatible, there are differences as shown in Table 43.

Table 42: **iCE65L04 CB196 Chip-scale BGA Pinout Table**

Ball Function	Ball Number	Pin Type	Bank
GBIN0/PIO0	A7	GBIN	0
GBIN1/PIO0	E7	GBIN	0
PIO0	A1	PIO	0
PIO0	A2	PIO	0
PIO0	A3	PIO	0
PIO0	A4	PIO	0

Ball Function	Ball Number	Pin Type	Bank
PIO0	A5	PIO	0
PIO0	A6	PIO	0
PIO0	A10	PIO	0
PIO0	A11	PIO	0
PIO0	A12	PIO	0
PIO0	B2	PIO	0
PIO0	B3	PIO	0
PIO0	B4	PIO	0
PIO0	B5	PIO	0
PIO0	B6	PIO	0
PIO0	B8	PIO	0
PIO0	B9	PIO	0
PIO0	B10	PIO	0
PIO0	B11	PIO	0
PIO0	C4	PIO	0
PIO0	C5	PIO	0
PIO0	C6	PIO	0
PIO0	C7	PIO	0
PIO0	C8	PIO	0
PIO0	C9	PIO	0
PIO0	C10	PIO	0
PIO0	C11	PIO	0
PIO0	D5	PIO	0
PIO0	D6	PIO	0
PIO0	D7	PIO	0
PIO0	D8	PIO	0
PIO0	D9	PIO	0
PIO0	D10	PIO	0
PIO0	E6	PIO	0
PIO0	E8	PIO	0
PIO0	E9	PIO	0
VCCIO_0	A8	VCCIO	0
VCCIO_0	F6	VCCIO	0
GBIN2/PIO1	F10	GBIN	1
GBIN3/PIO1	G12	GBIN	1
PIO1	B13	PIO	1
PIO1	B14	PIO	1
PIO1	C12	PIO	1
PIO1	C13	PIO	1
PIO1	C14	PIO	1
PIO1	D11	PIO	1
PIO1	D12	PIO	1
PIO1	D13	PIO	1
PIO1	D14	PIO	1
PIO1	E10	PIO	1
PIO1	E11	PIO	1
PIO1	E12	PIO	1
PIO1	E13	PIO	1
PIO1	E14	PIO	1
PIO1	F11	PIO	1
PIO1	F12	PIO	1
PIO1	F13	PIO	1

Ball Function	Ball Number	Pin Type	Bank
PIO1	F14	PIO	1
PIO1	G10	PIO	1
PIO1	G11	PIO	1
PIO1	G13	PIO	1
PIO1	G14	PIO	1
PIO1	H10	PIO	1
PIO1	H11	PIO	1
PIO1	H12	PIO	1
PIO1	H13	PIO	1
PIO1	J10	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	J13	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L13	PIO	1
PIO1	L14	PIO	1
PIO1	M13	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2 (◆)	***iCE65L04:*** L7 ***iCE65L08:*** N8	GBIN	2
GBIN5/PIO2 (◆)	***iCE65L04:*** P5 ***iCE65L08:*** M7	GBIN	2
PIO2	K5	PIO	2
PIO2	K6	PIO	2
PIO2	K7	PIO	2
PIO2	K8	PIO	2
PIO2	K9	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2	M6	PIO	2
PIO2 (◆)	***iCE65L04:*** M7 ***iCE65L08:*** P5	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	N3	PIO	2
PIO2	N4	PIO	2
PIO2	N5	PIO	2
PIO2	N6	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO2 (◆)	***iCE65L04:*** N8 ***iCE65L08:*** L7	PIO	2
PIO2	N9	PIO	2
PIO2	N11	PIO	2
PIO2	N12	PIO	2
PIO2	N13	PIO	2
PIO2	P1	PIO	2
PIO2	P2	PIO	2
PIO2	P3	PIO	2
PIO2	P4	PIO	2
PIO2	P7	PIO	2
PIO2	P8	PIO	2
PIO2	P9	PIO	2
PIO2/CBSEL0	L9	PIO	2
PIO2/CBSEL1	P10	PIO	2
VCCIO_2	J9	VCCIO	2
VCCIO_2	M5	VCCIO	2
VCCIO_2	N10	VCCIO	2
PIO3/DP00A	C1	DPIO	3
PIO3/DP00B	B1	DPIO	3
PIO3/DP01A	D3	DPIO	3
PIO3/DP01B	C3	DPIO	3
PIO3/DP02A	D1	DPIO	3
PIO3/DP02B	D2	DPIO	3
PIO3/DP03A (◆)	***iCE65L04:*** E1 ***iCE65L08:*** E2	DPIO	3
PIO3/DP03B (◆)	***iCE65L04:*** E2 ***iCE65L04:*** E1	DPIO	3
PIO3/DP04A	D4	DPIO	3
PIO3/DP04B	E4	DPIO	3
PIO3/DP05A (◆)	***iCE65L04:*** F3 ***iCE65L08:*** F4	DPIO	3
PIO3/DP05B (◆)	***iCE65L04:*** F4 ***iCE65L08:*** F3	DPIO	3
PIO3/DP06A	F5	DPIO	3
PIO3/DP06B	E5	DPIO	3
PIO3/DP07A (◆)	***iCE65L04:*** G2 ***iCE65L08:*** H4	DPIO	3
GBIN7/PIO3/DP07B (◆)	***iCE65L04:*** G1 ***iCE65L08:*** H3	GBIN	3
GBIN6/PIO3/DP08A	H1	GBIN	3
PIO3/DP08B	H2	DPIO	3
PIO3/DP09A	G3	DPIO	3
PIO3/DP09B	G4	DPIO	3
PIO3/DP10A	J1	DPIO	3
PIO3/DP10B	J2	DPIO	3
PIO3/DP11A (◆)	***iCE65L04:*** H4 ***iCE65L08:*** G1	DPIO	3
PIO3/DP11B (◆)	***iCE65L04:*** H3 ***iCE65L08:*** G2	DPIO	3
PIO3/DP12A	K2	DPIO	3
PIO3/DP12B	J3	DPIO	3

Ball Function	Ball Number	Pin Type	Bank
PIO3/DP13A	H5	DPIO	3
PIO3/DP13B	G5	DPIO	3
PIO3/DP14A	L1	DPIO	3
PIO3/DP14B	L2	DPIO	3
PIO3/DP15A	M1	DPIO	3
PIO3/DP15B	M2	DPIO	3
PIO3/DP16A (◆)	***iCE65L04:*** K3 ***iCE65L08:*** K4	DPIO	3
PIO3/DP16B (◆)	***iCE65L08:*** K4 ***iCE65L08:*** K3	DPIO	3
PIO3/DP17A	N1	DPIO	3
PIO3/DP17B	N2	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
GND	A9	GND	GND
GND	B12	GND	GND
GND	C2	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J5	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	K10	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	B7	VCC	VCC
VCC	F2	VCC	VCC
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VCC	K13	VCC	VCC
VCC	N7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package

Table 43 lists the package balls that are different between the pinouts for iCE65L04 and the iCE65L08 in the CB196 package. The table also describes the functional differences between these pins, which is critical when designing a CB196 footprint that supports both the iCE65L04 and the iCE65L08 devices. In some cases, only the differential inputs are swapped; single-ended I/Os are not affected. A swapped differential pair can be inverted internally for functional equivalence. In other cases, a global buffer input is swapped with another PIO pin in the same bank.

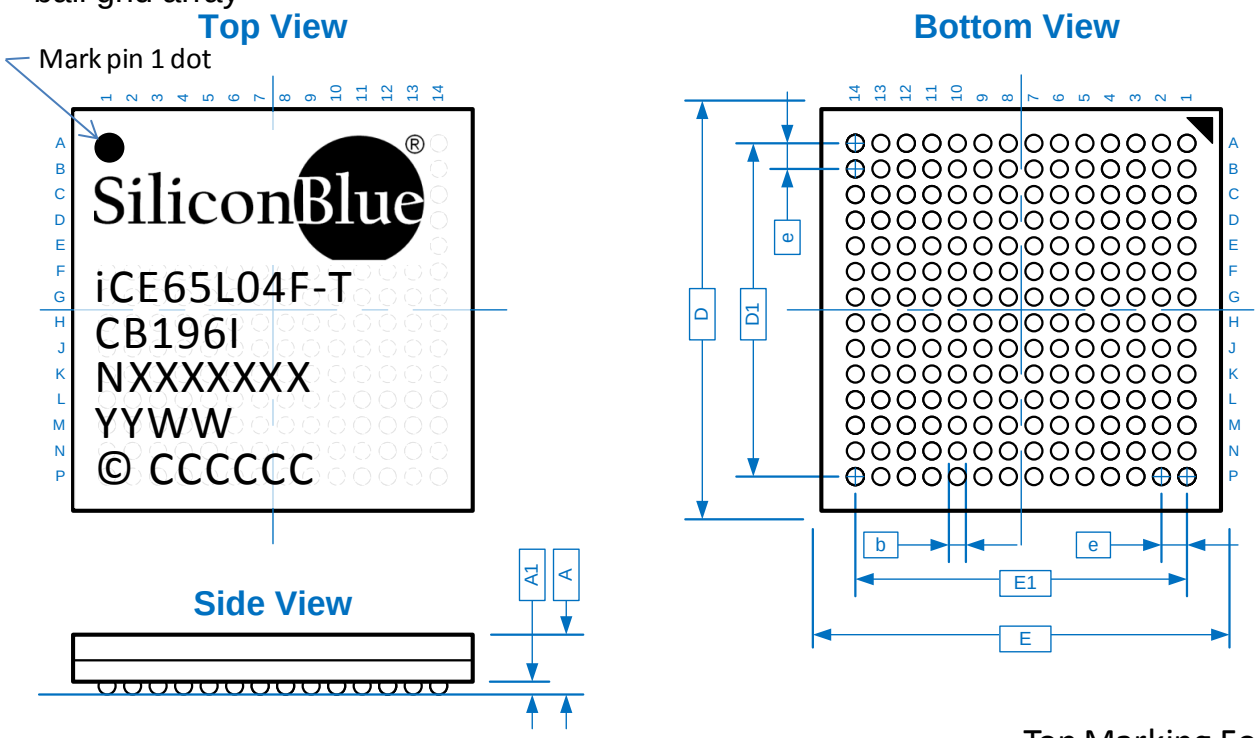
***Table 43:* Pinout Differences between iCE65L04 and iCE65L08 in CB196 Package**

Ball Number	iCE65L04	iCE65L08	Functional Difference
E1	PIO3/DP03A	PIO3/DP03B	Differential inputs swapped, single-ended I/Os not affected
E2	PIO3/DP03B	PIO3/DP03A	
F3	PIO3/DP05A	PIO3/DP05B	Differential inputs swapped, single-ended I/Os not affected
F4	PIO3/DP05B	PIO3/DP05A	
G1	GBIN7/PIO3/DP07B	PIO3/DP11A	Global buffer input GBIN7 and its associated differential input is swapped with another differential pair in I/O Bank 3
G2	PIO3/DP07A	PIO3/DP11B	
H3	PIO3/DP11B	GBIN7/PIO3/DP07B	
H4	PIO3/DP11A	PIO3/DP07A	
K3	PIO3/DP16A	PIO3/DP16B	Differential inputs swapped, single-ended I/Os not affected
K4	PIO3/DP16B	PIO3/DP16A	
L7	GBIN4/PIO2	PIO2	Global buffer input GBIN4 swapped with another PIO pin in I/O Bank 2
N8	PIO2	GBIN4/PIO2	
M7	PIO2	GBIN5/PIO2	Global buffer input GBIN5 swapped with another PIO pin in I/O Bank 2
P5	GBIN5/PIO2	PIO2	

Package Mechanical Drawing

Figure 47:
(a) iCE65L04 CB196 Package Mechanical Drawing

CB196: 8 x8 mm, 196-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		196		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L04F	Part number
	-T	Power/Speed
3	CB196I	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

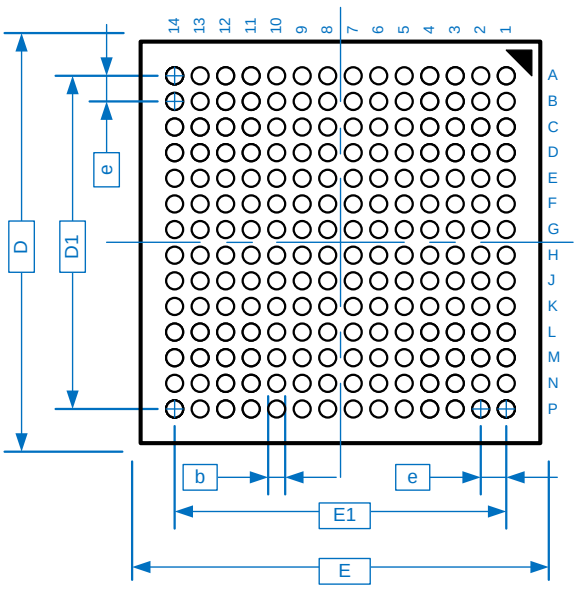
Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

(b) iCE65L08 CB196 Package Mechanical Drawing

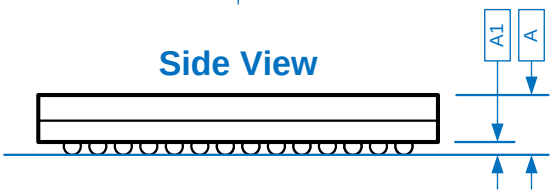
CB196: 8 x8 mm, 196-ball, 0.5 mm ball-pitch, fully-populated, chip-scale ball grid array

Top View

Bottom View



Side View



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			14		Columns
Number of Ball Rows	Y			14		Rows
Number of Signal Balls		n		196		Balls
Body Size	X	E	7.90	8.00	8.10	mm
	Y	D	7.90	8.00	8.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	6.50	—	
	Y	D1	—	6.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L08F	Part number
	-T	Power/Speed
3	CB196C	Package type
	ENG	Engineering
4	NXXXXXXX	Lot Number
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
42	34

CB284 Chip-Scale Ball-Grid Array

The CB284 package, partially-populated 0.5 mm pitch, ball grid array simplifies PCB layout with empty ball rings.

Footprint Diagram

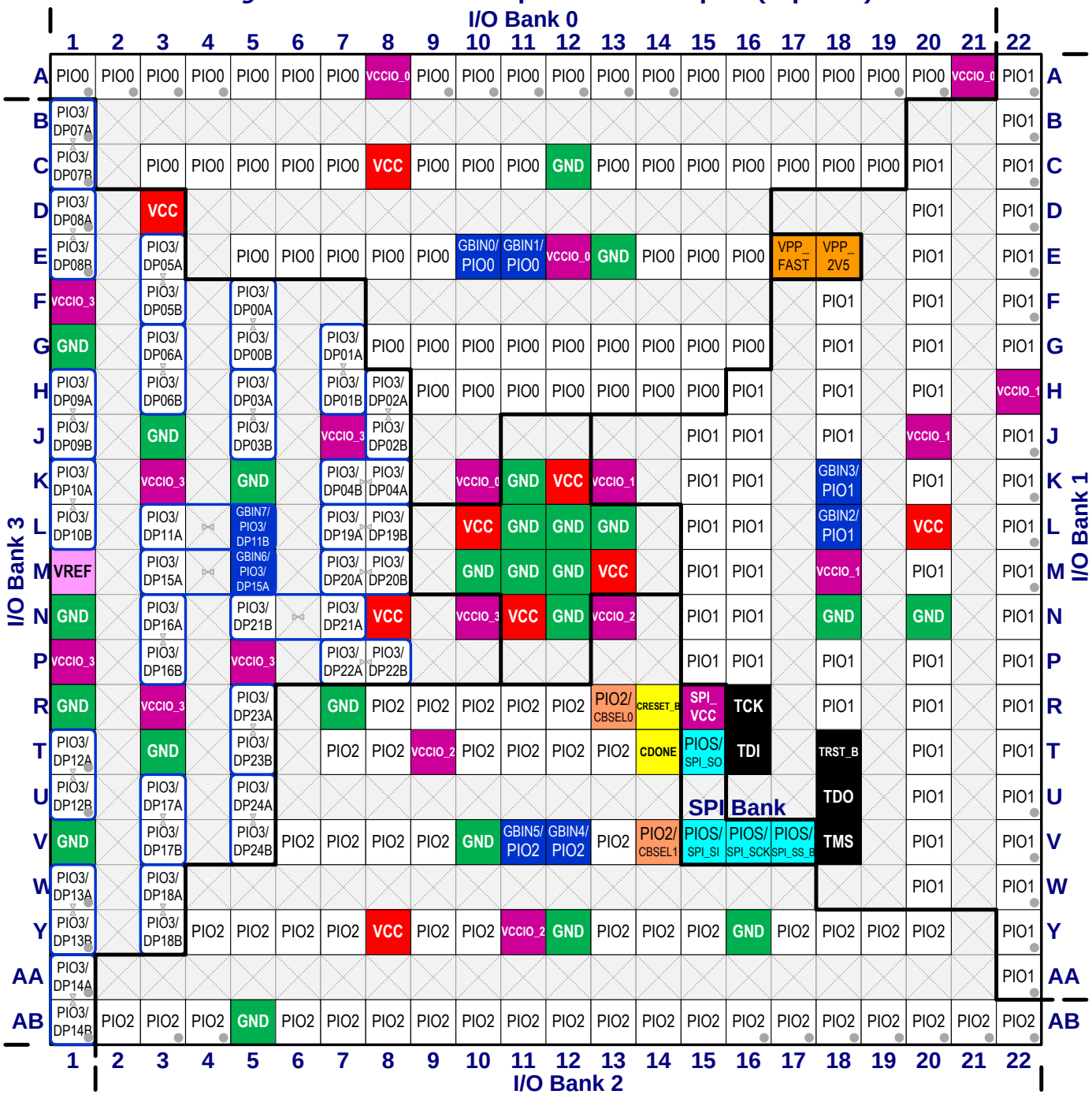
Figure 48 shows the CB284 chip-scale BGA footprint. The 8 x 8 mm CB132 package fits within the same ball pattern as the 12 x 12 mm CB284 package. In other words, the central 8 x 8 section of the CB284 footprint matches the CB132 footprint.

Figure 31 shows the conventions used in the diagram.

Also see Table 44 for a complete, detailed pinout for the 132-ball and 284-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

Figure 48: **iCE65 CB284 Chip-Scale BGA Footprint (Top View)**



Pinout Table

Table 44 provides a detailed pinout table for the two chip-scale BGA packages. Pins are generally arranged by I/O bank, then by ball function. The balls with a black circle (●) are unconnected balls (N.C.) for the iCE65L04 in the CB284 package. The CB132 package fits within the CB284 package footprint as shown in Figure 48. The right-most column shows which CB132 ball corresponds to the CB284.

The table also highlights the differential I/O pairs in I/O Bank 3.

Table 44: iCE65 CB284 Chip-scale BGA Pinout Table (with CB132 cross reference)

Ball Function	Ball Number	Pin Type by Device		Bank	CB132 Ball Equivalent
	iCE65L04 iCE65L08	iCE65L04	iCE65L08		
GBIN0/PIO0	E10	GBIN	GBIN	0	A6
GBIN1/PIO0	E11	GBIN	GBIN	0	A7
PIO0 (●)	A1	N.C.	PIO	0	—
PIO0 (●)	A2	N.C.	PIO	0	—
PIO0 (●)	A3	N.C.	PIO	0	—
PIO0 (●)	A4	N.C.	PIO	0	—
PIO0	A5	PIO	PIO	0	—
PIO0	A6	PIO	PIO	0	—
PIO0	A7	PIO	PIO	0	—
PIO0 (●)	A9	N.C.	PIO	0	—
PIO0 (●)	A10	N.C.	PIO	0	—
PIO0 (●)	A11	N.C.	PIO	0	—
PIO0 (●)	A12	N.C.	PIO	0	—
PIO0 (●)	A13	N.C.	PIO	0	—
PIO0	A15	PIO	PIO	0	—
PIO0	A16	PIO	PIO	0	—
PIO0	A17	PIO	PIO	0	—
PIO0	A18	PIO	PIO	0	—
PIO0 (●)	A14	N.C.	PIO	0	—
PIO0 (●)	A19	N.C.	PIO	0	—
PIO0 (●)	A20	N.C.	PIO	0	—
PIO0	C3	PIO	PIO	0	—
PIO0	C4	PIO	PIO	0	—
PIO0	C5	PIO	PIO	0	—
PIO0	C6	PIO	PIO	0	—
PIO0	C7	PIO	PIO	0	—
PIO0	C9	PIO	PIO	0	—
PIO0	C10	PIO	PIO	0	—
PIO0	C11	PIO	PIO	0	—
PIO0	C13	PIO	PIO	0	—
PIO0	C14	PIO	PIO	0	—
PIO0	C15	PIO	PIO	0	—
PIO0	C16	PIO	PIO	0	—
PIO0	C17	PIO	PIO	0	—
PIO0	C18	PIO	PIO	0	—
PIO0	C19	PIO	PIO	0	—
PIO0	E5	PIO	PIO	0	A1
PIO0	E6	PIO	PIO	0	A2
PIO0	E7	PIO	PIO	0	A3
PIO0	E8	PIO	PIO	0	A4
PIO0	E9	PIO	PIO	0	A5
PIO0	E14	PIO	PIO	0	A10

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO0	E15	PIO	PIO	0	A11
PIO0	E16	PIO	PIO	0	A12
PIO0	G8	PIO	PIO	0	C4
PIO0	G9	PIO	PIO	0	C5
PIO0	G10	PIO	PIO	0	C6
PIO0	G11	PIO	PIO	0	C7
PIO0	G12	PIO	PIO	0	C8
PIO0	G13	PIO	PIO	0	C9
PIO0	G14	PIO	PIO	0	C10
PIO0	G15	PIO	PIO	0	C11
PIO0	G16	PIO	PIO	0	C12
PIO0	H9	PIO	PIO	0	D5
PIO0	H10	PIO	PIO	0	D6
PIO0	H11	PIO	PIO	0	D7
PIO0	H12	PIO	PIO	0	D8
PIO0	H13	PIO	PIO	0	D9
PIO0	H14	PIO	PIO	0	D10
PIO0	H15	PIO	PIO	0	D11
VCCIO_0	A8	VCCIO	VCCIO	0	—
VCCIO_0	A21	VCCIO	VCCIO	0	—
VCCIO_0	E12	VCCIO	VCCIO	0	A8
VCCIO_0	K10	VCCIO	VCCIO	0	F6
GBIN2/PIO1	L18	GBIN	GBIN	1	G14
GBIN3/PIO1	K18	GBIN	GBIN	1	F14
PIO1 (●)	A22	N.C.	PIO	1	—
PIO1 (●)	AA22	N.C.	PIO	1	—
PIO1 (●)	B22	N.C.	PIO	1	—
PIO1	C20	PIO	PIO	1	—
PIO1 (●)	C22	N.C.	PIO	1	—
PIO1	D20	PIO	PIO	1	—
PIO1 (●)	D22	N.C.	PIO	1	—
PIO1	E20	PIO	PIO	1	—
PIO1 (●)	E22	N.C.	PIO	1	—
PIO1	F18	PIO	PIO	1	B14
PIO1	F20	PIO	PIO	1	—
PIO1 (●)	F22	N.C.	PIO	1	—
PIO1	G18	PIO	PIO	1	C14
PIO1	G20	PIO	PIO	1	—
PIO1	G22	PIO	PIO	1	—
PIO1	H16	PIO	PIO	1	D12
PIO1	H18	PIO	PIO	1	D14
PIO1	H20	PIO	PIO	1	—
PIO1	J15	PIO	PIO	1	E11
PIO1	J16	PIO	PIO	1	E12
PIO1	J18	PIO	PIO	1	E14
PIO1 (●)	J22	N.C.	PIO	1	—
PIO1	K15	PIO	PIO	1	F11
PIO1	K16	PIO	PIO	1	F12
PIO1	K20	PIO	PIO	1	—
PIO1 (●)	K22	N.C.	PIO	1	—

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO1	L15	PIO	PIO	1	G11
PIO1	L16	PIO	PIO	1	G12
PIO1 (●)	L22	N.C.	PIO	1	—
PIO1	M15	PIO	PIO	1	H11
PIO1	M16	PIO	PIO	1	H12
PIO1	M20	PIO	PIO	1	—
PIO1 (●)	M22	N.C.	PIO	1	—
PIO1	N15	PIO	PIO	1	J11
PIO1	N16	PIO	PIO	1	J12
PIO1	N22	PIO	PIO	1	—
PIO1	P15	PIO	PIO	1	K11
PIO1	P16	PIO	PIO	1	K12
PIO1	P18	PIO	PIO	1	K14
PIO1	P20	PIO	PIO	1	—
PIO1	P22	PIO	PIO	1	—
PIO1	R18	PIO	PIO	1	L14
PIO1	R20	PIO	PIO	1	—
PIO1	R22	PIO	PIO	1	—
PIO1	T20	PIO	PIO	1	—
PIO1	T22	PIO	PIO	1	—
PIO1	U20	PIO	PIO	1	—
PIO1 (●)	U22	N.C.	PIO	1	—
PIO1	V20	PIO	PIO	1	—
PIO1 (●)	V22	N.C.	PIO	1	—
PIO1	W20	PIO	PIO	1	—
PIO1 (●)	W22	N.C.	PIO	1	—
PIO1 (●)	Y22	N.C.	PIO	1	—
TCK	R16	JTAG	JTAG	1	L12
TDI	T16	JTAG	JTAG	1	M12
TDO	U18	JTAG	JTAG	1	N14
TMS	V18	JTAG	JTAG	1	P14
TRST_B	T18	JTAG	JTAG	1	M14
VCCIO_1	H22	VCCIO	VCCIO	1	—
VCCIO_1	J20	VCCIO	VCCIO	1	—
VCCIO_1	K13	VCCIO	VCCIO	1	F9
VCCIO_1	M18	VCCIO	VCCIO	1	H14
CDONE	T14	CONFIG	CONFIG	2	M10
CRESET_B	R14	CONFIG	CONFIG	2	L10
GBIN4/PIO2	V12	GBIN	GBIN	2	P7
GBIN5/PIO2	V11	GBIN	GBIN	2	P8
PIO2	R8	PIO	PIO	2	L4
PIO2	R9	PIO	PIO	2	L5
PIO2	R10	PIO	PIO	2	L6
PIO2	R11	PIO	PIO	2	L7
PIO2	R12	PIO	PIO	2	L8
PIO2	T7	PIO	PIO	2	M3
PIO2	T8	PIO	PIO	2	M4
PIO2	T10	PIO	PIO	2	M6
PIO2	T11	PIO	PIO	2	M7
PIO2	T12	PIO	PIO	2	M8

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO2	T13	PIO	PIO	2	M9
PIO2	V6	PIO	PIO	2	P2
PIO2	V7	PIO	PIO	2	P3
PIO2	V8	PIO	PIO	2	P4
PIO2	V9	PIO	PIO	2	P5
PIO2	V13	PIO	PIO	2	P9
PIO2	Y4	PIO	PIO	2	—
PIO2	Y5	PIO	PIO	2	—
PIO2	Y6	PIO	PIO	2	—
PIO2	Y7	PIO	PIO	2	—
PIO2	Y9	PIO	PIO	2	—
PIO2	Y10	PIO	PIO	2	—
PIO2	Y13	PIO	PIO	2	—
PIO2	Y14	PIO	PIO	2	—
PIO2	Y15	PIO	PIO	2	—
PIO2	Y17	PIO	PIO	2	—
PIO2	Y18	PIO	PIO	2	—
PIO2	Y19	PIO	PIO	2	—
PIO2	Y20	PIO	PIO	2	—
PIO2	AB2	PIO	PIO	2	—
PIO2 (●)	AB3	N.C.	PIO	2	—
PIO2 (●)	AB4	N.C.	PIO	2	—
PIO2	AB6	PIO	PIO	2	—
PIO2	AB7	PIO	PIO	2	—
PIO2	AB8	PIO	PIO	2	—
PIO2	AB9	PIO	PIO	2	—
PIO2	AB10	PIO	PIO	2	—
PIO2	AB11	PIO	PIO	2	—
PIO2	AB12	PIO	PIO	2	—
PIO2	AB13	PIO	PIO	2	—
PIO2	AB14	PIO	PIO	2	—
PIO2	AB15	PIO	PIO	2	—
PIO2 (●)	AB16	N.C.	PIO	2	—
PIO2 (●)	AB17	N.C.	PIO	2	—
PIO2 (●)	AB18	N.C.	PIO	2	—
PIO2 (●)	AB19	N.C.	PIO	2	—
PIO2 (●)	AB20	N.C.	PIO	2	—
PIO2 (●)	AB21	N.C.	PIO	2	—
PIO2 (●)	AB22	N.C.	PIO	2	—
PIO2/CBSEL0	R13	PIO	PIO	2	L9
PIO2/CBSEL1	V14	PIO	PIO	2	P10
VCCIO_2	N13	VCCIO	VCCIO	2	J9
VCCIO_2	T9	VCCIO	VCCIO	2	M5
VCCIO_2	Y11	VCCIO	VCCIO	2	—
PIO3/DP00A	F5	DPIO	DPIO	3	B1
PIO3/DP00B	G5	DPIO	DPIO	3	C1
PIO3/DP01A	G7	DPIO	DPIO	3	C3
PIO3/DP01B	H7	DPIO	DPIO	3	D3
PIO3/DP02A	H8	DPIO	DPIO	3	D4
PIO3/DP02B	J8	DPIO	DPIO	3	E4

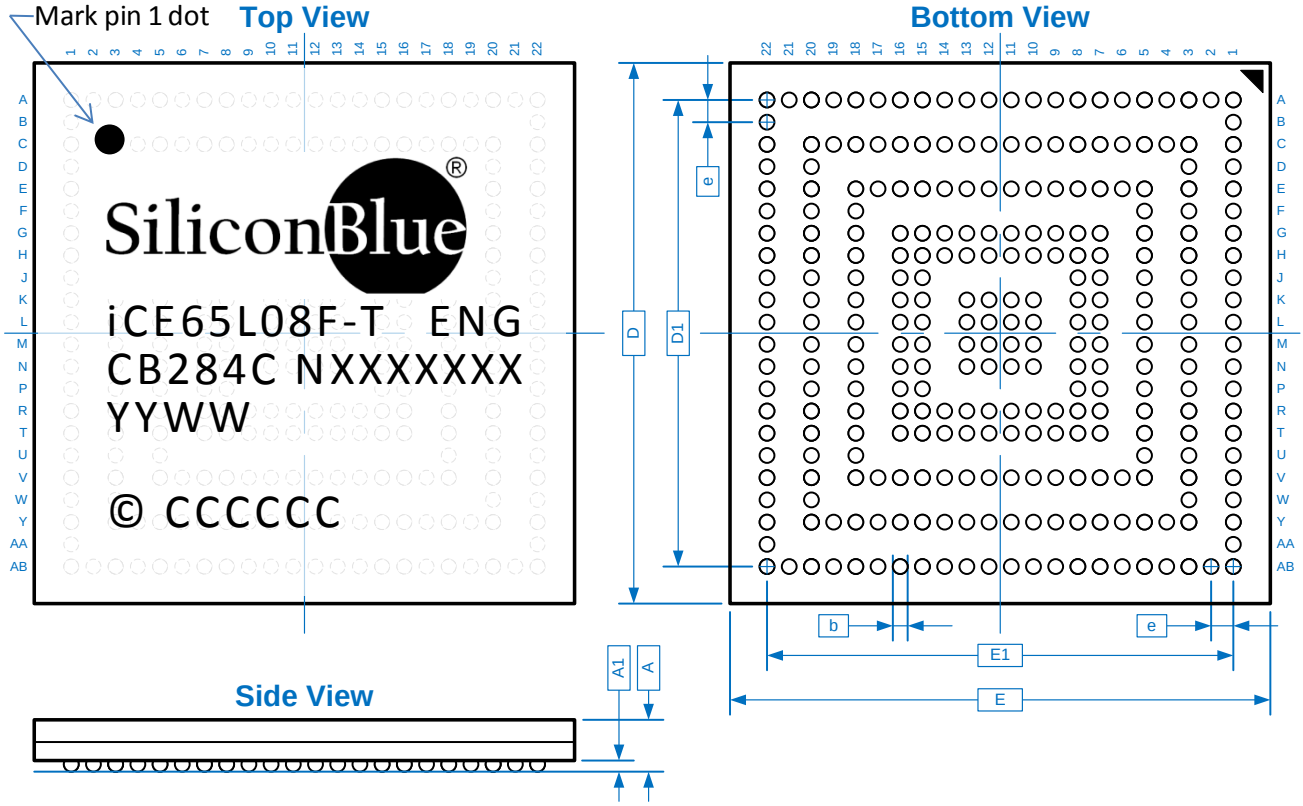
Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO3/DP03A	H5	DPIO	DPIO	3	D1
PIO3/DP03B	J5	DPIO	DPIO	3	E1
PIO3/DP04A	K8	DPIO	DPIO	3	F4
PIO3/DP04B	K7	DPIO	DPIO	3	F3
PIO3/DP05A	E3	DPIO	DPIO	3	—
PIO3/DP05B	F3	DPIO	DPIO	3	—
PIO3/DP06A	G3	DPIO	DPIO	3	—
PIO3/DP06B	H3	DPIO	DPIO	3	—
PIO3/DP07A (●)	B1	N.C.	DPIO	3	—
PIO3/DP07B (●)	C1	N.C.	DPIO	3	—
PIO3/DP08A (●)	D1	N.C.	DPIO	3	—
PIO3/DP08B (●)	E1	N.C.	DPIO	3	—
PIO3/DP09A	H1	DPIO	DPIO	3	—
PIO3/DP09B	J1	DPIO	DPIO	3	—
PIO3/DP10A	K1	DPIO	DPIO	3	—
PIO3/DP10B	L1	DPIO	DPIO	3	—
PIO3/DP11A	L3	DPIO	DPIO	3	—
GBIN7/PIO3/DP11B	L5	GBIN	GBIN	3	G1
PIO3/DP12A (●)	T1	N.C.	DPIO	3	—
PIO3/DP12B (●)	U1	N.C.	DPIO	3	—
PIO3/DP13A (●)	W1	N.C.	DPIO	3	—
PIO3/DP13B (●)	Y1	N.C.	DPIO	3	—
PIO3/DP14A (●)	AA1	N.C.	DPIO	3	—
PIO3/DP14B (●)	AB1	N.C.	DPIO	3	—
GBIN6/PIO3/DP15A	M5	GBIN	GBIN	3	H1
PIO3/DP15B	M3	DPIO	DPIO	3	—
PIO3/DP16A	N3	DPIO	DPIO	3	—
PIO3/DP16B	P3	DPIO	DPIO	3	—
PIO3/DP17A	U3	DPIO	DPIO	3	—
PIO3/DP17B	V3	DPIO	DPIO	3	—
PIO3/DP18A	W3	DPIO	DPIO	3	—
PIO3/DP18B	Y3	DPIO	DPIO	3	—
PIO3/DP19A	L7	DPIO	DPIO	3	G3
PIO3/DP19B	L8	DPIO	DPIO	3	G4
PIO3/DP20A	M7	DPIO	DPIO	3	H3
PIO3/DP20B	M8	DPIO	DPIO	3	H4
PIO3/DP21A	N7	DPIO	DPIO	3	J3
PIO3/DP21B	N5	DPIO	DPIO	3	J1
PIO3/DP22A	P7	DPIO	DPIO	3	K3
PIO3/DP22B	P8	DPIO	DPIO	3	K4
PIO3/DP23A	R5	DPIO	DPIO	3	L1
PIO3/DP23B	T5	DPIO	DPIO	3	M1
PIO3/DP24A	U5	DPIO	DPIO	3	N1
PIO3/DP24B	V5	DPIO	DPIO	3	P1
VCCIO_3	F1	VCCIO	VCCIO	3	—
VCCIO_3	P1	VCCIO	VCCIO	3	—

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
VCCIO_3	J7	VCCIO	VCCIO	3	E3
VCCIO_3	K3	VCCIO	VCCIO	3	—
VCCIO_3	N10	VCCIO	VCCIO	3	J6
VCCIO_3	P5	VCCIO	VCCIO	3	K1
VCCIO_3	R3	VCCIO	VCCIO	3	—
VREF	M1	VREF	VREF	3	—
PIOS/SPI_SO	T15	SPI	SPI	SPI	M11
PIOS/SPI_SI	V15	SPI	SPI	SPI	P11
PIOS/SPI_SCK	V16	SPI	SPI	SPI	P12
PIOS/SPI_SS_B	V17	SPI	SPI	SPI	P13
SPI_VCC	R15	SPI	SPI	SPI	L11
GND	C12	GND	GND	GND	—
GND	E13	GND	GND	GND	A9
GND	J3	GND	GND	GND	—
GND	K5	GND	GND	GND	F1
GND	K11	GND	GND	GND	F7
GND	L11	GND	GND	GND	G7
GND	L12	GND	GND	GND	G8
GND	L13	GND	GND	GND	G9
GND	M10	GND	GND	GND	H6
GND	M11	GND	GND	GND	H7
GND	M12	GND	GND	GND	H8
GND	N1	GND	GND	GND	—
GND	N12	GND	GND	GND	J8
GND	N18	GND	GND	GND	J14
GND	N20	GND	GND	GND	—
GND	R7	GND	GND	GND	L3
GND	T3	GND	GND	GND	—
GND	V1	GND	GND	GND	—
GND	V10	GND	GND	GND	P6
GND	Y12	GND	GND	GND	—
GND	Y16	GND	GND	GND	—
GND	AB5	GND	GND	GND	—
GND	G1	GND	GND	GND	—
GND	R1	GND	GND	GND	—
VCC	C8	VCC	VCC	VCC	—
VCC	D3	VCC	VCC	VCC	—
VCC	K12	VCC	VCC	VCC	F8
VCC	L10	VCC	VCC	VCC	G6
VCC	L20	VCC	VCC	VCC	—
VCC	M13	VCC	VCC	VCC	H9
VCC	N8	VCC	VCC	VCC	J4
VCC	N11	VCC	VCC	VCC	J7
VCC	Y8	VCC	VCC	VCC	—
VPP_2V5	E18	VPP	VPP	VPP	A14
VPP_FAST	E17	VPP	VPP	VPP	A13

Package Mechanical Drawing

Figure 49: CB284 Package Mechanical Drawing

CB284: 12 x 12 mm, 284-ball, 0.5 mm ball-pitch, chip-scale ball grid array



Description		Symbol	Min.	Nominal	Max.	Units
Number of Ball Columns	X			22		Columns
Number of Ball Rows	Y			22		Rows
Number of Signal Balls		n		284		Balls
Body Size	X	E	11.90	12.00	12.10	mm
	Y	D	11.90	12.00	12.10	
Ball Pitch		e	—	0.50	—	
Ball Diameter		b	0.27	—	0.37	
Edge Ball Center to Center	X	E1	—	10.50	—	
	Y	D1	—	10.50	—	
Package Height		A	—	—	1.00	
Stand Off		A1	0.16	—	0.26	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L08F	Part number
	-T	Power/Speed
	ENG	Engineering
3	CB284C NXXXXXXX	Package type and Lot number
4	YYWW	Date Code
5	N/A	Blank
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
35	28

Die Cross Reference

The tables in this section list all the pads on a specific die type and provide a cross reference on how a specific pad connects to a ball or pin in each of the available package offerings. Similarly, the tables provide the pad coordinates for the die-based version of the product (DiePlus). These tables also provide a way to prototype with one package option and then later move to a different package or die.

As described in "Input and Output Register Control per PIO Pair" on page 16, PIO pairs share register control inputs. Similarly, as described in "Differential Inputs and Outputs" on page 12, a PIO pair can form a differential input or output. PIO pairs in I/O Bank 3 are optionally differential inputs or differential outputs. PIO pairs in all other I/O Banks are optionally differential outputs. In the tables, differential pairs are surrounded by a heavy blue box.

iCE65L04

Table 45 lists all the pads on the iCE65L04 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L04 DiePlus product, please refer to the following data sheet.

DiePlus Advantage FPGA Known Good Die

Table 45: iCE65L04 Die Cross Reference

iCE65L04	DiePlus						
Pad Name	VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	1	B1	C1	F5	1	129.40	2,687.75
PIO3_01/DP00B	2	C1	B1	G5	2	231.40	2,642.74
PIO3_02/DP01A	3	C3	D3	G7	3	129.40	2,597.75
PIO3_03/DP01B	4	D3	C3	H7	4	231.40	2,552.74
GND	5	F1	F1	K5	5	129.40	2,507.75
GND	—	—	—	—	6	231.40	2,462.74
VCCIO_3	6	E3	E3	J7	7	129.40	2,417.75
VCCIO_3	—	—	—	—	8	231.40	2,372.74
PIO3_04/DP02A	7	D4	D1	H8	9	129.40	2,327.75
PIO3_05/DP02B	8	E4	D2	J8	10	231.40	2,292.74
PIO3_06/DP03A	—	D1	E1	H5	11	129.40	2,257.75
PIO3_07/DP03B	—	E1	E2	J5	12	231.40	2,222.74
VCC	—	—	H9	D3	13	129.40	2,187.75
PIO3_08/DP04A	9	F4	D4	K8	14	231.40	2,152.74
PIO3_09/DP04B	10	F3	E4	K7	15	129.40	2,117.75
PIO3_10/DP05A	—	—	F3	E3	16	231.40	2,082.74
PIO3_11/DP05B	—	—	F4	F3	17	129.40	2,047.75
GND	—	H6	A9	M10	18	231.40	2,012.74
PIO3_12/DP06A	—	—	F5	G3	19	129.40	1,977.75
PIO3_13/DP06B	—	—	E5	H3	20	231.40	1,942.74
GND	—	—	A9	J3	21	129.40	1,907.75
GND	—	—	—	—	22	231.40	1,872.74
PIO3_14/DP07A	—	—	—	H1	23	129.40	1,837.75
PIO3_15/DP07B	—	—	—	J1	24	231.40	1,802.74
VCCIO_3	—	—	K1	K3	25	129.40	1,767.75
VCC	11	G6	G6	L10	26	231.40	1,732.74
PIO3_16/DP08A	—	—	—	K1	27	129.40	1,697.75
PIO3_17/DP08B	—	—	—	L1	28	231.40	1,662.74

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_18/DP09A	12	—	G2	L3	29	129.40	1,627.75
GBIN7/PIO3_19/DP09B	13	G1	G1	L5	30	231.40	1,592.74
VCCIO_3	14	J6	J6	N10	31	129.40	1,557.75
VREF	N/A	N/A	N/A	M1	32	231.40	1,522.74
GND	—	—	A9	N1	33	129.40	1,487.75
GBIN6/PIO3_20/DP10A	15	H1	H1	M5	34	231.40	1,452.74
PIO3_21/DP10B	16	—	H2	M3	35	129.40	1,417.75
GND	17	H7	A9	M11	36	231.40	1,382.74
PIO3_22/DP11A	—	—	G3	N3	37	129.40	1,347.75
PIO3_23/DP11B	—	—	G4	P3	38	231.40	1,312.74
VCCIO_3	—	—	K1	R3	39	129.40	1,277.75
VCCIO_3	—	—	—	—	40	231.40	1,242.74
GND	—	—	A9	T3	41	129.40	1,207.75
GND	—	—	—	—	42	231.40	1,172.74
PIO3_24/DP12A	—	—	J1	U3	43	129.40	1,137.75
PIO3_25/DP12B	—	—	J2	V3	44	231.40	1,102.74
GND	—	—	A9	V1	45	129.40	1,067.75
PIO3_26/DP13A	—	—	H4	W3	46	231.40	1,032.74
PIO3_27/DP13B	—	—	H3	Y3	47	129.40	997.75
PIO3_28/DP14A	18	G3	K2	L7	48	231.40	962.74
PIO3_29/DP14B	19	G4	J3	L8	49	129.40	927.75
PIO3_30/DP15A	—	H3	H5	M7	50	231.40	892.74
PIO3_31/DP15B	—	H4	G5	M8	51	129.40	857.75
VCC	—	J4	F2	N8	52	231.40	822.74
PIO3_32/DP16A	20	J3	L1	N7	53	129.40	787.75
PIO3_33/DP16B	21	J1	L2	N5	54	231.40	752.74
VCCIO_3	22	K1	K1	P5	55	129.40	717.75
VCCIO_3	—	—	—	—	56	231.40	682.74
GND	23	L3	L3	R7	57	129.40	637.75
GND	—	—	—	—	58	231.40	592.74
PIO3_34/DP17A	—	K3	M1	P7	59	129.40	547.75
PIO3_35/DP17B	—	K4	M2	P8	60	231.40	502.74
PIO3_36/DP18A	24	L1	K3	R5	61	129.40	457.75
PIO3_37/DP18B	25	M1	K4	T5	62	231.40	412.74
PIO3_38/DP19A	—	N1	N1	U5	63	129.40	367.75
PIO3_39/DP19B	—	P1	N2	V5	64	231.40	322.74
PIO2_00	—	—	—	AB2	65	545.00	139.20
PIO2_01	—	P2	L4	V6	66	595.00	37.20
PIO2_02	—	M3	M3	T7	67	645.00	139.20
GND	—	—	C2	AB5	68	695.00	37.20
PIO2_03	26	L4	P1	R8	69	745.00	139.20
PIO2_04	27	P3	N3	V7	70	795.00	37.20
PIO2_05	28	M4	P2	T8	71	845.00	139.20
PIO2_06	29	L5	L5	R9	72	895.00	37.20
PIO2_07	30	P4	M4	V8	73	930.00	139.20

iCE65L04 Pad Name	DiePlus				Pad	X (µm)	Y (µm)
	VQ100	CB132	CB196	CB284			
PIO2_08	—	L6	P3	R10	74	965.00	37.20
VCCIO_2	31	M5	M5	T9	75	1,000.00	139.20
PIO2_09	—	P5	K5	V9	76	1,035.00	37.20
PIO2_10	—	M6	N4	T10	77	1,070.00	139.20
GND	32	P6	H7	V10	78	1,105.00	37.20
PIO2_11	—	—	P4	Y4	79	1,140.00	139.20
PIO2_12	—	—	L6	Y5	80	1,175.00	37.20
PIO2_13	—	—	—	AB6	81	1,210.00	139.20
PIO2_14	—	—	—	AB7	82	1,245.00	37.20
PIO2_15	—	—	—	AB8	83	1,280.00	139.20
PIO2_16	—	—	—	AB9	84	1,315.00	37.20
PIO2_17	—	—	—	AB10	85	1,350.00	139.20
PIO2_18	—	—	—	AB11	86	1,385.00	37.20
GND	—	J8	H8	N12	87	1,420.00	139.20
PIO2_19	—	—	K6	Y6	88	1,455.00	37.20
PIO2_20	—	—	N5	Y7	89	1,490.00	139.20
VCC	—	—	J4	Y8	90	1,525.00	37.20
PIO2_21	—	—	M6	Y9	91	1,560.00	139.20
PIO2_22	—	—	N6	Y10	92	1,595.00	37.20
GBIN5/PIO2_23	33	P7	P5	V11	93	1,630.00	139.20
GBIN4/PIO2_24	34	P8	L7	V12	94	1,665.00	37.20
PIO2_25	—	—	—	AB12	95	1,700.00	139.20
VCCIO_2	—	—	J9	Y11	96	1,735.00	37.20
PIO2_26	—	—	—	AB13	97	1,770.00	139.20
PIO2_27	—	—	K7	AB14	98	1,805.00	37.20
GND	—	—	J5	Y12	99	1,840.00	139.20
PIO2_28	—	—	K9	AB15	100	1,875.00	37.20
PIO2_29	—	—	M7	Y13	101	1,910.00	139.20
PIO2_30	—	—	K8	Y14	102	1,945.00	37.20
PIO2_31	—	—	P7	Y15	103	1,980.00	139.20
PIO2_32	—	—	L8	Y17	104	2,015.00	37.20
PIO2_33	—	—	P8	Y18	105	2,050.00	139.20
PIO2_34	—	—	N8	Y19	106	2,085.00	37.20
PIO2_35	—	—	M8	Y20	107	2,120.00	139.20
VCC	35	J7	J7	N11	108	2,155.00	37.20
VCC	—	—	—	—	109	2,190.00	139.20
PIO2_36	36	P9	P9	V13	110	2,225.00	37.20
PIO2_37	37	M7	N9	T11	111	2,260.00	139.20
VCCIO_2	38	J9	N10	N13	112	2,295.00	37.20
PIO2_38	—	L7	M9	R11	113	2,330.00	139.20
GND	39	H8	J8	M12	114	2,365.00	37.20
PIO2_39	—	M8	N12	T12	115	2,400.00	139.20
PIO2_40	—	L8	N11	R12	116	2,435.00	37.20
PIO2_41	40	M9	N13	T13	117	2,470.00	139.20
PIO2_42/CBSEL0	41	L9	L9	R13	118	2,505.00	37.20
PIO2_43/CBSEL1	42	P10	P10	V14	119	2,540.00	139.20
CDONE	43	M10	M10	T14	120	2,575.00	37.20

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
CRESET_B	44	L10	L10	R14	121	2,625.00	139.20
PIOS_00/SPI_SO	45	M11	M11	T15	122	2,690.00	37.20
PIOS_01/SPI_SI	46	P11	P11	V15	123	2,740.00	139.20
GND	47	—	P6	Y16	124	2,790.00	37.20
PIOS_02/SPI_SCK	48	P12	P12	V16	125	2,840.00	139.20
PIOS_03/SPI_SS_B	49	P13	P13	V17	126	2,890.00	37.20
SPI_VCC	50	L11	L11	R15	127	2,990.00	37.20
TDI	N/A	M12	M12	T16	128	3,610.80	342.00
TMS	N/A	P14	P14	V18	129	3,712.80	392.00
TCK	N/A	L12	L12	R16	130	3,610.80	442.00
TDO	N/A	N14	N14	U18	131	3,712.80	492.00
TRST_B	N/A	M14	M14	T18	132	3,610.80	542.00
PIO1_00	51	L14	K11	R18	133	3,712.80	592.00
PIO1_01	52	K12	L13	P16	134	3,610.80	642.00
PIO1_02	53	K11	K12	P15	135	3,712.80	692.00
PIO1_03	54	K14	M13	P18	136	3,610.80	727.00
GND	55	J14	J14	N18	137	3,712.80	762.00
GND	55	J14	J14	N18	138	3,610.80	797.00
PIO1_04	56	J12	J10	N16	139	3,712.80	832.00
PIO1_05	57	J11	L14	N15	140	3,610.80	867.00
VCCIO_1	58	H14	H14	M18	141	3,712.80	902.00
VCCIO_1	—	—	—	—	142	3,610.80	937.00
PIO1_06	59	H12	J11	M16	143	3,712.80	972.00
PIO1_07	60	H11	K14	M15	144	3,610.80	1,007.00
PIO1_08	—	—	H10	W20	145	3,712.80	1,042.00
PIO1_09	—	—	J13	V20	146	3,610.80	1,077.00
PIO1_10	—	—	J12	U20	147	3,712.80	1,112.00
VCC	61	H9	N7	M13	148	3,610.80	1,147.00
VCC	—	—	—	—	149	3,712.80	1,182.00
PIO1_11	—	—	H13	T22	150	3,610.80	1,217.00
PIO1_12	—	—	H12	R22	151	3,712.80	1,252.00
PIO1_13	—	—	—	P22	152	3,610.80	1,287.00
PIO1_14	—	—	—	N22	153	3,712.80	1,322.00
PIO1_15		—	G13	T20	154	3,610.80	1,357.00
PIO1_16	—	—	H11	R20	155	3,712.80	1,392.00
PIO1_17	—	—	G14	P20	156	3,610.80	1,427.00
GND	—	—	K10	N20	157	3,712.80	1,462.00
GND	—	—	—	—	158	3,610.80	1,497.00
PIO1_18	—	—	G10	M20	159	3,712.80	1,532.00
GBIN3/PIO1_19	62	F14	G12	K18	160	3,610.80	1,567.00
GBIN2/PIO1_20	63	G14	F10	L18	161	3,712.80	1,602.00
PIO1_21	—	—	F14	K20	162	3,610.80	1,637.00
VCCIO_1	—	—	H14	J20	163	3,712.80	1,672.00
VCCIO_1	—	—	—	—	164	3,610.80	1,707.00
PIO1_22	—	—	F13	H20	165	3,712.80	1,742.00
PIO1_23	—	—	D13	G20	166	3,610.80	1,777.00

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO1_24	—	—	G11	F20	167	3,712.80	1,812.00
PIO1_25	—	—	F11	E20	168	3,610.80	1,847.00
PIO1_26	—	—	E10	D20	169	3,712.80	1,882.00
PIO1_27	—	—	E14	C20	170	3,610.80	1,917.00
GND	—	G8	G8	L12	171	3,712.80	1,952.00
GND	—	—	—	—	172	3,610.80	1,987.00
PIO1_28	—	—	F12	G22	173	3,712.80	2,022.00
PIO1_29	—	G12	D14	L16	174	3,610.80	2,057.00
PIO1_30	64	G11	E13	L15	175	3,712.80	2,092.00
PIO1_31	65	F12	C14	K16	176	3,610.80	2,127.00
VCC	—	—	K13	L20	177	3,712.80	2,162.00
VCC	—	—	—	—	178	3,610.80	2,197.00
PIO1_32	66	E14	E11	J18	179	3,712.80	2,232.00
PIO1_33	—	F11	C13	K15	180	3,610.80	2,267.00
VCCIO_1	67	F9	F9	K13	181	3,712.80	2,302.00
VCCIO_1	—	—	—	—	182	3,610.80	2,337.00
PIO1_34	68	E12	E12	J16	183	3,712.80	2,377.00
PIO1_35	69	D14	B14	H18	184	3,610.80	2,427.00
GND	70	G9	G9	L13	185	3,712.80	2,477.00
PIO1_36	71	E11	B13	J15	186	3,610.80	2,527.00
PIO1_37	72	D12	D12	H16	187	3,712.80	2,577.00
PIO1_38	73	C14	C12	G18	188	3,610.80	2,627.00
PIO1_39	74	B14	D11	F18	189	3,712.80	2,677.00
VPP_2V5	75	A14	A14	E18	190	3,610.80	2,739.68
VPP_FAST	76	A13	A13	E17	191	3,097.00	2,962.80
VCC	77	F8	F8	K12	192	2,997.00	2,860.80
VCC	77	F8	F8	K12	193	2,947.00	2,962.80
PIO0_00	78	A12	C11	E16	194	2,897.00	2,860.80
PIO0_01	—	C12	—	G16	195	2,847.00	2,962.80
PIO0_02	79	A11	A12	E15	196	2,797.00	2,860.80
PIO0_03	80	C11	B11	G15	197	2,747.00	2,962.80
PIO0_04	—	D11	—	H15	198	2,697.00	2,860.80
PIO0_05	81	A10	D10	E14	199	2,647.00	2,962.80
PIO0_06	82	C10	A11	G14	200	2,612.00	2,860.80
PIO0_07	83	D10	D9	H14	201	2,577.00	2,962.80
GND	84	A9	H6	E13	202	2,542.00	2,860.80
GND	—	—	—	—	203	2,507.00	2,962.80
PIO0_08	85	C9	C10	G13	204	2,472.00	2,860.80
PIO0_09	86	D9	A10	H13	205	2,437.00	2,962.80
PIO0_10	87	C8	B10	G12	206	2,402.00	2,860.80
PIO0_11	—	D8	E9	H12	207	2,367.00	2,962.80
PIO0_12	—	—	—	A18	208	2,332.00	2,860.80
PIO0_13	—	—	—	A17	209	2,297.00	2,962.80
PIO0_14	—	—	—	A16	210	2,262.00	2,860.80
PIO0_15	—	—	—	A15	211	2,227.00	2,962.80
VCCIO_0	88	A8	A8	E12	212	2,192.00	2,860.80
VCCIO_0	—	—	—	—	213	2,157.00	2,962.80

iCE65L04 Pad Name	DiePlus VQ100	CB132	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_16	—	—	—	C19	214	2,122.00	2,860.80
PIO0_17	—	—	C9	C18	215	2,087.00	2,962.80
PIO0_18	—	—	B9	C17	216	2,052.00	2,860.80
PIO0_19	—	—	D8	C16	217	2,017.00	2,962.80
PIO0_20	—	—	C8	C15	218	1,982.00	2,860.80
PIO0_21	—	—	E8	C14	219	1,947.00	2,962.80
PIO0_22	—	—	B8	C13	220	1,912.00	2,860.80
GBIN1/PIO0_23	89	A7	E7	E11	221	1,877.00	2,962.80
GND	—	—	B12	C12	222	1,842.00	2,860.80
GND	—	—	—	—	223	1,807.00	2,962.80
GBIN0/PIO0_24	90	A6	A7	E10	224	1,772.00	2,860.80
PIO0_25	—	—	D7	C11	225	1,737.00	2,962.80
PIO0_26	—	—	C7	C10	226	1,702.00	2,860.80
PIO0_27	—	—	E6	C9	227	1,667.00	2,962.80
VCC	—	—	B7	C8	228	1,632.00	2,860.80
VCC	—	—	—	—	229	1,597.00	2,962.80
PIO0_28	—	—	A6	C7	230	1,562.00	2,860.80
PIO0_29	—	—	B6	C6	231	1,527.00	2,962.80
PIO0_30	—	—	A5	C5	232	1,492.00	2,860.80
PIO0_31	—	—	D6	C4	233	1,457.00	2,962.80
GND	—	F7	F7	K11	234	1,422.00	2,860.80
GND	—	—	—	—	235	1,387.00	2,962.80
PIO0_32	—	—	—	C3	236	1,352.00	2,860.80
PIO0_33	—	—	—	A7	237	1,317.00	2,962.80
PIO0_34	—	—	—	A6	238	1,282.00	2,860.80
PIO0_35	—	—	—	A5	239	1,247.00	2,962.80
PIO0_36	91	C7	C6	G11	240	1,212.00	2,860.80
VCCIO_0	92	F6	F6	K10	241	1,177.00	2,962.80
VCCIO_0	92	F6	F6	K10	242	1,142.00	2,860.80
PIO0_37	93	D7	C5	H11	243	1,107.00	2,962.80
PIO0_38	94	C6	B5	G10	244	1,072.00	2,860.80
PIO0_39	95	A5	A4	E9	245	1,037.00	2,962.80
PIO0_40	96	D6	B4	H10	246	1,002.00	2,860.80
PIO0_41	97	C5	D5	G9	247	967.00	2,962.80
PIO0_42	—	A4	A3	E8	248	917.00	2,860.80
GND	98	G7	G7	L11	249	867.00	2,962.80
PIO0_43	99	D5	B3	H9	250	817.00	2,860.80
PIO0_44	—	C4	C4	G8	251	767.00	2,962.80
PIO0_45	100	A3	A2	E7	252	717.00	2,860.80
PIO0_46	—	A2	A1	E6	253	667.00	2,962.80
PIO0_47	—	A1	B2	E5	254	617.00	2,860.80

iCE65L08

Table 46 lists all the pads on the iCE65L08 die and how these pads connect to the balls or pins in the supported package styles. Most VCC, VCCIO, and GND pads are double-bonded inside the package although the table shows only a single connection.

For additional information on the iCE65L08 DiePlus product, please refer to the following data sheet.

- DiePlusAdvantage FPGA Known Good Die

Table 46: iCE65L08 Die Cross Reference

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_00/DP00A	—	B1	1	129.735	3,882.665
PIO3_01/DP00B	—	C1	2	231.735	3,837.665
PIO3_02/DP01A	C1	F5	3	129.735	3,792.665
PIO3_03/DP01B	B1	G5	4	231.735	3,747.665
GND	C2	K5	5	129.735	3,702.665
GND	—	—	6	231.735	3,657.665
VCCIO_3	E3	J7	7	129.735	3,612.665
VCCIO_3	—	—	8	231.735	3,567.665
PIO3_04/DP02A	D3	E3	9	129.735	3,512.665
PIO3_05/DP02B	C3	F3	10	231.735	3,477.665
PIO3_06/DP03A	D1	G3	11	129.735	3,442.665
PIO3_07/DP03B	D2	H3	12	231.735	3,407.665
VCC	F2	D3	13	129.735	3,372.665
VCC	—	—	14	231.735	3,337.665
PIO3_08/DP04A	D4	D1	15	129.735	3,302.665
PIO3_09/DP04B	E4	E1	16	231.735	3,267.665
PIO3_10/DP05A	—	H1	17	129.735	3,232.665
PIO3_11/DP05B	—	J1	18	231.735	3,197.665
GND	F1	M10	19	129.735	3,162.665
GND	—	—	20	231.735	3,127.665
PIO3_12/DP06A	E2	H5	21	129.735	3,092.665
PIO3_13/DP06B	E1	J5	22	231.735	3,057.665
GND	L3	J3	23	129.735	3,022.665
GND	—	—	24	231.735	2,987.665
PIO3_14/DP07A	F5	K1	25	129.735	2,952.665
PIO3_15/DP07B	E5	L1	26	231.735	2,917.665
VCCIO_3	E3	K3	27	129.735	2,882.665
VCCIO_3	—	—	28	231.735	2,847.665
VCC	G6	L10	29	129.735	2,812.665
VCC	—	—	30	231.735	2,777.665
PIO3_16/DP08A	F4	G7	31	129.735	2,742.665
PIO3_17/DP08B	F3	H7	32	231.735	2,707.665
VCCIO_3	K1	F1	33	129.735	2,672.665
VCCIO_3	—	—	34	231.735	2,637.665
GND	—	G1	35	129.735	2,602.665
GND	—	—	36	231.735	2,567.665
PIO3_18/DP09A	G3	K8	37	129.735	2,532.665
PIO3_19/DP09B	G4	K7	38	231.735	2,497.665

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_20/DP10A	—	H8	39	129.735	2,462.665
PIO3_21/DP10B	—	J8	40	231.735	2,427.665
PIO3_22/DP11A	G1	T1	41	129.735	2,392.665
PIO3_23/DP11B	G2	U1	42	231.735	2,357.665
VCCIO_3	K1	N10	43	129.735	2,322.665
VCCIO_3	—	—	44	231.735	2,287.665
VREF	N/A	M1	45	129.735	2,252.665
VREF	N/A	—	46	231.735	2,217.665
GND	J5	N1	47	129.735	2,182.665
GND	—	—	48	231.735	2,147.665
VCCIO_3	J6	P1	49	129.735	2,112.665
VCCIO_3	—	—	50	231.735	2,077.665
GND	H6	R1	51	129.735	2,042.665
GND	—	—	52	231.735	2,007.665
PIO3_24/DP12A	H4	L3	53	129.735	1,972.665
GBIN7/PIO3_25/DP12B	H3	L5	54	231.735	1,937.665
GND	H7	V1	55	129.735	1,902.665
GBIN6/PIO3_26/DP13A	H1	M5	56	231.735	1,867.665
PIO3_27/DP13B	H2	M3	57	129.735	1,832.665
PIO3_28/DP14A	—	N7	58	231.735	1,798.665
PIO3_29/DP14B	—	N5	59	129.735	1,762.665
PIO3_30/DP15A	J1	N3	60	231.735	1,727.665
PIO3_31/DP15B	J2	P3	61	129.735	1,692.665
GND	J5	M11	62	231.735	1,657.665
GND	—	—	63	129.735	1,622.665
PIO3_32/DP16A	H5	W1	64	231.735	1,587.665
PIO3_33/DP16B	G5	Y1	65	129.735	1,552.665
VCCIO_3	J6	R3	66	231.735	1,517.665
VCCIO_3	—	—	67	129.735	1,482.665
GND	J5	T3	68	231.735	1,447.665
GND	—	—	69	129.735	1,412.665
PIO3_34/DP17A	K2	AA1	70	231.735	1,377.665
PIO3_35/DP17B	J3	AB1	71	129.735	1,342.665
PIO3_36/DP18A	—	L7	72	231.735	1,307.665
PIO3_37/DP18B	—	L8	73	129.735	1,272.665
PIO3_38/DP19A	—	M7	74	231.735	1,237.665
PIO3_39/DP19B	—	M8	75	129.735	1,202.665
PIO3_40/DP20A	L1	P7	76	231.735	1,167.665
PIO3_41/DP20B	L2	P8	77	129.735	1,132.665
VCC	J4	N8	78	231.735	1,097.665
VCC	—	—	79	129.735	1,062.665
PIO3_42/DP21A	K4	R5	80	231.735	1,027.665
PIO3_43/DP21B	K3	T5	81	129.735	992.665
VCCIO_3	K1	P5	82	231.735	957.665
VCCIO_3	—	—	83	129.735	912.665
GND	L3	R7	84	231.735	867.665
GND	—	—	85	129.735	822.67

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO3_44/DP22A	M1	U3	86	231.735	777.67
PIO3_45/DP22B	M2	V3	87	129.735	732.67
PIO3_46/DP23A	N1	U5	88	231.735	687.67
PIO3_47/DP23B	N2	V5	89	129.735	642.67
PIO3_48/DP24A	—	W3	90	231.735	597.67
PIO3_49/DP24B	—	Y3	91	129.735	552.665
PIO2_00	P1	AB2	92	510.0	139.5
PIO2_01	M3	R8	93	560.0	37.5
PIO2_02	P2	Y4	94	610.0	139.5
GND	P6	AB5	95	660.0	37.5
GND	—	—	96	710.0	139.5
PIO2_03	M4	T7	97	760.0	37.5
PIO2_04	N3	AB3	98	810.0	139.5
PIO2_05	—	R9	99	859.3	37.5
PIO2_06	—	Y5	100	910.0	139.5
PIO2_07	L4	T8	101	960.0	37.5
PIO2_08	P3	V6	102	1,012.5	139.5
VCCIO_2	M5	T9	103	1,047.5	37.5
VCCIO_2	—	—	104	1,082.5	139.5
PIO2_09	P4	R10	105	1,117.5	37.5
PIO2_10	N4	AB4	106	1,152.5	139.5
GND	H8	V10	107	1,187.5	37.5
GND	—	—	108	1,222.5	139.5
PIO2_11	K5	V7	109	1,257.5	37.5
PIO2_12	P5	Y7	110	1,292.5	139.5
PIO2_13	—	V9	111	1,327.5	37.5
PIO2_14	—	Y6	112	1,362.5	139.5
PIO2_15	—	AB7	113	1,397.5	37.5
PIO2_16	—	AB6	114	1,432.5	139.5
PIO2_17	L5	Y9	115	1,467.5	37.5
PIO2_18	N5	V8	116	1,502.3	139.5
GND	P6	N12	117	1,537.3	37.5
GND	—	—	118	1,572.5	139.5
PIO2_19	N6	AB8	119	1,607.5	37.5
PIO2_20	K6	AB9	120	1,642.5	139.5
VCC	J7	Y8	121	1,677.5	37.5
VCC	—	—	122	1,712.5	139.5
PIO2_21	L6	T10	123	1,747.5	37.5
PIO2_22	M6	AB10	124	1,782.5	139.5
PIO2_23	—	AB11	125	1,817.5	37.5
PIO2_24	—	AB12	126	1,852.5	139.5
PIO2_25	L7	Y10	127	1,887.5	37.5
PIO2_26	P7	AB13	128	1,922.5	139.5
PIO2_27	K7	AB14	129	1,957.5	37.5
VCCIO_2	N10	Y11	130	1,992.5	139.5
VCCIO_2	—	—	131	2,027.5	37.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO2_28	—	Y13	132	2,062.5	139.5
GBIN5/PIO2_29	M7	V11	133	2,097.5	37.5
GBIN4/PIO2_30	N8	V12	134	2,132.5	139.5
GND	J8	Y12	135	2,167.5	37.5
GND	—	—	136	2,202.5	139.5
PIO2_31	P8	Y14	137	2,237.5	37.5
PIO2_32	—	AB15	138	2,272.5	139.5
PIO2_33	M8	V13	139	2,307.5	37.5
PIO2_34	—	AB16	140	2,342.5	139.5
PIO2_35	L8	Y15	141	2,377.5	37.5
PIO2_36	—	AB17	142	2,412.5	139.5
PIO2_37	N9	AB18	143	2,447.5	37.5
PIO2_38	—	AB19	144	2,482.5	139.5
PIO2_39	—	AB20	145	2,517.5	37.5
PIO2_40	—	AB21	146	2,552.5	139.5
PIO2_41	—	Y17	147	2,587.5	37.5
PIO2_42	—	AB22	148	2,622.5	139.5
PIO2_43	—	Y18	149	2,657.5	37.5
PIO2_44	P9	Y19	150	2,692.5	139.5
VCC	N7	N11	151	2,727.5	37.5
VCC	—	—	152	2,762.5	139.5
PIO2_45	M9	Y20	153	2,797.5	37.5
PIO2_46	K8	T11	154	2,832.5	139.5
VCCIO_2	J9	N13	155	2,867.5	37.5
VCCIO_2	—	—	156	2,902.5	139.5
PIO2_47	N11	R11	157	2,937.5	37.5
GND	J8	M12	158	2,972.5	139.5
GND	—	—	159	3,007.5	37.5
PIO2_48	N12	T12	160	3,042.5	139.5
PIO2_49	K9	R12	161	3,077.5	37.5
PIO2_50	N13	T13	162	3,112.5	139.5
PIO2_51/CBSEL0	L9	R13	163	3,147.5	37.5
PIO2_52/CBSEL1	P10	V14	164	3,182.5	139.5
CDONE	M10	T14	165	3,217.5	37.5
CRESET_B	L10	R14	166	3,260.0	139.5
PIOS_00/SPI_SO	M11	T15	167	3,320.0	37.5
PIOS_01/SPI_SI	P11	V15	168	3,370.0	139.5
GND	J8	Y16	169	3,420.0	37.5
GND	—	—	170	3,470.0	139.5
PIOS_02/SPI_SCK	P12	V16	171	3,520.0	37.5
PIOS_03/SPI_SS_B	P13	V17	172	3,570.0	139.5
VCC	—	—	173	3,620.0	37.5
VCC	—	—	174	3,670.0	139.5
SPI_VCC	L11	R15	175	3,720.0	37.5
SPI_VCC	—	—	176	3,770.0	139.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
TDI	M12	T16	177	4,470.5	634.615
TMS	P14	V18	178	4,572.5	684.615
TCK	L12	R16	179	4,470.5	734.615
TDO	N14	U18	180	4,572.5	784.615
TRST_B	M14	T18	181	4,470.5	834.615
PIO1_00	M13	R18	182	4,572.5	884.615
PIO1_01	K11	P16	183	4,470.5	934.615
PIO1_02	L13	P15	184	4,572.5	984.615
PIO1_03	L14	P18	185	4,470.5	1,034.615
GND	G9	N18	186	4,572.5	1,084.615
GND	—	—	187	4,470.5	1,134.615
PIO1_04	J11	N16	188	4,572.5	1,184.615
PIO1_05	K12	N15	189	4,470.5	1,234.62
VCCIO_1	F9	M18	190	4,572.5	1,287.115
VCCIO_1	—	—	191	4,470.5	1,322.115
PIO1_06	J12	M15	192	4,572.5	1,357.115
PIO1_07	K14	M16	193	4,470.5	1,392.115
PIO1_08	—	T20	194	4,572.5	1,427.115
PIO1_09	—	W20	195	4,470.5	1,462.115
PIO1_10	—	V20	196	4,572.5	1,497.115
VCC	H9	M13	197	4,470.5	1,532.115
VCC	—	—	198	4,572.5	1,567.115
PIO1_11	—	R20	199	4,470.5	1,602.115
PIO1_12	—	Y22	200	4,572.5	1,637.115
PIO1_13	—	AA22	201	4,470.5	1,672.115
PIO1_14	—	U20	202	4,572.5	1,707.115
PIO1_15	J13	W22	203	4,470.5	1,742.115
PIO1_16	H11	P20	204	4,572.5	1,777.115
PIO1_17	J10	V22	205	4,470.5	1,812.115
PIO1_18	H12	U22	206	4,572.5	1,847.115
GND	K10	N20	207	4,470.5	1,882.115
GND	—	—	208	4,572.5	1,917.110
PIO1_19	H13	T22	209	4,470.5	1,952.115
PIO1_20	—	M20	210	4,572.5	1,987.115
PIO1_21	H10	R22	211	4,470.5	2,022.115
PIO1_22	—	P22	212	4,572.5	2,057.115
VCCIO_1	F9	J20	213	4,470.5	2,092.115
VCCIO_1	—	—	214	4,572.5	2,127.115
PIO1_23	G10	M22	215	4,470.5	2,162.115
PIO1_24	G11	N22	216	4,572.5	2,197.115
PIO1_25	—	K22	217	4,470.5	2,232.115
PIO1_26	—	L22	218	4,572.5	2,267.115
GBIN3/PIO1_27	G12	K18	219	4,470.5	2,302.11
GBIN2/PIO1_28	F10	L18	220	4,572.5	2,337.115
PIO1_29	—	J22	221	4,470.5	2,372.115

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO1_30	—	K20	222	4,572.5	2,407.115
PIO1_31	G14	F22	223	4,470.5	2,442.115
PIO1_32	—	G22	224	4,572.5	2,477.115
PIO1_33	F11	E22	225	4,470.5	2,512.115
PIO1_34	F12	L16	226	4,572.5	2,547.115
PIO1_35	G13	D22	227	4,470.5	2,582.115
GND	G8	L12	228	4,572.5	2,617.115
GND	—	—	229	4,470.5	2,652.115
PIO1_36	E10	K16	230	4,572.5	2,687.12
VCCIO_1	H14	H22	231	4,470.5	2,722.12
VCCIO_1	—	—	232	4,572.5	2,757.12
PIO1_37	F14	H20	233	4,470.5	2,792.12
PIO1_38	E11	J18	234	4,572.5	2,827.12
PIO1_39	D12	C22	235	4,470.5	2,862.12
PIO1_40	F13	J16	236	4,572.5	2,897.12
PIO1_41	E13	B22	237	4,470.5	2,932.12
PIO1_42	E12	H18	238	4,572.5	2,967.12
PIO1_43	E14	G20	239	4,470.5	3,002.12
PIO1_44	—	L15	240	4,572.5	3,037.12
PIO1_45	—	A22	241	4,470.5	3,072.12
PIO1_46	—	H16	242	4,572.5	3,107.12
VCC	K13	L20	243	4,470.5	3,142.12
VCC	—	—	244	4,572.5	3,177.12
PIO1_47	D14	F20	245	4,470.5	3,229.615
PIO1_48	D11	K15	246	4,572.5	3,279.615
VCCIO_1	H14	K13	247	4,470.5	3,329.615
VCCIO_1	—	—	248	4,572.5	3,379.615
PIO1_49	C14	E20	249	4,470.5	3,429.62
PIO1_50	D13	J15	250	4,572.5	3,479.615
GND	J14	L13	251	4,470.5	3,529.615
GND	—	—	252	4,572.5	3,579.615
PIO1_51	B14	D20	253	4,470.5	3,629.615
PIO1_52	C13	G18	254	4,572.5	3,679.595
PIO1_53	B13	C20	255	4,470.5	3,729.595
PIO1_54	C12	F18	256	4,572.5	3,779.595
VPP_2V5	A14	E18	257	4,470.5	3,879.575
VPP_FAST	A13	E17	258	3,866.975	4,054.5
VCC	F8	K12	259	3,766.98	4,156.5
VCC	—	—	260	3,716.98	4,054.5
PIO0_00	—	G16	261	3,666.98	4,156.5
PIO0_01	—	C19	262	3,616.98	4,054.5
PIO0_02	C11	H15	263	3,566.98	4,156.5
PIO0_03	—	C18	264	3,516.98	4,054.5
PIO0_04	A12	H14	265	3,466.98	4,156.5
VCCIO_0	F6	A21	266	3,416.98	4,054.5
PIO0_05	B11	C17	267	3,366.98	4,156.5
PIO0_06	D10	E16	268	3,316.98	4,054.5
PIO0_07	A11	G15	269	3,266.98	4,156.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
GND	F7	E13	270	3,216.98	4,054.5
GND	—	—	271	3,166.98	4,156.5
PIO0_08	D9	E15	272	3,116.98	4,054.5
PIO0_09	C10	G14	273	3,064.48	4,156.5
PIO0_10	A10	A20	274	3,029.48	4,054.5
PIO0_11	B10	H13	275	2,994.48	4,156.5
PIO0_12	—	A19	276	2,959.48	4,054.5
PIO0_13	E9	G13	277	2,924.48	4,156.5
PIO0_14	—	C16	278	2,889.48	4,054.5
PIO0_15	—	E14	279	2,854.48	4,156.5
VCCIO_0	F6	E12	280	2,819.48	4,054.5
VCCIO_0	—	—	281	2,784.48	4,156.5
PIO0_16	—	A18	282	2,749.48	4,054.5
PIO0_17	—	A17	283	2,714.48	4,156.5
PIO0_18	C9	C15	284	2,679.48	4,054.5
PIO0_19	—	A16	285	2,644.48	4,156.5
PIO0_20	B9	C14	286	2,609.48	4,054.5
PIO0_21	—	H12	287	2,574.48	4,156.5
PIO0_22	D8	A15	288	2,539.48	4,054.5
PIO0_23	C8	H11	289	2,504.48	4,156.5
PIO0_24	E8	C13	290	2,469.48	4,054.5
PIO0_25	—	A14	291	2,434.48	4,156.5
GND	B12	C12	292	2,399.48	4,054.5
GND	—	—	293	2,364.48	4,156.5
PIO0_26	B8	A13	294	2,329.48	4,054.5
PIO0_27	D7	A12	295	2,294.48	4,156.5
PIO0_28	—	C11	296	2,259.48	4,054.5
GBIN1/PIO0_29	E7	E11	297	2,224.48	4,156.5
GBIN0/PIO0_30	A7	E10	298	2,189.48	4,054.5
PIO0_31	—	G12	299	2,154.48	4,156.5
VCCIO_0	A8	A8	300	2,119.48	4,054.5
VCCIO_0	—	—	301	2,084.48	4,156.5
PIO0_32	C7	A11	302	2,049.48	4,054.5
PIO0_33	—	G11	303	2,014.48	4,156.5
PIO0_34	E6	A10	304	1,979.48	4,054.5
PIO0_35	—	C10	305	1,944.48	4,156.5
VCC	B7	C8	306	1,909.48	4,054.5
VCC	—	—	307	1,874.48	4,156.5
PIO0_36	—	A9	308	1,839.48	4,054.5
PIO0_37	A6	A7	309	1,804.48	4,156.5
PIO0_38	B6	C9	310	1,769.48	4,054.5
PIO0_39	A5	A6	311	1,734.48	4,156.5
GND	G7	K11	312	1,699.48	4,054.5
GND	—	—	313	1,664.48	4,156.5
PIO0_40	D6	E9	314	1,629.48	4,054.5
PIO0_41	C6	G10	315	1,594.48	4,156.5

iCE65L08 Pad Name	Available Packages		DiePlus		
	CB196	CB284	Pad	X (µm)	Y (µm)
PIO0_42	C5	A5	316	1,559.48	4,054.5
PIO0_43	B5	G9	317	1,524.48	4,156.5
PIO0_44	A4	A3	318	1,489.48	4,054.5
PIO0_45	—	A4	319	1,454.48	4,156.5
PIO0_46	—	A2	320	1,419.48	4,054.5
PIO0_47	—	C7	321	1,384.48	4,156.5
PIO0_48	—	C6	322	1,331.98	4,054.5
VCCIO_0	A8	K10	323	1,281.98	4,156.5
VCCIO_0	—	—	324	1,231.98	4,054.5
PIO0_49	—	E8	325	1,181.98	4,156.5
PIO0_50	B4	A1	326	1,131.98	4,054.5
PIO0_51	C4	E7	327	1,081.98	4,156.5
PIO0_52	A3	C5	328	1,031.98	4,054.5
PIO0_53	B3	E6	329	981.98	4,156.5
PIO0_54	D5	C3	330	931.98	4,054.5
GND	A9	L11	331	881.98	4,156.5
GND	—	—	332	831.98	4,054.5
PIO0_55	B2	G8	333	781.98	4,156.5
PIO0_56	A2	C4	334	731.98	4,054.5
PIO0_57	A1	H10	335	681.98	4,156.5
PIO0_58	—	E5	336	631.98	4,054.5
PIO0_59	—	H9	337	581.98	4,156.5

Electrical Characteristics

All parameter limits are specified under worst-case supply voltage, temperature, and processing conditions.

Absolute Maximum Ratings

Stresses beyond those listed under Table 47 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 47: Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
VCC	Core supply Voltage	–0.5	1.42	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply			V
VPP_FAST	Optional fast NVCM programming supply			V
VCCIO_0 **VCCIO_1** **VCCIO_2** **SPI_VCC**	I/O bank supply voltage (I/O Banks 0, 1, and 2 plus SPI interface)	–0.5	4.00	V
VCCIO_3	I/O Bank 3 supply voltage	–0.5	iCE65L01: 4.00 iCE65L04/08: 3.6	V
VIN_0 **VIN_1** **VIN_2** **VIN_SPI**	Voltage applied to PIO pin within a specific I/O bank (I/O Banks 0, 1, and 2 plus SPI interface)	–1.0	5.5	V
VIN_3 **VIN_VREF**	Voltage applied to PIO pin within I/O Bank 3	–0.5	iCE65L01: 4.00 iCE65L04/08: 3.6	V
IOUT	DC output current per pin	—	20	mA
T_J	Junction temperature	–55	125	°C
T_{STG}	Storage temperature, no bias	–65	150	°C

Recommended Operating Conditions

Table 48: **Recommended Operating Conditions**

Symbol	Description		Minimum	Nominal	Maximum	Units
VCC	Core supply voltage	–L: Ultra-Low Power mode	0.95	1.00	1.05	V
		–L: Low Power –T: High Performance	1.14	1.20	1.26	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply	Release from Power-on Reset	1.30	—	3.47	V
		Configure from NVCM	2.30	—	3.47	V
		NVCM programming	2.30	—	3.00	V
VPP_FAST	Optional fast NVCM programming supply		Leave unconnected in application			
SPI_VCC	SPI interface supply voltage		1.71	—	3.47	V
VCCIO_0 VCCIO_1 VCCIO_2 VCCIO_3 SPI_VCC	I/O standards, all banks*	**LVCMOS33**	3.14	3.30	3.47	V
		Non-standard voltage: in between 2.5V and 3.3V use LVCMOS25 in iCEcube2	Nominal -5%	2.5< Nominal <3.3	Nominal +5%	V
		LVCMOS25, LVDS	2.38	2.50	2.63	V
		LVCMOS18, SubLVDS	1.71	1.80	1.89	V
		LVCMOS15	1.43	1.50	1.58	V
VCCIO_3	I/O standards only available in iCE65L04/08 I/O Bank 3*	**SSTL2**	2.38	2.50	2.63	V
		SSTL18	1.71	1.80	1.89	V
		MDDR	1.71	1.80	1.89	V
T_A	Ambient temperature	Commercial (C)	0	—	70	°C
		Industrial (I)	–40	—	85	°C
T_{PROG}	NVCM programming temperature		10	25	30	°C

NOTE:

VPP_FAST is only used for fast production programming. Leave floating or unconnected in application. When the iCE65 device is active, VPP_2V5 must be connected to a valid voltage.

I/O Characteristics

Table 49: PIO Pin Electrical Characteristics

Symbol	Description		Conditions	Minimum	Nominal	Maximum	Units
I_I	Input pin leakage current	I/O Bank 0, 1, 2	V_{IN} = $VCCIO_{max}$ to 0 V			±10	µA
		I/O Bank 3	V_{IN} = $VCCIO_{max}$				
I_{OZ}	Three-state I/O pin (Hi-Z) leakage current		V_O = $VCCIO_{max}$ to 0 V			±10	µA
C_{PIO}	PIO pin input capacitance				6		pF
C_{GBIN}	GBIN global buffer pin input capacitance				6		pF
R_{PULLUP}	Internal PIO pull-up resistance during configuration		VCCIO = 3.3V		40		kΩ
			VCCIO = 2.5V		50		kΩ
			VCCIO = 1.8V		90		kΩ
			VCCIO = 1.5V				kΩ
			VCCIO = 1.2V				kΩ
V_{HYST}	Input hysteresis		VCCIO = 1.5V to 3.3V		50		mV

NOTE: All characteristics are characterized and may or may not be tested on each pin on each device.

Single-ended I/O Characteristics

Table 50: I/O Characteristics (I/O Banks 0, 1, 2 and SPI only) (I/O Bank 3 iCE65L01 only)

I/O Standard	Nominal I/O Bank Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current at Voltage (mA)	
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{OL}	I_{OH}
LVCMOS33	3.3V	0.80	2.00	0.4	2.40	8	8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	6	6
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	1.40	4	4
LVCMOS15	1.5V	Not supported Use I/O Bank 3		0.4	1.20	2	2

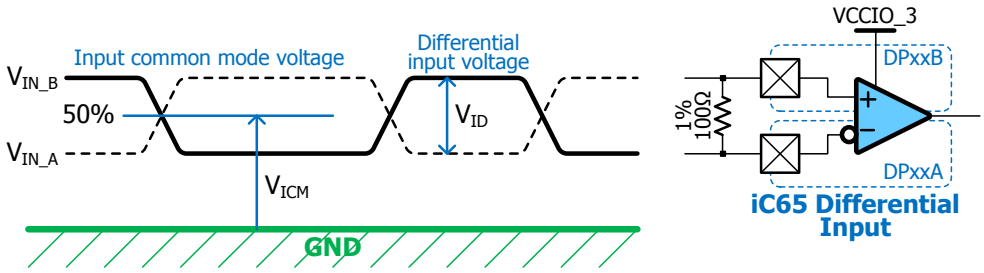
Table 51: I/O Characteristics (I/O Bank 3 and iCE65L04/08 only)

I/O Standard	Supply Voltage	Input Voltage (V)		Output Voltage (V)		I/O Attribute Name	mA at Voltage
		Max. V_{IL}	Min. V_{IH}	Max. V_{OL}	Min. V_{OH}		I_{OL}, I_{OH}
LVCMOS33	3.3V	0.80	2.20	0.4	2.40	SL_LVCMOS33_8	±8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	SB_LVCMOS25_16	±16
						SB_LVCMOS25_12	±12
						SB_LVCMOS25_8 *	±8
						SB_LVCMOS25_4	±4
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_LVCMOS18_10	±10
						SB_LVCMOS18_8	±8
						SB_LVCMOS18_4 *	±4
						SB_LVCMOS18_2	±2
LVCMOS15	1.5V	35% VCCIO	65% VCCIO	25% VCCIO	75% VCCIO	SB_LVCMOS15_4	±4
						SB_LVCMOS15_2 *	±2
MDDR	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_MDDR10	±10
						SB_MDDR8	±8
						SB_MDDR4 *	±4
						SB_MDDR2	±2
SSTL2 (Class 2)	2.5V	VREF–0.180	VREF+0.180	0.35	VTT+0.430	SB_SSTL2_CLASS_2	±16.2
SSTL2 (Class 1)				0.54		SB_SSTL2_CLASS_1	±8.1
SSTL18 (Full)	1.8V	VREF–0.125	VREF+0.125	0.28	VTT+0.280	SB_SSTL18_FULL	±13.4
SSTL18 (Half)				VTT–0.475	VTT+0.475	SB_SSTL18_HALF	±6.7

NOTES:
SSTL2 and SSTL18 I/O standards require the VREF input pin, which is only available on the CB284 package and die-based products.

Differential Inputs

Figure 50: Differential Input Specifications



Input common mode voltage: $$V_{ICM} = \frac{VCCIO_3}{2} \pm \Delta V_{ICM}$$

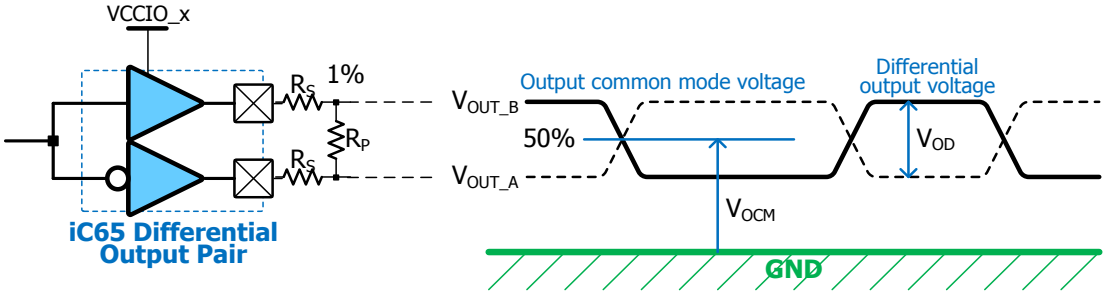
Differential input voltage: $$V_{ID} = |V_{IN_B} - V_{IN_A}|$$

Table 52: **Recommended Operating Conditions for Differential Inputs**

I/O Standard	VCCIO_3 (V)			V_{ID} (mV)			V_{ICM} (V)		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	250	350	450	$\frac{VCCIO_3}{2} - 0.30$	$\frac{VCCIO_3}{2}$	$\frac{VCCIO_3}{2} + 0.30$
SubLVDS	1.71	1.80	1.89	100	150	200	$\frac{VCCIO_3}{2} - 0.25$	$\frac{VCCIO_3}{2}$	$\frac{VCCIO_3}{2} + 0.25$

Differential Outputs

Figure 51: Differential Output Specifications



Output common mode voltage: $$V_{OCM} = \frac{VCCIO_x}{2} \pm \Delta V_{OCM}$$

Differential output voltage: $$V_{OD} = |V_{OUT_B} - V_{OUT_A}|$$

Table 53: **Recommended Operating Conditions for Differential Outputs**

I/O Standard	VCCIO_x (V)			Ω		V_{OD} (mV)			V_{OCM} (V)		
	Min	**Nom**	**Max**	**R_S**	**R_P**	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
LVDS	2.38	2.50	2.63	150	140	300	350	400	$\frac{VCCIO}{2} - 0.15$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.15$
SubLVDS	1.71	1.80	1.89	270	120	100	150	200	$\frac{VCCIO}{2} - 0.10$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.10$

I/O Banks 0, 1, 2 and SPI Bank Characteristic Curves

Figure 52: **Typical LVCMOS Output Low Characteristics (I/O Banks 0, 1, 2, and SPI)**

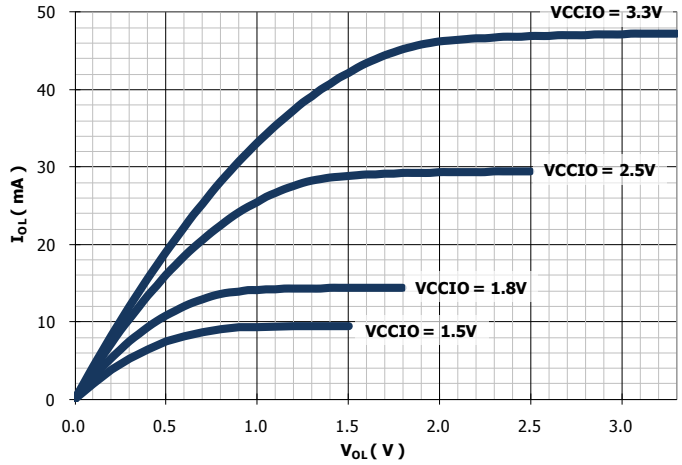


Figure 53: **Typical LVCMOS Output High Characteristics (I/O Banks 0, 1, 2, and SPI)**

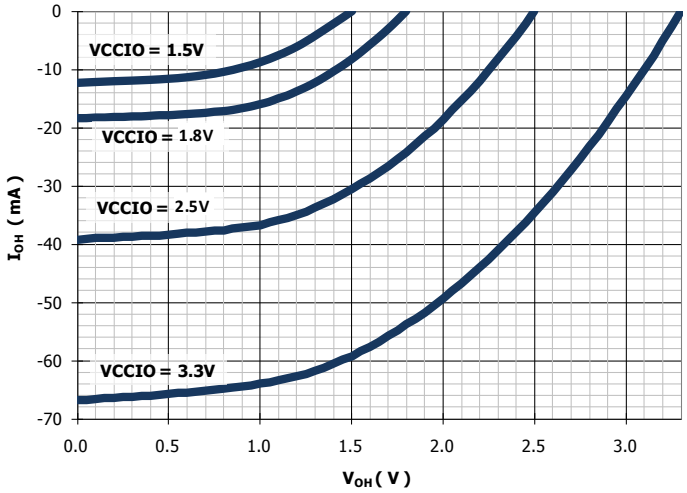
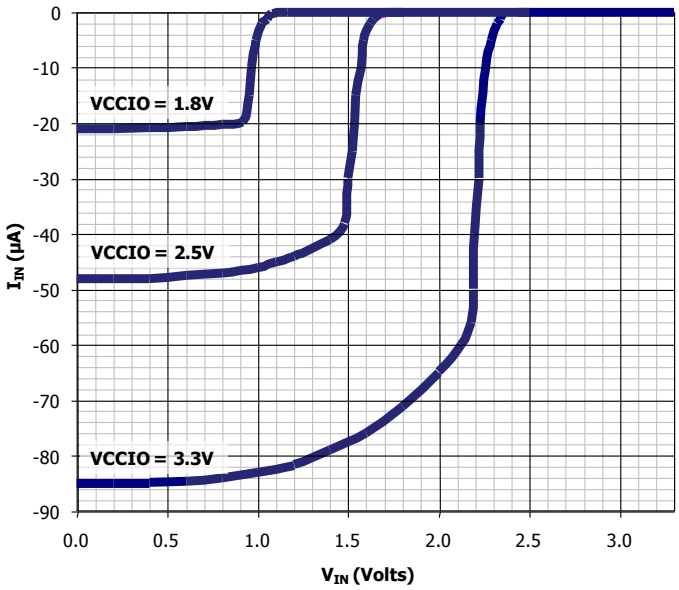


Figure 54: **Input with Internal Pull-Up Resistor Enabled (I/O Banks 0, 1, 2, and SPI)**



AC Timing Guidelines

The following examples provide some guidelines of device performance. The actual performance depends on the specific application and how it is physically implemented in the iCE65 FPGA using the Lattice iCEcube software. The following guidelines assume typical conditions (VCC = 1.0 V or 1.2 V as specified, temperature = 25 °C). Apply derating factors using the iCEcube timing analyzer to adjust to other operating regimes.

Programmable Logic Block (PLB) Timing

Table 54 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 55 and Figure 56.

Figure 55 PLB Sequential Timing Circuit

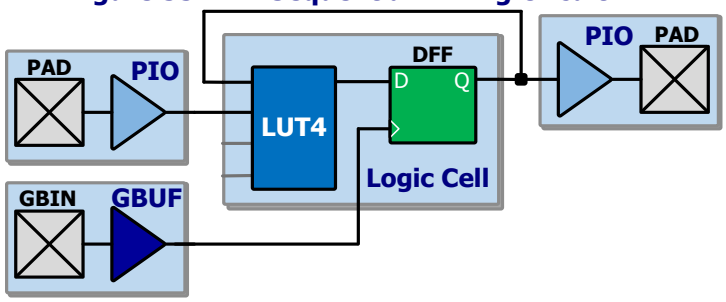


Figure 56 **PLB Combinational Timing Circuit**

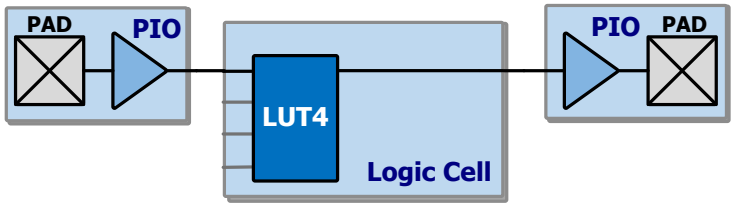


Table 54: **Typical Programmable Logic Block (PLB) Timing**

Symbol	From	To	Description	L01 –T 1.2 V Typ.	L04, L08 –L 1.0 V Typ.	L04, L08 –L 1.2 V Typ.	L04, L08 –T 1.2 V Typ.	Units
		Sequential Logic Paths						
F_{TOGGLE}	GBIN input	GBIN input	Flip-flop toggle frequency. DFF flip-flop output fed back to LUT4 input with 4-input XOR, clocked on same clock edge.	256	224	256	256	MHz
t_{CKO}	DFF clock input	PIO output	Logic cell flip-flop (DFF) clock-to-output time, measured from the DFF CLK input to PIO output, including interconnect delay.	5.4	16.5	8.7	7.1	ns
t_{GBCKLC}	GBIN input	DFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the logic cell DFF flip-flop.	2.2	7.3	3.8	2.7	ns
t_{SULI}	PIO input	GBIN input	Minimum setup time on PIO input, through LUT4, to DFF flip-flop D-input before active clock edge on the GBIN input, including interconnect delay.	1.0	4.0	2.1	1.2	ns
t_{HDLI}	GBIN input	PIO input	Minimum hold time on PIO input, through LUT4, to DFF flip-flop D-input after active clock edge on the GBIN input, including interconnect delay.	0	0	0	0	ns
		Combinational Logic Paths						
t_{LUT4IN}	PIO input	LUT4 input	Asynchronous delay from PIO input pad to adjacent PLB interconnect.	2.6	9.8	5.2	3.3	ns
t_{ILO}	LUT4 input	LUT4 output	Logic cell LUT4 combinational logic propagation delay, regardless of logic complexity from input to output.	0.6	1.9	1.0	0.6	ns
t_{LUT4IN}	LUT4 output	PIO output	Asynchronous delay from adjacent PLB interconnect to PIO output pad.	4.9	16.0	8.4	6.6	ns

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 57: **Programmable I/O (PIO) Pad-to-Pad Timing Circuit**

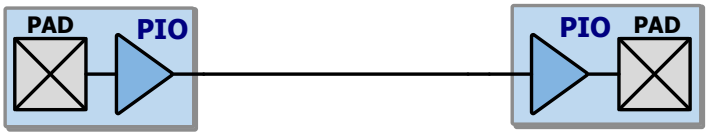


Figure 58: **Programmable I/O (PIO) Sequential Timing Circuit**

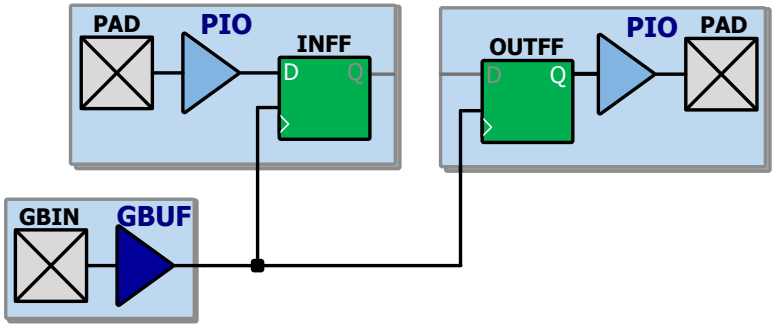


Table 55: **Typical Programmable Input/Output (PIO) Timing (LVCMOS25)**

Symbol	From	To	Device: iCE65	L01	L04, L08			Units
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
			Description	Typ.	Typ.	Typ.	Typ.	
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns

RAM4K Block

Table 56 provides timing information for the logic in a RAM4K block, which includes the paths shown in Figure 59.

Figure 59: RAM4K Timing Circuit

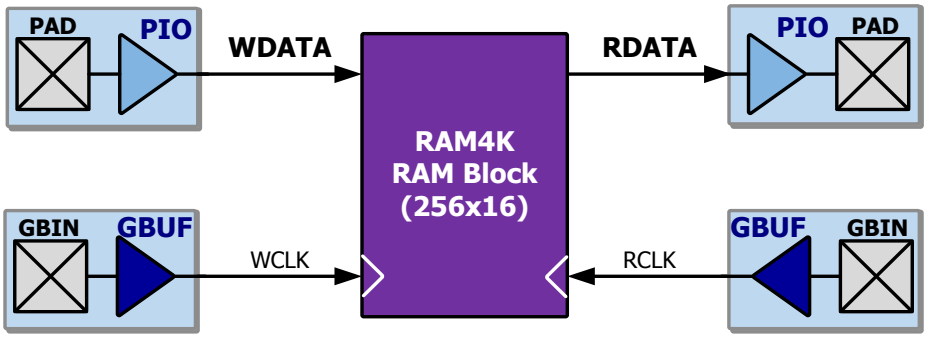


Table 56: Typical RAM4K Block Timing

Symbol	From	To	Device: iCE65 / Description	L01	L04, L08			Units
			Power/Speed Grade	–T	–L	–L	–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
			Description	Typ.	Typ.	Typ.	Typ.	
Write Setup/Hold Time								
t_{SUWD}	PIO input	GBIN input	Minimum write data setup time on PIO inputs before active clock edge on GBIN input, include interconnect delay.	0.6	3.1	1.7	0.8	ns
t_{HDWD}	GBIN input	PIO input	Minimum write data hold time on PIO inputs after active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
Read Clock-Output-Time								
t_{CKORD}	RCLK clock input	PIO output	Clock-to-output delay from RCLK input pin, through RAM4K RDATA output flip-flop to PIO output pad, including interconnect delay.	5.6	17.1	9.1	7.3	ns
t_{GBCKRM}	GBIN input	RCLK clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to the RCLK clock input.	2.1	7.3	3.8	2.6	ns
Write and Read Clock Characteristics								
t_{RMWCKH}	WCLK RCLK	WCLK RCLK	Write clock High time	0.54	1.14	0.54	0.54	ns
t_{RMWCKL}			Write clock Low time	0.63	1.32	0.63	0.63	ns
t_{RMWCYC}			Write clock cycle time	1.27	2.64	1.27	1.27	ns
F_{WMAX}			Sustained write clock frequency	256	256	256	256	MHz

Internal Configuration Oscillator Frequency

Table 57 shows the operating frequency for the iCE65's internal configuration oscillator.

Table 57: Internal Oscillator Frequency

Symbol	Oscillator Mode	Frequency (MHz)		Description
		Min.	Max.	
f_{OSCD}	**Default**	4.0	6.8	Default oscillator frequency. Slow enough to safely operate with any SPI serial PROM.
f_{OSCL}	**Low Frequency**	14	21	Supported by most SPI serial Flash PROMs
f_{OSCH}	**High Frequency**	21	31	Supported by some high-speed SPI serial Flash PROMs
	Off	0	0	Oscillator turned off by default after configuration to save power.

Configuration Timing

Table 58 shows the maximum time to configure an iCE65 device, by oscillator mode. The calculations use the slowest frequency for a given oscillator mode from Table 57 and the maximum configuration bitstream size from Table 1 which includes full RAM4K block initialization. The configuration bitstream selects the desired oscillator mode based on the performance of the configuration data source.

***Table 58:* Maximum SPI Master or NVCM Configuration Timing by Oscillator Mode**

Symbol	Description	Device	Default	Low Freq.	High Freq.	Units
$t_{CONFIGL}$	Time from when minimum Power-on Reset (POR) threshold is reached until user application starts.	**iCE65L01**	53	25	11	ms
		iCE65L04	115	55	25	ms
		iCE65L08	230	110	50	ms

Table 59 provides timing for the CRESET_B and CDONE pins.

Table 59: General Configuration Timing

Symbol	From	To	Description		All Grades		Units
					Min.	Max.	
t_{CRESET_B}	CREST_B	CREST_B	Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge		200	—	ns
t_{DONE_IO}	CDONE High	PIO pins active	Number of configuration clock cycles after CDONE goes High before the PIO pins are activated.		—	49	Clock cycles
			SPI Peripheral Mode (Clock = SPI_SCK, cycles measured rising-edge to rising-edge)		Depends on SPI_SCK frequency		
			NVCM or SPI Master Mode by internal oscillator frequency setting (Clock = internal oscillator)	Default	7.20	12.25	µs
				Low	2.34	3.50	µs
				High	1.59	2.33	µs

Table 60 provides various timing specifications for the SPI peripheral mode interface.

Table 60: SPI Peripheral Mode Timing

Symbol	From	To	Description		All Grades Min.	All Grades Max.	Units
t_{CR_SCK}	CRESET_B	SPI_SCK	Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE65 FPGA is clearing its internal configuration memory	iC65L01	800	—	µs
				iC65L04	800		
				iC65L08	1200		
$t_{SUSPISI}$	SPI_SI	SPI_SCK	Setup time on SPI_SI before the rising SPI_SCK clock edge		12	—	ns
$t_{HDSPISI}$	SPI_SCK	SPI_SI	Hold time on SPI_SI after the rising SPI_SCK clock edge		12	—	ns
$t_{SPISCKH}$	SPI_SCK	SPI_SCK	SPI_SCK clock High time		20	—	ns
$t_{SPISCKL}$	SPI_SCK	SPI_SCK	SPI_SCK clock Low time		20	—	ns
$t_{SPISCKCYC}$	SPI_SCK	SPI_SCK	SPI_SCK clock period*		40	1,000	ns
F_{SPI_SCK}	SPI_SCK	SPI_SCK	Sustained SPI_SCK clock frequency*		1	25	MHz

* = Applies after sending the synchronization pattern.

Power Consumption Characteristics

Core Power

Table 61 shows the power consumed on the internal VCC supply rail when the device is filled with 16-bit binary counters, measured with a 32.768 kHz and at 32.0 MHz. Low power (-L) at 1.0 V operation and high-performance (-T) version at 1.2V operation is provided.

***Table 61:* VCC Power Consumption for Device Filled with 16-Bit Binary Counters**

Symbol	Description	Grade	VCC	iCE65L01 Typical	iCE65L01 Max.	iCE65L04 Typical	iCE65L04 Max.	iCE65L08 Typical	iCE65L08 Max.	Units
I_{CC0K}	f =0,	-L	1.0V	12		26		54		µA
		-T	1.2V	19		43		90		
I_{CC32K}	f ≤ 32.768 kHz	-L	1.0V	15		31		62		µA
		-T	1.2V	23		50		100		
I_{CC32M}	f = 32.0 MHz	-L	1.0V	3		7		14		mA
		-T	1.2V	4		8		17		

I/O Power

Table 62 provides the static current by I/O bank. The typical current for I/O Banks 0, 1, 2 and the SPI bank is not measurable within the accuracy of the test environment. The PIOs in I/O Bank 3 use different circuitry and dissipate a small amount of static current.

Table 62: I/O Bank Static Current (f = 0 MHz)

Symbol	Description		Typical	Max	Units
I_{CCO_0}	I/O Bank 0	Static current consumption per I/O bank. f = 0 MHz. No PIO pull-up resistors enabled. All inputs grounded. All outputs driving Low.	« 1		µA
I_{CCO_1}	I/O Bank 1		« 1		µA
I_{CCO_2}	I/O Bank 2		« 1		µA
I_{CCO_3}	I/O Bank 3		iCE65L01: « 1 iCE65L04/08: 1.2		µA
I_{CCO_SPI}	SPI Bank		« 1		µA

NOTE: The typical static current for I/O Banks 0, 1, 2, and the SPI bank is less than the accuracy of the device tester.

Power Estimator

To estimate the power consumption for a specific application, please download and use the iCE65 Power Estimator Spreadsheet our use the power estimator built into the iCEcube software.

- iCE65 Power Estimator Spreadsheet

Notes

Revision History

Version	Date	Description
2.42	30-MAR-2012	Changed company name. Updated Table 1
2.41	1-AUG-2011	Added VQ100 marking for NVCM programming.
2.4	13-MAY-2011	Added L01 CB121 package Figure 39. Added note "else VCCIO_1 draws current" to JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, Table 32. Input pin leakage current Table 49 split by bank. QN84 package drawing, Figure 35, added note "underside metal is at ground potential", increased thermal resistance. Added Marking Format and Thermal resistance to CB81 Packag Mechanical Drawing Figure 33. Added coplanarity specification to VQ100 Package Mechanical Drawing Figure 37
2.3	18-OCT-2010	Added L01 CB81 and L08 CB132 packages.
2.2.3	12-OCT-2010	Changed Figure 29: Application Processor Waveforms for SPI Peripheral Mode Configuration Process and Table 60 from 300 µs CRESET_B to 800 µs for iCE65L01/04 and 1200 µs for iCE65L08.
2.2.2	8-OCT-2010	Added iCE65L04 marking specification to Figure 47 CB196 Package Mechanical Drawing.
2.2.1	5-OCT-2010	Changed FSPI_SCK from 0.125 MHz to 1 MHz in SPI Peripheral Configuration Interface and in Table 60.
2.2	6-AUG-2010	Programmable Interconnect section removed.
2.1.1	26-MAY-2010	Switched labels on Figure 53 LVCMOS Output High, VCCIO = 1.8V with VCCIO = 2.5V.
2.1	15-MAR-2010	Added JTAG unused input tie off guideline. Added marking specification and thermal characteristics to package drawings. Added production datasheet for iCE65L01 with timing update, including QN84, VQ100 and CB132. Added NVCM shut-off on SPI configuration. Added non-standard VCCIO operating conditions. Increased the minimum voltage supply specification for LVCMOS33 to 3.14V in Table 48.
2.0.1	12-NOV-2009	Recommended Operation Conditions, Table 47, replaced junction with ambient.
2.0	14-SEPT-2009	Finalized production data sheet for iCE65L04 and iCE65L08. Improved SubLVDS input specification V_{ICM} in Table 52. CS63 and CC72 packages removed and placed in iCE DiCE KGD, Known Good Die datasheet. Added "IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank". Added "Printed Circuit Board Layout Information".
1.5.1	13-JUL-2009	Updated the text in "SPI PROM Requirements" section. Minor label change in Figure 48.
1.5	20-JUN-2009	Updated timing information and added –T high-speed device option (affected Figure 2, Table 48, Table 54, Table 55, Table 56, and Table 61). Added support for 3.3V LVCMOS I/Os in I/O Bank 3 (affected Figure 7, Table 5, Table 7, Table 8, Table 47, Table 48, and Table 51). Added a section about the SPI Peripheral Configuration Interface and timing in Table 60. Added a warning that a Warm Boot operation can only jump to another configuration image that has Warm Boot disabled. Updated configuration image size and configuration time for the iCE65L02 in Table 27 and Table 58. Reduced the minimum voltage supply specification for LVCMOS33 to 2.7V in Table 48. Added information about which power rails can be disconnected without effecting the Power-On Reset (POR) circuit and clarified description of VPP_2V5 pin in Table 36. Added I/O characterization curves (Figure 52, Figure 53, and Figure 54). Minor changes to Figure 20 and Figure 21. Changed timing per Figures 54-58 and Tables 55-57.
1.4.4	25-MAR-2009	Clarified the voltage requirements for the VPP_2V5 pin in Table 36 and notes under Table 48.
1.4.3	9-MAR-2009	Removed volatile-only (-V) product offering from Figure 2. Corrected NC on ball V22, removed it for ball T22 on CB284 package (Figure 48).
1.4.2	27-FEB-2009	Updated Table 14, Table 23, Table 26, Table 30, Table 33, Table 35, and Table 46. Updated I/O Bank 3 information in Table 7 and Table 48.
1.4.1	24-FEB-2009	Based on characterization data, reduced 32KHz operating current by 40% in Table 1, Table 61, and Figure 1. Corrected that SSTL18 standards require VREF pin in Table 7. Correct ball numbers for GBIN4/GBIN5 for CS110 package.
1.4	9-FEB-2009	Added footprint and pinout information for the VQ100 Very-thin Quad Flat Package. Added footprint for iCE65L08 in CB196 (Figure 46) and added Table 43 showing the differences between the 'L04 and 'L08 in the CB196 package. Unified the package footprint nomenclature in the Package and Pinout Information section. Added note to Global Buffer Inputs that the differential clock direct input is not available on the CB132 package. Added tables showing the ball/pin number for various control functions, by package (Table 14, Table 23, Table 26, Table 30, and Table 33). Corrected the GBIN/GBUF designations. GBIN4 and GBIN5 were swapped as were GBIN6 and GBIN7. This change affected all pinout tables and footprint diagrams. Updated and corrected "Differential Global Buffer Input." Tested and corrected the clock-enable and reset connections between global buffers and various resources (Table 11, Table 12, and Table 13). Added "Automatic Global Buffer Insertion, Manual Insertion." Added "Die Cross Reference" section. Improved industrial temperature range by lowering

		minimum temperature to –40°C in Figure 2 and Table 48. Added NVCM programming temperature to Table 48.
1.3	17-DEC-2008	Added footprint and pinout information for the CS110 Wafer-Level Chip-Scale Ball Grid Array. Clarified that the CB196 footprint shown is for the iCE65L04; the iCE65L08 footprint for the CB196 package is similar but different. Added updated information on Differential Inputs and Outputs, including support for SubLVDS. Updated Electrical Characteristics and AC Timing Guidelines sections. Added support for the LVCMOS15 I/O standard. Corrected the diagram showing the direct differential clock input, Figure 16. Updated the number of I/Os by package in Table 34. Updated company address. Other minor updates throughout.
1.2	11-OCT-2008	Updated I/O Bank 3 characteristics in Table 7 and Table 51. Corrected label in Figure 14. Added JTAG configuration to Table 20. Added pull-up resistor information in Table 22 and Figure 21. Added "Internal Device Reset" section. Updated internal oscillator performance in and Table 57. Updated configuration timing in Table 58 based on new oscillator timing. Completely reorganized the "Package and Pinout Information" section. Added information on CS63 and CB196 packages. Updated information on VPP_2V5 signal in Table 36. Reduced package height for CB132 and CB284 packages to 1.0 mm. Added "Differential Inputs" and "Differential Outputs" sections.
1.1	4-SEPT-2008	Updated package roadmap (Table 2) and updated ordering codes (Figure 2). Updated Figure 7. Updated Figure 24. Added CS63 package footprint (Figure 36), pinout (Table 39) and Package.
1.0	31-MAY-2008	Initial public release.

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