THE DATASHEET OF

ICL3243CAZ-T

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ICL3221, ICL3222, ICL3223, ICL3232, ICL3241, ICL3243

One Microamp Supply-Current, +3V to +5.5V, 250kbps, RS-232 Transmitters/Receivers

The ICL3221, ICL3222, ICL3223, ICL3232, ICL3241, ICL3243 (ISL32xx) devices are 3.0V to 5.5V powered RS-232 transmitters/receivers that meet EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. Targeted applications are PDAs, notebook, and laptop computers where the low operational power consumption and even lower standby power consumption are critical. Efficient on-chip charge pumps, coupled with manual and automatic power-down functions (except for the ICL3232), reduce the standby supply current to a 1µA trickle. Small footprint packaging, and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are ensured at worst case load conditions. This family is fully compatible with 3.3V only systems, mixed 3.3V and 5.0V systems, and 5.0V only systems.

The ICL324x are 3-driver, 5-receiver devices that provide a complete serial port suitable for laptop or notebook computers. Both devices also include noninverting always-active receivers for “wake-up” capability.

The ICL3221, ICL3223 and ICL3243 feature an automatic powerdown function that powers down the on-chip power-supply and driver circuits. Power-down occurs when an attached peripheral device is shut off or the RS-232 cable is removed, conserving system power automatically without changes to the hardware or operating system. These devices power up again when a valid RS-232 voltage is applied to any receiver input.

Table 1 on page 6 summarizes the features of the devices represented by this datasheet, while Application Note AN9863 summarizes the features of each device comprising the ICL32xx 3V family.

Related Literature

For a full list of related documents, visit our website:

- ICL3221, ICL3222, ICL3223, ICL3232, ICL3241, and ICL3243 device pages

Features

- RoHS Compliant
- 15kV ESD protected (Human Body Model)
- Drop-in replacements for MAX3221, MAX3222, MAX3223, MAX3232, MAX3241, MAX3243, SP3243
- ICL3221 is a low-power, pin compatible upgrade for 5V MAX221
- ICL3222 is a low-power, pin compatible upgrade for 5V MAX242, and SP312A
- ICL3232 is a low-power upgrade for HIN232/ICL232 and pin compatible competitor devices
- RS-232 compatible with V_{CC} = 2.7V
- Meets EIA/TIA-232 and V.28/V.24 specifications at 3V
- Latch-up free
- On-chip voltage converters require only four external 0.1µF capacitors
- Manual and automatic powerdown features (except ICL3232)
- Assured mouse driveability (ICL324x only)
- Receiver hysteresis for improved noise immunity
- Assured minimum data rate: 250kbps
- Assured minimum slew rate: 6V/µs
- Wide power supply range: single +3V to +5.5V
- Low supply current in powerdown state:1µA

Applications

- Any system requiring RS-232 communication ports
  - Battery powered, hand-held, and portable equipment
  - Laptop computers, Notebooks
  - Modems, printers, and other peripherals
  - Digital cameras
  - Cellular/mobile phones

Contents

1. Overview . . . 3
1.1 Typical Operating Circuits . . . 3
1.2 Ordering Information . . . 4
1.3 Pin Configurations . . . 6
1.4 Pin Descriptions . . . 8

2. Specifications . . . 9
2.1 Absolute Maximum Ratings . . . 9
2.2 Thermal Information . . . 9
2.3 Recommended Operating Conditions . . . 10
2.4 Electrical Specifications . . . 10

3. Typical Performance Curves . . . 12

4. Application Information . . . 13
4.1 Charge Pump . . . 13
4.1.1 Charge Pump Absolute Maximum Ratings . . . 13
4.2 Transmitters . . . 14
4.3 Receivers . . . 14
4.4 Low Power Operation . . . 15
4.5 Powerdown Functionality (Except ICL3232) . . . 15
4.5.1 Software Controlled (Manual) Powerdown . . . 15
4.5.2 $\overline{\text{INVALID}}$ Output . . . 16
4.5.3 Automatic Powerdown (ICL3221/23/43 Only) . . . 18
4.6 Receiver ENABLE Control (ICL3221/22/23/41 Only) . . . 19
4.7 Capacitor Selection . . . 19
4.8 Power Supply Decoupling . . . 19
4.9 Operation Down to 2.7V . . . 19
4.10 Transmitter Outputs when Exiting Powerdown . . . 20
4.11 Mouse Driveability . . . 20
4.12 High Data Rates . . . 20
4.13 Interconnection with 3V and 5V Logic . . . 21
4.14 Pin Compatible Replacements For 5V Devices . . . 22

5. Die Characteristics . . . 23

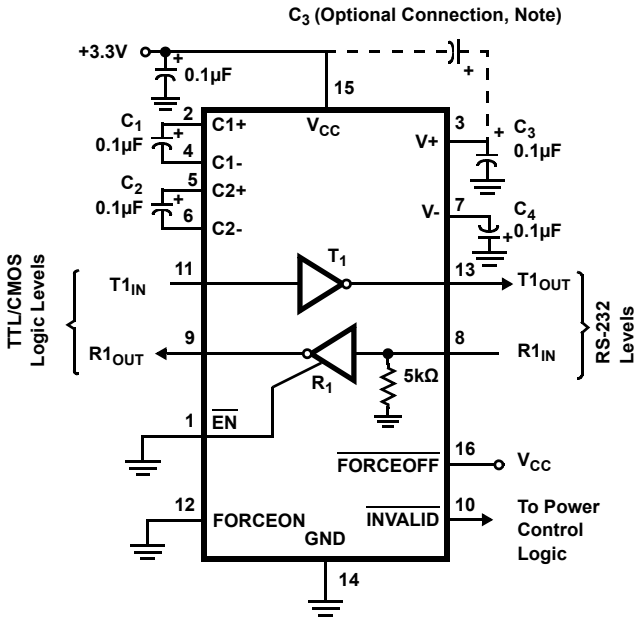
6. Revision History . . . 24

7. Package Outline Drawings . . . 25

1. Overview

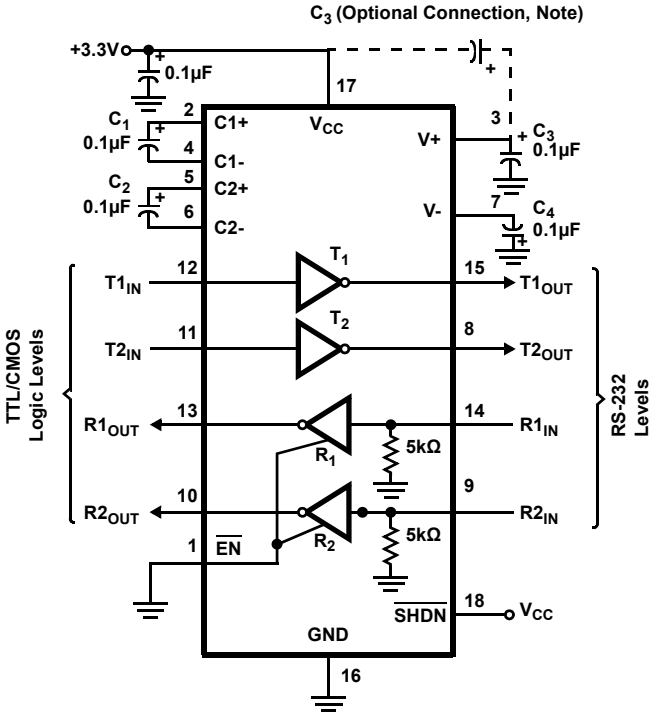
1.1 Typical Operating Circuits

ICL3221



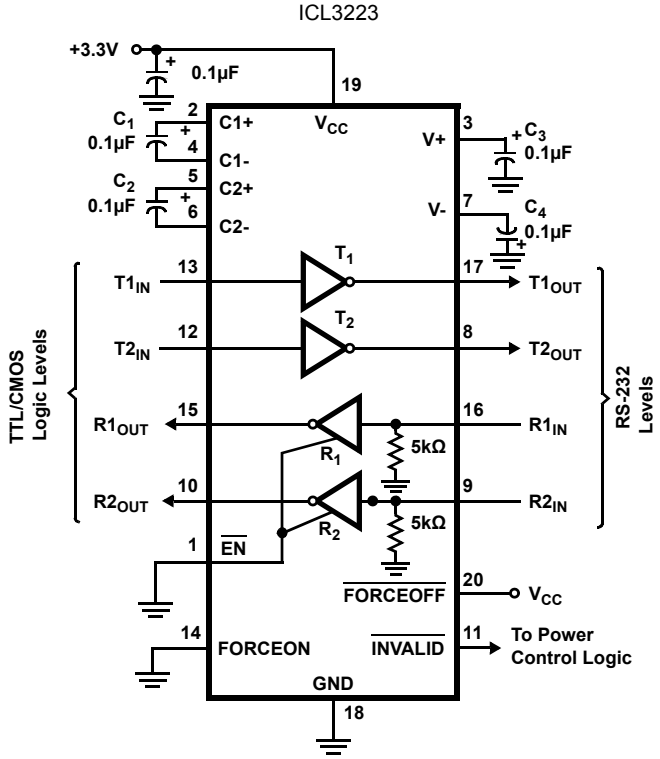
NOTE: The negative terminal of C_3 can be connected to either V_{CC} or GND

ICL3222

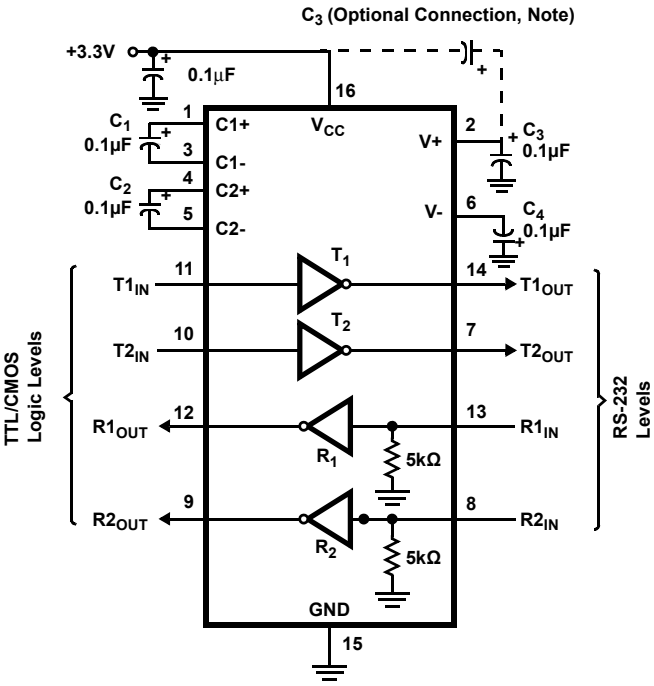


NOTE: The negative terminal of C_3 can be connected to either V_{CC} or GND

ICL3223

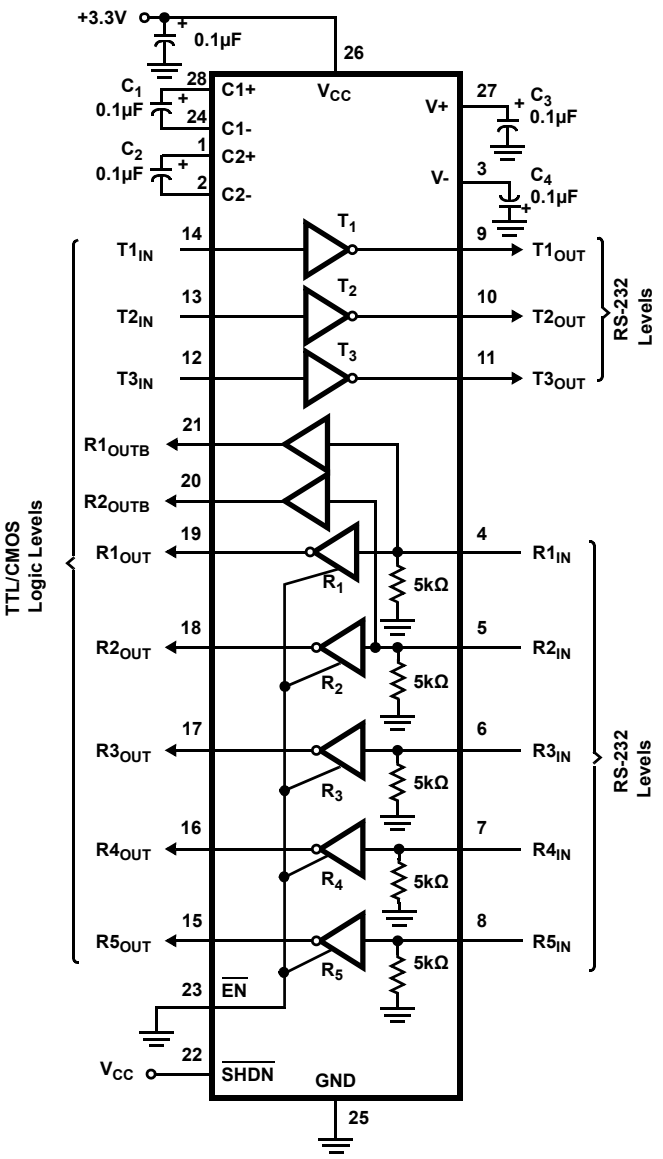


ICL3232

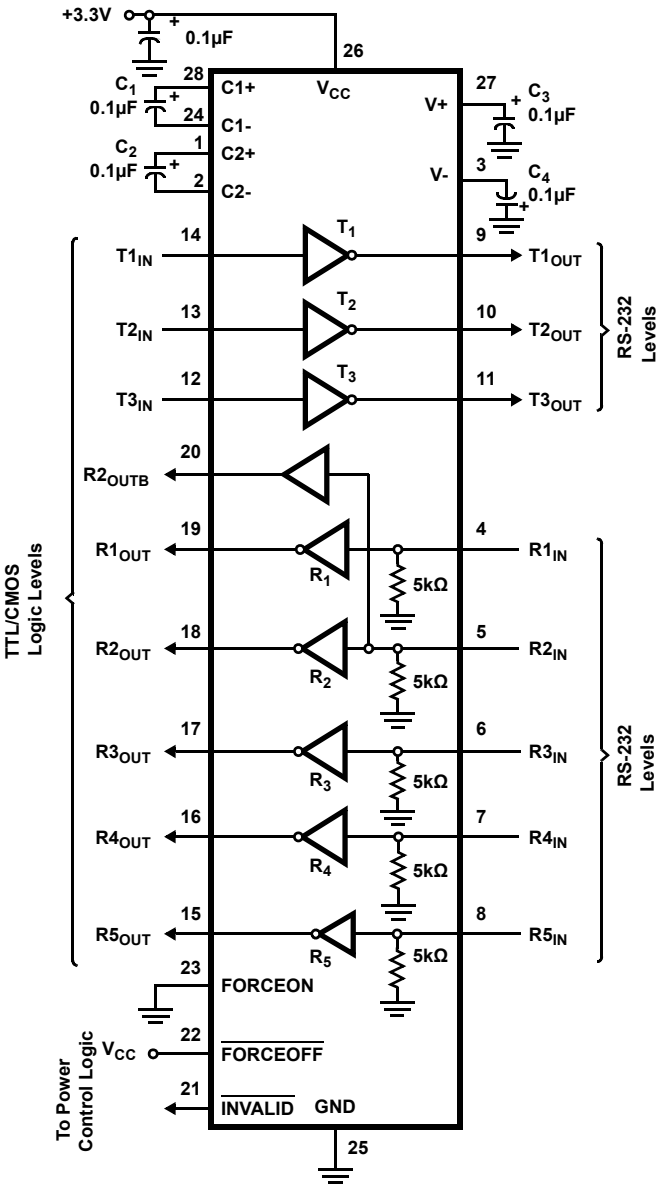


NOTE: The negative terminal of C_3 can be connected to either V_{CC} or GND

ICL3241



ICL3243



1.2 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp. Range (°c)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ICL3221CAZ	ICL3221CAZ	0 to 70	-	16 Ld SSOP	M16.209
ICL3221CAZ-T	ICL3221CAZ	0 to 70	1k	16 Ld SSOP	M16.209
ICL3221CVZ	3221CVZ	0 to 70	-	16 Ld TSSOP	M16.173
ICL3221CVZ-T	3221CVZ	0 to 70	2.5k	16 Ld TSSOP	M16.173
ICL3221IAZ	ICL3221IAZ	-40 to 85	-	16 Ld SSOP	M16.209
ICL3221IAZ-T	ICL3221IAZ	-40 to 85	1k	16 Ld SSOP	M16.209
ICL3221IAZ-T7A	ICL3221IAZ	-40 to 85	250	16 Ld SSOP	M16.209
ICL3222CAZ **(No longer available, recommended replacement: ICL3222ECAZ)**	ICL3222CAZ	0 to 70	-	20 Ld SSOP	M20.209

Part Number (Notes 2, 3)	Part Marking	Temp. Range (°c)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ICL3222CBZ **(No longer available, recommended replacement: ICL3222EIBZ)**	3222CBZ	0 to 70	-	18 Ld SOIC	M18.3
ICL3222CVZ	ICL3222CVZ	0 to 70	-	20 Ld TSSOP	M20.173
ICL3222CVZ-T	ICL3222CVZ	0 to 70	2.5k	20 Ld TSSOP	M20.173
ICL3222IAZ **(No longer available, recommended replacement: ICL3222EIAZ)**	ICL3222IAZ	-40 to 85	-	20 Ld SSOP	M20.209
ICL3222IVZ **(No longer available, recommended replacement: ICL3222EIVZ)**	ICL3222IVZ	-40 to 85	-	20 Ld TSSOP	M20.173
ICL3223CAZ **(No longer available, recommended replacement: ICL3223ECAZ)**	ICL3223CAZ	0 to 70	-	20 Ld SSOP	M20.209
ICL3223IAZ	ICL3223IAZ	-40 to 85	-	20 Ld SSOP	M20.209
ICL3223IAZ-T	ICL3223IAZ	-40 to 85	1k	20 Ld SSOP	M20.209
ICL3223IVZ	ICL3223IVZ	-40 to 85	-	20 Ld TSSOP	M20.173
ICL3223IVZ-T	ICL3223IVZ	-40 to 85	2.5k	20 Ld TSSOP	M20.173
ICL3232CAZ **(No longer available, recommended replacement: ICL3232ECAZ)**	3232CAZ	0 to 70	-	16 Ld SSOP	M16.209
ICL3232CBZ **(No longer available, recommended replacement: ICL3232ECBZ)**	3232CBZ	0 to 70	-	16 Ld SOIC	M16.3
ICL3232CBNZ	3232CBNZ	0 to 70	-	16 Ld SOIC (N)	M16.15
ICL3232CBNZ-T	3232CBNZ	0 to 70	2.5k	16 Ld SOIC (N)	M16.15
ICL3232CPZ	ICL3232CPZ	0 to 70	-	16 Ld PDIP	E16.3
ICL3232CVZ	3232CVZ	0 to 70	-	16 Ld TSSOP	M16.173
ICL3232CVZ-T	3232CVZ	0 to 70	2.5k	16 Ld TSSOP	M16.173
ICL3232IAZ **(No longer available, recommended replacement: ICL3232EIAZ)**	3232IAZ	-40 to 85	-	16 Ld SSOP	M16.209
ICL3232IBZ **(No longer available, recommended replacement: ICL3232EIBZ)**	3232IBZ	-40 to 85	-	16 Ld SOIC	M16.3
ICL3232IBNZ	3232IBNZ	-40 to 85	-	16 Ld SOIC (N)	M16.15
ICL3232IBNZ-T	3232IBNZ	-40 to 85	2.5k	16 Ld SOIC (N)	M16.15
ICL3232IBNZ-T7A	3232IBNZ	-40 to 85	250	16 Ld SOIC (N)	M16.15
ICL3232IVZ	3232IVZ	-40 to 85	-	16 Ld TSSOP	M16.173
ICL3232IVZ-T	3232IVZ	-40 to 85	2.5k	16 Ld TSSOP	M16.173
ICL3232IVZ-T7A	3232IVZ	-40 to 85	250	16 Ld TSSOP	M16.173
ICL3241CAZ **(No longer available, recommended replacement: ICL3241ECAZ)**	ICL3241CAZ	0 to 70	-	28 Ld SSOP	M28.209
ICL3241CVZ **(No longer available, recommended replacement: ICL3241ECVZ)**	ICL3241CVZ	0 to 70	-	28 Ld TSSOP	M28.173
ICL3241IAZ **(No longer available, recommended replacement: ICL3241EIAZ)**	ICL3241IAZ	-40 to 85	-	28 Ld SSOP	M28.209

Part Number (Notes 2, 3)	Part Marking	Temp. Range (°c)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ICL3243CAZ **(No longer available, recommended replacement: ICL3243ECAZ)**	ICL3243CAZ	0 to 70	-	28 Ld SSOP	M28.209
ICL3243CBZ	ICL3243CBZ	0 to 70	-	28 Ld SOIC	M28.3
ICL3243CBZ-T	ICL3243CBZ	0 to 70	1k	28 Ld SOIC	M28.3
ICL3243CVZ **(No longer available, recommended replacement: ICL3243ECVZ)**	ICL3243CVZ	0 to 70	-	28 Ld TSSOP	M28.173
ICL3243IAZ **(No longer available, recommended replacement: ICL3243EIAZ)**	ICL3243IAZ	-40 to 85	-	28 Ld SSOP	M28.209

Notes:

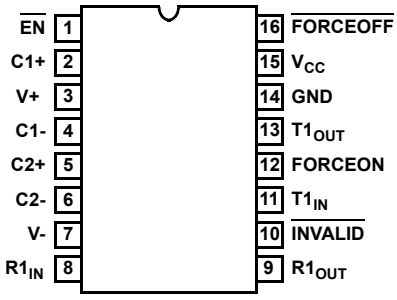
1. See TB347 for details about reel specifications.
2. Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ICL3221, ICL3222, ICL3223, ICL3232, ICL3241,and ICL3243 device pages. For more information about MSL, see TB363.

Table 1. Summary of Features

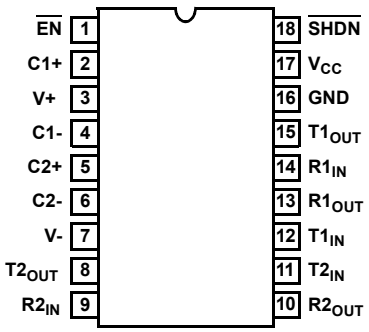
Part Number	No. of Tx.	No. of Rx.	No. of Monitor Rx. (R_{OUTB})	Data Rate (kbps)	Rx. Enable Function?	Ready Output?	Manual Power- Down?	Automatic Powerdown Function?
ICL3221	1	1	0	250	Yes	No	Yes	Yes
ICL3222	2	2	0	250	Yes	No	Yes	No
ICL3223	2	2	0	250	Yes	No	Yes	Yes
ICL3232	2	2	0	250	No	No	No	No
ICL3241	3	5	2	250	Yes	No	Yes	No
ICL3243	3	5	1	250	No	No	Yes	Yes

1.3 Pin Configurations

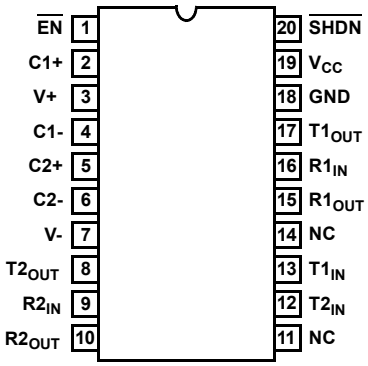
ICL3221 (SSOP, TSSOP)
Top View



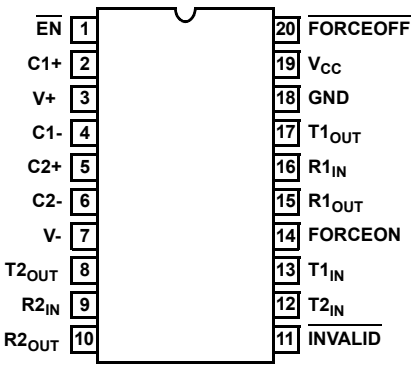
ICL3222 (SOIC)
Top View



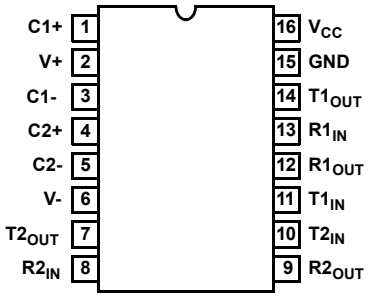
ICL3222 (SSOP, TSSOP)
Top View



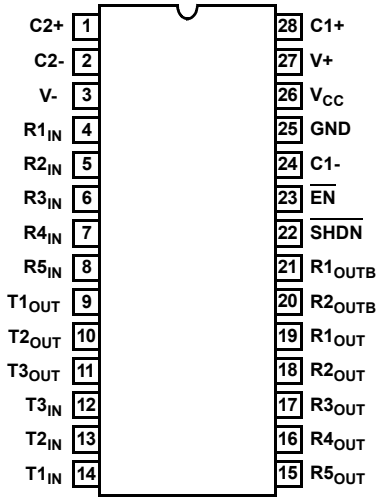
ICL3223 (SSOP, TSSOP)
Top View



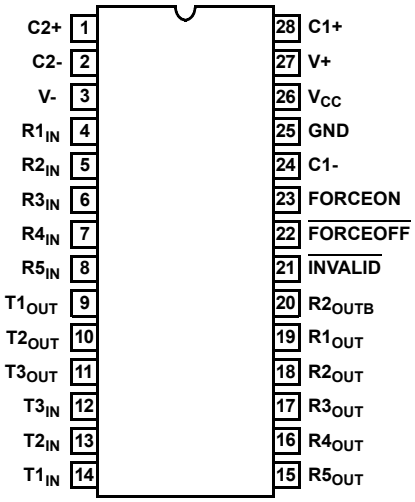
ICL3232 (PDIP, SOIC, SSOP, TSSOP)
Top View



ICL3241 (SSOP, TSSOP)
Top View



ICL3243 (SOIC, SSOP, TSSOP)
Top View



1.4 Pin Descriptions

Pin	Function
V_{CC}	System power supply input (3.0V to 5.5V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
T_{IN}	TTL/CMOS compatible transmitter Inputs.
T_{OUT}	RS-232 level (nominally ±5.5V) transmitter outputs.
R_{IN}	RS-232 compatible receiver inputs.
R_{OUT}	TTL/CMOS level receiver outputs.
R_{OUTB}	TTL/CMOS level, noninverting, always enabled receiver outputs.
$\overline{\text{INVALID}}$	Active low output that indicates if no valid RS-232 levels are present on any receiver input.
$\overline{\text{EN}}$	Active low receiver enable control; doesn't disable R_{OUTB} outputs.
$\overline{\text{SHDN}}$	Active low input to shut down transmitters and on-board power supply to place device in low power mode.
$\overline{\text{FORCEOFF}}$	Active low to shut down transmitters and on-chip power supply. This overrides any automatic circuitry and FORCEON (See Table 5 on page 15).
FORCEON	Active high input to override automatic powerdown circuitry thereby keeping transmitters active. ($\overline{\text{FORCEOFF}}$ must be high).

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{CC} to Ground	-0.3	6	V
V+ to Ground	-0.3	7	V
V- to Ground	+0.3	-7	V
V+ to V-		14	V
Input Voltages			
T_{IN}, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$, $\overline{SHDN}$	-0.3	6	V
R_{IN}		±25	V
Output Voltages			
T_{OUT}		±13.2	V
R_{OUT}, $\overline{INVALID}$	-0.3	V_{CC} +0.3	V
Short-Circuit Duration			
T_{OUT}		Continuous	
ESD Rating	(See ESD Performance)		

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
16 Ld PDIP Package (Note 5)	90
16 Ld Wide SOIC Package	100
16 Ld Narrow SOIC Package	115
18 Ld SOIC Package	75
28 Ld SOIC Package	75
16 Ld SSOP Package	135
20 Ld SSOP Package	122
16 Ld TSSOP Package	145
20 Ld TSSOP Package	140
28 Ld SSOP and TSSOP Packages	100

Notes:

4. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379.
5. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile (SOIC, SSOP, TSSOP Only)	see TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range			
ICL32xxCx	0	+70	°C
ICL32xxIx	-40	+85	°C

2.4 Electrical Specifications

Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; unless otherwise specified. Typicals are at T_A = 25°C

Parameter	Test Conditions		Temp (°C)	Min	Typ	Max	Unit
DC Characteristics							
Supply Current, Automatic Power-Down	All R_{IN} open, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC} (ICL3221, ICL3223, ICL3243 only)		25	-	1.0	10	µA
Supply Current, Powerdown	$\overline{FORCEOFF}$ = $\overline{SHDN}$ = GND (except ICL3232)		25	-	1.0	10	µA
Supply Current, Automatic Power-Down Disabled	All outputs unloaded, FORCEON = $\overline{FORCEOFF}$ = $\overline{SHDN}$ = V_{CC}	V_{CC} = 3.15V, ICL3221-32	25	-	0.3	1.0	mA
		V_{CC} = 3.0V, ICL3241-43	25	-	0.3	1.0	mA
Logic and Transmitter Inputs and Receiver Outputs							
Input Logic Threshold Low	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$		Full	-	-	0.8	V
Input Logic Threshold High	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$	V_{CC} = 3.3V	Full	2.0	-	-	V
		V_{CC} = 5.0V	Full	2.4	-	-	V
Input Leakage Current	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$, $\overline{SHDN}$		Full	-	±0.01	±1.0	µA
Output Leakage Current (Except ICL3232)	$\overline{FORCEOFF}$ = GND or $\overline{EN}$ = V_{CC}		Full	-	±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC} - 0.6	V_{CC} - 0.1	-	V
Automatic Powerdown (ICL3221, ICL3223, ICL3243 only, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC})							
Receiver Input Thresholds to Enable Transmitters	ICL32xx powers up (See Figure 12)		Full	-2.7	-	2.7	V
Receiver Input Thresholds to Disable Transmitters	ICL32xx powers down (See Figure 12)		Full	-0.3	-	0.3	V
$\overline{INVALID}$ Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
$\overline{INVALID}$ Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC}-0.6	-	-	V
Receiver Threshold to Transmitters Enabled Delay (t_{WU})			25	-	100	-	µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High Delay (t_{INVH})			25	-	1	-	µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low Delay (t_{INVL})			25	-	30	-	µs
Receiver Inputs							
Input Voltage Range			Full	-25	-	25	V
Input Threshold Low	V_{CC} = 3.3V		25	0.6	1.2	-	V
	V_{CC} = 5.0V		25	0.8	1.5	-	V
Input Threshold High	V_{CC} = 3.3V		25	-	1.5	2.4	V
	V_{CC} = 5.0V		25	-	1.8	2.4	V
Input Hysteresis			25	-	0.3	-	V

Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; unless otherwise specified. Typicals are at T_A = 25°C **(Continued)**

Parameter	Test Conditions		Temp (°C)	Min	Typ	Max	Unit
Input Resistance			25	3	5	7	kΩ
Transmitter Outputs							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kΩ to Ground		Full	±5.0	±5.4	-	V
Output Resistance	V_{CC} = V+ = V- = 0V, Transmitter Output = ±2V		Full	300	10M	-	W
Output Short-Circuit Current			Full	-	±35	±60	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 5.5V Automatic Powerdown or $\overline{FORCEOFF}$ = $\overline{SHDN}$ = GND		Full	-	-	±25	µA
Mouse Driveability (ICL324X Only)							
Transmitter Output Voltage (See Figure 15)	$T1_{IN}$ = $T2_{IN}$ = GND, $T3_{IN}$ = V_{CC}, $T3_{OUT}$ loaded with 3kΩ to GND, $T1_{OUT}$ and $T2_{OUT}$ loaded with 2.5mA each		Full	±5	-	-	V
Timing Characteristics							
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		Full	250	500	-	kbps
Receiver Propagation Delay	Receiver input to receiver output, C_L = 150pF	t_{PHL}	25	-	0.3	-	µs
		t_{PLH}	25	-	0.3	-	µs
Receiver Output Enable Time	Normal operation (except ICL3232)		25	-	200	-	ns
Receiver Output Disable Time	Normal operation (except ICL3232)		25	-	200	-	ns
Transmitter Skew	t_{PHL} - t_{PLH}		Full	-	200	1000	ns
Receiver Skew	t_{PHL} - t_{PLH}		Full	-	100	500	ns
Transition Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, Measured from 3V to -3V or -3V to 3V	C_L = 200pF to 2500pF	25	4	8.0	30	V/µs
		C_L = 200pF to 1000pF	25	6	-	30	V/µs
ESD Performance							
RS-232 Pins (T_{OUT}, R_{IN})	Human Body Model	ICL3221 - ICL3243	25	-	±15	-	kV
	IEC61000-4-2 Contact Discharge	ICL3221 - ICL3243	25	-	±8	-	kV
	IEC61000-4-2 Air Gap Discharge	ICL3221 - ICL3232	25	-	±8	-	kV
		ICL3241 - ICL3243	25	-	±6	-	kV
All Other Pins	Human Body Model	ICL3221 - ICL3243	25	-	±2	-	kV

3. Typical Performance Curves

V_{CC} = 3.3V, T_A = 25°C

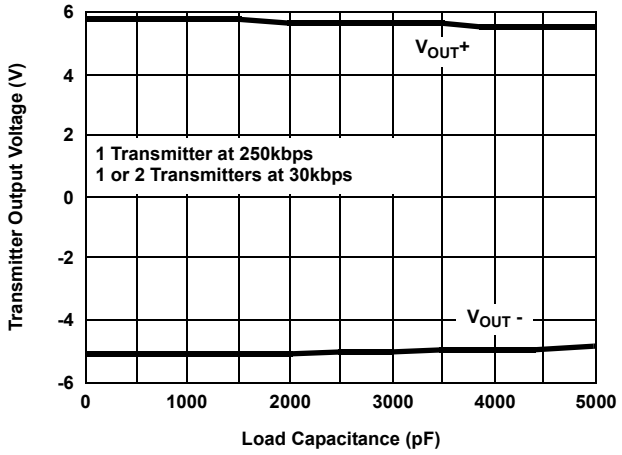


Figure 1. Transmitter Output Voltage vs Load Capacitance

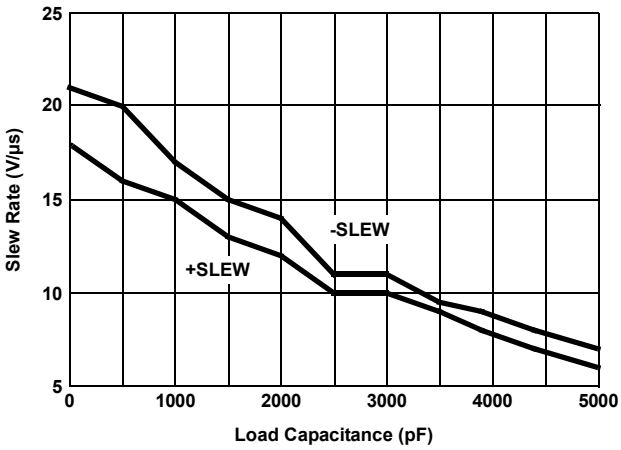


Figure 2. Slew Rate vs Load Capacitance

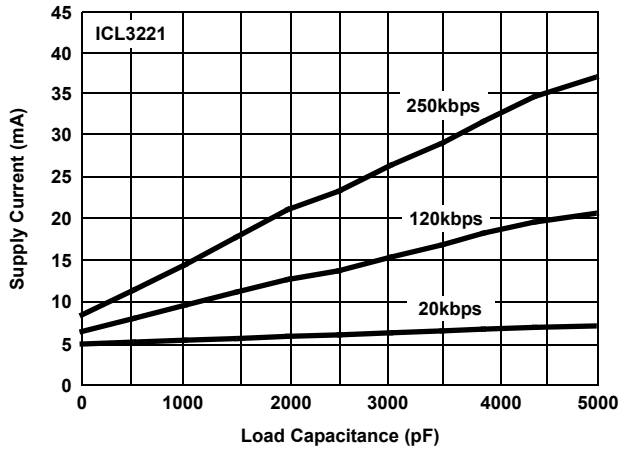


Figure 3. Supply Current vs Load Capacitance when Transmitting Data

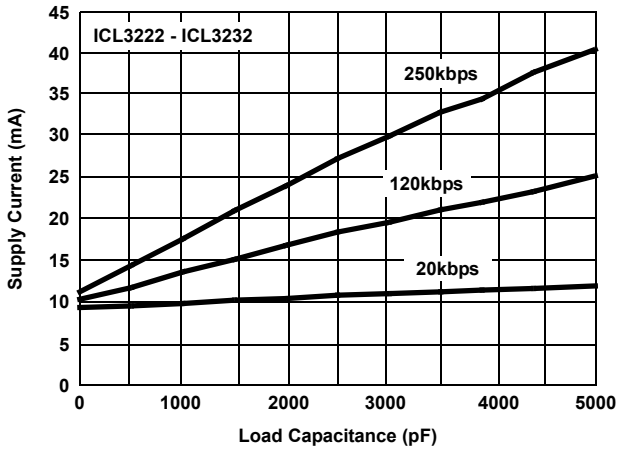


Figure 4. Supply Current vs Load Capacitance when Transmitting Data

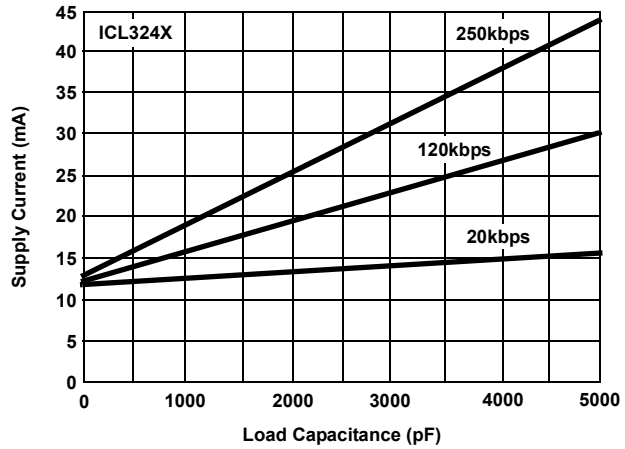


Figure 5. Supply Current vs Load Capacitance when Transmitting Data

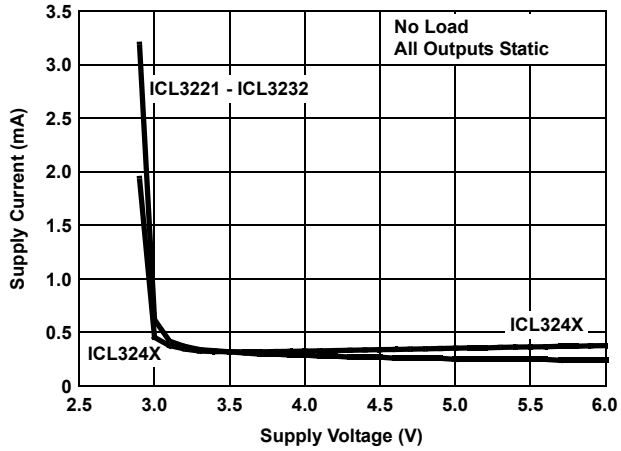


Figure 6. Supply Current vs Supply Voltage

4. Application Information

The ICL32xx interface ICs operate from a single +3V to +5.5V supply, ensure a 250kbps minimum data rate, require only four small external 0.1µF capacitors, feature low-power consumption, and meet all EIA RS-232C and V.28 specifications. The circuit is divided into three sections:

- Charge-pump
- Transmitters
- Receivers

4.1 Charge Pump

The ICL32xx family uses regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3.0V, which allows these devices to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1µF capacitors for the voltage doubler and inverter functions at V_{CC} = 3.3V. See Capacitor Selection and Table 6 on page 19 for capacitor recommendations for other operating conditions. The charge pumps operate discontinuously (for example, they turn off as soon as the V+ and V- supplies are pumped up to the nominal values), resulting in significant power savings.

4.1.1 Charge Pump Absolute Maximum Ratings

These 3V to 5V RS-232 transceivers have been fully characterized for 3.0V to 3.6V operation, and at critical points for 4.5V to 5.5V operation. Furthermore, load conditions were favorable using static logic states only.

The specified maximum values for V+ and V- are +7V and -7V, respectively. These limits apply for VCC values set to 3.0V and 3.6V (see Table 2). For VCC values set to 4.5V and 5.5V, the maximum values for V+ and V- can approach +9V and -7V respectively (see Table 3). The breakdown characteristics for V+ and V- were measured with ±13V.

Table 2. V+ and V- Values for V_{CC} = 3.0V to 3.6V

C_1 (µF)	C_2, C_3, C_4 (µF)	Load	T1IN (Logic State)	V+ (V)		V- (V)	
				V_{CC} = 3.0V	V_{CC} = 3.6V	V_{CC} = 3.0V	V_{CC} = 3.6V
0.1	0.1	Open	H	5.8	6.56	-5.6	-5.88
			L	5.8	6.56	-5.6	-5.88
			2.4kbps	5.8	6.56	-5.6	-5.88
		3kΩ // 1000pF	H	5.88	6.6	-5.56	-5.92
			L	5.76	6.36	-5.56	-5.76
			2.4kbps	6	6.64	-5.64	-5.96
0.047	0.33	Open	H	5.68	6	-5.6	-5.6
			L	5.68	6	-5.6	-5.6
			2.4kbps	5.68	6	-5.6	-5.6
		3kΩ // 1000pF	H	5.76	6.08	-5.64	-5.64
			L	5.68	6.04	-5.6	-5.6
			2.4kbps	5.84	6.16	-5.64	-5.72
1	1	Open	H	5.88	6.24	-5.6	-5.6
			L	5.88	6.28	-5.6	-5.64
			2.4kbps	5.8	6.2	-5.6	-5.6
		3kΩ // 1000pF	H	5.88	6.44	-5.64	-5.72
			L	5.88	6.04	-5.64	-5.64
			2.4kbps	5.92	6.4	-5.64	-5.64

Table 3. V+ and V- Values for Vcc = 4.5V to 5.5V

C_1 (µF)	C_2, C_3, C_4 (µF)	Load	T1IN (Logic State)	V+ (V)		V- (V)	
				V_{CC} = 4.5V	V_{CC} = 5.5V	V_{CC} = 4.5V	V_{CC} = 5.5V
0.1	0.1	Open	H	7.44	8.48	-6.16	-6.4
			L	7.44	8.48	-6.16	-6.44
			2.4kbps	7.44	8.48	-6.17	-6.44
		3kΩ // 1000pF	H	7.76	8.88	-6.36	-6.72
			L	7.08	8	-5.76	-5.76
			2.4kbps	7.76	8.84	-6.4	-6.64
0.047	0.33	Open	H	6.44	6.88	-5.8	-5.88
			L	6.48	6.88	-5.84	-5.88
			2.4kbps	6.44	6.88	-5.8	-5.88
		3kΩ // 1000pF	H	6.64	7.28	-5.92	-6.04
			L	6.24	6.6	-5.52	-5.52
			2.4kbps	6.72	7.16	-5.92	-5.96
1	1	Open	H	6.84	7.6	-5.76	-5.76
			L	6.88	7.6	-5.76	-5.76
			2.4kbps	6.92	7.56	-5.72	-5.76
		3kΩ // 1000pF	H	7.28	8.16	-5.8	-5.92
			L	6.44	6.84	-5.64	-6.84
			2.4kbps	7.08	7.76	-5.8	-5.8

The resulting new maximum voltages at V+ and V- are listed in Table 4.

Table 4. New Measured Withstanding Voltages

V+, V- to Ground	±13V
V+ to V-	20V

4.2 Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. These transmitters are coupled with the on-chip ± 5.5V supplies and deliver true RS-232 levels across a wide range of single supply system voltages.

Except for the ICL3232, all transmitter outputs disable and assume a high impedance state when the device enters the powerdown mode (See Table 5 on page 15). These outputs can be driven to ±12V when disabled.

All devices ensure a 250kbps data rate for full load conditions (3kΩ and 1000pF), $V_{CC} \geq 3.0V$, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq 3.3V$, R_L = 3kΩ, and C_L = 250pF, one transmitter easily operates at 900kbps.

Transmitter inputs float if left unconnected and may cause I_{CC} increases. Connect unused inputs to GND for the best performance.

4.3 Receivers

All the ICL32xx devices contain standard inverting receivers that three-state (except for the ICL3232) using the $\overline{EN}$ or $\overline{FORCEOFF}$ control lines. Additionally, the two ICL324X products include noninverting (monitor) receivers (denoted by the R_{OUTB} label) that are always active, regardless of the state of any control lines. All the receivers convert RS-232 signals to CMOS output levels and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 7) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

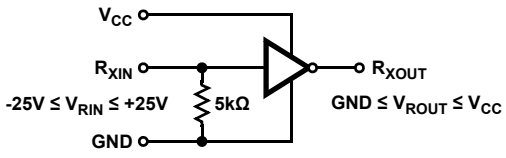


Figure 7. Inverting Receiver Connections

The ICL3221/22/23/41 inverting receivers disable only when $\overline{EN}$ is driven high. ICL3243 receivers disable during forced (manual) powerdown, but not during automatic powerdown (See Table 5).

ICL324X monitor receivers remain active even during manual powerdown and forced receiver disable, making them extremely useful for Ring Indicator monitoring. Standard receivers driving powered down peripherals must be disabled to prevent current flow through the peripheral's protection diodes (See Figures 8 and 9). When disabled, the receivers cannot be used for wake up functions, but the corresponding monitor receiver can be dedicated to this task as shown in Figure 9 on page 17.

4.4 Low Power Operation

The 3V devices require a nominal supply current of 0.3mA, even at V_{CC} = 5.5V, during normal operation (not in powerdown mode), which is considerably less than the 5mA to 11mA current required by comparable 5V RS-232 devices, allowing you to reduce system power simply by switching to this new family.

4.5 Powerdown Functionality (Except ICL3232)

The already low current requirement drops significantly when the device enters powerdown mode. In power-down, supply current drops to 1µA, because the on-chip charge pump turns off (V+ collapses to V_{CC}, V- collapses to GND), and the transmitter outputs three-state. Inverting receiver outputs may disable in power-down; see Table 5 for details. This micro-power mode makes these devices ideal for battery powered and portable applications.

4.5.1 Software Controlled (Manual) Powerdown

Most devices in the ICL32xx family provide pins that allow you to force the IC into the low power, standby state.

On the ICL3222 and ICL3241, the powerdown control is using a simple shutdown ($\overline{SHDN}$) pin. Driving this pin high enables normal operation, and driving it low forces the IC into its powerdown state. Connect $\overline{SHDN}$ to V_{CC} if the powerdown function is not needed. Note that all the receiver outputs remain enabled during shutdown (See Table 5). For the lowest power consumption during powerdown, the receivers should also be disabled by driving the $\overline{EN}$ input high (See next section, and Figures 8 and 9).

The ICL3221, ICL3223, and ICL3243 use a two pin approach where the FORCEON and $\overline{FORCEOFF}$ inputs determine the IC's mode. For always enabled operation, FORCEON and $\overline{FORCEOFF}$ are both strapped high. Under logic or software control, only the $\overline{FORCEOFF}$ input needs to be driven to switch between active and powerdown modes. The FORCEON state is not critical because $\overline{FORCEOFF}$ overrides FORCEON. However, if strictly manual control over powerdown is needed, you must strap FORCEON high to disable the automatic power-down circuitry. ICL3243 inverting (standard) receiver outputs also disable when the device is in manual powerdown, thereby eliminating the possible current path through a shutdown peripheral's input protection diode (See Figures 8 and 9).

Table 5. Powerdown and Enable Logic Truth Table

RS-232 Signal Present at Receiver Input?	$\overline{FORCEOFF}$ or $\overline{SHDN}$ Input	FORCEON Input	$\overline{EN}$ Input	Transmitter Outputs	Receiver Outputs	R_{OUTB} Outputs (Note 6)	$\overline{INVALID}$ Output	Mode of Operation
ICL3222, ICL3241								
N.A.	L	N.A.	L	High-Z	Active	Active	N.A.	Manual Powerdown
N.A.	L	N.A.	H	High-Z	High-Z	Active	N.A.	Manual Powerdown w/Rcvr. Disabled
N.A.	H	N.A.	L	Active	Active	Active	N.A.	Normal Operation

Table 5. Powerdown and Enable Logic Truth Table (Continued)

RS-232 Signal Present at Receiver Input?	$\overline{FORCEOFF}$ or $\overline{SHDN}$ Input	FORCEON Input	$\overline{EN}$ Input	Transmitter Outputs	Receiver Outputs	R_{OUTB} Outputs (Note 6)	$\overline{INVALID}$ Output	Mode of Operation
ICL3222, ICL3241								
N.A.	H	N.A.	H	Active	High-Z	Active	N.A.	Normal Operation w/Rcvr. Disabled
ICL3221, ICL3223								
No	H	H	L	Active	Active	N.A.	L	Normal Operation (Auto Powerdown Disabled)
No	H	H	H	Active	High-Z	N.A.	L	
Yes	H	L	L	Active	Active	N.A.	H	Normal Operation (Auto Powerdown Enabled)
Yes	H	L	H	Active	High-Z	N.A.	H	
No	H	L	L	High-Z	Active	N.A.	L	Powerdown Due to Auto Power-Down Logic
No	H	L	H	High-Z	High-Z	N.A.	L	
Yes	L	X	L	High-Z	Active	N.A.	H	Manual Powerdown
Yes	L	X	H	High-Z	High-Z	N.A.	H	Manual Powerdown w/Rcvr. Disabled
No	L	X	L	High-Z	Active	N.A.	L	Manual Powerdown
No	L	X	H	High-Z	High-Z	N.A.	L	Manual Powerdown w/Rcvr. Disabled
ICL3243								
No	H	H	N.A.	Active	Active	Active	L	Normal Operation (Auto Powerdown Disabled)
Yes	H	L	N.A.	Active	Active	Active	H	Normal Operation (Auto Powerdown Enabled)
No	H	L	N.A.	High-Z	Active	Active	L	Powerdown Due to Auto Power-Down Logic
Yes	L	X	N.A.	High-Z	High-Z	Active	H	Manual Powerdown
No	L	X	N.A.	High-Z	High-Z	Active	L	Manual Powerdown

Note:
6. Applies only to the ICL3241 and ICL3243.

4.5.2 $\overline{INVALID}$ Output

The $\overline{INVALID}$ output always indicates whether a valid RS-232 signal is present at any of the receiver inputs (See Table 5), giving you a way to determine when the interface block should power down. In the case of a disconnected interface cable where all the receiver inputs are floating (but pulled to GND by the internal receiver pull down resistors), the $\overline{INVALID}$ logic detects the invalid levels and drives the output low. The power management logic then uses this indicator to power down the interface block. Reconnecting the cable restores valid levels at the receiver inputs, $\overline{INVALID}$ switches high, and the power management logic wakes up the interface block. $\overline{INVALID}$ can also be used to indicate the DTR or RING INDICATOR signal as long as the other receiver inputs are floating or driven to GND (as in the case of a powered down driver). Connecting $\overline{FORCEOFF}$ and FORCEON together disables the automatic powerdown feature, enabling them to function as a manual $\overline{SHUTDOWN}$ input (See Figure 10).

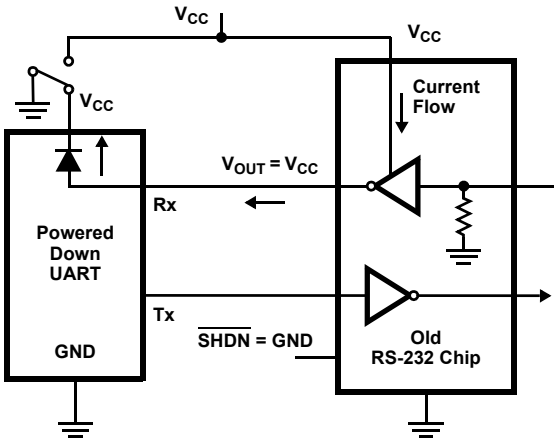


Figure 8. Power Drain Through Powered Down Peripheral

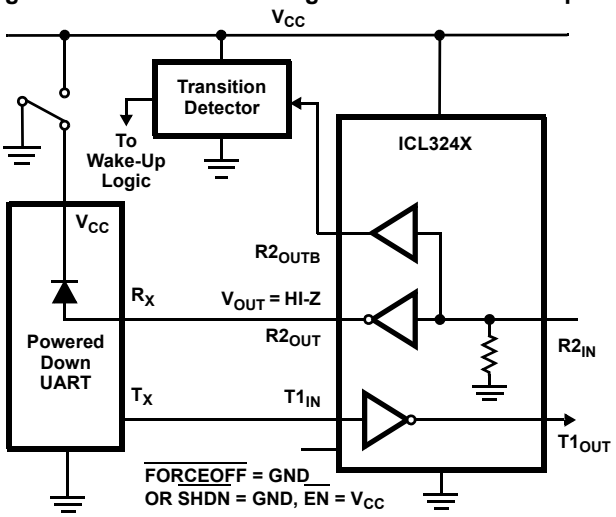


Figure 9. Disabled Receivers Prevent Power Drain

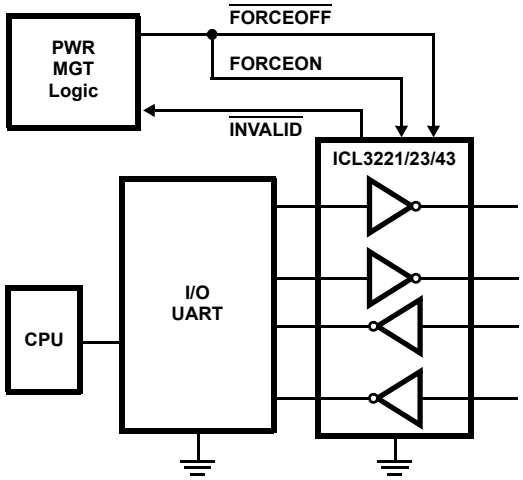


Figure 10. Connections for Manual Powerdown when No Valid Receiver Signals are Present

With any of the above control schemes, the time required to exit powerdown and resume transmission is only 100µs. A mouse or other application may need more time to wake up from shutdown. If automatic powerdown is being used, the RS-232 device reenters powerdown if valid receiver levels are not re-established within 30µs of the ICL32xx powering up. Figure 11 on page 18 shows a circuit that keeps the ICL32xx from initiating automatic

power-down for 100ms after powering up, which gives the slow-to-wake peripheral circuit time to re-establish valid RS-232 output levels.

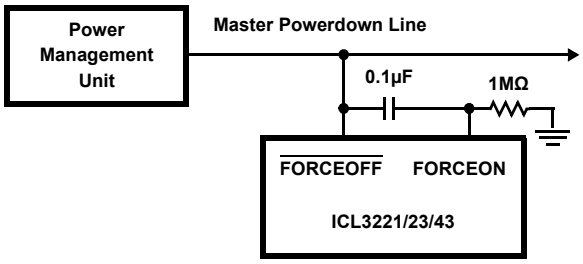


Figure 11. Circuit to Prevent Auto Powerdown for 100ms After Forced Power-UP

4.5.3 Automatic Powerdown (ICL3221/23/43 Only)

Even greater power savings are available by using the ICL3221, ICL3223, or ICL3243's automatic powerdown function. When no valid RS-232 voltages (See Figure 12) are sensed on any receiver input for 30µs, the charge-pump and transmitters powerdown, thereby reducing supply current to 1µA. Invalid receiver levels occur whenever the driving peripheral's outputs are shut off (powered down) or when the RS-232 interface cable is disconnected. The ICL32xx devices power back up whenever they detect a valid RS-232 voltage level on any receiver input, which provides additional system power savings without changes to the existing operating system.

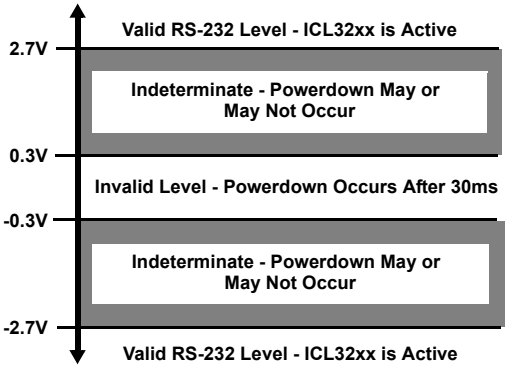


Figure 12. Definition of Valid RS-232 Receiver Levels

Automatic powerdown operates when the FORCEON input is low, and the $\overline{\text{FORCEOFF}}$ input is high. Tying FORCEON high disables automatic powerdown, but manual powerdown is always available using the overriding $\overline{\text{FORCEOFF}}$ input. Table 5 on page 15 summarizes the automatic powerdown functionality.

Devices with the automatic powerdown feature include an $\overline{\text{INVALID}}$ output signal, which switches low to indicate that invalid levels have persisted on all of the receiver inputs for more than 30µs (See Figure 13). $\overline{\text{INVALID}}$ switches high 1µs after detecting a valid RS-232 level on a receiver input. $\overline{\text{INVALID}}$ operates in all modes (forced or automatic powerdown, or forced on), so it is also useful for systems employing manual powerdown circuitry. When automatic powerdown is used, $\overline{\text{INVALID}}$ = 0 indicates that the ICL32xx is in powerdown mode.

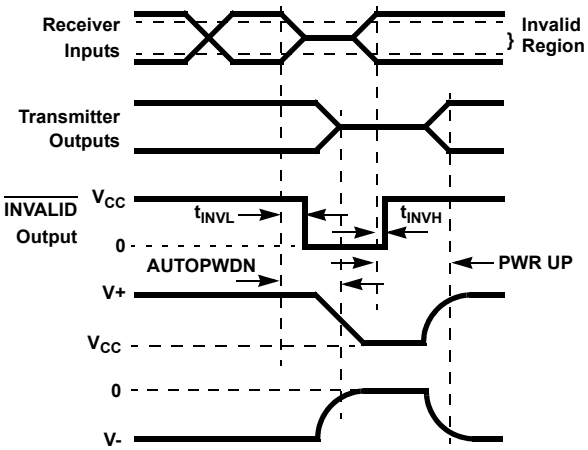


Figure 13. Automatic Powerdown and $\overline{\text{INVALID}}$ Timing Diagrams

The time to recover from automatic powerdown mode is typically 100µs.

4.6 Receiver ENABLE Control (ICL3221/22/23/41 Only)

ICL3221, ICL3222, ICL3223, and ICL3241 also feature an $\overline{\text{EN}}$ input to control the receiver outputs. Driving $\overline{\text{EN}}$ high disables all the inverting (standard) receiver outputs placing them in a high impedance state, which is useful to eliminate supply current, due to a receiver output forward biasing the protection diode, when driving the input of a powered down (V_{CC} = GND) peripheral (See Figure 8 on page 17). The enable input has no effect on transmitter nor monitor (R_{OUTB}) outputs.

4.7 Capacitor Selection

The charge pumps require 0.1µF capacitors for 3.3V operation. For other supply voltages see Table 6 for capacitor values. Do not use values smaller than those listed in Table 6. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C_2, C_3, and C_4 can be increased without increasing C_1's value; however, do not increase C_1 without also increasing C_2, C_3, and C_4 to maintain the proper ratios (C_1 to the other capacitors).

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's Equivalent Series Resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

Table 6. Required Capacitor Values

V_{CC} (V)	C_1 (µF)	C_2, C_3, C_4 (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47

4.8 Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

4.9 Operation Down to 2.7V

ICL32xx transmitter outputs meet RS-562 levels (±3.7V), at full data rate, with V_{CC} as low as 2.7V. RS-562 levels typically ensure interoperability with RS-232 devices.

4.10 Transmitter Outputs when Exiting Powerdown

Figure 14 shows the response of two transmitter outputs when exiting powerdown mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

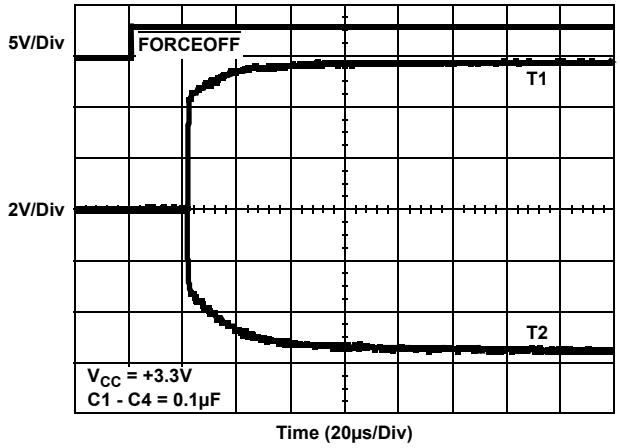


Figure 14. Transmitter Outputs when Exiting Powerdown

4.11 Mouse Driveability

The ICL324X have been specifically designed to power a serial mouse while operating from low voltage supplies. Figure 15 shows the transmitter output voltages under increasing load current. The on-chip switching regulator ensures the transmitters will supply at least ±5V during worst case conditions (15mA for paralleled V+ transmitters, 7.3mA for single V- transmitter). The Automatic Powerdown feature does not work with a mouse, so $\overline{\text{FORCEOFF}}$ and FORCEON should be connected to V_{CC}.

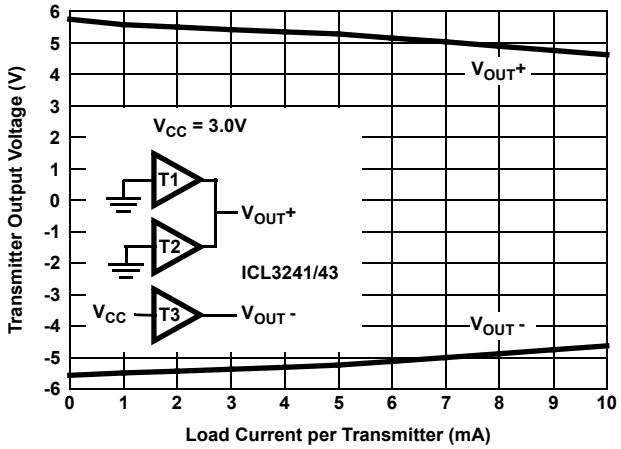


Figure 15. Transmitter Output Voltage vs Load Current (per Transmitter, Such as, Double Current Axis for Total V_{OUT+} Current)

4.12 High Data Rates

The ICL32xx maintain the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 16 details a transmitter loopback test circuit, and Figure 17 illustrates the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF at 120kbps. Figure 18 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

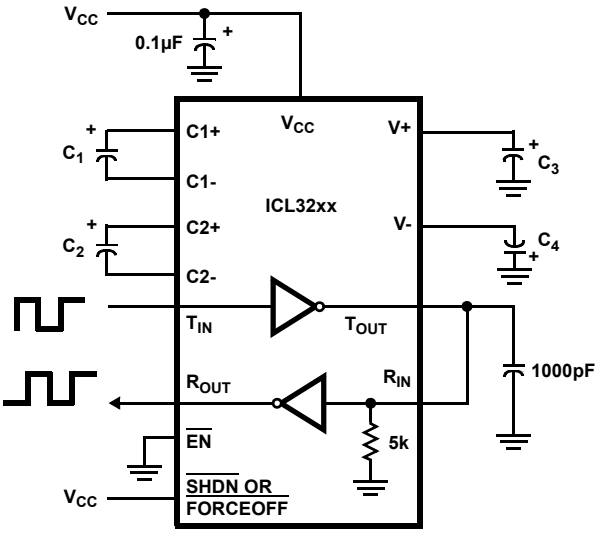


Figure 16. Transmitter Loopback Test Circuit

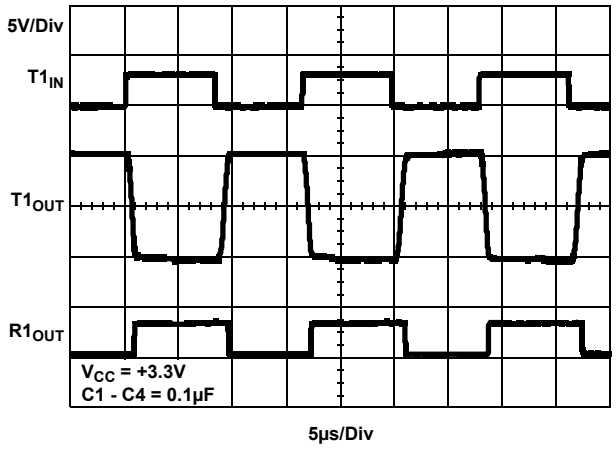


Figure 17. Loopback Test at 120kbps

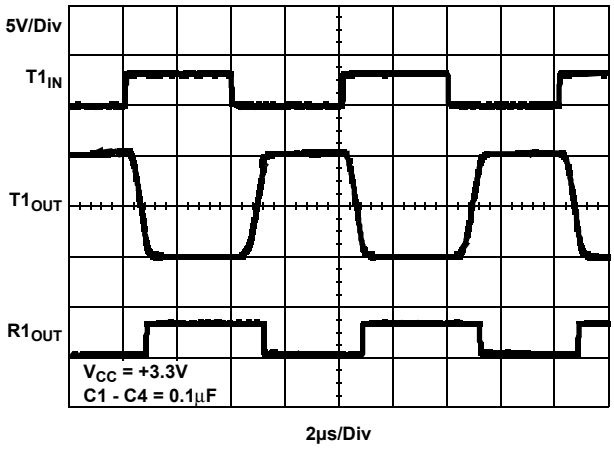


Figure 18. Loopback Test at 250kbps

4.13 Interconnection with 3V and 5V Logic

The ICL32xx directly interface with 5V CMOS and TTL logic families. With the ICL32xx at 3.3V, and the logic supply at 5V, AC, HC, and CD4000 outputs can drive ICL32xx inputs, but ICL32xx outputs do not reach the minimum V_{IH} for these logic families. See Table 7 for more information.

Table 7. Logic Family Compatibility with Various Supply Voltages

System Power-Supply Voltage (V)	V_{CC} Supply Voltage (V)	Compatibility
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. ICL32xx outputs are incompatible with AC, HC, and CD4000 CMOS inputs.

4.14 Pin Compatible Replacements For 5V Devices

The ICL3221/22/32 are pin compatible with existing 5V RS-232 transceivers (see the "Features" on page 1 for details), which coupled with the low I_{CC} and wide operating supply range, make the ICL32xx potential lower power, higher performance, drop-in replacements for existing 5V applications. As long as the ±5V RS-232 output swings are acceptable, and transmitter input pull-up resistors are not required, the ICL32xx should work in most 5V applications.

When replacing a device in an existing 5V application, it is acceptable to terminate C_3 to V_{CC} as shown on the "Typical Operating Circuits" on page 3. Terminate C_3 to GND if possible, as slightly better performance results from this configuration.

5. Die Characteristics

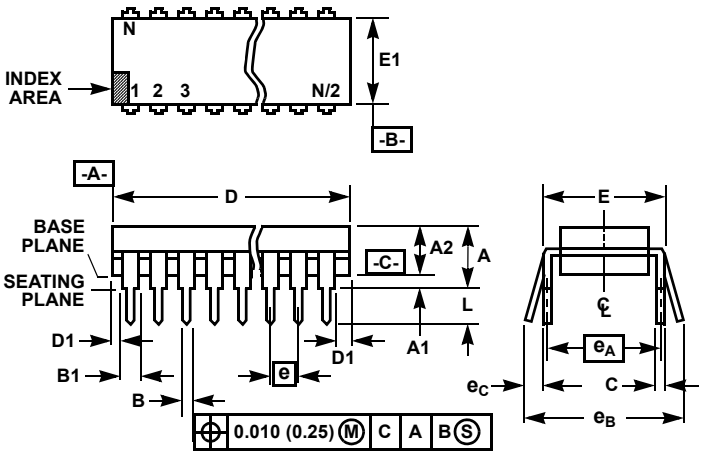
Substrate Potential (Powered Up)	GND
Transistor Count	ICL3221: 286 ICL3222: 338 ICL3223: 357 ICL3232: 296 ICL324X: 464
Process	Si Gate CMOS

6. Revision History

Rev.	Date	Description
23	Apr 26, 2019	Updated to latest formatting. Added Related Literature section. Updated Ordering information table by adding active tape and reel information, updated notes, adding note 3, removed retired parts, and stamped EOL parts. Added “Charge Pump Absolute Maximum Ratings” on page 13. Removed About Intersil section. Updated M16.15 to the latest revision changes are as follows: Update graphics to new standard layout, removing the dimension table. Updated disclaimer.
22	Sep 1, 2015	- Ordering Information Table on page 2. - Added Revision History. - Added About Intersil Verbiage. - Updated POD M16.173 to latest revision changes are as follow: Convert to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes. - Updated POD M20.173 to most current version changes are as follow: Convert to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes. - Updated POD M28.173 to most current version changes are as follow: Convert to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes. -Updated POD M28.3 to most current version change is as follows: Added land pattern.

7. Package Outline Drawings

For the most recent package outline drawing, see E16.3.



Notes:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

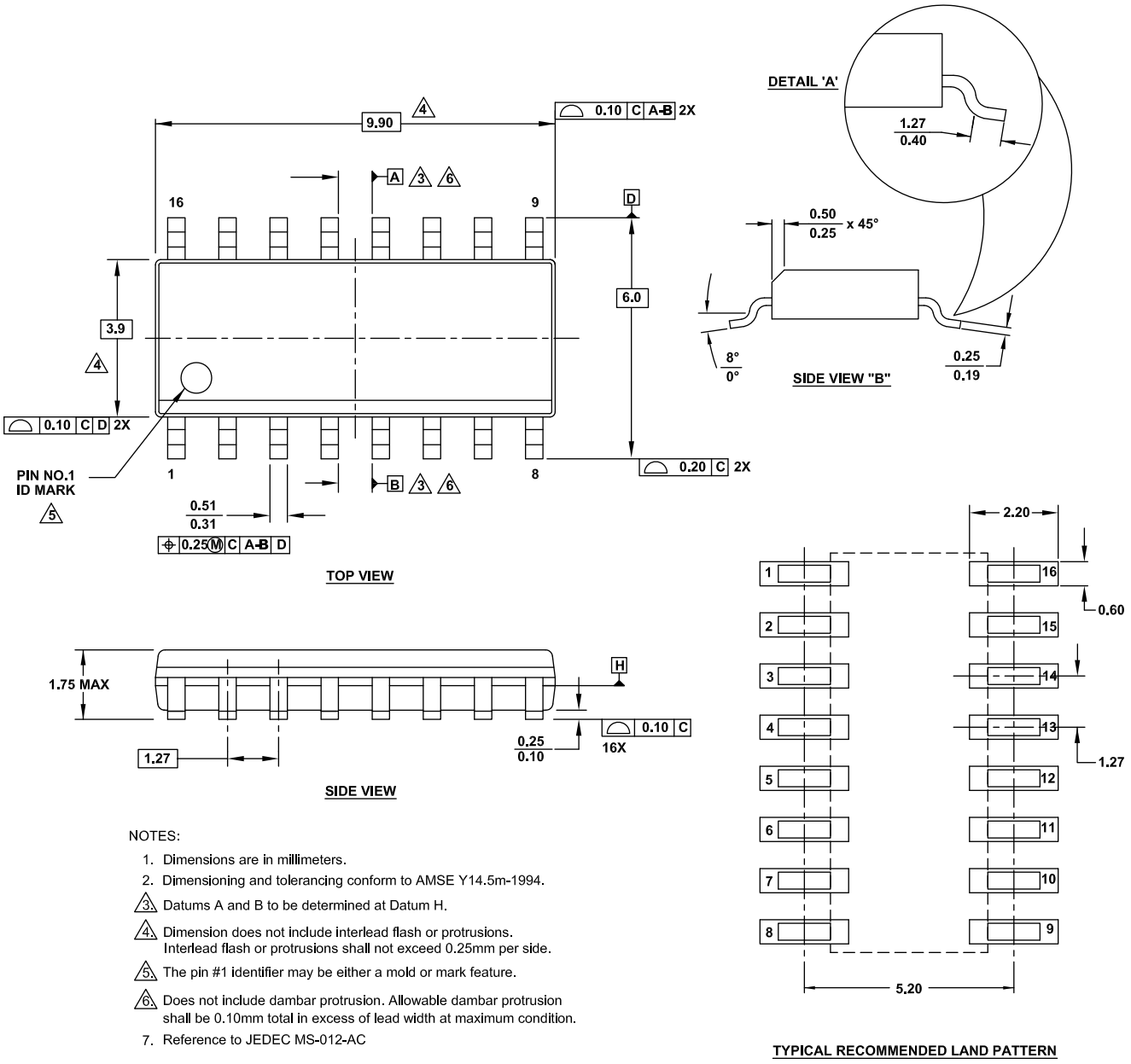
E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE (PDIP)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

M16.15 (JEDEC MS-012-AC ISSUE C)
16 Lead Narrow Body Small Outline Plastic Package
Rev 2, 11/17

For the most recent package outline drawing, see M16.15.

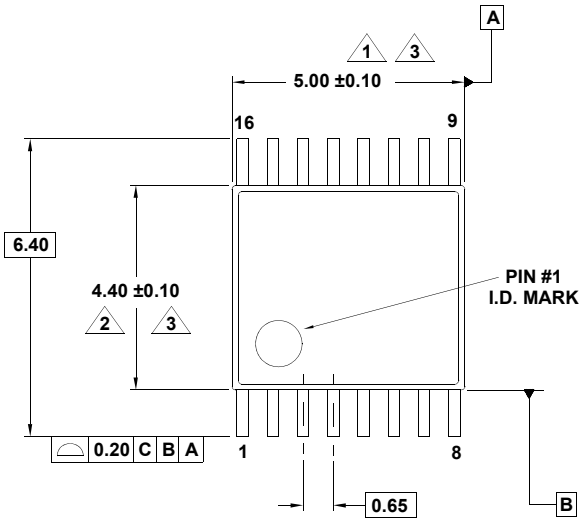


NOTES:

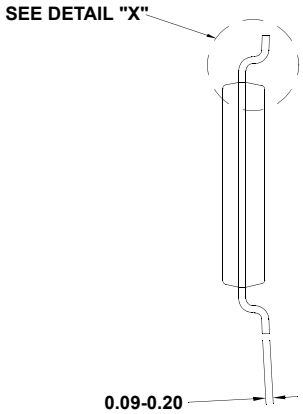
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AC

M16.173
16 Lead Thin Shrink Small Outline Package (TSSOP)
Rev 2, 5/10

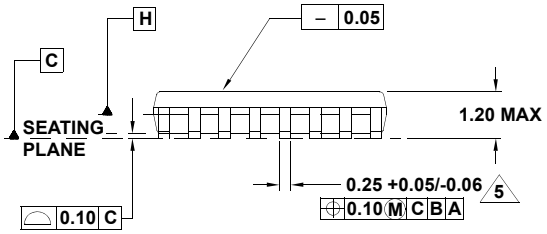
For the most recent package outline drawing, see M16.173.



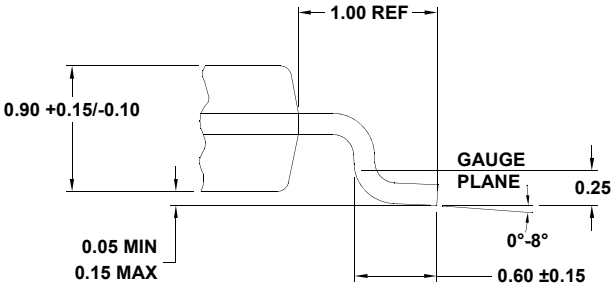
TOP VIEW



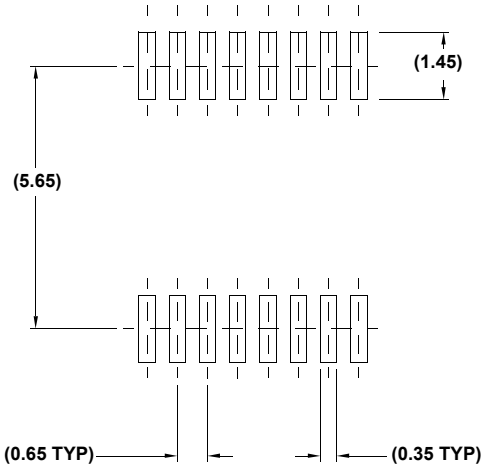
END VIEW



SIDE VIEW



DETAIL "X"

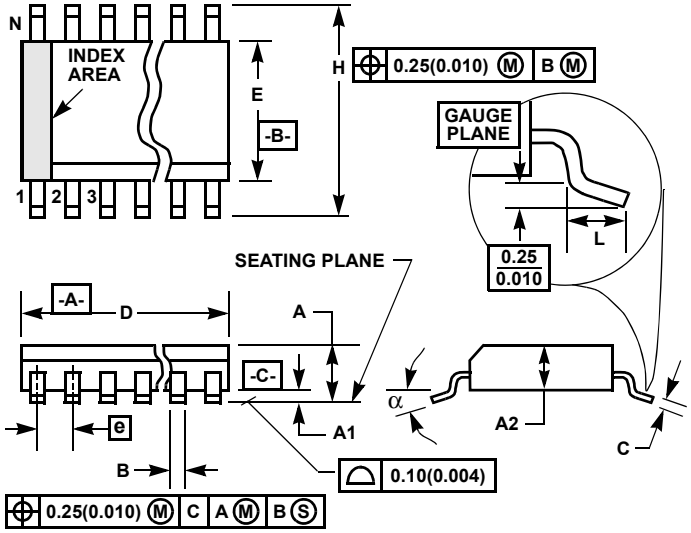


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

For the most recent package outline drawing, see M16.209.



Notes:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.209 (JEDEC MO-150-AC ISSUE B)

16 Lead Shrink Small Outline Plastic Package (SSOP)

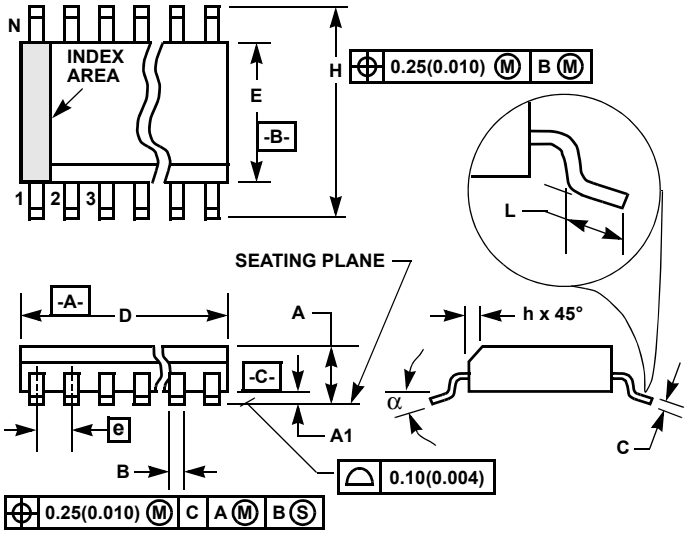
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.233	0.255	5.90	6.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 3 6/05

For the most recent package outline drawing, see M16.3.

M16.3 (JEDEC MS-013-AA ISSUE C)

16 Lead Wide Body Small Outline Plastic Package (SOIC)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

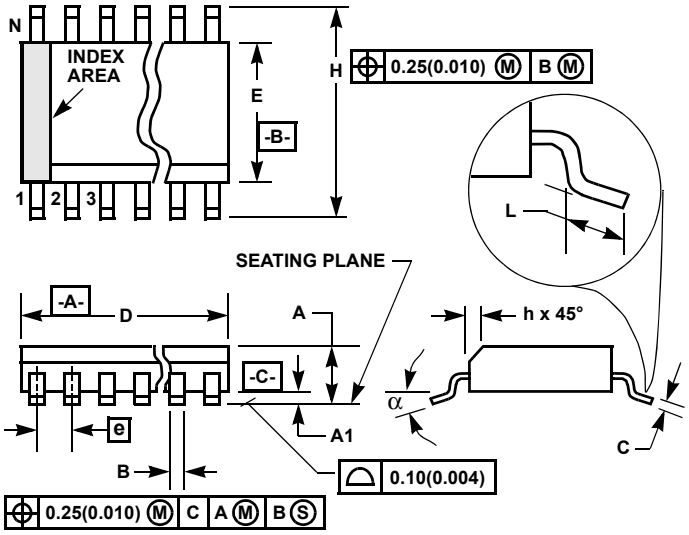
Notes:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

For the most recent package outline drawing, see M18.3.

M18.3 (JEDEC MS-013-AB ISSUE C)

18 Lead Wide Body Small Outline Plastic Package (SOIC)



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4469	0.4625	11.35	11.75	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	18		18		7
α	0°	8°	0°	8°	-

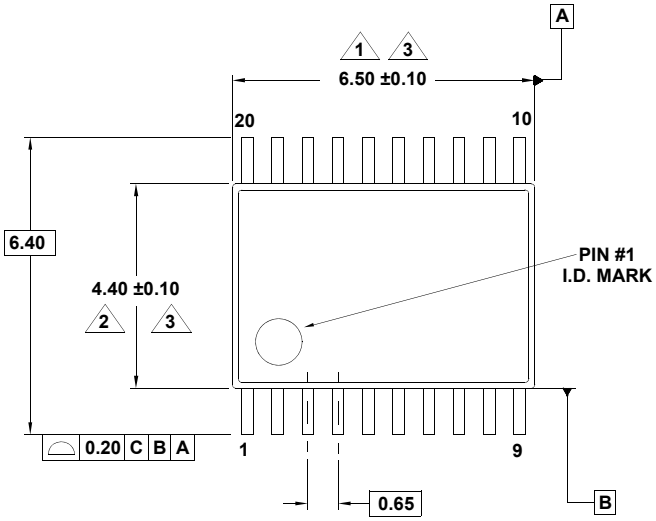
Rev. 1 6/05

Notes:

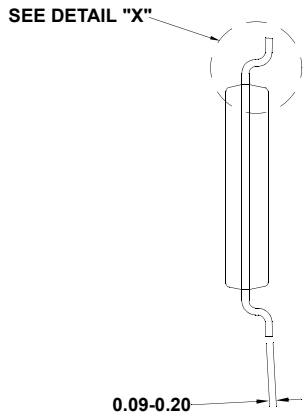
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M20.173
20 Lead Thin Shrink Small Outline Package (TSSOP)
Rev 2, 5/10

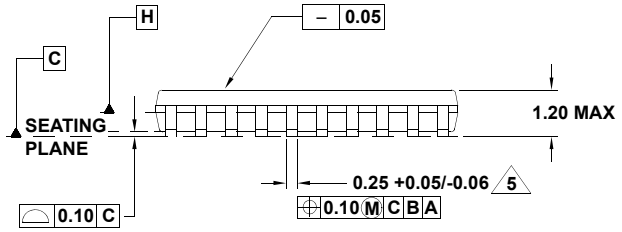
For the most recent package outline drawing, see M20.173.



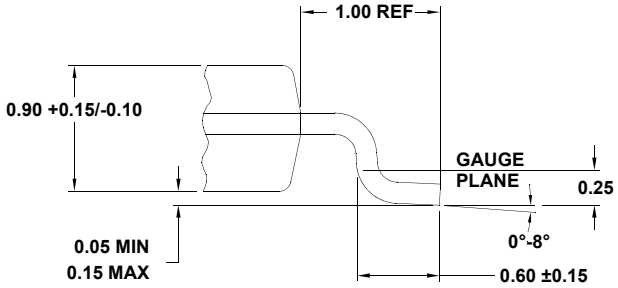
TOP VIEW



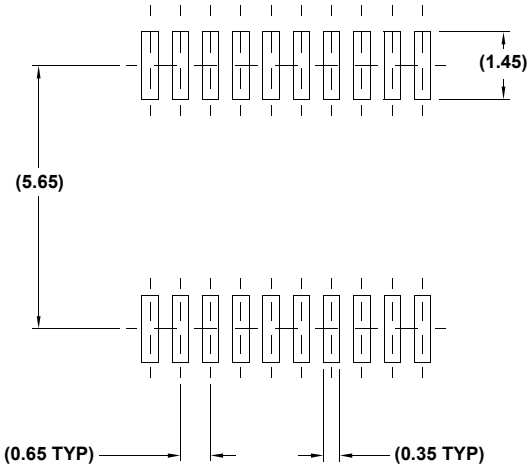
END VIEW



SIDE VIEW



DETAIL "X"



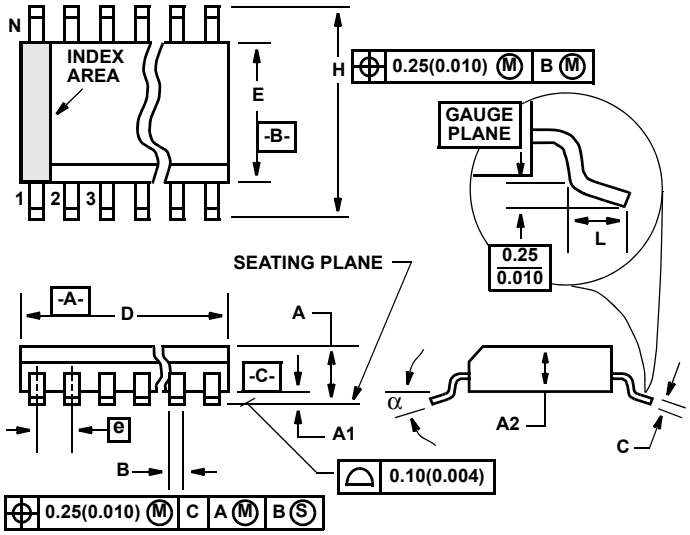
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

For the most recent package outline drawing, see M20.209.

M20.209 (JEDEC MO-150-AE ISSUE B)
20 Lead Shrink Small Outline Plastic Package (SSOP)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.068	0.078	1.73	1.99	
A1	0.002	0.008’	0.05	0.21	
A2	0.066	0.070’	1.68	1.78	
B	0.010’	0.015	0.25	0.38	9
C	0.004	0.008	0.09	0.20’	
D	0.278	0.289	7.07	7.33	3
E	0.205	0.212	5.20’	5.38	4
e	0.026 BSC		0.65 BSC		
H	0.301	0.311	7.65	7.90’	
L	0.025	0.037	0.63	0.95	6
N	20		20		7
α	0 deg.	8 deg.	0 deg.	8 deg.	

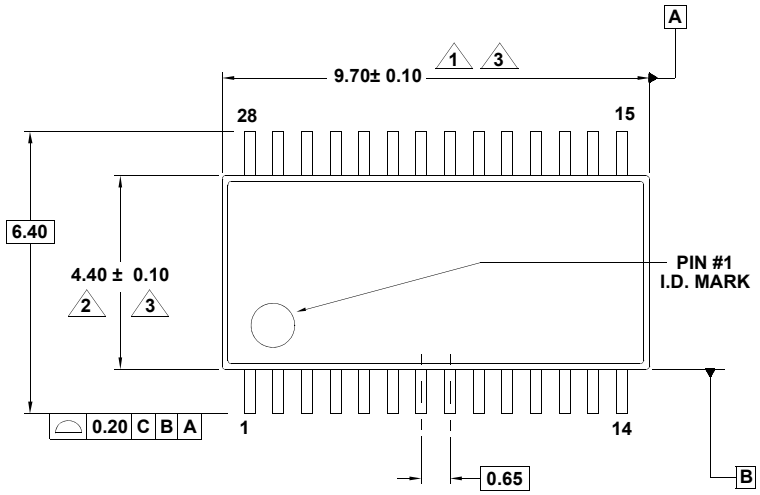
Rev. 3 11/02

Notes:

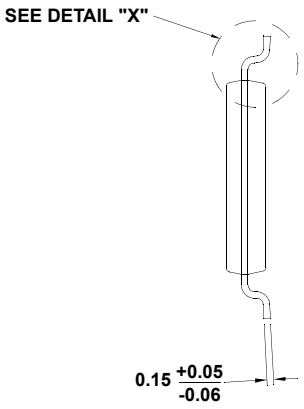
1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.173
28 Lead Thin Shrink Small Outline Package (TSSOP)
Rev 1, 5/10

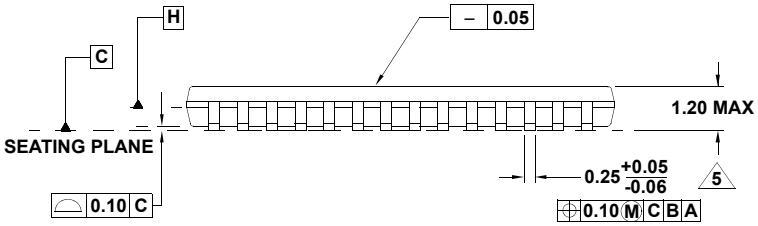
For the most recent package outline drawing, see M28.173.



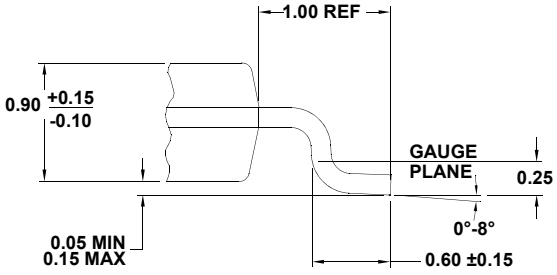
TOP VIEW



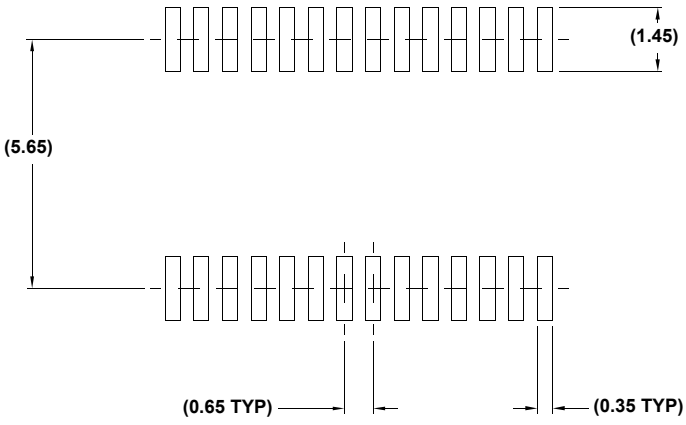
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

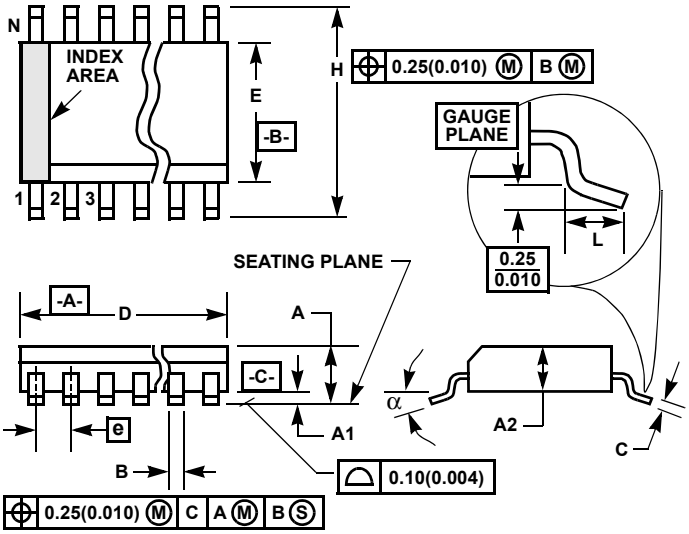
NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

For the most recent package outline drawing, see M28.209.

M28.209 (JEDEC MO-150-AH ISSUE B)

28 Lead Shrink Small Outline Plastic Package (SSOP)



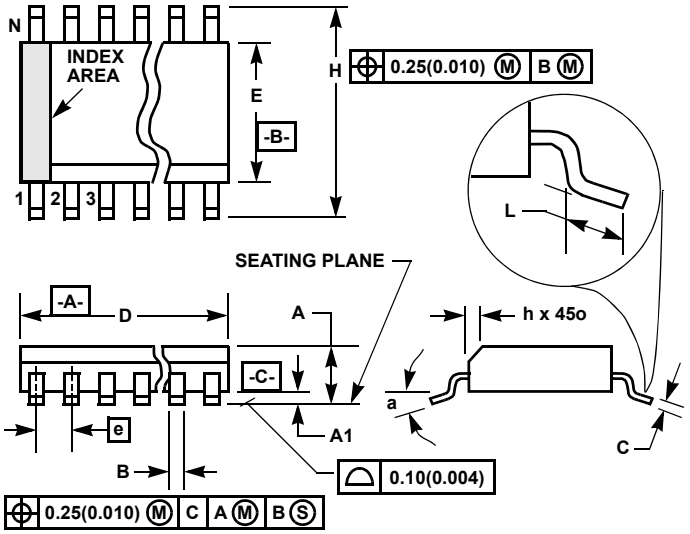
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.390	0.413	9.90	10.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 2 6/05

Notes:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

For the most recent package outline drawing, see M28.3.



M28.3 (JEDEC MS-013-AE ISSUE C)

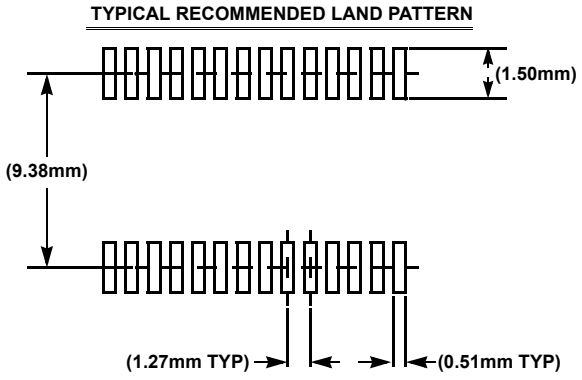
28 Lead Wide Body Small Outline Plastic Package (SOIC)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0º	8º	0º	8º	-

Rev. 1, 1/13

Notes:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.



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