THE DATASHEET OF

ICS840021AGLFT

FEMTOCLOCK™ CRYSTAL-TO-LVCMOS/LVTTL CLOCK GENERATOR

ICS840021

General Description

The ICS840021 is a Gigabit Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from IDT. The ICS840021 uses a 25MHz crystal to synthesize 125MHz. The ICS840021 has excellent phase jitter performance, over the 1.875MHz – 20MHz integration range. The ICS840021 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

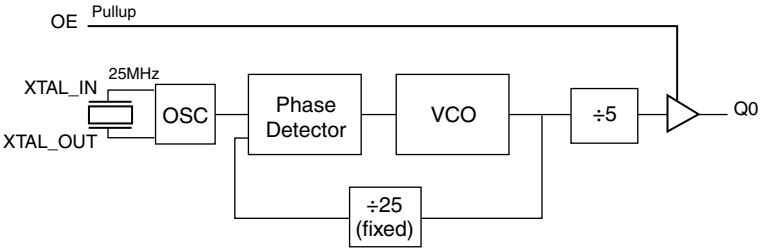
Features

- One LVCMOS/LVTTL output, 7Ω output impedance
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- Output frequency: 125MHz
- VCO range: 560MHz to 680MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.34ps (typical) 3.3V
- RMS phase noise at 125MHz (typical)
- Phase noise:

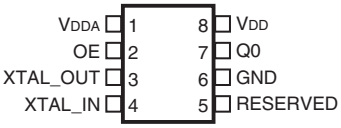
Offset	Noise Power
100Hz	-96.9 dBc/Hz
1kHz	-122.2 dBc/Hz
10kHz	-131.1 dBc/Hz
100Hz	-129.5 dBc/Hz

- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS840021

8-Lead TSSOP

4.40mm x 3.0mm x 0.925mm package body

G Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	OE	Input	Pullup	Output enable pin. When HIGH, Q0 output is enabled. When LOW, forces Q0 to high-impedance state. LVCMOS/LVTTL interface levels.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	Reserved	Reserved		Reserve pin.
6	GND	Power		Power supply ground.
7	Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels. 7Ω output impedance.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 1, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD} = 3.465V		24		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance		5	7	12	Ω

Function Table

Table 3. Control Function Table

Control Input	Output
OE	**Q0**
0	High-Impedance
1	Active

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				75	mA
I_{DDA}	Analog Supply Current				15	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	V_{DD} =3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output High Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit" diagram.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

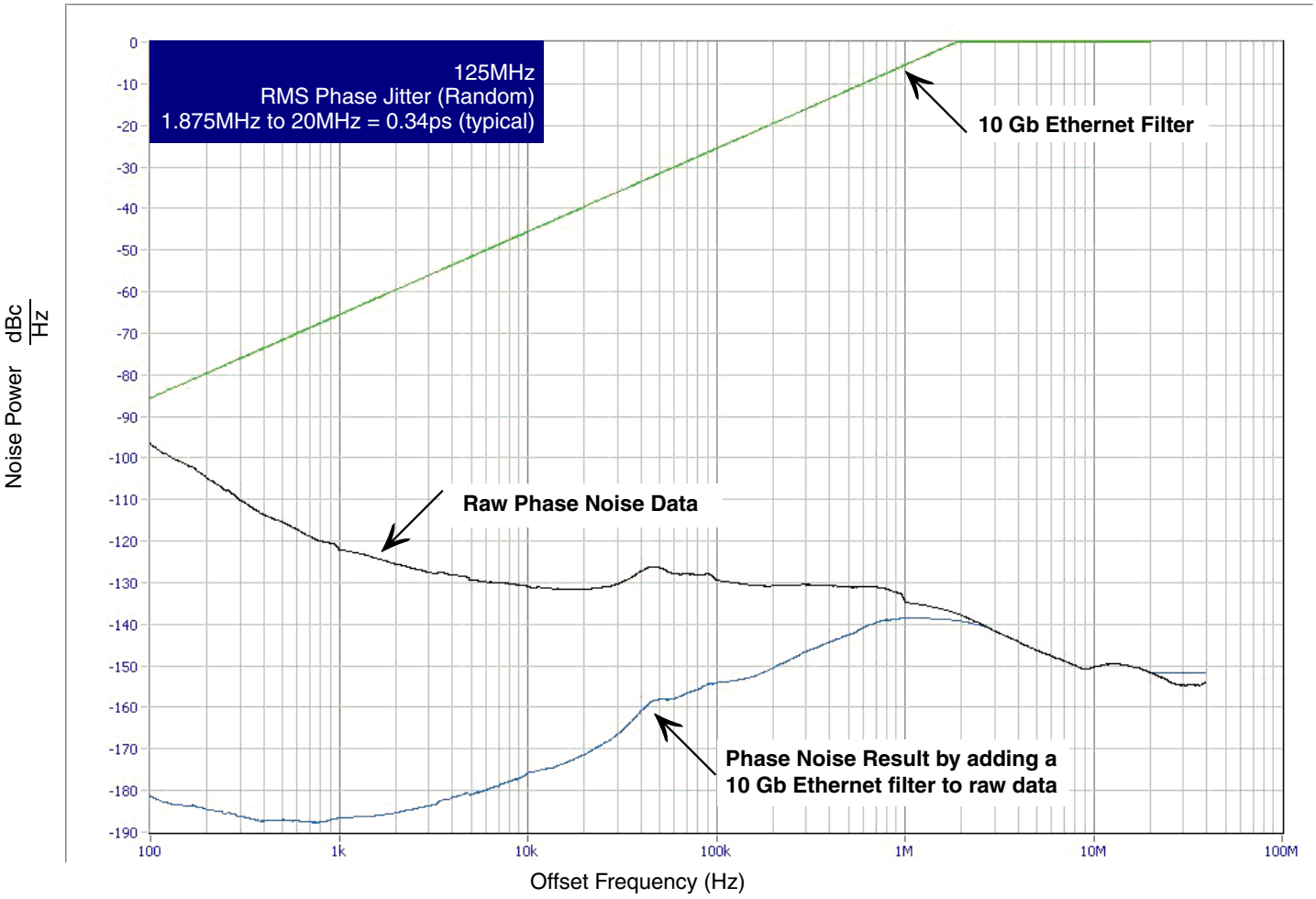
AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

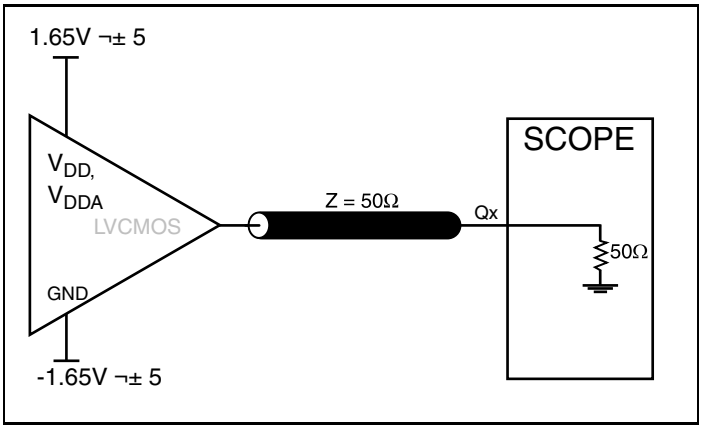
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			125		MHz
$t_{jit}(Ø)$	RMS Phase Jitter, Random; NOTE 1	Integration Range: 1.875MHz – 20MHz		0.34		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		550	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Please refer to Phase Noise Plots.

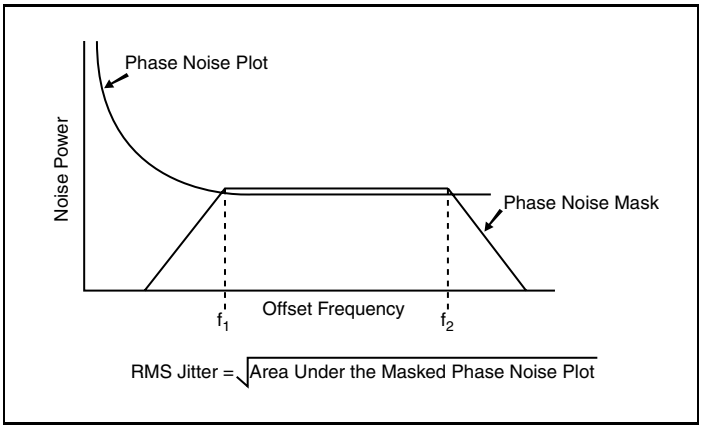
Typical Phase Noise at 125MHz



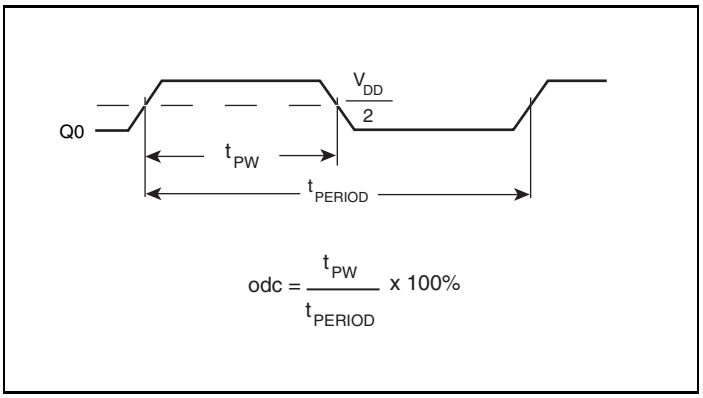
Parameter Measurement Information



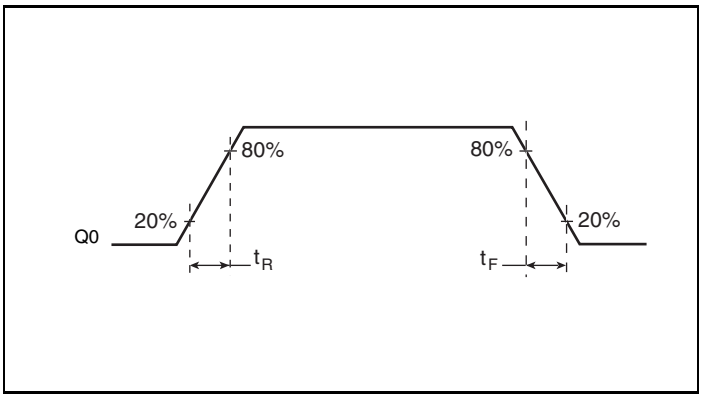
3.3V Output Load AC Test Circuit



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS840021provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

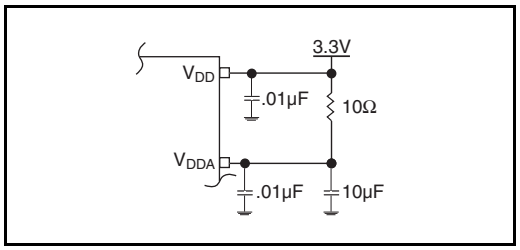


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS840021 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

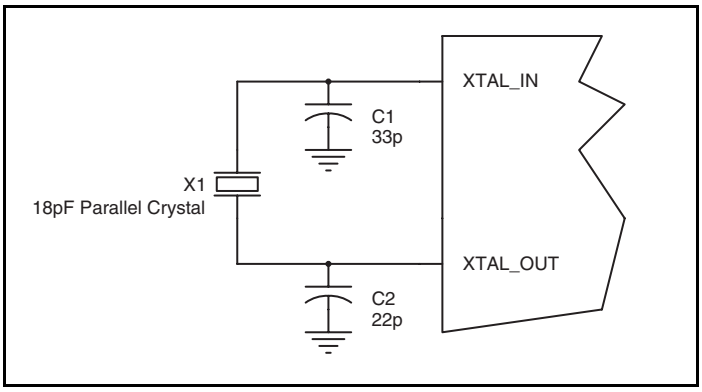


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

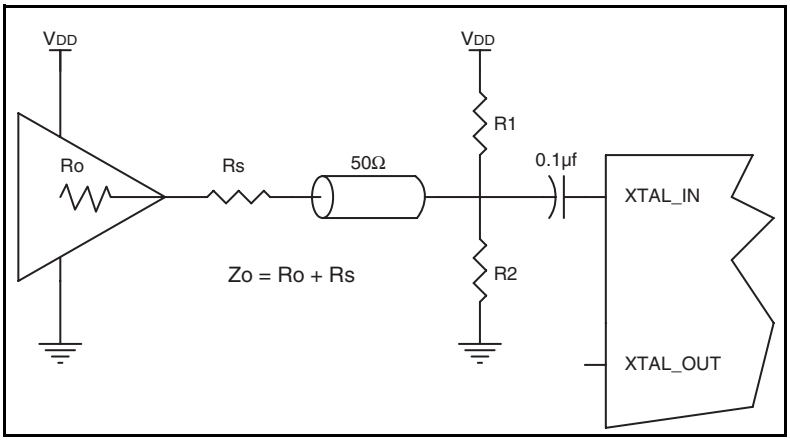


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Application Schematic

Figure 4A shows a schematic example of the ICS840021. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18pF parallel resonant 25MHz crystal is used for generating 125MHz output frequency. The C1 = 27pF and C2 = 33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.

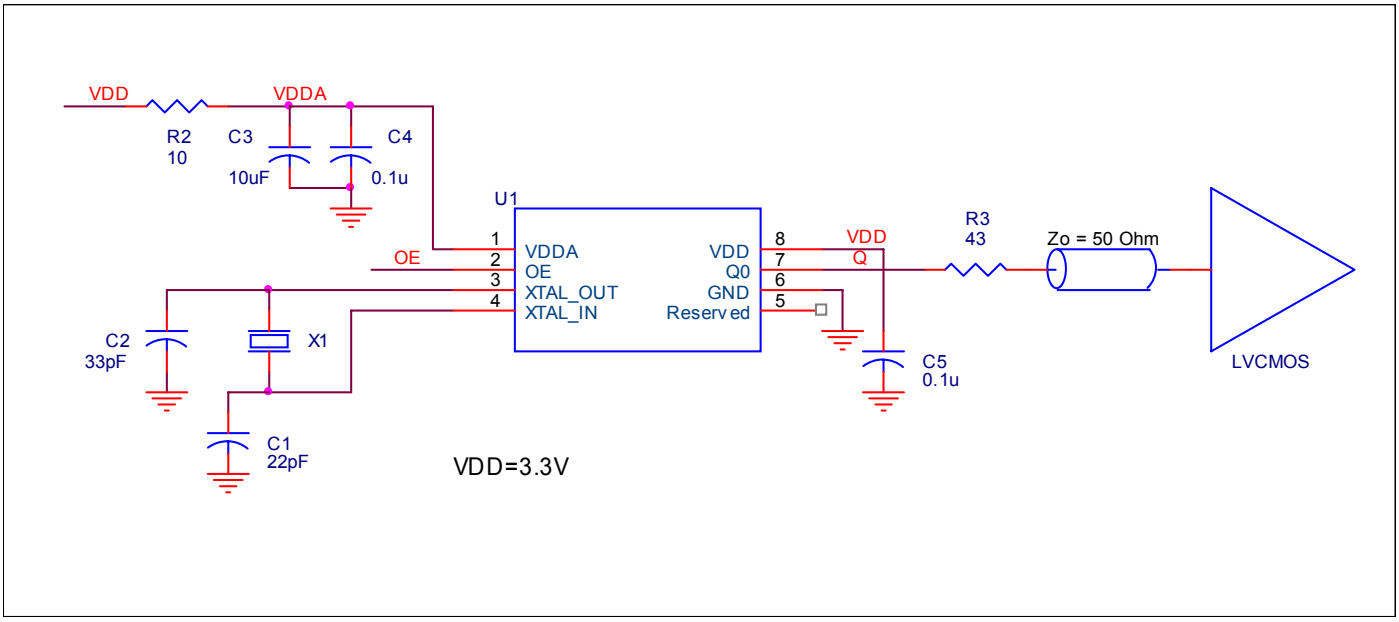


Figure 4A. ICS840021 Schematic Example

PC Board Layout Example

Figure 4B shows an example of ICS840021 P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the *Table 7.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

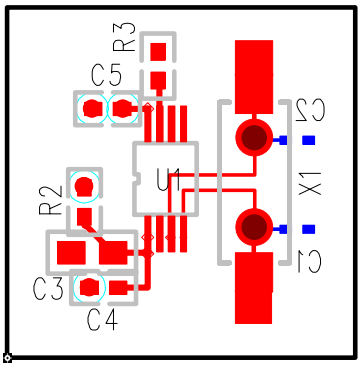


Figure 4B. ICS840021 PC Board Layout Example

Table 7. Footprint Table

Reference	Size
C1, C2	0402
C3	0805
C4, C5	0603
R2, R3	0603

NOTE: Table 7, lists component sizes shown in this layout example.

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

Transistor Count

The transistor count for ICS840021 is: 1961

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

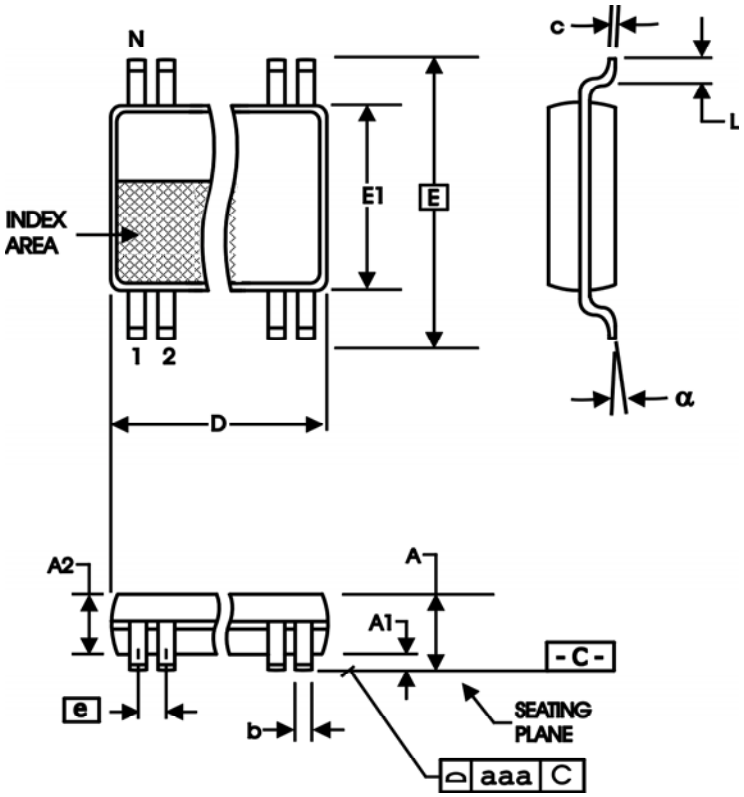


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840021AG	021AG	8 Lead TSSOP	Tube	0°C to 70°C
840021AGT	021AG	8 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
840021AGLF	021AL	“Lead-Free” 8 Lead TSSOP	Tube	0°C to 70°C
840021AGLFT	021AL	“Lead-Free” 8 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T10	10	Ordering Information Table - correct count from 154 to 100.	10/14/04
A	T8	3 8	Absolute Maximum Ratings - corrected Package Thermal Impedance air flow. Corrected air flow in table.	11/30/04
A	T10	1 10	Features section - added Lead-free bullet. Ordering Information Table - added lead-free part number and marking.	10/7/05
A		8	Added *LVCMOS to XTAL Interface* section. Changed formatting throughout data sheet.	1/10/09
B	T1	1 2	Pin Assignment - changed pin 5 from nc to Reserved. Pin Description Table - changed pin 5 from nc to Reserved.	4/15/09

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