



**THE DATASHEET OF
ICS8725AY01L**





GENERAL DESCRIPTION

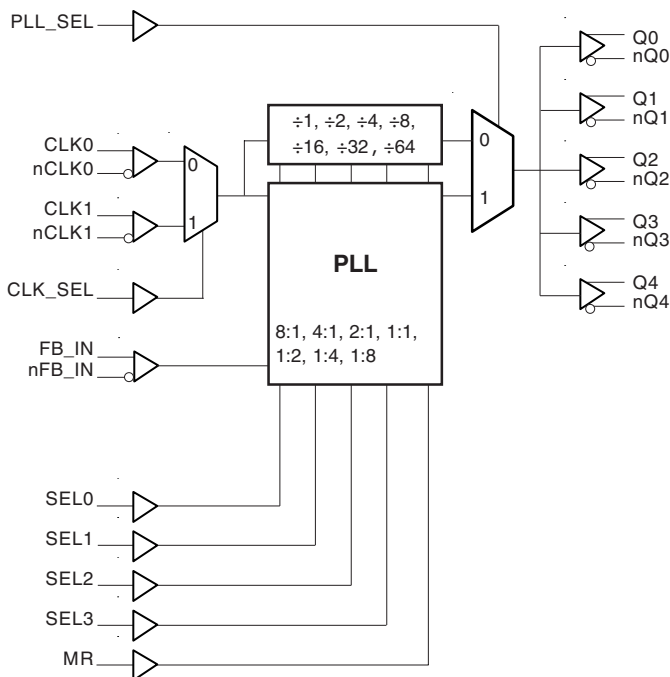


The ICS8725-01 is a highly versatile 1:5 Differential-to-HSTL clock generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8725-01 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 700MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

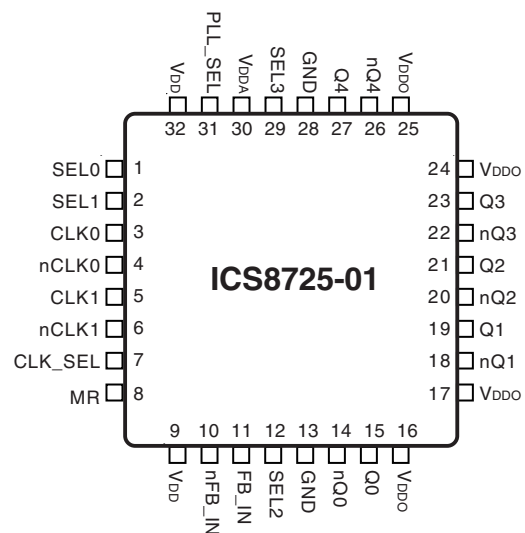
FEATURES

- Five differential HSTL outputs
- Selectable differential CLKx, nCLKx input pairs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, HSTL, SSTL, HCSL
- Output frequency range: 31.25MHz to 700MHz
- Input frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Static phase offset: ±100ps
- Cycle-to-cycle jitter: 25ps
- Output skew: 25ps
- 3.3V core, 1.8V output operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View



TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|----------------|------------------------|--------|----------|---|
| 1, 2, 12, 29 | SEL0, SEL1, SEL2, SEL3 | Input | Pulldown | Determines output divider values in Table 3. LVCMOS/LVTTL interface levels. |
| 3 | CLK0 | Input | Pulldown | Non-inverting differential clock input. |
| 4 | nCLK0 | Input | Pullup | Inverting differential clock input. |
| 5 | CLK1 | Input | Pulldown | Non-inverting differential clock input. |
| 6 | nCLK1 | Input | Pullup | Inverting differential clock input. |
| 7 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects CLK1, nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS/LVTTL interface levels. |
| 8 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 9, 32 | V _{DD} | Power | | Core supply pins. |
| 10 | nFB_IN | Input | Pullup | Feedback input to phase detector for regenerating clocks with "zero delay". |
| 11 | FB_IN | Input | Pulldown | Feedback input to phase detector for regenerating clocks with "zero delay". |
| 13, 28 | GND | Power | | Power supply ground. |
| 14, 15 | nQ0, Q0 | Output | | Differential output pair. HSTL interface levels. |
| 16, 17, 24, 25 | V _{DDO} | Power | | Output supply pins. |
| 18, 19 | nQ1, Q1 | Output | | Differential output pair. HSTL interface levels. |
| 20, 21 | nQ2, Q2 | Output | | Differential output pair. HSTL interface levels. |
| 22, 23 | nQ3, Q3 | Output | | Differential output pair. HSTL interface levels. |
| 26, 27 | nQ4, Q4 | Output | | Differential output pair. HSTL interface levels. |
| 30 | V _{DDA} | Power | | Analog supply pin. |
| 31 | PLL_SEL | Input | Pullup | Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |



TABLE 3A. CONTROL INPUT FUNCTION TABLE

| Inputs | | | | | Outputs PLL_SEL = 1 PLL Enable Mode |
|--------|------|------|------|----------------------------------|---|
| SEL3 | SEL2 | SEL1 | SEL0 | Reference Frequency Range (MHz)* | Q0:Q4, nQ0:nQ4 |
| 0 | 0 | 0 | 0 | 250 - 700 | ÷ 1 |
| 0 | 0 | 0 | 1 | 125 - 350 | ÷ 1 |
| 0 | 0 | 1 | 0 | 62.5 - 175 | ÷ 1 |
| 0 | 0 | 1 | 1 | 31.25 - 87.5 | ÷ 1 |
| 0 | 1 | 0 | 0 | 250 - 700 | ÷ 2 |
| 0 | 1 | 0 | 1 | 125 - 350 | ÷ 2 |
| 0 | 1 | 1 | 0 | 62.5 - 175 | ÷ 2 |
| 0 | 1 | 1 | 1 | 250 - 700 | ÷ 4 |
| 1 | 0 | 0 | 0 | 125 - 350 | ÷ 4 |
| 1 | 0 | 0 | 1 | 250 - 700 | ÷ 8 |
| 1 | 0 | 1 | 0 | 125 - 350 | x 2 |
| 1 | 0 | 1 | 1 | 62.5 - 175 | x 2 |
| 1 | 1 | 0 | 0 | 31.25 - 87.5 | x 2 |
| 1 | 1 | 0 | 1 | 62.5 - 175 | x 4 |
| 1 | 1 | 1 | 0 | 31.25 - 87.5 | x 4 |
| 1 | 1 | 1 | 1 | 31.25 - 87.5 | x 8 |

*NOTE: VCO frequency range for all configurations above is 250MHz to 700MHz.

TABLE 3B. PLL BYPASS FUNCTION TABLE

| Inputs | | | | | Outputs PLL_SEL = 0 PLL Bypass Mode |
|--------|------|------|------|----------------|---|
| SEL3 | SEL2 | SEL1 | SEL0 | Q0:Q4, nQ0:nQ4 | |
| 0 | 0 | 0 | 0 | ÷ 4 | |
| 0 | 0 | 0 | 1 | ÷ 4 | |
| 0 | 0 | 1 | 0 | ÷ 4 | |
| 0 | 0 | 1 | 1 | ÷ 8 | |
| 0 | 1 | 0 | 0 | ÷ 8 | |
| 0 | 1 | 0 | 1 | ÷ 8 | |
| 0 | 1 | 1 | 0 | ÷ 16 | |
| 0 | 1 | 1 | 1 | ÷ 16 | |
| 1 | 0 | 0 | 0 | ÷ 32 | |
| 1 | 0 | 0 | 1 | ÷ 64 | |
| 1 | 0 | 1 | 0 | ÷ 2 | |
| 1 | 0 | 1 | 1 | ÷ 2 | |
| 1 | 1 | 0 | 0 | ÷ 4 | |
| 1 | 1 | 0 | 1 | ÷ 1 | |
| 1 | 1 | 1 | 0 | ÷ 2 | |
| 1 | 1 | 1 | 1 | ÷ 1 | |



ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_O | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | 47.9°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDO} | Output Supply Voltage | | 1.6 | 1.8 | 2.0 | V |
| I_{DD} | Power Supply Current | | | | 120 | mA |
| I_{DDA} | Analog Supply Current | | | | 15 | mA |
| I_{DDO} | Output Supply Current | No Load | | 0 | | mA |

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|-------------------------------------|---|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | CLK_SEL, MR, SEL0, SEL1, SEL2, SEL3 | $V_{DD} = V_{IN} = 3.465V$ $V_{DDO} = 2V$ | | 150 | μA |
| | | PLL_SEL | $V_{DD} = V_{IN} = 3.465V$ $V_{DDO} = 2V$ | | 5 | μA |
| I_{IL} | Input Low Current | CLK_SEL, MR, SEL0, SEL1, SEL2, SEL3 | $V_{DD} = 3.465V$, $V_{DDO} = 2V$, $V_{IN} = 0V$ | -5 | | μA |
| | | PLL_SEL | $V_{DD} = 3.465V$, $V_{DDO} = 2V$, $V_{IN} = 0V$ | -150 | | μA |

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------|----------------------|-----------------------------------|---------|-----------------|---------|
| I_{IH} | Input High Current | CLK0, CLK1, FB_IN | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| | | nCLK0, nCLK1, nFB_IN | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| I_{IL} | Input Low Current | CLK0, CLK1, FB_IN | $V_{DD} = 3.465V$, $V_{IN} = 0V$ | -5 | | μA |
| | | nCLK0, nCLK1, nFB_IN | $V_{DD} = 3.465V$, $V_{IN} = 0V$ | -150 | | μA |
| V_{PP} | Peak-to-Peak Input Voltage | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | 0.5 | | $V_{DD} - 0.85$ | V |

NOTE 1: For single ended applications, the maximum input voltage for CLKx, nCLKx is $V_{DD} + 0.3V$.

NOTE 2: Common mode voltage is defined as V_{IH} .



TABLE 4D. HSTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|---------|---------|---------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | 1 | | 1.4 | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | 0 | | 0.4 | V |
| V_{OX} | Output Crossover Voltage; NOTE 2 | | 40 | | 60 | % |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.1 | V |

NOTE 1: Outputs terminated with 50Ω to ground.

NOTE 2: Defined with respect to output voltage swing at a given condition.

TABLE 5. INPUT FREQUENCY CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units | |
|----------|-----------------|-----------------------------|-------------|---------|---------|-------|-----|
| f_{IN} | Input Frequency | CLK0, nCLK0, CLK1, nCLK1 | PLL_SEL = 1 | 31.25 | | 700 | MHz |
| | | | PLL_SEL = 0 | | | 700 | MHz |

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|----------------------------------|---------------------------------|---------------|----------|---------------|-------|
| f_{MAX} | Output Frequency | | | | 700 | MHz |
| t_{PD} | Propagation Delay; NOTE 1 | PLL_SEL = 0V $f \leq 700MHz$ | 3.4 | 3.9 | 4.4 | ns |
| $t(\emptyset)$ | Static Phase Offset; NOTE 2, 5 | PLL_SEL = 3.3V | -100 | | 100 | ps |
| $t_{sk(o)}$ | Output Skew; NOTE 3, 5 | | | | 25 | ps |
| $f_{jit(cc)}$ | Cycle-to-Cycle Jitter; NOTE 5, 6 | | | | 25 | ps |
| $f_{jit(\emptyset)}$ | Phase Jitter; NOTE 4, 5, 6 | | | | ± 50 | ps |
| t_L | PLL Lock Time | | | | 1 | ms |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% @ 50MHz | 300 | | 700 | ps |
| t_{PW} | Output Pulse Width | | tcycle/2 - 85 | tcycle/2 | tcycle/2 + 85 | ps |

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

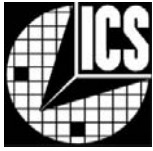
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at output differential cross points.

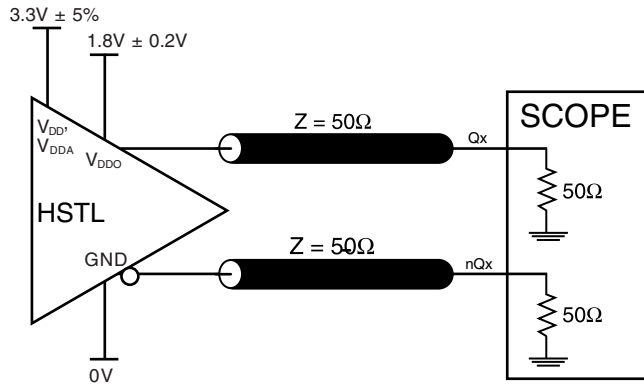
NOTE 4: Phase jitter is dependent on the input source used.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

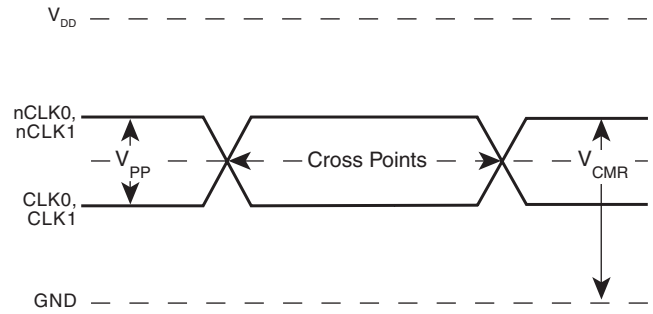
NOTE 6: Characterized at VCO frequency of 622MHz.



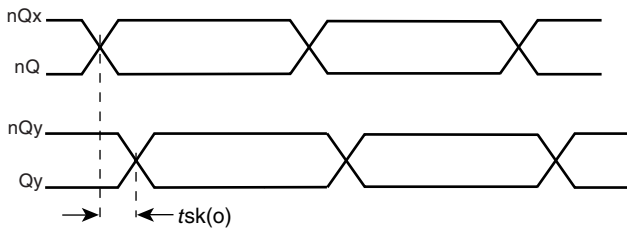
PARAMETER MEASUREMENT INFORMATION



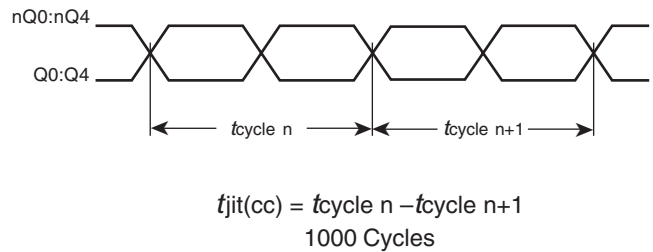
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



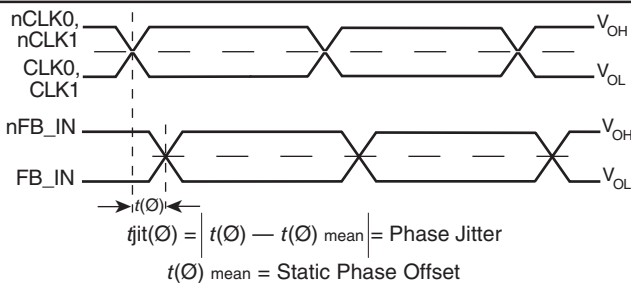
DIFFERENTIAL INPUT LEVEL



OUTPUT SKEW

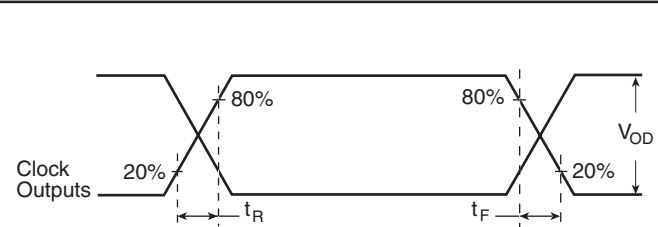


CYCLE-TO-CYCLE JITTER

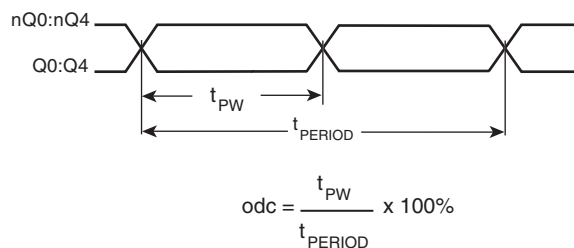


(where $t(\varnothing)$ is any random sample, and $t(\varnothing)_{mean}$ is the average of the sampled cycles measured on controlled edges)

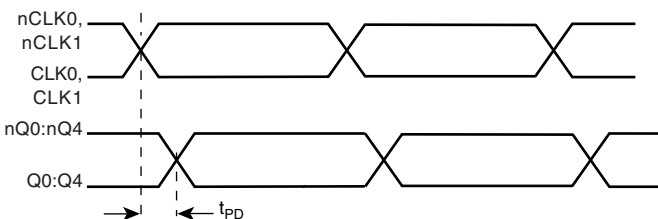
PHASE JITTER AND STATIC PHASE OFFSET



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



PROPAGATION DELAY



APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8725-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{DDA} pin.

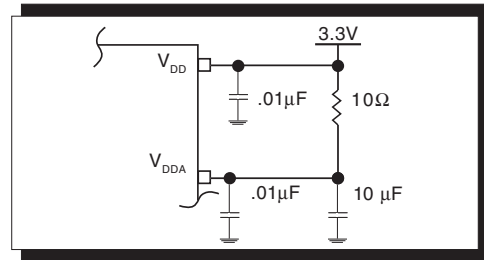


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors $R1$, $R2$ and $C1$. This bias circuit should be located as close as possible to the input pin. The ratio

of $R1$ and $R2$ might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3\text{V}$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

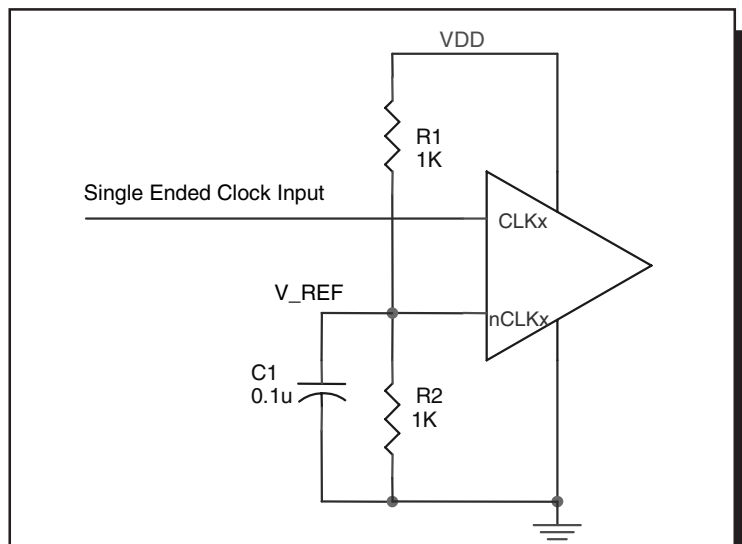


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT



DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, HSTL, SSTL, HCSSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for ICS HiPerClockS HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.

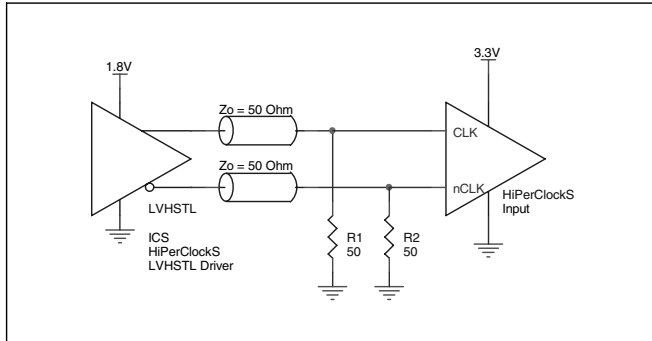


FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER

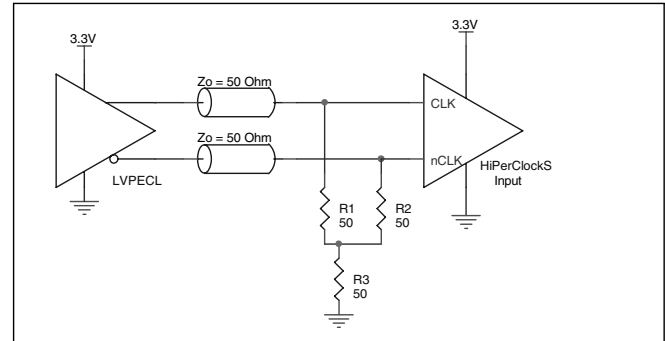


FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

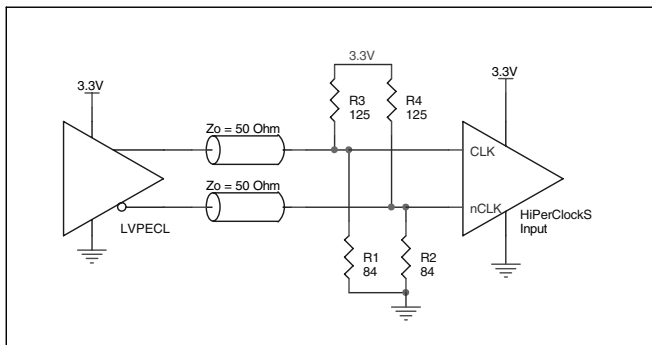


FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

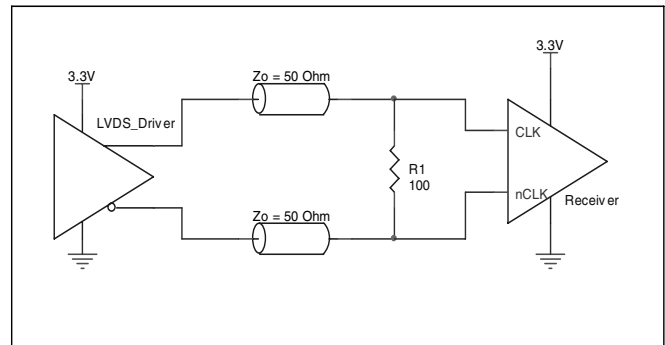


FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUT:

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from CLK to ground.

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

OUTPUTS:

HSTL OUTPUT

All unused HSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.



LAYOUT GUIDELINE

The schematic of the ICS8725-01 layout example is shown in *Figure 4A*. The ICS8725-01 recommended PCB board layout for this example is shown in *Figure 4B*. This layout example is used as a general guideline. The layout in the actual system will

depend on the selected component types, the density of the components, the density of the traces, and the stacking of the P.C. board.

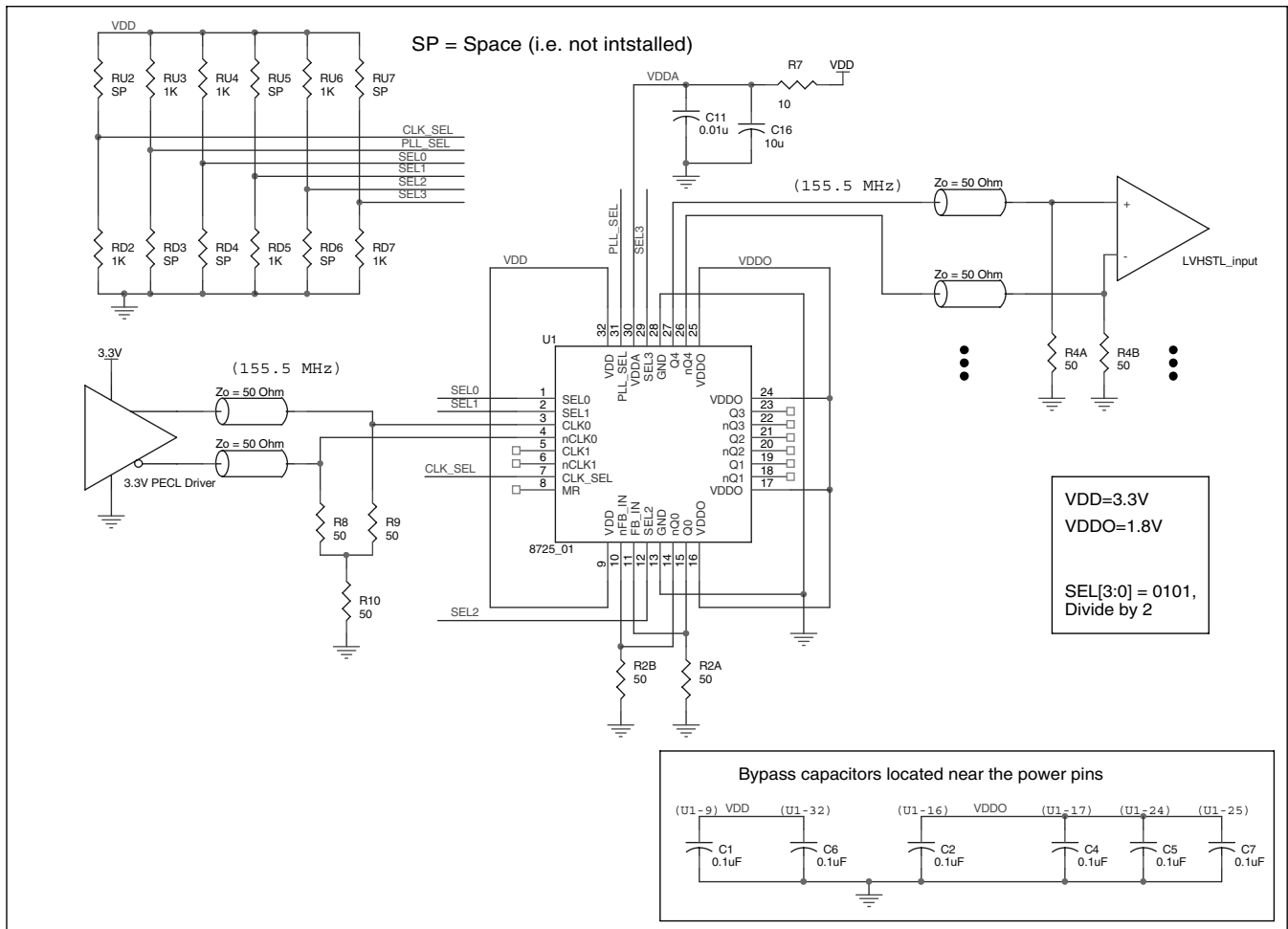


FIGURE 4A. ICS8725-01 HSTL ZERO DELAY BUFFER SCHEMATIC EXAMPLE



The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

POWER AND GROUNDING

Place the decoupling capacitors C1, C6, C2, C4, and C5, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the

trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

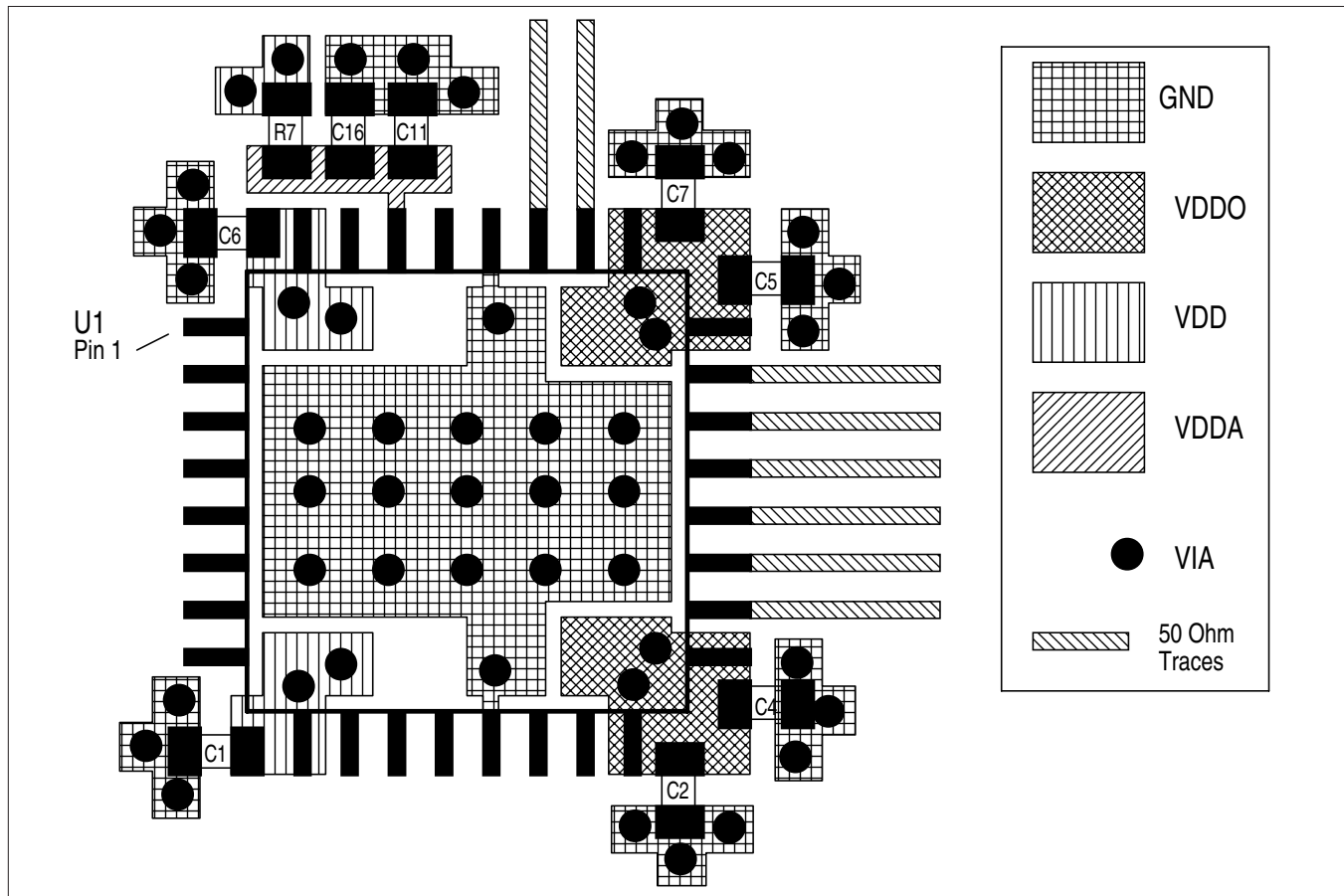


FIGURE 4B. PCB BOARD LAYOUT FOR ICS8725-01



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8725-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8725-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (120mA + 15mA) = 468mW$
- Power (outputs)_{MAX} = **32.8mW/Loaded Output pair**
If all outputs are loaded, the total power is $5 * 32.8mW = 164mW$

Total Power_{MAX} (3.465V, with all outputs switching) = $468mW + 164mW = 632mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 7 below. Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.632\text{W} * 42.1^\circ\text{C/W} = 96.6^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32-pin LQFP, Forced Convection

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

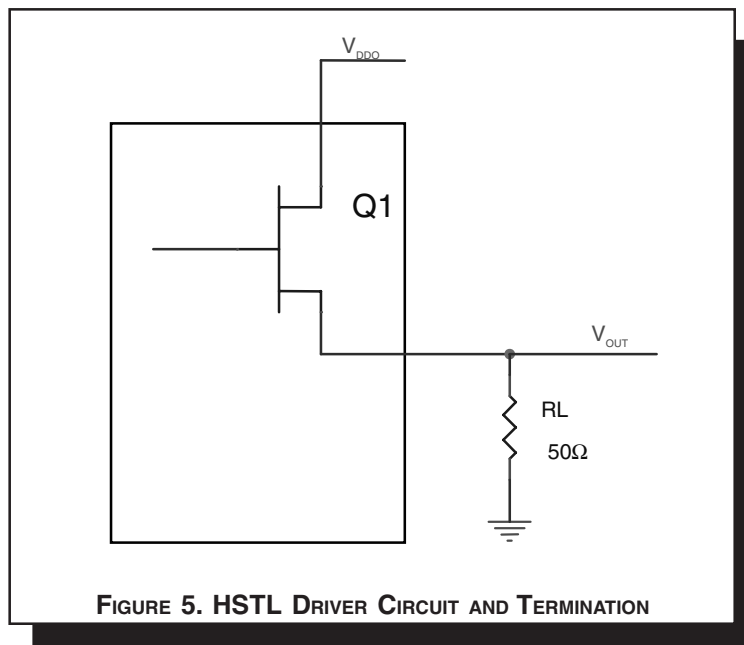
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 5*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$$Pd_H = (V_{OH_MIN} / R_L) * (V_{DDO_MAX} - V_{OH_MIN})$$

$$Pd_L = (V_{OL_MAX} / R_L) * (V_{DDO_MAX} - V_{OL_MAX})$$

$$Pd_H = (1V/50\Omega) * (2V - 1V) = \mathbf{20mW}$$

$$Pd_L = (0.4V/50\Omega) * (2V - 0.4V) = \mathbf{12.8mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{32.8mW}$$



RELIABILITY INFORMATION

TABLE 8. θ_{JA} vs. AIR FLOW TABLE FOR 32 LEAD LQFP

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------|------------|------------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8725-01 is: 2969



PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

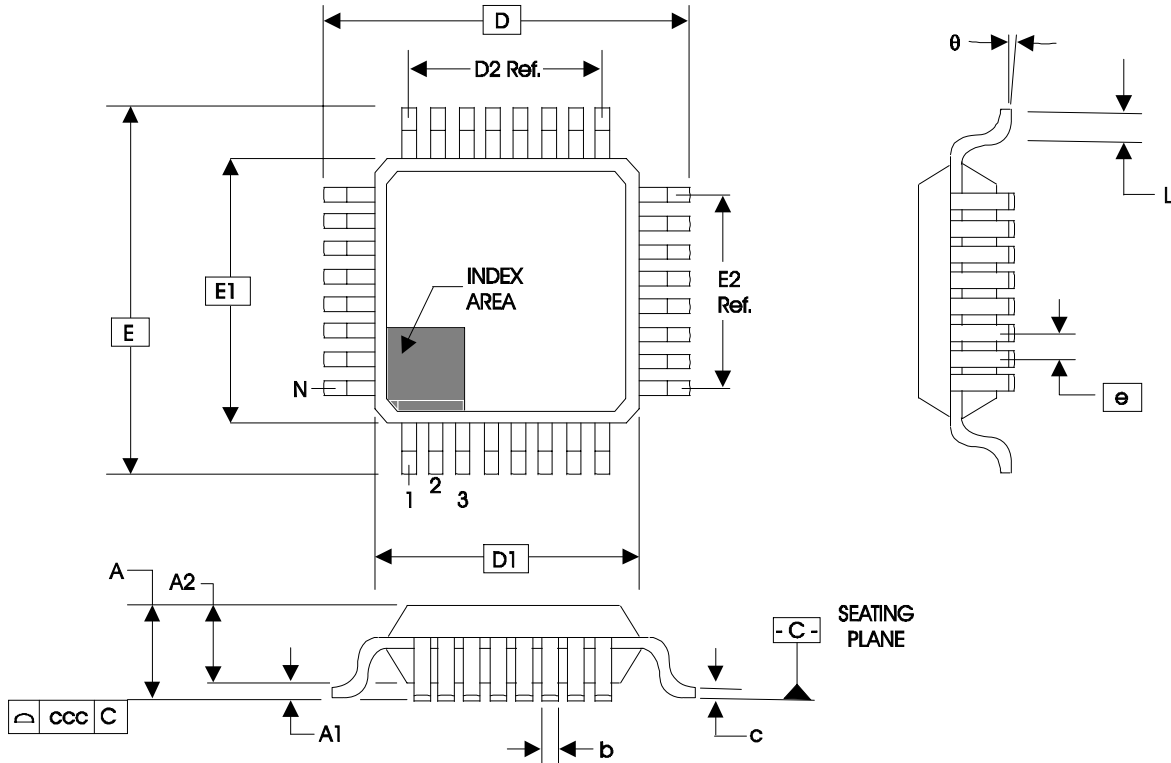


TABLE 9. PACKAGE DIMENSIONS

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | |
|--|------------|---------|---------|
| SYMBOL | BBA | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | 32 | | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | -- | 0.20 |
| D | 9.00 BASIC | | |
| D1 | 7.00 BASIC | | |
| D2 | 5.60 Ref. | | |
| E | 9.00 BASIC | | |
| E1 | 7.00 BASIC | | |
| E2 | 5.60 Ref. | | |
| e | 0.80 BASIC | | |
| L | 0.45 | 0.60 | 0.75 |
| theta | 0° | -- | 7° |
| ccc | -- | -- | 0.10 |

Reference Document: JEDEC Publication 95, MS-026



Integrated
Circuit
Systems, Inc.

ICS8725-01

1:5 DIFFERENTIAL-TO-HSTL ZERO DELAY CLOCK GENERATOR

TABLE 10. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|--------------------------|--------------------|-------------|
| ICS8725AY-01 | ICS8725AY-01 | 32 Lead LQFP | tray | 0°C to 70°C |
| ICS8725AY-01T | ICS8725AY-01 | 32 Lead LQFP | 1000 tape & reel | 0°C to 70°C |
| ICS8725AY-01LF | ICS8725AY01L | 32 Lead "Lead-Free" LQFP | tray | 0°C to 70°C |
| ICS8725AY-01LFT | ICS8725AY01L | 32 Lead "Lead-Free" LQFP | 1000 tape & reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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| REVISION HISTORY SHEET | | | | |
|------------------------|----------|-----------------------|---|----------|
| Rev | Table | Page | Description of Change | Date |
| A | 6 | 1 5 | Updated Block Diagram. Changed PLL Reference Zero Delay to Static Phase Offset. | 11/2/01 |
| A | 3A 6 | 3 5 | Added note at bottom of the table. Added Note 6. | 11/20/01 |
| A | 1 | 2 8 | Pin Description Table - revised MR description. Updated Output Rise/Fall Time Diagram. Format changes. | 8/22/02 |
| A | T1 T2 | 2 2 4 7 8 | Changed LVHSTL to HSTL throughout data sheet to conform with JEDEC terminology. Pin Description table - revised MR and V_{DD} descriptions. Pin Characteristics table - changed C_{IN} 4pF max. to 4pF typical. Absolute Maximum Ratings - updated Inputs ratings. Added Power Supply Filtering Techniques section. Added Differential Input Interface section. Updated format throughout data sheet. | 9/26/03 |
| B | T4D | 5 | HSTL table - changed V_{OX} minimum to 40% and maximum to 60%; added NOTE 2. | 11/11/04 |
| B | T10 | 1 15 | Features Section - add Lead-Free bullet. Ordering Information Table - added Lead-Free package and note. | 6/9/05 |
| B | | 8 11-12 | Added <i>Recommendations for Unused Input and Output Pins</i> . Corrected Power Considerations, Power Dissipation calculation. | 11/15/05 |

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