AAS33001

Precision Angle Sensor IC with Incremental and Motor Commutation Outputs and On-Chip Linearization

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC, for angular position, rotational speed, and direction measurement
  - Capable of sensing magnet rotational speeds targeting 12.5-bit effective resolution with 300 G field; higher effective resolution possible at higher field strengths
  - Circular vertical Hall (CVH) technology provides a single-channel sensor system, with air gap independence
- On-chip 32 segment linearization to improve angle accuracy
  - Reduces impact of magnet to sensor misalignment
  - Reduces impact of imperfect magnetization of target magnet
- ASIL-Compliant: ASIL B safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual
  - Single-die version designed to meet ASIL B requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the AAS33001 Safety Manual
  - Dual-die version designed to meet ASIL D requirements when integrated and used in conjunction with the appropriate system-level control, in the manner prescribed in the AAS33001 Safety Manual

A2 SiL ISO 26262 ASIL Compliant

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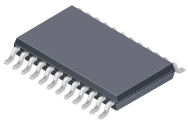
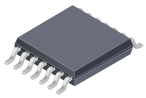
PACKAGES

24-pin eTSSOP (Suffix LP)



14-pin TSSOP (Suffix LE)



Not to scale

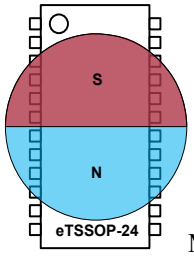
DESCRIPTION

The AAS33001 is a 360° angle sensor IC that provides contactless high-resolution angular position data based on magnetic circular vertical Hall (CVH) technology. It has a system-on-chip (SoC) architecture that includes: a CVH front end, digital signal processing to calculate the angular position data, and multiple output formats: serial protocol (SPI), pulse-width modulation (PWM), and either motor commutation (UVW) or encoder outputs (A, B, I). It also includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles, for flexible programming of calibration parameters. The AAS33001 is ideal for automotive applications requiring 0° to 360° angle measurements, such as electronic power steering (EPS), electronic power braking (EPB or IDB), transmission actuators, and brushless DC (BLDC) pumps.

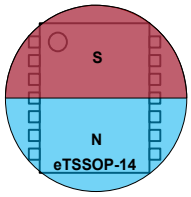
The AAS33001 includes on-chip 32 segment linearization. This can be used to calibrate out errors due to misalignment between the magnet and the sensor or imperfect magnetization of the target magnet (which can present itself as a misalignment of the magnet to the sensor).

The AAS33001 supports customer integration into safety-critical applications. This Allegro IC can support ASIL B fail-operational systems when properly integrated, though judgment of the achievement of safety is dependent on the customer's implementation and analyses.

The AAS33001 is available in a dual-die 24-pin eTSSOP and a single-die 14-pin TSSOP package. The packages are lead (Pb) free with 100% matte tin leadframe plating. The 1 mm thin package reduces the minimum air gap between the CVH transducer and the target magnet. The AAS33001 device is pin-compatible with the A1333 to enable easy migration.



Magnet oriented for 0° output



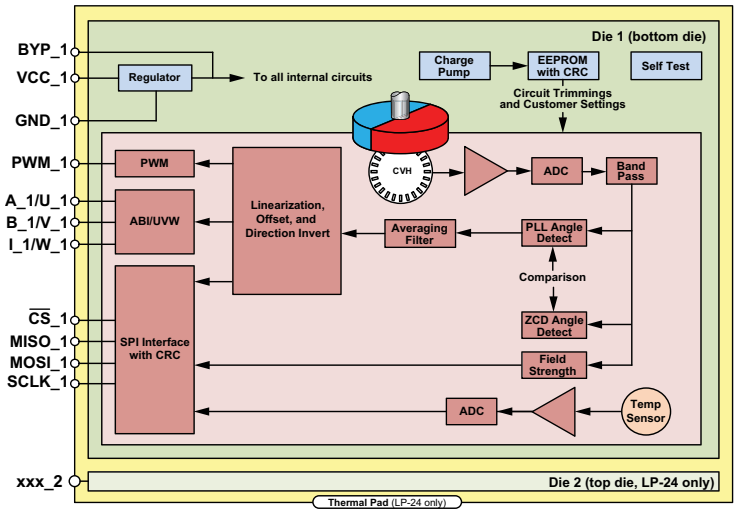


Figure 1: AAS33001 Magnetic Circuit and IC Diagram

FEATURES AND BENEFITS (continued)

- High diagnostic coverage
  - On-chip diagnostics include logic built-in self-test (LBIST), signal-path diagnostics, and watchdogs to support safety-critical (ASIL) applications
  - 4-bit CRC on SPI
- On-chip EEPROM for storing factory and customer calibration parameters
  - Single-bit error correction; dual-bit error detection, error correction control (ECC)
- Supports operating in harsh conditions required for automotive and industrial applications, including direct connection to 12 V battery
  - Operating temperature range from –40°C to 150°C
  - Operating supply voltage range from 3.7 to 18 V, absolute maximum of 28 V continuous
    - Can support ISO 7637-2 Pulse 5b up to 39 V
- Multiple output formats supported for ease of system integration
  - ABI and UVW interfaces provide high-resolution and lowest-latency angle data
  - PWM interface provides initial position for ABI/UVW interfaces
  - 10 MHz SPI for low-latency angle and diagnostic data; enables multiple independent ICs to be connected to the same bus
    - 3.3 V and 5 V SPI interfaces are supported
  - Output resolution on ABI and UVW are selectable
- Multiple programming/configuration formats supported
  - The system can be completely controlled and programmed over SPI, including EEPROM writes
  - For systems with limited pins available, writing and reading can be performed over the VCC and PWM pins. This allows the EEPROM of a device that has only the ABI/UVW and PWM pins connected to be configured in the production line.
- 1 mm thin surface-mount TSSOP packages for both single- and dual-die versions to minimize air gap from target magnet to CVH transducer for improved field strength
  - Pin-compatible to single- and dual-die A1333 devices
  - Stacked dual-die construction to improve channel-to-channel matching for systems that require redundant sensors

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SELECTION GUIDE

Part Number	System Die	Interface Voltage (V)	Package	Packing
AAS33001LLPBTR-DD	Dual	3.3	24-pin eTSSOP	4000 pieces per 13-inch reel
AAS33001LLEATR	Single	3.3	14-pin TSSOP	4000 pieces per 13-inch reel
AAS33001LLPBTR-5-DD	Dual	5	24-pin eTSSOP	4000 pieces per 13-inch reel
AAS33001LLEATR-5	Single	5	14-pin TSSOP	4000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Sampling angles, respecting T_J(max)	28	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	–18	V
All Other Pins Forward Voltage	V_{IN}		5.5	V
All Other Pins Reverse Voltage	V_R		–0.5	V
Operating Ambient Temperature	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		170	°C
Storage Temperature	T_{stg}		–65 to 170	°C

THERMAL CHARACTERISTICS: MAY REQUIRE DERATING AT MAXIMUM CONDITIONS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LP-24 package with exposed thermal pad; measured on JEDEC JESD51-7 2s2p board	69	°C/W
		LE-14 package; measured on JEDEC JESD51-7 2s2p board	82	°C/W

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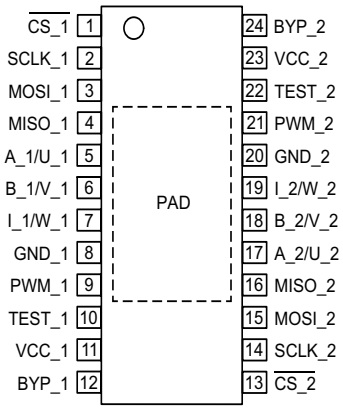
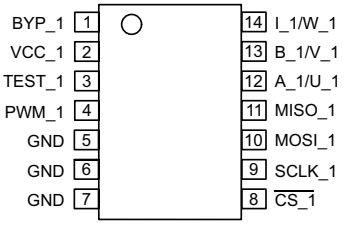
PINOUT DIAGRAMS AND TERMINAL LIST TABLE

PINOUT DIAGRAMS

LP 24-PIN ETSSOP



LE 14-PIN TSSOP



TERMINAL LIST TABLE

Pin Name	Pin Number		Function
	LE-14	LP-24	
PWM_1	4	9	PWM angle output (die 1)
BYP_1	1	12	External bypass capacitor terminal for internal regulator (die 1)
A_1/U_1	12	5	Option 1: Quadrature A output signal (die 1) Option 2: U (phase 1) output signal (die 1)
B_1/V_1	13	6	Option 1: Quadrature B output signal (die 1) Option 2: V (phase 2) output signal (die 1)
VCC_1	2	11	Power supply
I_1/W_1	14	7	Option 1: Quadrature I (index) output signal (die 1) Option 2: W (phase 3) output signal (die 1)
VCC_2	–	23	Power supply
MISO_2	–	16	SPI controller-input/peripheral-output (die 2)
SCLK_2	–	14	SPI clock terminal input (die 2)
MOSI_2	–	15	SPI controller-output/peripheral-input (die 2); also address selection for Manchester interface
$\overline{\text{CS\_2}}$	–	13	SPI chip-select terminal, active low input (die 2); also address selection for Manchester interface
GND	5, 6, 7	–	Device ground terminal
GND_1	–	8	Device ground terminal
GND_2	–	20	Device ground terminal
PWM_2	–	21	PWM angle output (die 2)
BYP_2	–	24	External bypass capacitor terminal for internal regulator (die 2)
A_2/U_2	–	17	Option 1: Quadrature A output signal (die 2) Option 2: U (phase 1) output signal (die 2)
B_2/V_2	–	18	Option 1: Quadrature B output signal (die 2) Option 2: V (phase 2) output signal (die 2)
I_2/W_2	–	19	Option 1: Quadrature I (index) output signal (die 1) Option 2: W (phase 3) output signal (die 1)
MISO_1	11	4	SPI controller-input/peripheral-output (die 1)
SCLK_1	9	2	SPI clock terminal input (die 1)
MOSI_1	10	3	SPI controller-output/peripheral-input (die 1); also address selection for Manchester interface
$\overline{\text{CS\_1}}$	8	1	SPI chip-select terminal, active low input (die 1); also address selection for Manchester interface
TEST_1	3	10	Connect to ground (die 1)
TEST_2	–	22	Connect to ground (die 2)
PAD	–	PAD	Exposed pad for thermal dissipation

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OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		3.7	–	18	V
Supply Current	$I_{CC(full)}$	For single die	–	15	19	mA
Power-On Reset Threshold Voltage [3]	V_{PORHI}	V_{CC} rising, dV/dt = 1 V/ms, T_A = 25°C	–	–	3.7	V
	V_{PORLOW}	V_{CC} falling, dV/dt = 1 V/ms, T_A = 25°C	3.3	–	–	V
Undervoltage Warning Level [6]	V_{UV}	T_A = –40°C to 150°C	3.7	3.82	4	V
Supply Zener Clamp Voltage	V_{ZSUP}	I_{CC} = $I_{CC(AWAKE)}$ + 3 mA, T_A = 25°C	26.5	–	–	V
Reverse Battery Current	I_{RCC}	V_{RCC} = –18 V, T_A = 25°C	–	–	5	mA
Power-On Time [4]	t_{PO}	Power-on diagnostics disabled, interface working, but angle not yet settled	–	300	–	µs
Bypass Pin Output Voltage [5]	V_{BYP}	T_A = 25°C, C_{BYP} = 0.1 µF, 3.3 V interface	2.97	3.3	3.63	V
		T_A = 25°C, C_{BYP} = 0.1 µF, 5 V interface enabled and V_{CC} ≥ 5 V	4	5	5.5	V
SPI AND ABI/UVW INTERFACE SPECIFICATIONS (for 3.3 V interface)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Output High Voltage	V_{OH}	MISO and ABI/UVW pins, C_L = 20 pF, T_A = 25°C	2.93	3.3	3.63	V
Output Low Voltage	V_{OL}	MISO and ABI/UVW pins, C_L = 20 pF, T_A = 25°C	–	0.3	–	V
SPI AND ABI/UVW INTERFACE SPECIFICATIONS (for 5 V interface)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Output High Voltage	V_{OH}	MISO and ABI/UVW pins, C_L = 20 pF, T_A = 25°C, V_{CC} ≥ 5 V	4	5	5.5	V
Output Low Voltage	V_{OL}	MISO and ABI/UVW pins, C_L = 20 pF, T_A = 25°C	–	0.3	–	V
SPI INTERFACE SPECIFICATIONS						
SPI Clock Frequency [6]	f_{SCLK}	MISOx pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle [6]	D_{fSCLK}	SPI_{CLKDC}	40	–	60	%
SPI Frame Rate [6]	t_{SPI}		5.8	–	588	kHz
Chip Select to First SCLK Edge [6]	t_{CS}	Time from $\overline{CS}$x going low to SCLKx falling edge	50	–	–	ns
Chip Select Inactive Time	t_{CSH}	Time in which $\overline{CS}$x is held high before the next frame	150	–	–	ns
Data Output Valid Time [6]	t_{DAV}	Data output valid after SCLKx falling edge	–	–	50	ns
MOSI Setup Time [6]	t_{SU}	Input setup time before SCLKx rising edge	25	–	–	ns
MOSI Hold Time [6]	t_{HD}	Input hold time after SCLKx rising edge	50	–	–	ns
SCLK to CS Hold Time [6]	t_{CHD}	Hold SCLKx high time before $\overline{CS}$x rising edge	5	–	–	ns
Load Capacitance [6]	C_L	Loading on digital output (MISOx) pin	–	–	20	pF

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency	f_{PWM}	PWM frequency minimum setting, T_A in specification	–	98	–	Hz
		PWM programmable options (number of steps)	–	128	–	steps
		PWM frequency maximum setting, T_A in specification	–	3.125	–	kHz
PWM Output Low Clamp	$D_{PWM(min)}$	Corresponding to digital angle of 0x000	–	5	–	%
PWM Output High Clamp	$D_{PWM(max)}$	Corresponding to digital angle of 0xFFF	–	95	–	%
INCREMENTAL OUTPUT SPECIFICATIONS						
ABI and UVW Output Angular Hysteresis [6]	hys_{ANG}	Programmable	0	–	1.38	degrees
MANCHESTER INTERFACE SPECIFICATIONS						
Manchester High Voltage [6]	$V_{MAN(H)}$	Applied to VCC line	7.3	8	$V_{CC(max)}$	V
Manchester Low Voltage [6]	$V_{MAN(L)}$	Applied to VCC line	$V_{CC(min)}$	5	5.7	V
Manchester Bitrate [6]	f_{MAN}	Line state changes once or twice per bit; maximum speed is usually limited by VCC line capacitance	2.2	–	100	kbit/s
BUILT-IN SELF-TEST						
Logic BIST Time	t_{LBIST}	Configurable to run on power-up or on user request	–	30	–	ms
Circular Vertical Hall Self-Test Time	t_{CVHST}	Configurable to run on power-up or on user request	–	30	–	ms
MAGNETIC CHARACTERISTICS						
Magnetic Field	B	Range of input field	–	–	1200	G

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
ANGLE CHARACTERISTICS						
Output [7]	RES_{ANGLE}	Both 12- and 15-bit angle values are available via SPI	–	12 or 15	–	bit
Angle Refresh Rate [8]	t_{ANG}	No averaging	–	1	–	µs
Response Time [6]	$t_{RESPONSE}$	Angular latency; valid for ABI or UVW interface	–	10	–	µs
Angle Error [9]	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1	±0.4	1	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.3	±0.7	1.3	degrees
Temperature Drift	$ANGLE_{DRIFT}$	T_A = 150°C, B = 300 G, angle change from 25°C	–1.4	–	1.4	degrees
		T_A = –40°C, B = 300 G, angle change from 25°C	–	0.9	–	degrees
Angle Noise [10][11]	N_{ANG}	T_A = 25°C, B = 300 G, no internal filtering, target rpm = 0, 3-sigma noise	–	±0.22	–	degrees
		T_A = 150°C, B = 300 G, no internal filtering, target rpm = 0, 3-sigma noise	–	±0.28	–	degrees
Effective Resolution [12]		B = 300 G, T_A = 25°C	–	12.47	–	bits
Angle Drift Over Lifetime [13]	$ANGLE_{Drift\_Life}$	B = 300 G, average maximum drift observed following AEC-Q100 qualification testing	–	0.5	–	degrees

[1] Typical data is at T_A = 25°C and V_{CC} = 5 V, and is for design estimates only.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] At power-on, a die does not respond to commands until V_{CC} rises to greater than V_{PORHI}. After that, the die performs and responds typically until V_{CC} reduces to less than V_{PORLOW}.
[4] During the power-on phase, the AAS33001 SPI transactions are not guaranteed.
[5] The output voltage and current specifications are to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents that are to be expected during typical operation.
[6] Parameter is not guaranteed at final test. Determined by design.
[7] RES_{ANGLE} represents the number of bits of data available for reading from the die registers.
[8] The rate at which a new angle reading becomes ready.
[9] Error value as measured at Allegro final test before any on-chip linearization is applied. Actual raw angle error performance in application can vary with multiple factors (e.g., magnet-to-sensor alignment, etc.). Using the on-chip linearization features of the AAS33001 can significantly reduce these errors.
[10] Error and noise values are with no further signal processing. Angle noise can be reduced with internal filtering and slower angle-refresh rate.
[11] This value represents 3-sigma or three times the standard deviation of the measured samples.
[12] Effective resolution is calculated using:

$$log_2(360) - log_2\left(\overline{\frac{1}{n}\sum_{i=1}^{n}\sigma_i}\right)$$

where σ is the standard deviation based on 30 measurements taken at each of the 32 angular positions, I = 11.25, 22.5, … 360.
[13] Maximum observed angle drift following AEC-Q100 stress is 1.4 degrees.

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FUNCTIONAL DESCRIPTION

Overview

The AAS33001 is a rotary-position Hall-sensor-based device. It incorporates one or two electrically independent Hall sensor dies in the same surface-mount package to provide solid-state consistency and reliability, and to support a wide variety of automotive applications. Each Hall-sensor-based die measures the direction of the magnetic field vector through 360° in the x-y plane (parallel to the branded face of the device) and computes an angle measurement based on the actual physical reading, as well as any internal parameters that have been set by the user. The output of each die is used by the host microcontroller to provide a single channel of target data.

This device is an advanced, programmable system-on-chip (SoC). Each integrated circuit includes a circular vertical Hall (CVH) analog front end, a high-speed sampling analog-to-digital converter (ADC), digital filtering, digital signal processing, a digital control SPI interface, motor commutation outputs (UVW), and encoder outputs (A, B, I).

Advanced offset, gain, and linearization adjustment options are available in the AAS33001. These options can be configured in onboard EEPROM, providing a wide range of sensing solutions in the same device.

Angle Measurement

The AAS33001 can monitor the angular position of a rotating magnet at speeds ranging from 0 to more than 15,000 rpm. The AAS33001 has a typical output refresh rate of 1 µs.

Readout in SPI is possible with 12-bit resolution with error flags included in the same word, or in 15-bit resolution without included error flags. Reading out the angle takes 16 SPI clock cycles. For details about SPI use, see the SPI Interface section.

PWM output is always resolved to a 12-bit angle resolution.

ABI/UVW resolution can be set to the level desired by the customer.

The sensor readout is processed and linearized in various steps. These are detailed in Figure 3.

System-Level Timing

Internal registers are updated with a new angle value every t_{ANG}. Due to signal-path delay, the angle is $t_{RESPONSE}$ old at each update. In other words, $t_{RESPONSE}$ is the delay from the time of magnet sampling until generation of a processed angle value. The streaming protocols ABI and UVW, which require no external trigger, update every t_{ANG} (if an angle change has occurred). SPI, which is asynchronously clocked, results in a varying latency depending on sampling frequency and SCLK speed. The values that are presented to the user are copied from the data path to the output registers between 0 and 125 ns after the SPI falling chip-select edge. The first bit never contains data. If the SPI clock is 10 MHz, the data are clocked out after 1.6 µs. Because the data are sampled in at the first clock edge at an age of maximum $t_{RESPONSE}$, their age after the SPI transaction has finished is between 1.6 and 1.6 + $t_{RESPONSE}$ µs.

The update rate and the signal delay of the different angle-output paths depending on the sensor settings are shown in Figure 2.

The value of the ANGLE_ZCD register is updated approximately every 32 µs. The value of the register GAUSS is update approximately every 128 µs.

Power-Up

Upon applying power to the AAS33001, the device automatically runs through an initialization routine. The purpose of this initialization is to ensure that the device comes up in the same predictable operating condition every power cycle. This initialization routine takes a finite amount of time to complete, which is referred to as power-on time, t_{PO}. Regardless of the state of the device before a power cycle, the device repowers with EEPROM shadow bits copied from the EEPROM anew, and serial registers in their default states. For example, on every power-up, the device powers with the ZERO_OFFSET stored in the EEPROM. The extended write access field WRITE_ADR is set back to its default value, zero.

PWM Output

The AAS33001 provides a pulse-width-modulated output with duty cycle proportional to measured angle. The PWM duty cycle is clamped at 5% and 95% DC for diagnostic purposes. 5% DC corresponds to 0 degrees of angle; 95% DC corresponds to 360° of angle. The 0% and 100% (pulled low and pulled high) states are reserved for error condition notifications. The rising edges of the output are always at the same points in time, while the falling edge moves from 5% to 95% over angles of 0 to 360 degrees.

In case of errors:

- If PEO = 1, errors affect the PWM pin.
- If PES = 0, the PWM pin is tristated.
- If PES = 1, the output frequency is halved and the outputs are fixed to the levels in Table 1.

Table 1: PWM Output Errors

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Error	Priority	Duty Cycle %	Description / Persistence
WDE	1 (highest)	5	Watchdog error. Permanent error until restart.
EUE	2	10.625	EEPROM uncorrectable error. Permanent error until restart.
STF	3	16.25	Self-test failure. Permanent error until restart.
PLK	4	21.875	PLL not locked. Persists until PLL locks.
ZIE	5	27.5	Zero-crossing integrity error. Persists as long as the issue exists.
AVG	6	33.125	Angle averaging error. Outputs once then clears.
UV	7	38.75	Undervoltage (UVA and/or UVCC dependent on serial error masks). Persists until no unmasked undervoltage.
MSL	8	44.375	Persists until field strength exceeds the low threshold.
ESE	9	50	EEPROM correctable error. Outputs once, then clears.
SAT	10	55.625	Saturation error. Persists as long as the issue exists.
MSH	11	61.25	Persists until field strength is less than the high threshold.
TR	12 (lowest)	66.875	Persists until temperature is within range.

The duty cycle of the pin can be configured using the PWM_BAND and the PWM_FREQ fields, yielding the frequencies shown in Table 2.

Table 2: PWM Frequency Table (Hz)

		PWM_BAND							
		0	1	2	3	4	5	6	7
PWM_FREQ	0	3125	2778	2273	1667	1087	641	352	185
	1	3101	2740	2222	1613	1042	610	333	175
	2	3077	2703	2174	1563	1000	581	316	166
	3	3053	2667	2128	1515	962	556	301	157
	4	3030	2632	2083	1471	926	532	287	150
	5	3008	2597	2041	1429	893	510	275	143
	6	2985	2564	2000	1389	862	490	263	137
	7	2963	2532	1961	1351	833	472	253	131
	8	2941	2500	1923	1316	806	455	243	126
	9	2920	2469	1887	1282	781	439	234	121
	10	2899	2439	1852	1250	758	424	225	116
	11	2878	2410	1818	1220	735	410	217	112
	12	2857	2381	1786	1190	714	397	210	108
	13	2837	2353	1754	1163	694	385	203	105
	14	2817	2326	1724	1136	676	373	197	101
	15	2797	2299	1695	1111	658	362	191	98

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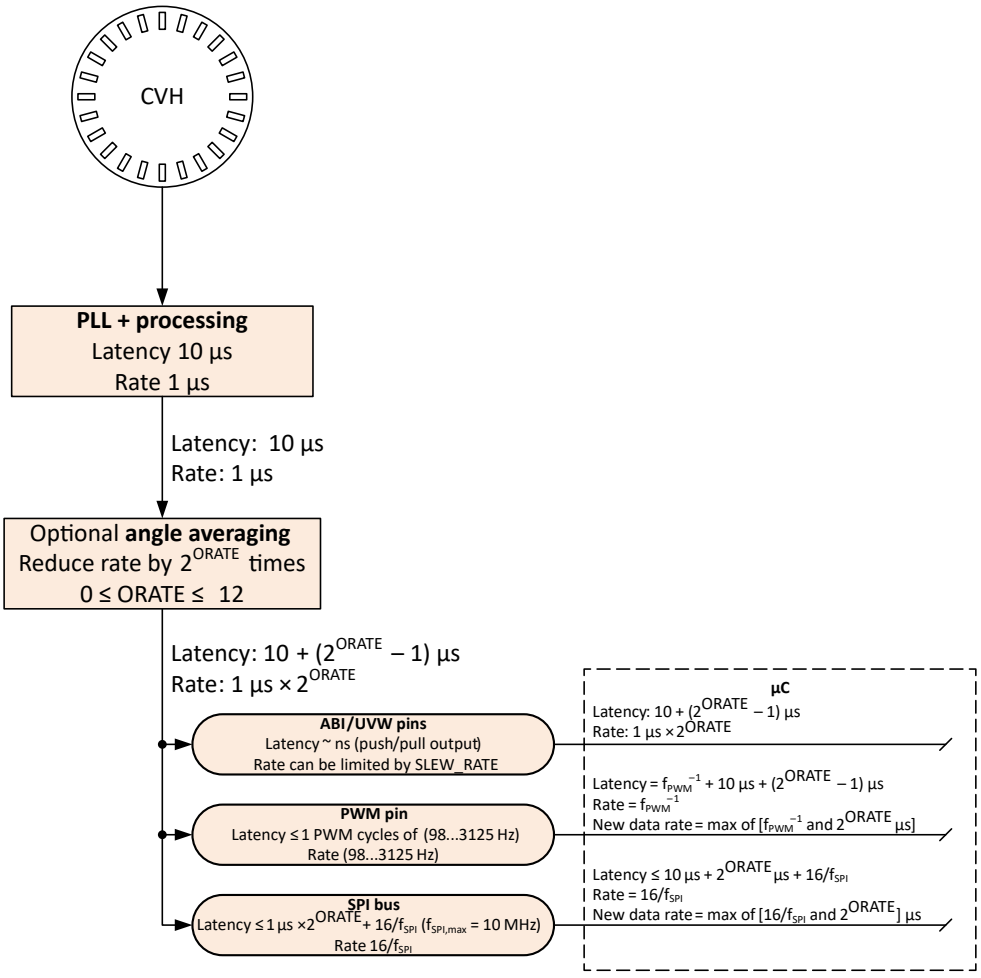

Figure 2: Signal Latency and Update Rates

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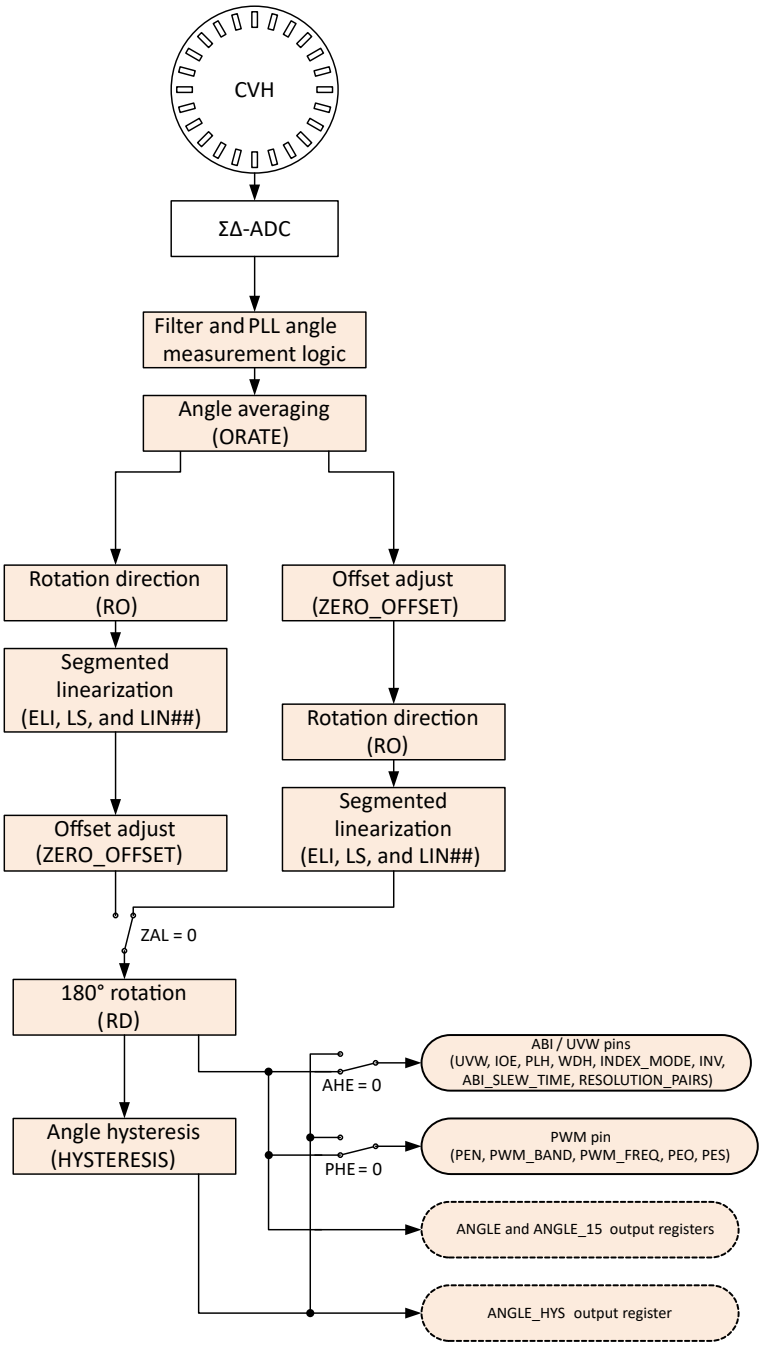

Figure 3: Angle Data Flow Chart
Text in all capitals denotes registers that affect their containing block.

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Linearization

The AAS33001 contains linearization functionality. Linearization allows for conversion of the initially sensor-measured magnetic field data into customer-desired linear output. This can be used to correct minor imperfections in the encoder signal.

Linearization converts the electrical angles (the angle as measured by the sensor front end) into mechanical angles (the actual angle of the encoder signal).

To use the linearization feature, it is most convenient to use the Allegro AAS33001 Samples Programmer Graphical User Interface (GUI). It allows the user to measure points along the mechanical rotation, calculate all parameters that need to be written into the sensor, and write these values into the sensor. To use this function, the user must be able to read and control the mechanical angle.

The sensor performs linearization by taking the measured electrical angles and, depending on the angle measured, subtracting a linearization coefficient stored in EEPROM. There are 32 of these linearization coefficients in the EEPROM. The angle value at a sensor angle reading of 0, 11.25, 22.5, … 348.75 electrical degrees are to be modified by the values in EEPROM fields LIN0, LIN1, LIN2, … LIN31. The EEPROM LIN values are subtracted from the electrical sensor angles, as shown in Table 3.

The LIN fields are 12-bit signed values. Each LIN coefficient has a range of –2048 to 2047 LSB, which corresponds to a correction of the electrical angle by 22.5 to –22.49 degrees (EEPROM field LS = 0) or by 45 to –44.98 degrees (EEPROM field LS = 1). When the electrical angle is between two of the linearization points, the sensor calculates the appropriate correction value for this angle by linear interpolation between the two coefficients next to the value. For example, if the sensor measures an angle of 5.625°, the output is 5.625 – (LIN0 + LIN1) / 2.

An example of a nonlinear curve that is corrected by the sensor is shown in Figure 4. In this example, the values of LIN0, LIN1, LIN2, and LIN3 are negative numbers, while LIN4 is a positive number. The linearized output angle in the example is close to the mechanical angle, but not perfect. This was done deliberately for the purpose of showing a more-realistic example.

The output delay of the AAS33001 is not affected by enabling or disabling linearization. If linearization is disabled, the EEPROM LIN fields can be used for other customer purposes.

Table 3: Linearization Coefficients

Electrical Angle (°) Measured By Sensor	Correction Value Written in EEPROM	Output Angle Visible on Sensor Output
0.00	LIN0	Output = 0.00 – LIN0
11.25	LIN1	Output = 11.25 – LIN1
22.50	LIN2	Output = 22.50 – LIN2
33.75	LIN3	Output = 33.75 – LIN3
45.00	LIN4	Output = 45.00 – LIN4
56.25	LIN5	Output = 56.25 – LIN5
67.50	LIN6	Output = 67.50 – LIN6
78.75	LIN7	Output = 78.75 – LIN7
90.00	LIN8	Output = 90.00 – LIN8
101.25	LIN9	Output = 101.25 – LIN9
112.50	LIN10	Output = 112.50 – LIN10
123.75	LIN11	Output = 123.75 – LIN11
135.00	LIN12	Output = 135.00 – LIN12
146.25	LIN13	Output = 146.25 – LIN13
157.50	LIN14	Output = 157.50 – LIN14
168.75	LIN15	Output = 168.75 – LIN15
180.00	LIN16	Output = 180.00 – LIN16
191.25	LIN17	Output = 191.25 – LIN17
202.50	LIN18	Output = 202.50 – LIN18
213.75	LIN19	Output = 213.75 – LIN19
225.00	LIN20	Output = 225.00 – LIN20
236.25	LIN21	Output = 236.25 – LIN21
247.50	LIN22	Output = 247.50 – LIN22
258.75	LIN23	Output = 258.75 – LIN23
270.00	LIN24	Output = 270.00 – LIN24
281.25	LIN25	Output = 281.25 – LIN25
292.50	LIN26	Output = 292.50 – LIN26
303.75	LIN27	Output = 303.75 – LIN27
315.00	LIN28	Output = 315.00 – LIN28
326.25	LIN29	Output = 326.25 – LIN29
337.50	LIN30	Output = 337.50 – LIN30
348.75	LIN31	Output = 348.75 – LIN31

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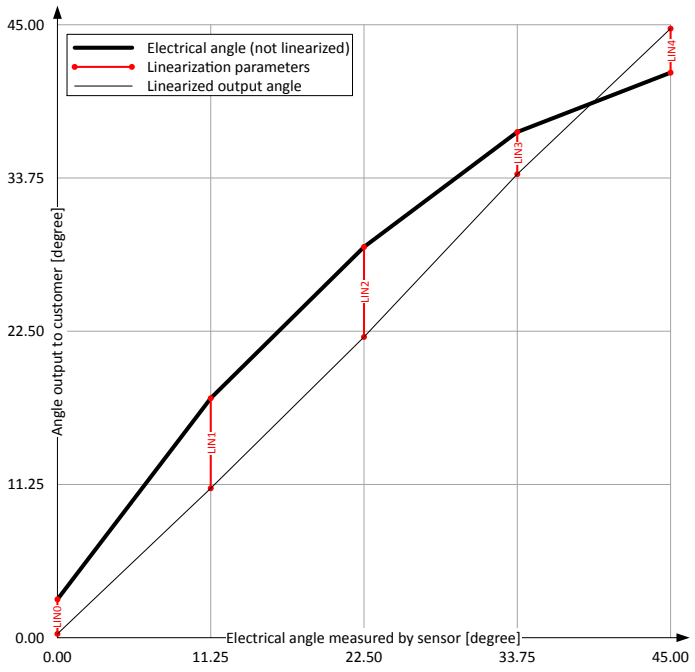

Figure 4: Linearization Example

Incremental Output Interface (ABI)

The AAS33001 offers an incremental output mode in the form of quadrature A/B and index (I) outputs to emulate an optical or mechanical encoder. The A and B signals toggle with a 50% duty cycle (relative to angular distance, not necessarily time) at a frequency of 2N cycles per magnetic revolution, giving a cycle resolution of (360 / 2^N) degrees per cycle. B is offset from A by ¼ of the cycle period. The I signal is an index pulse that occurs once per revolution to mark the zero (0) angle position. One revolution is shown in Figure 5.

Because A and B are offset by ¼ of a cycle, they are in quadrature and together have four unique states per cycle. Each state represents R = [360 / (4 × 2^N)] degrees of the full revolution. This angular distance is the quadrature resolution of the encoder. The order in which the states change, or the order of the edge transitions from A to B, allow the direction of rotation to be determined. If a given B edge (rising/falling) precedes the following A edge, the angle is increasing from the perspective of the electrical (sensor) angle and the angle position should be incremented by the quadrature resolution (R) at each state transition. Conversely, if a given A edge precedes the following B edge, the angle is decreasing from the perspective of the electrical (sensor) angle and the angle position should be decremented by the quadrature resolution (R) at each state transition. The angle position accumulator wraps each revolution back to 0. The quadrature states are designated as Q1 through Q4 in the following diagrams, and are defined as follows:

State Name	A	B
Q1	0	0
Q2	0	1
Q3	1	1
Q4	1	0

Note that the A/B progression is a grey coding sequence where only one signal transitions at a time. The state progression must be as follows to be valid:

Increasing angle: Q1 → Q2 → Q3 → Q4 → Q1 → Q2 → Q3 → Q4

Decreasing angle: Q4 → Q3 → Q2 → Q1 → Q4 → Q3 → Q2 → Q1

The duration of one cycle is referred to as 360 electrical degrees, or 360e. One half of a cycle is therefore 180e, and one quarter of a cycle (one quadrature state, or R degrees) is 90e. This is the

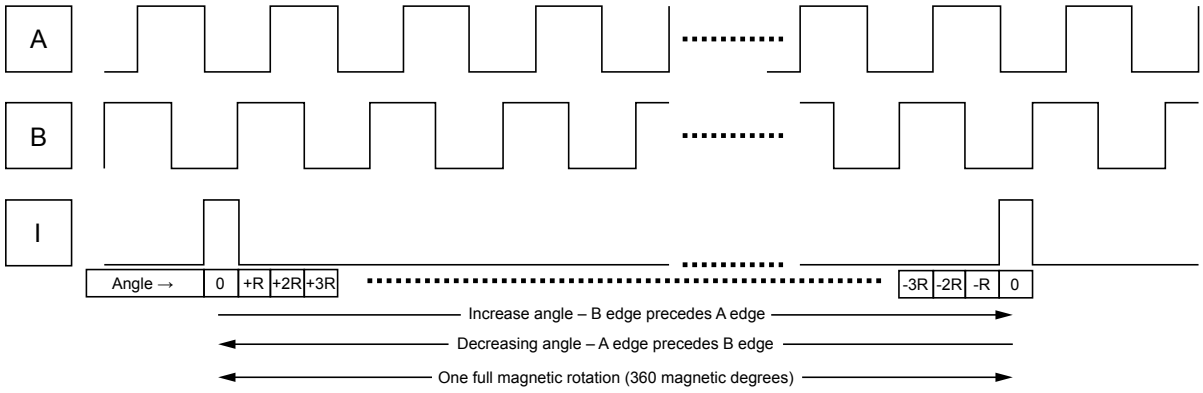

Figure 5: One Full Revolution

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terminology used to express variance from perfect signal behavior. Ideally, the A and B cycle would be as shown in Figure 6 for a constant velocity.

In reality, the edge rate of the A and B signals, and the switching threshold of the receiver inputs/outputs (I/Os), affect the quadrature periods (see Figure 7).

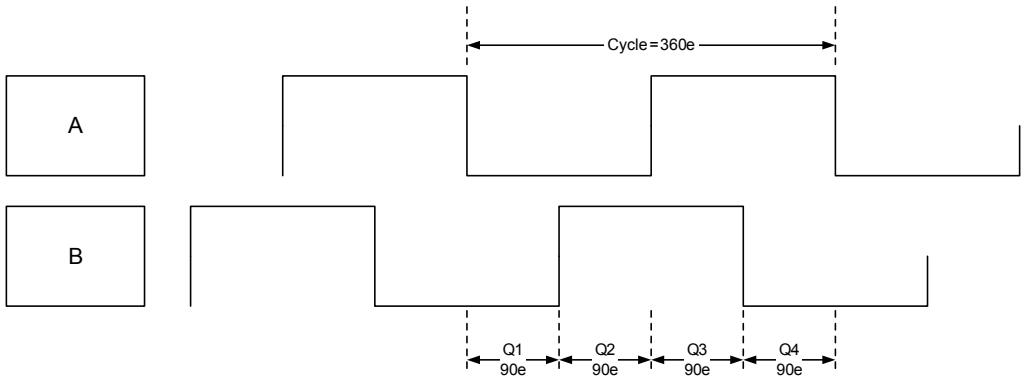

Figure 6: Electrical Cycle

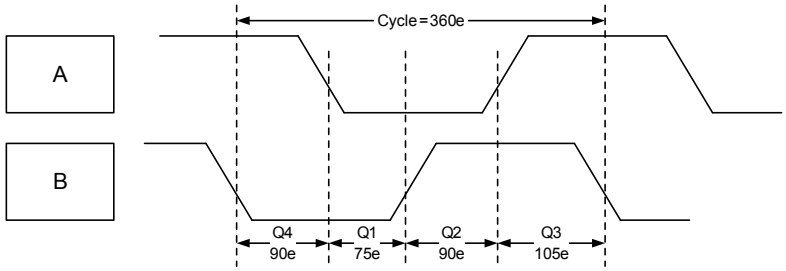

Figure 7: Electrical Cycle

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RESOLUTION

The AAS33001 supports the following ABI output resolutions.

This is set via the RESOLUTION_PAIRS field in EEPROM.

Table 4: ABI Output Resolution

EEPROM Resolution Field	Cycle Resolution (Bits = N)	Quadrature Resolution (Bits = 4 × N)	Cycles per Revolution (A or B)	Quadrature States per Revolution	Cycle Resolution (Degrees)	Quadrature Resolution (R) (Degrees)
0	Factory Use Only					
1	Factory Use Only					
2	Factory Use Only					
3	11	13	2048	8192	0.176	0.044
4	10	12	1024	4096	0.352	0.088
5	9	11	512	2048	0.703	0.176
6	8	10	256	1024	1.406	0.352
7	7	9	128	512	2.813	0.703
8	6	8	64	256	5.625	1.406
9	5	7	32	128	11.250	2.813
10	4	6	16	64	22.500	5.625
11	3	5	8	32	45.000	11.250
12	2	4	4	16	90.000	22.5
13	1	3	2	8	180.0	45.0
14	0	2	1	4	360.0	90.0
15	n/a	n/a	n/a	n/a	n/a	n/a

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SLEW-RATE LIMITING

Slew-rate limiting is enabled when the ABI.ABI_SLEW_TIME field is non-zero. This option separates the sample update rate from the ABI output rate and can be used to control two circumstances:

- The angle sample does not monotonically increase or decrease at the quadrature resolution, thereby skipping one or more quadrature states. In this case, the slew-rate limiting logic transitions the ABI signals in the required valid sequence, at the slew rate, until the ABI output catches up with the angle samples, at which point the typical sample-rate output resumes. This skipping is most likely to occur either at very low velocities if the noise is high, or at very high velocities if the angle changes more than the quadrature resolution in one angle-sample period.
- The ABI receiver at the host end cannot reliably detect edge transitions that are spaced at the sample rate of 1 µs. The slew-limit time can be set greater than the nominal angle sample update period, providing the velocity of the angle rotation does not, on average, require ABI transitions greater than the angle sample rate.

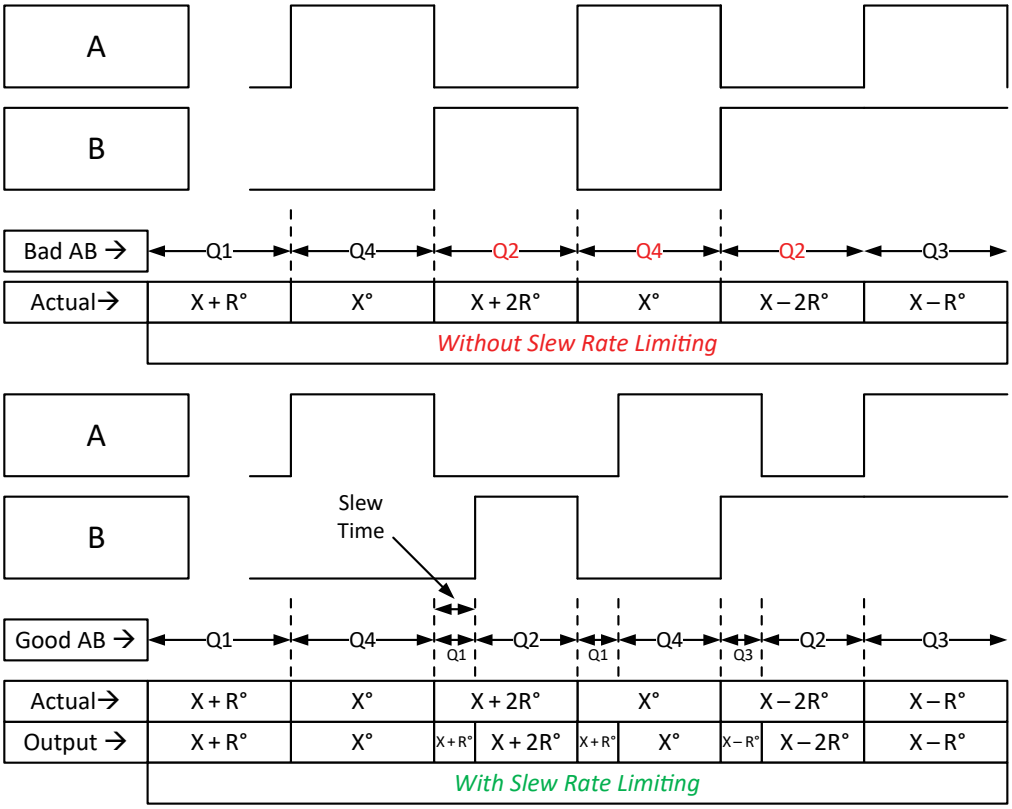

Figure 8: Slew-Rate Limiting

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INDEX PULSE

The index pulse, I (or Z in some descriptions), marks the absolute zero (0) position of the encoder. Under rotation, this allows the receiver to synchronize to a known mechanical/magnetic position, then use the incremental A/B signals to keep track of the absolute position. To support a range of ABI receivers, the I pulse has four widths, defined in Figure 9.

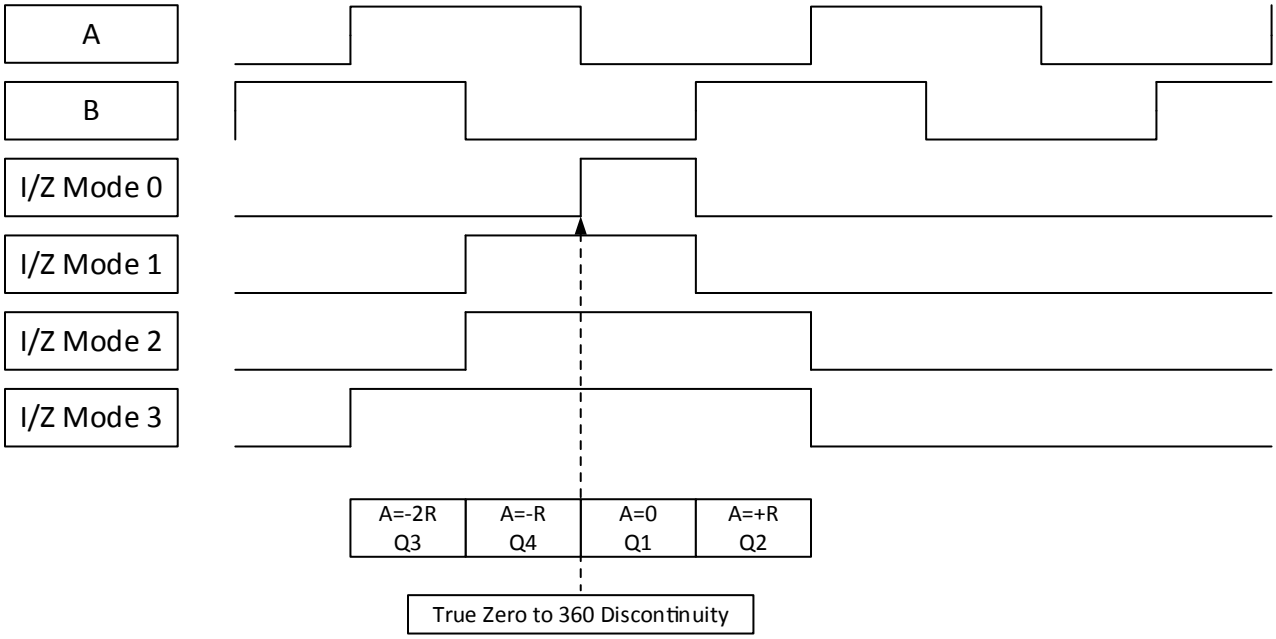

Figure 9: Index Pulse

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Brushless DC Motor Output (UVW)

The AAS33001 offers U, V, and W signals for stator commutation of brushless DC (BLDC) motors. The device is mode-selectable for 1 to 16 pole-pairs. The BLDC signals (U, V, and W) are generated based on the quantity of pole-pairs and on angle data from the angle sensor. The U, V, and W outputs switch when the measured mechanical angle crosses the value where a change should occur. If hysteresis is used, the output update method is different. The output behavior when hysteresis is enabled is described in the Angle Hysteresis section. The UVW waveforms for three and five pole-pair BLDC motors are shown in Figure 10 and Figure 11.

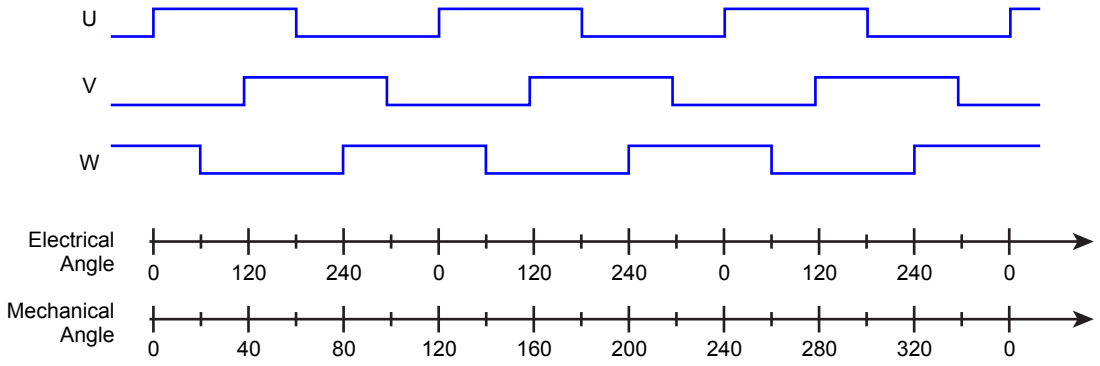

Figure 10: U, V, W Outputs for Three-Pole-Pair BLDC Motor

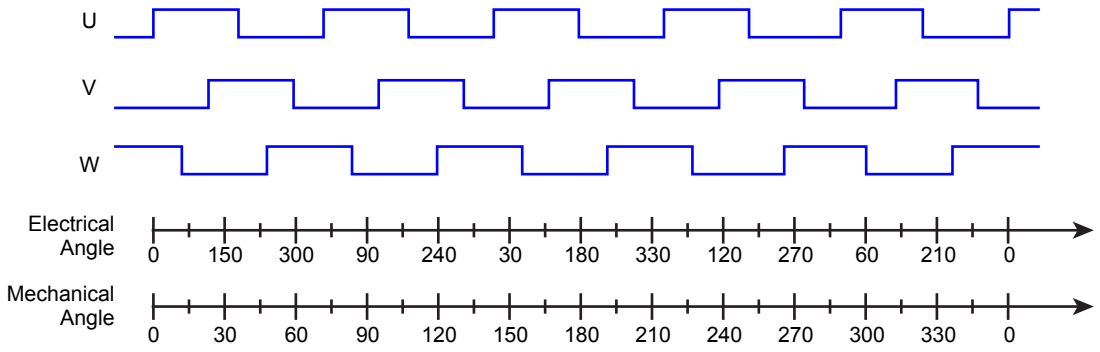

Figure 11: U, V, W Outputs for Five-Pole-Pair BLDC Motor

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Quantity of Poles (RESOLUTION_PAIRS)	Quantity of Pole-Pairs	Conversion from Electrical Degrees to Mechanical Degrees	
		Electrical (°)	Mechanical (°)
0000	1	90	90
0001	2	90	45
0010	3	90	30
0011	4	90	22.5
0100	5	90	18
0101	6	90	15
0110	7	90	12.857…
0111	8	90	11.25
1000	9	90	10
1001	10	90	9
1010	11	90	8.1818…
1011	12	90	7.5
1100	13	90	6.9231…
1101	14	90	6.4286…
1110	15	90	6
1111	16	90	5.625

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ABI Behavior at Power-Up

At power-up, the AAS33001 ABI interface communicates the current position. This means that reading the angle through the PWM output is not needed to find the current position when using the ABI interface. The behavior at start-up is the following:

- During t_{PO}, the state of the interface is undefined
- During a delay phase, the output displays a 0° angle. With default settings, the 0° angle is indicated by A = B = low and I = high.
- The interface then catches up with the actual measured angle by moving in a positive or negative direction, whichever is faster. The time for catching up is, at most:

$$t_{SETTLE(MAX)} = \frac{180°}{R} \times ABI\_slew\_time$$

where R is the quadrature resolution.

- After catching up with the output angle is complete, the sensor operates as typical.

If ABI_SLEW_TIME is set to 0, there is no catch-up phase. The output jumps to the final position immediately, e.g., with A = high and B = low. With ABI_SLEW_TIME set to 0, the user cannot determine the position at startup from the ABI interface.

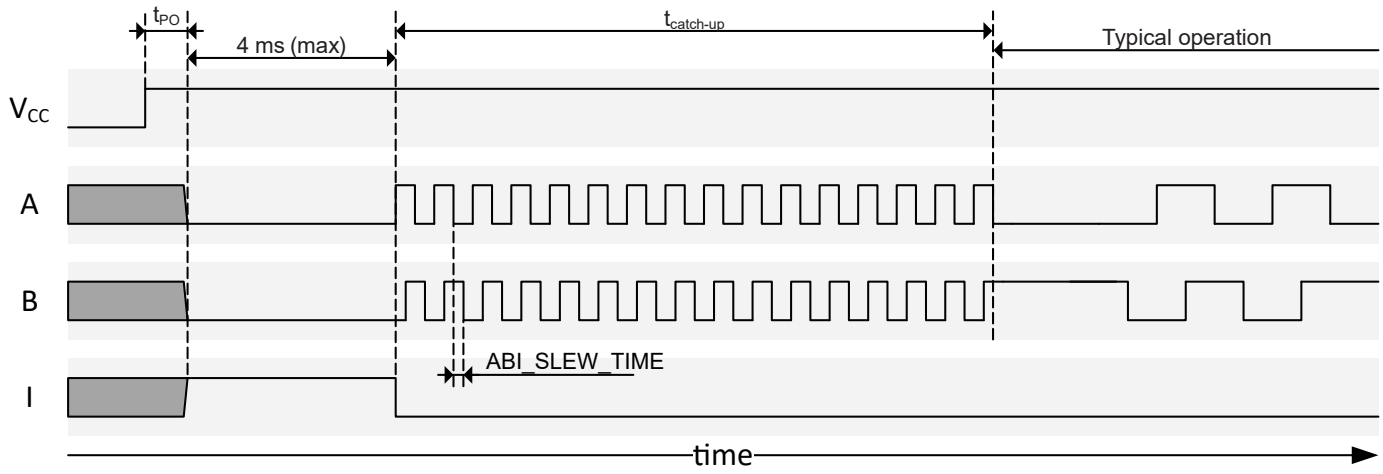

Figure 12: ABI Startup Behavior

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Angle Hysteresis

Hysteresis can be applied to the compensated angle to moderate jitter in the angle output due to noise or mechanical vibration. In the AAS33001, the hysteresis field (ANG.HYSTERESIS) defines the width of an angle window at 14-bit resolution. Mathematically, the width of this window is:

$$ANG.HYSTERESIS \times (360 / 16384) \text{ degrees} \quad ,$$

giving a range of 0 to 1.384 degrees.

The hysteresis-compensated angle can be routed to the ABI or UVW interface by setting the ABI.AHE bit to 1. On the SPI or Manchester interface, the hysteresis-compensated angle can be read via an alternate register (HANG.ANGLE_HYS) at 12-bit resolution.

The effect of the hysteresis is shown in Figure 13. The current angle position as measured by the sensor is at the head of the hysteresis window. As long as the sensor (electrical) angle advances in the same direction of rotation, the output angle is the sensor angle, minimizing latency. If the sensor angle reverses direction, the output angle is held static until the sensor angle exits the hysteresis window in either direction. If the exit is in the opposite direction of rotation where the head was, the head flips to the opposite end of the hysteresis window and that becomes the new reference direction. The current direction of rotation, or head for the purposes of hysteresis, is viewable via the STA.ROT bit, where 0 is in the increasing-angle direction and 1 is in the decreasing-angle direction.

This behavior has the following consequences:

1. If the hysteresis window is greater than the output resolution, the output angle skips consecutive incremental steps. If the hysteresis-compensated angle is selected for the ABI output, this results in an integrity failure due to skipped quadrature states. To avoid this, it is recommended that the slew-rate limiting be enabled on the ABI interface if hysteresis is used.
2. If there is jitter due to noise or mechanical vibration, especially at a static angle position or very slow rotation, the angle tends to bias to one side of the window, depending on the direction of rotation as the angular velocity approaches zero (i.e., towards the current head) rather than to the average position of the jitter.

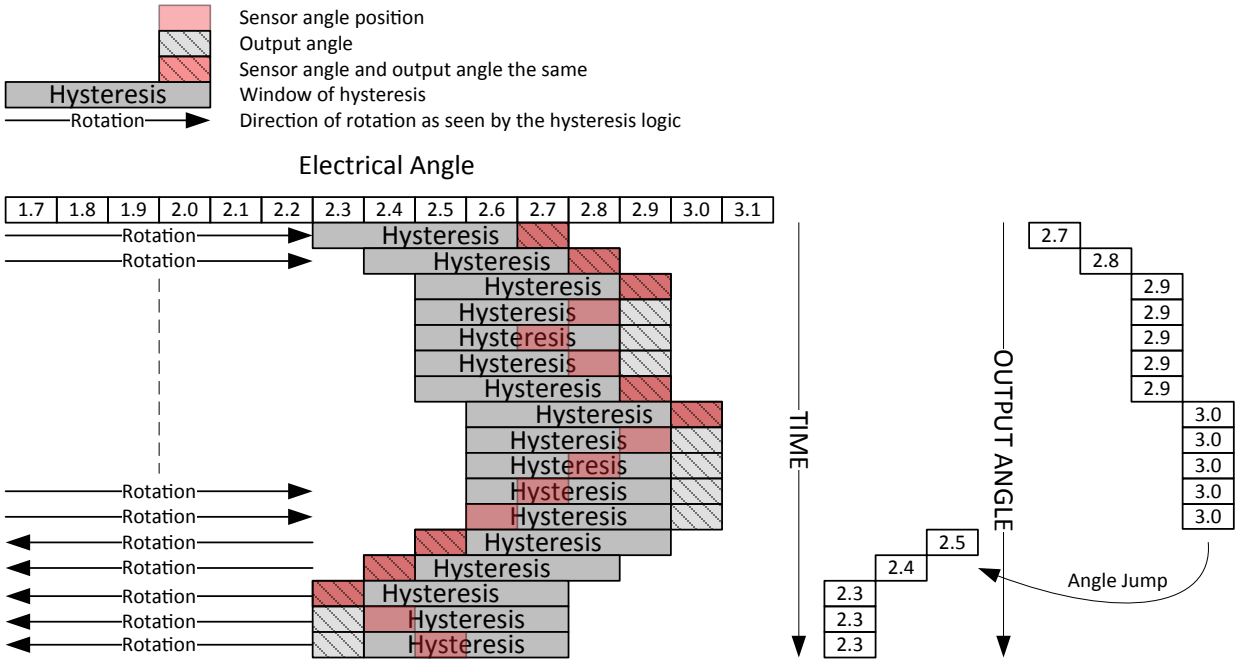

Figure 13: Effect of Hysteresis

Note: The rotation direction resets to 0, or increasing-angle direction. At power-up or after LBIST, the hysteresis window always lags behind the initial angle position; therefore, if hysteresis is enabled, a decreasing-angle direction of rotation does not register until the hysteresis window has passed.

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DEVICE PROGRAMMING INTERFACE

The AAS33001 can be programmed in two ways:

- Using the *SPI interface* for input and output, while supplying the VCC pin with typical operating voltage
- Using a *Manchester protocol* on the supply pin for input, and the PWM pin for output.

The AAS33001 does not require special supply voltages to write to the EEPROM.

All setting fields and all data fields of the sensor can be read and written using both protocols. If EEPROM locking is used (detailed in the EEPROM Write Lock section), write access using either of the protocols is prevented.

A separate setting to completely disable the Manchester interface is available in the DM field of the EEPROM. Using this setting causes the sensor to ignore any commands entered using Manchester protocol. The SPI interface does not become disabled by disabling the Manchester interface.

Interface Structure

The AAS33001 consists of two memory blocks. The primary serial interface registers are used for direct writes and reads by the host controller for frequently required data (for example, angle data, warning flags, field strength, and temperature). All forms of communication (even to the extended locations) operate through the primary registers, whether it be via SPI or Manchester.

The primary serial registers also provide a data and address location for accessing extended memory locations. Accessing these extended locations is achieved in an indirect fashion: The controller writes into the primary interface to give a command to the sensor to access the extended locations. The read/write is executed and the result is again presented in the primary interface.

This concept is shown in Figure 14.

For writing extended locations, the primary interface offers extended write address, data, and control registers. For details about use of these registers, refer to the Write Transaction to EEPROM and Other Extended Locations section.

For reading extended locations, the primary interface offers extended read address, data, and control registers. For details about use of these registers, refer to the Read Transaction from EEPROM and Other Extended Locations section.

EEPROM writing requires additional procedures. For more information about EEPROM and shadow memory read and write access, see the EEPROM and Shadow Memory Usage section.

The primary serial interface can be accessed using the SPI and using the Manchester interface. These two interfaces are detailed in the SPI Interface and Manchester Interface sections.

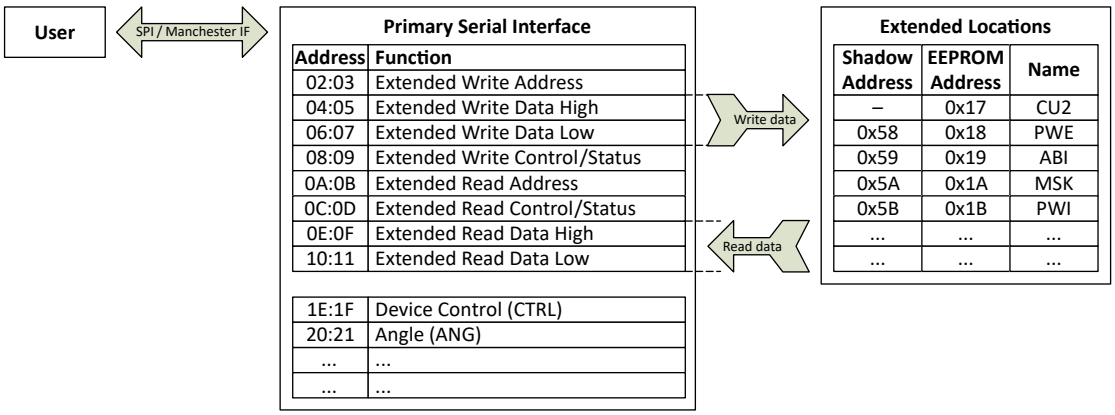

Figure 14: Serial Registers Allow Access to Extended Memory (EEPROM and Shadow)

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SPI Interface

The AAS33001 provides a full-duplex 4-pin SPI interface for each die, using SPI mode 3 (CPHA = 1, CPOL = 1). All programming can be performed using this interface; all programming can also be performed using the Manchester interface.

If the SPI interface is not used, do not leave the chip-select line floating; rather, follow the recommendations in the Typical SPI and ABI/UVW Applications section.

The sensor responds to commands received on the controller-output peripheral-input (MOSI), serial clock (SCLK), and chip-select (CSB) pins, and outputs data on the controller-input peripheral out (MISO) pin. All three input pins are 3.3 V and 5 V SPI compatible, with threshold values determined by factory EEPROM settings. The MISO output voltage level conforms to 3.3 V or 5 V SPI levels, based on factory settings. For ordering options of each variant, see the Selection Guide.

The setup for communication using the SPI interface is given in Figure 15.

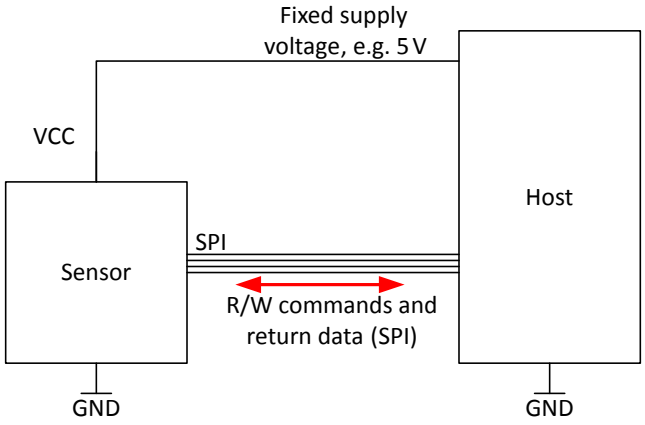

Figure 15: Programming Connections for SPI Interface

TIMING

The interface timing parameters from the specification table are defined in Figure 16 and Figure 17.

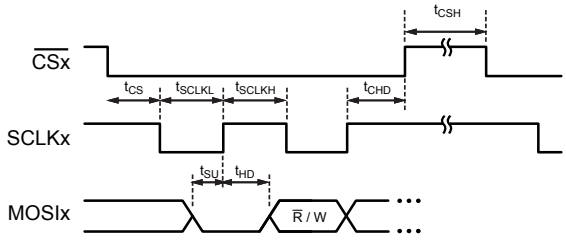

Figure 16: SPI Interface Timing Input

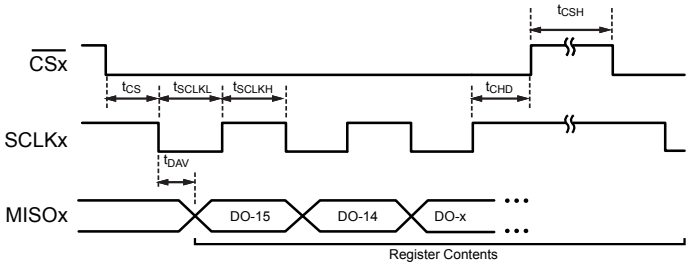

Figure 17: SPI Interface Timing Output

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MESSAGE FRAME SIZE

The SPI interface requires 16-, 17-, or 20-bit packet lengths. An extended 20-bit SPI packet allows 4 bits of CRC to accompany every data packet. A 17-bit packet is only allowed if the EEPROM/shadow bit S17 is set to 1.

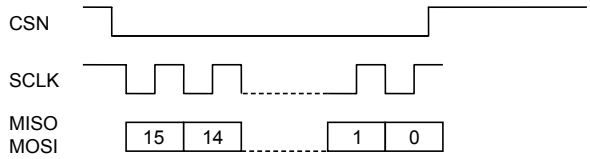

Figure 18: 16-Bit SPI Frame

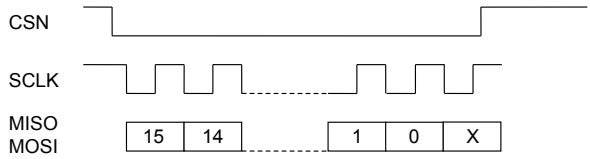

Figure 19: 17-Bit SPI Frame

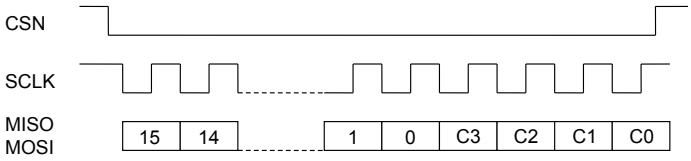

Figure 20: 20-Bit SPI Frame

If more clock pulses than expected were detected by the sensor in an SPI transaction, the interface warning WARN.IER activates. This warning does not activate during clean SPI transactions with 16 or 20 bits, or with clean 17-bit transactions when S17 is enabled.

The purpose of the 17-bit SPI option is to allow delayed reading of the MISO line by the host. Some hosts allow sampling of data from the peripheral—not on the rising edge, but on the next falling edge of SCLK. This way, in case of long interface delays caused by large line capacitance or very long cables, the permissible clock speed can be increased. However, a 17th falling edge is required to read the 16th bit coming from the sensor. For the sensor to not display an error when this 17th clock is found, the bit S17 must be set.

WRITE CYCLE

Write cycles consist of a 1 low bit, 1 read/write (R/W) bit (write = high), 6 address bits (corresponding to the primary serial register), 8 data bits, and 4 optional CRC bits. To write a full 16-bit serial register, two write commands are required (even and odd byte addresses). MOSI bits are clocked in on the rising edge of the controller-generated SCLK signal.

READ CYCLE

Reading data always involves at least two SPI frames. In the first frame, the read command is sent; in the second frame, the result from the first read is received. While receiving data from the last read command, it is possible to send another read command (duplexed read). This way, every frame except the first one contains data from the sensor. This is useful for very fast reading of angle data.

When receiving the last frame, the host can transmit a command with MOSI set to all zeros. This represents a read command from register 0x00 and does not change the state of the sensor. Reading from register 0x00 outputs the value 0x0000.

In frames where a previous read command was not sent, the MISO data output should be ignored.

Because an SPI read command can transmit 16 data bits at one

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time, and the primary serial registers are built from one even and one odd byte, the entire 16-bit contents of one serial register may be transmitted with one SPI frame. This is accomplished by providing an even serial address value. If an odd-value address is sent, only the contents of the single byte are returned, with the eight most significant bits within the SPI packet set to zero.

Example: To read all 16 bits of the error register (0x24:0x25), an SPI read request using address 0x24 should be sent. If only the 8 LSBs are desired, the address 0x25 should be used. Examples of both an SPI write and an SPI read request, using a 16-bit SPI message frame, are shown in Figure 21.

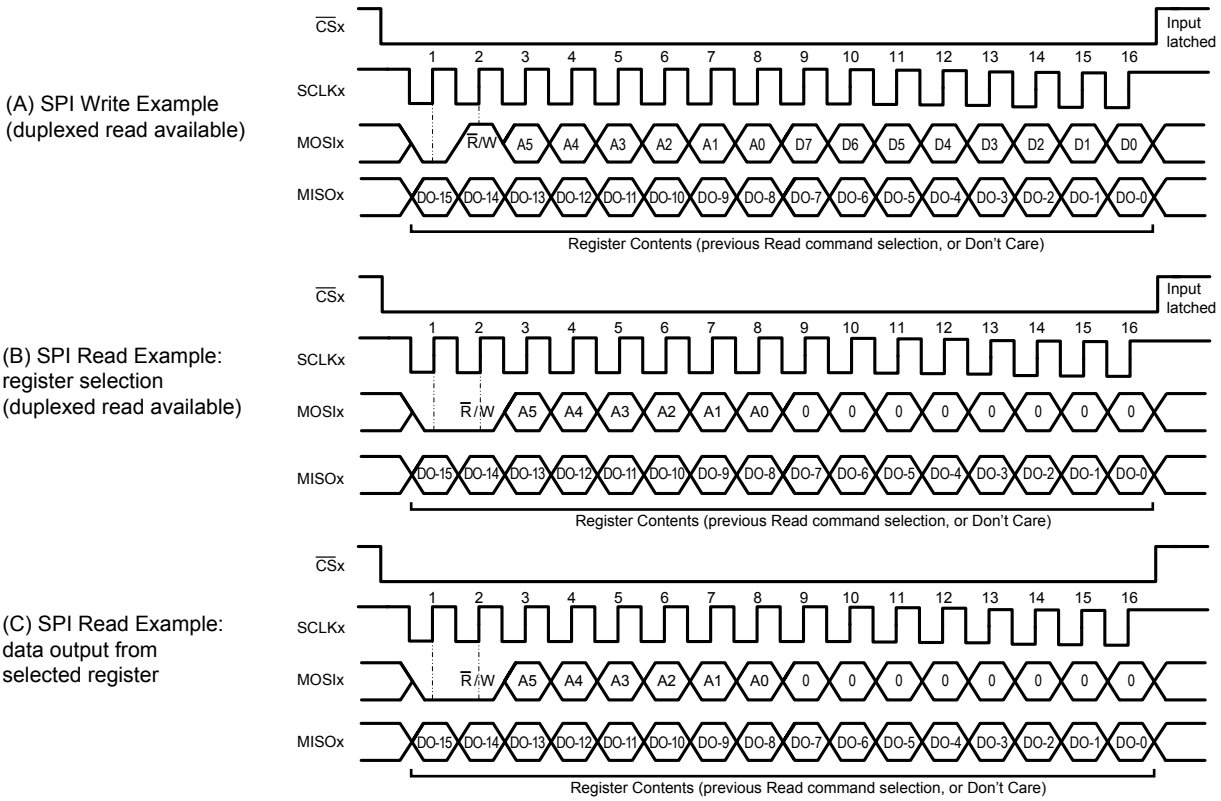

Figure 21: SPI Read and Write Pulse Sequences

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CRC

If the user wants to check the data coming from the sensor, it is possible to use 20-bit SPI frames. Without requiring additional setting, a 4-bit CRC is automatically generated and placed on the MISO line if more than 16 bits are read from the sensor.

The four additional CRC bits on the MOSI line coming from the host are ignored by the sensor, unless the PWI.SC bit is set within EEPROM. When the incoming CRC check is enabled, an incoming SPI packet with an incorrect CRC is discarded, and the CRC error flag is set in serial register WARN.CRC.

The CRC is based on the polynomial $x^4 + x + 1$ with the linear feedback shift register preset to all 1s. The 16-bit packet is shifted through from bit 15 (MSB) to bit 0 (LSB). The CRC logic is shown in Figure 22. Data are fed into the CRC logic with MSB first. Output is sent as C3-C2-C1-C0.

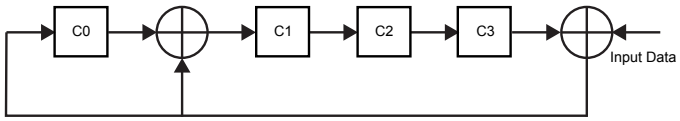

Figure 22: SPI CRC

The CRC output by the sensor on the MISO pin is always calculated correctly. The CRC from the host on the MOSI pin must be correct if the CRC enable bit PWI.SC in the EEPROM iss set.

NOTE: If the extended read data (ERD) register is read before the ERCS.ERD bit indicates a read is complete, there is a possibility of a CRC error, because the data could change during the read. Do not read the ERD register until it is known to be stable based on the completed-bit indication or waiting sufficient time.

The CRC can be calculated with the following C code:

```
/*
* CalculateCRC
*
* Take the 16-bit input and generate a 4-bit CRC
* Polynomial = x^4 + x + 1
* LFSR preset to all 1's
*/
uint8_t CalculateCRC(uint16_t input)
{
 bool CRC0 = true;
 bool CRC1 = true;
 bool CRC2 = true;
 bool CRC3 = true;
 int i;
 bool DoInvert;
 uint16_t mask = 0x8000;

 for (i = 0; i < 16; ++i)
 {
 DoInvert = ((input & mask) != 0) ^ CRC3; // XOR required?

 CRC3 = CRC2;
 CRC2 = CRC1;
 CRC1 = CRC0 ^ DoInvert;
 CRC0 = DoInvert;
 mask >>= 1;
 }

 return (CRC3 ? 8U : 0U) + (CRC2 ? 4U : 0U) + (CRC1 ? 2U :
0U) + (CRC0 ? 1U : 0U);
}
```

This code can be tested at http://codepad.org/jPPW1CQ4.

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Manchester Interface

To facilitate addressable device programming when using the unidirectional PWM output mode with no need for additional wiring, the AAS33001 incorporates a serial interface on the VCC line. All programming can be performed using this interface; all programming can also be performed using the SPI interface.

This interface allows an external controller to read and write registers in the AAS33001 EEPROM and volatile memory. The device uses a point-to-point communication protocol, based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0 and a falling edge indicates a 1), with address and data transmitted MSB first. The addressable Manchester code implementation uses the logic states of the CSN/MOSI pins to set address values for each die. In this way, individual communication with up to four AAS33001 dies is possible. Using a broadcast Manchester command, any die receiving the command responds. To prevent any undesired programming of the AAS33001, the serial interface can be disabled by setting the disable Manchester bit, PWI.DM, to 1. With this bit set, the sensor ignores any Manchester input on VCC.

The setup for communication using the Manchester interface is given in Figure 23.

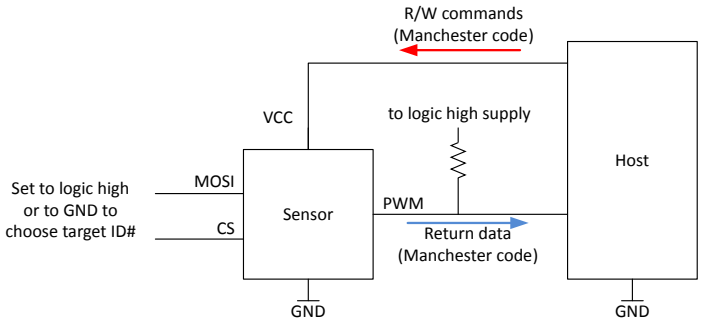

Figure 23: Manchester Interface Programming Setup

CONCEPT OF MANCHESTER COMMUNICATION

The Manchester interface allows programming and readout with a minimal number of pins involved. This is beneficial for sensor subassemblies connected to wiring harnesses, because fewer connections are needed. The supply level is typically modulated between 5 V and 8 V ($V_{MAN(H)}$ and $V_{MAN(L)}$) to produce a low signal and a high signal. In the absence of a clock signal, Manchester encoding is used, allowing the sensor to determine the bit rate that the host is using.

The controller can freely choose any supported Manchester communication frequency for each transaction. The sensor recognizes the transaction speed used by the controller and sends the response at the same data rate.

Because Manchester commands are sent on the supply line, the speed is usually limited by capacitances on the supply line. A reduction of the bit rate, or using a stronger line driver, can help to ensure stable communication.

If a correct read command is sent, the sensor responds to the controller using the open-drain output on the PWM line. The high level is determined by the PWM pull-up (usually 3.3 V or 5 V), and the low level is close to GND. The PWM uses an open-drain output, setting the logic levels to GND and logic level high (see Figure 23). A sufficient pull-up resistor (e.g., 4.7 kΩ) must be used to pull the line to a maximum logic-high level V_{IN}.

ENTERING MANCHESTER COMMUNICATION MODE

Provided the disable Manchester bit is not set in EEPROM, the AAS33001 continuously monitors the VCC line for valid Manchester commands. The part does not take action until a valid Manchester access code is received.

There are two special Manchester code commands used to activate or deactivate the serial interface and to specify the output format used during read operations:

1. Manchester Access Code: Enters Manchester communication mode; Manchester code output on the PWM pin. For an example, see the Manchester Access Code section.
2. Manchester Exit Code: Returns the PWM pin to normal operation. For an example, see the Manchester Exit Code section.

Once the Manchester communication mode is entered, the PWM output pin ceases to provide angle data, interrupting any data transmission in progress.

TRANSACTION TYPES

The AAS33001 receives all commands via the VCC pin and responds to read commands via the PWM pin. This implementation of Manchester encoding requires the communication pulses be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages on the VCC line. Each transaction is initiated by a command from the controller; the sensor does not initiate any transactions. Two commands are recognized by the AAS33001: write and read.

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CONTROLLER MANCHESTER MESSAGE STRUCTURE

The general format of a command message frame is shown in Figure 24. Note that, in the Manchester coding used, a bit value of 1 is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary.

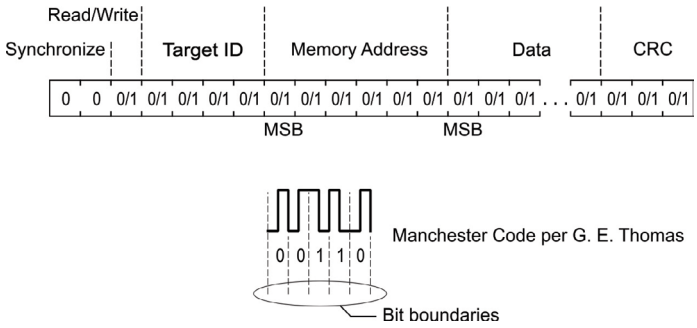

Figure 24: Manchester Message Format

A brief description of the bit fields is provided in Table 5:

Table 5: Manchester Message Bit Fields

Bits	Parameter Name	Description
2	Synchronization	Value 00 sent to identify a command start and to synchronize sensor clock
1	Read/Write	0 = write, 1 = read
4	Target ID	Select the target ID for this transaction [ID3 ID2 ID1 ID0] are each adressed/ ignored by a 1/0 at their address, so that a write to [0011] writes to ID0 and ID1 Reading from several sensors at the same time results in corrupted outputs if the output pins are tied together Writing to [0000] is a broadcast write; it is written to all sensor dies
6	Address	Serial address for read/write
16	Data	Only for writes: 16-bit write data Omit for read commands
3	CRC	3-bit CRC, needed for all commands

When the AAS33001 is operating in PWM mode, the die ID value is determined by the state of the CSN and MOSI pins, as detailed in Table 6.

Table 6: Pin Values

MOSI	CS	ID Value
0	0	ID0
0	1	ID1
1	0	ID2
1	1	ID3

Using the 4 bits of the chip-select field, die can be selected via their ID value, allowing up to four die to be individually addressed and providing for different group-addressing schemes.

Example: If target ID = [1 0 1 0], all die with ID3 or ID1 is selected. If target ID is set to [0 0 0 0], an ID comparison is not performed, allowing all sensors to be addressed at once. In case of PWM line-sharing for Manchester communication, reading must be performed one die at a time.

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SENSOR MANCHESTER MESSAGE STRUCTURE

If a read command with the desired register number is sent from the controller to the sensor, the device responds with a read response frame using the Manchester protocol over the PWM output.

The following command messages can be exchanged between the device and the external controller:

- Manchester Access Code (host to sensor)
- Manchester Exit Code (host to sensor)
- Manchester Write Command (host to sensor)
- Manchester Read Command (host to sensor)
- Manchester Read Response (sensor to host)

In addition to the contents of the requested memory location, a Return Status field is included with every Read Response. This field provides the ID used to communicate with the part and any errors which may have occurred during the transaction. These bits are:

- **ID:** ID (CSN/MOSI) unless BC = 1 (ID is 00)
- **BC:** Broadcast; ID field was zero or SPI mode is active
- **AE:** Abort error; edge-detection failure after synchronization detection
- **OR:** Overrun error; a new Manchester command is received before the previous request completes
- **CS:** Checksum error; a prior command had a checksum error

For EEPROM address information, refer to the EEPROM and Shadow Register Table. For serial address locations, refer to the Primary Serial Interface Registers Reference section.

MANCHESTER ACCESS CODE

The Manchester access code must be sent before other Manchester commands.

The Manchester access code always operates as a broadcast pulse, meaning the sensor does not look at the target ID field. For example, if two sensors configured with ID0 and ID1 respectively are sharing a common VCC line, a Manchester access code with a target ID value of [0 0 1 0] results in both sensors entering Manchester serial communication mode.

Table 7: Manchester Access Code

Bits	Parameter Name	Description
2	Synchronization	00
1	Read/Write	0
4	Target ID	0000 (this command is always a broadcast, even if it is addressed)
6	Address	111111 (fixed number for Manchester access message)
16	Data	0x62D2 (fixed number for Manchester access message)
3	CRC	3-bit CRC

An example is shown in Figure 25, with target ID = [0 0 0 1], data = access code = 0x62D2, and CRC = 110.

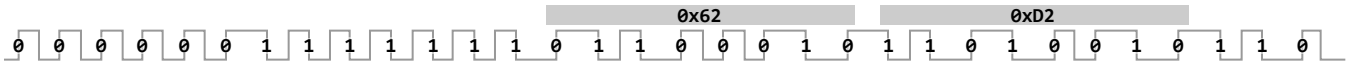

Figure 25: Target ID = [0 0 0 1], Data = Access Code = 0x62D2, CRC = 110

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MANCHESTER EXIT CODE

The Manchester exit code can be sent after Manchester access is complete in order to avoid accidental decoding of Manchester commands.

The Manchester exit code always operates as a broadcast pulse, meaning the sensor does not look at the target ID field. For example, if two sensors configured with ID0 and ID1 respectively are sharing a common VCC line, a Manchester access code with a target ID value of [0 0 1 0] results in both sensors exiting Manchester serial communication mode.

Table 8: Manchester Exit Code

Bits	Parameter Name	Description
2	Synchronization	00
1	Read/Write	0
4	Target ID	0000 (this command is always a broadcast, even if it is addressed)
6	Address	111111 (fixed number for Manchester exit message)
16	Data	0x0000 (any value except 0x62D2 can be used for Manchester exit message)
3	CRC	3-bit CRC

An example is shown in Figure 26, with target ID = [0 0 0 1], data = 0x0000, and CRC = 110.

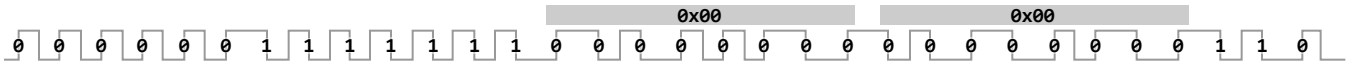

Figure 26: Target ID = [0 0 0 1], Data = 0x0000, CRC = 110

MANCHESTER READ COMMAND

Determines the serial address within the sensor from which the next read response transmits data. The sensor must receive a Manchester access code before responding to a read command.

This command is sent by the controller.

Table 9: Manchester Read Command

Bits	Parameter Name	Description
2	Synchronization	00
1	Read/Write	1
4	Target ID	Depends on targeted sensor ID, e.g., to target ID0, use 0001
6	Address	Serial register address, e.g., 0x10 for READ_DATA_LO, or 0x20 for ANGLE
3	CRC	3-bit CRC

An example is shown in Figure 27, where register 0x20 ANGLE is read from target ID [0 0 0 1] with CRC = 111. The two synchronization pulses from the read response on the PWM return line are also shown.

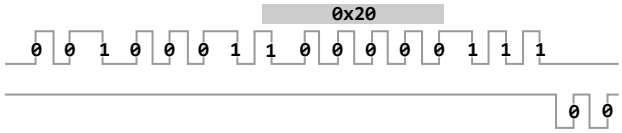

Figure 27: Target ID = [0 0 0 1], ANGLE = 0x20, CRC = 111

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MANCHESTER READ RESPONSE

The read response transmits data from the sensor to the controller after a read command. These data are sent by the sensor on the open-drain PWM pin. A pull-up resistor is needed for this to work.

Read from an even address returns even byte [15:8] and odd byte [7:0].

Read from an odd address returns odd byte [7:0] only. Data bits [15:8] are zeroes.

Table 10: Manchester Read Response

Bits	Parameter Name	Description
2	Synchronization	00
2	ID	Target ID of the responding sensor die. 00 for ID0, 01 for ID1, 10 for ID2, 11 for ID3.
1	BC flag	Broadcast: Value set to 1 if read command was a broadcast command (target ID set to [0 0 0 0]), 0 if not.
1	AE flag	Abort error: Value set to 1 if a previous transaction is aborted and discarded, typically caused by incorrect bit lengths; 0 indicates a problem did not occur. The error is stored until it can be transmitted during the next read response and is cleared afterward.
1	OR flag	Overrun error: If a command is sent to the sensor while the sensor is still sending a read response, and this command is completely transmitted before the read response finishes, an overrun error has occurred. This error is then stored until it can be transmitted during the next read response and is cleared afterward.
1	CS flag	CRC error: Value set to 1 if a previous transaction had an incorrect CRC; 0 indicates a problem did not occur. The error is stored until it can be transmitted during the next read response and is cleared afterward.
16	data	Read from an even address: even byte [15:8] and odd byte [7:0]. Read from an odd address: odd byte [7:0] only. Data bits [15:8] are zeroes.
3	CRC	3-bit CRC.

An example is shown in Figure 28, where register 0x20 angle is read, and the response is ID 00 (ID0), the four flags are all zeroes (no errors), the data is 0x5C34, and the CRC is 100.

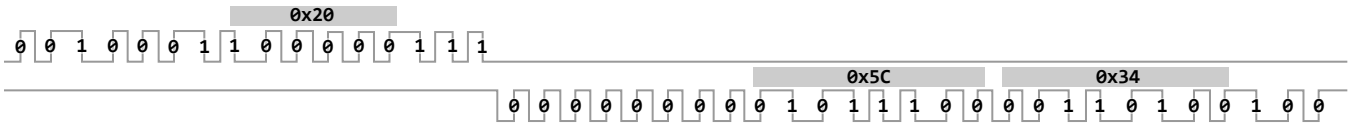

Figure 28: ID = 00, Error Flag = 0000, Data = 0x5C34, CRC = 100

MANCHESTER READ RESPONSE DELAY

The Manchester read reponse starts at the end of the read command. The response may start a ¼-bit time before the CRC finishes transmitting (overlap with last CRC bit) or ¼-bit time after the CRC finishes transmitting.

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CRC

The serial Manchester interface uses a cyclic redundancy check (CRC) for data-bit error checking of all bits that follow the two synchronization bits. The synchronization bits are not included in the CRC. The CRC algorithm is based on the polynomial:

$$g(x) = x^3 + x + 1.$$

The calculation is represented graphically in Figure 29. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111. Data are fed into the CRC logic with MSB first. Output is sent as C2-C1-C0.

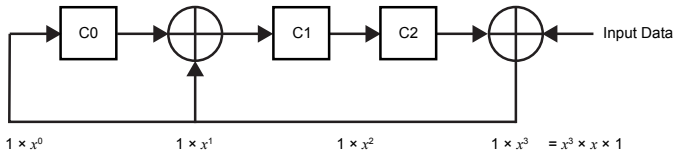

Figure 29: Manchester CRC Calculation

The 3-bit Manchester CRC can be calculated using the following C code:

```
// command: the manchester command, right justified, does not
include the space for the CRC
// numberOfBits: number of bits in the command not including
the 2 zero sync bits at the start of the command and the three
CRC bits
// Returns: The three bit CRC
// This code can be tested at http://codepad.org/yqTKnfmD
uint16_t ManchesterCRC(uint64_t data, uint16_t numberOfBits)
{
 bool C0 = false;
 bool C1 = false;
 bool C2 = false;
 bool C0p = true;
 bool C1p = true;
 bool C2p = true;
 uint64_t bitMask = 1;

 bitMask <<= numberOfBits - 1;

 // Calculate the state machine
 for (; bitMask != 0; bitMask >>= 1)
 {
 C2 = C1p;
 C0 = C2p ^ ((data & bitMask) != 0);
 C1 = C0 ^ C0p;

 C0p = C0;
 C1p = C1;
 C2p = C2;
 }

 return (C2 ? 4U : 0U) + (C1 ? 2U : 0U) + (C0 ? 1U : 0U);
}
```


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EEPROM AND SHADOW MEMORY USAGE

The device uses EEPROM to permanently store configuration parameters for operation. EEPROM is user-programmable and permanently stores operation parameter values or customer information. The operation parameters are downloaded to shadow (volatile) memory at power-up. Shadow fields are initially loaded from corresponding fields in EEPROM, but can be overwritten, either by performing an extended write to the shadow addresses, or by reprogramming the corresponding EEPROM fields and power cycling the IC. Use of shadow memory is substantially faster than accessing EEPROM. In situations where many parameters must be tested quickly, shadow memory is recommended for trying parameter values before permanently programming them into EEPROM. The shadow memory registers have the same format as the EEPROM and are accessed at extended addresses 0x40 higher than the equivalent EEPROM address. Unused bits in the EEPROM do not exist in the related shadow register and return 0 when read. Shadow registers do not contain the ECC bits. Shadow registers have the same protection restrictions as the EEPROM. All registers can be read without unlocking. The mapping of bits from register addresses in EEPROM to the corresponding register addresses in shadow is shown in the EEPROM table (see the EEPROM and Shadow Register Table).

Enabling EEPROM Access

To enable EEPROM write access after power-on reset, an unlock code must be written to the serial register KEYCODE. This involves five write commands, executed one after the other:

1. Write 0x00 to register 0x3C [15:8]
2. Write 0x27 to register 0x3C [15:8]
3. Write 0x81 to register 0x3C [15:8]
4. Write 0x1F to register 0x3C [15:8]
5. Write 0x77 to register 0x3C [15:8]

This process must be performed once after power-on reset if the customer intends to write to the EEPROM.

Writing to serial registers and reading from serial registers does not require the performance of a special process after power-on.

Reading all EEPROM cells is always possible.

EEPROM Write Lock

It is possible to protect the EEPROM against accidental writes.

- Setting the EEPROM field LOCK to the value 0xC (1100 in binary) blocks any writes to the EEPROM, so that permanent changes are not possible anymore. Temporary changes to the setting remain possible by writing to the shadow memory, but these changes are lost after a power cycle.
  This lock is permanent and cannot be reversed. Reading of the settings remains possible.
- Setting the EEPROM field LOCK to the value 0x3 (0011 in binary) locks EEPROM writes AND shadow memory writes. This means none of the sensor settings can be changed anymore.
  This lock is permanent and cannot be reversed. Reading of the settings remains possible.

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EEPROM Access Exceptions and Write Lock Exceptions

It is possible to allow writes to the fields CUST and CUST2 without having to enable EEPROM access, and even when the EEPROM write lock is enabled (LOCK = 0xC or LOCK = 0x3). This is controlled using the EEPROM fields CUD (customer uses disables), DEL (disable EEPROM lock) and DUR (disable unlock requirement). By default, the fields CUD, DEL, and DUR are all set to zero.

These settings control EEPROM access to different fields as shown in Table 11.

Table 11: EEPROM Access Exceptions for CUSTOMER and CUSTOMER2 Fields

CUD Setting	DUR Setting	DEL Setting	LOCK Setting	Writes to CUSTOMER2 (0x17) Possible…	Writes to CUSTOMER (0x1F) Possible…	Writes to All Other EEPROM Possible…
0	0	0/1	0x0	after keycode	after keycode	after keycode
0	1	0/1	0x0	always	after keycode	after keycode
0	0	0	0xC/0x3	never	never	never
0	0	1	0xC/0x3	after keycode	never	never
0	1	0	0xC/0x3	never	never	never
0	1	1	0xC/0x3	always	never	never
1	0	0/1	0x0	after keycode	after keycode	after keycode
1	1	0/1	0x0	always	always	after keycode
1	0	0	0xC/0x3	never	never	never
1	0	1	0xC/0x3	after keycode	after keycode	never
1	1	0	0xC/0x3	never	never	never
1	1	1	0xC/0x3	always	always	never

Write Transaction to EEPROM and Other Extended Locations

Invoking an extended write access is a three-step process:

1. Write the extended address into the EWA register (using SPI or Manchester direct access). EWA is the 8-bit extended address that determines which extended memory address is to be accessed.
2. Write the data that is to be transferred into the EWD registers (using SPI or Manchester direct access). This requires four SPI writes or two Manchester packets to load all 32 bits of data.
3. Invoke the extended access by writing the direct EWCS.EXW bit with 1.

The 32 bits of data in EWD are then written to the address specified in EWA.

The bit EWCS.WDN can be polled to determine when the write completes. This is only necessary for EEPROM writes, which can require up to 24 ms to complete. Shadow register writes complete immediately in one system clock cycle after synchronization.

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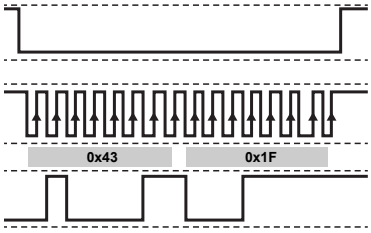
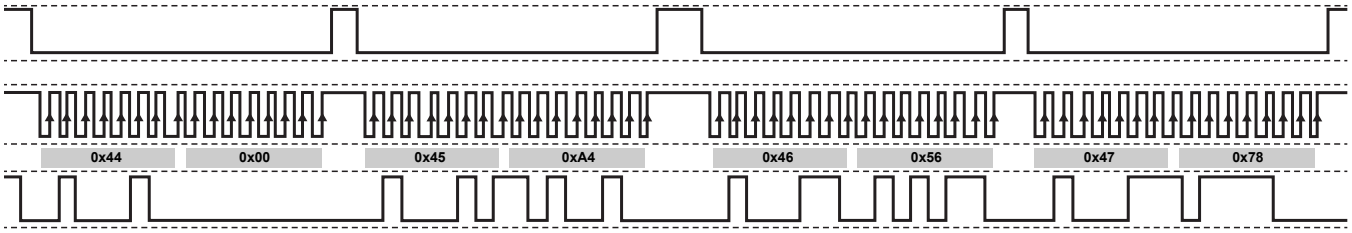
For example, to write location 0x1F in the EEPROM with 0x00A45678:

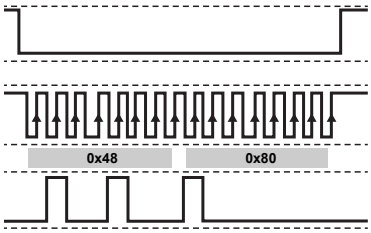
• Write 0x1F to the lower 8 bits of EWA register (0x1F to EWA + 1, address 0x03)



• Write 0x00A45678 to EWD (0x00 to EWD, 0xA4 to EWD + 1, 0x56 to EWD + 2, 0x78 to EWD + 3)

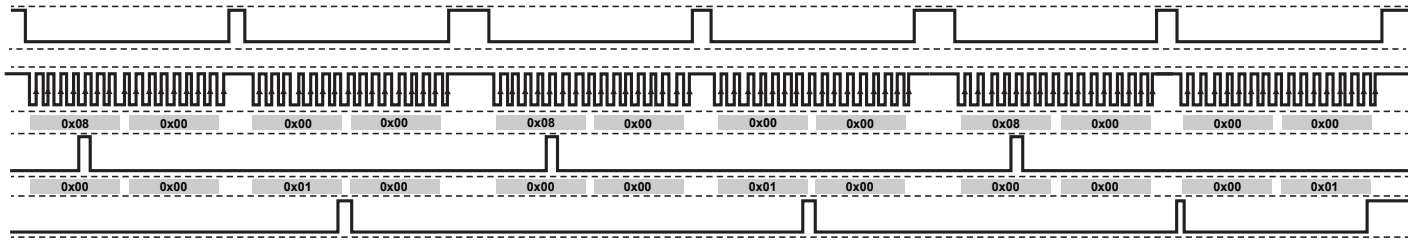


• Write 0x80 to EWCS



• Read EWCS + 1 until bit 0 (WDN) is set, or wait enough time.

In the example, register 0x08 is read, so that the second output byte is from register 0x09, then a waiting period occurs before bit 0 becomes 1, which happens in the last read.



If an access violation occurs (address not unlocked), the transaction terminates, the corresponding RDN or WDN bit becomes set, and the XEE warning bit asserts. The XEE bit in the ERR register also becomes set if the EEPROM write aborts.

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After writing to the EEPROM, verify that the write was successful by performing an EEPROM margin check.

EEPROM Margin Check

Due to nonidealities in transistors, current slowly leaks into or out of EEPROM cells and can, over time, cause small changes in the stored voltage level. Variances in voltage levels of the charge pump can result in a variety of stored EEPROM cell voltages when programming. If this value is marginally close to the threshold, the small drift over lifetime can cause this value to move across the threshold. This results in a corrupted EEPROM value. Because this drift happens slowly over time, if there is an issue, it may not appear for years. For this reason, it is important to perform margin testing (margining) to verify the internal voltage levels of EEPROM cells after programming and to ensure future issues do not occur.

Margining is performed by Allegro on all registers at final test. Because EEPROM cell voltages are only modified when writing to the cell, it is not necessary to perform margining on registers that have not been modified.

Margining is performed in two steps: the first checks the validity of the voltage stored on digital 1 cells, and the second checks the voltage stored on digital 0 cells. It is important to perform both steps to ensure that issues do not occur.

To perform margining, a value of 0b0001 must be written to the SPECIAL field of the CTRL register. This reduces the internal threshold value. Once this value is written, an EEPROM read uses this lower threshold when reading EEPROM values. Perform a read on all EEPROM registers that are being tested, and confirm they read correctly. If a stored voltage is marginal to the typical operating threshold, the value appears as a 1 when it should be a 0.

Repeat this test with the value of 0b0010 in the SPECIAL register to raise the threshold value to greater than the typical operation level. Again, read all EEPROM registers being tested. In this test, any stored high voltage that is marginal to the typical threshold appears as a 0 when the value should be 1.

If, during either test, a bit is read incorrectly, perform another EEPROM write of the desired values to the register, and retest the margins.

Unlike other values in the SPECIAL field, these values persist and can be read to confirm the write is successful. As a result, the SPECIAL register must be cleared (or power cycled) to return the threshold value to its typical level.

In Figure 30, $V_{NOM(H)}$ represents the nominal voltage programmed into EEPROM cells containing a 1, and $V_{NOM(L)}$ represents the nominal voltage programmed into EEPROM cells containing a 0. The red and blue lines represent the actual voltage levels in the programmed cells for 1 and 0 values respectively. As can be observed, at time 0 when the margin test is run, both high and low levels still appear to be the correct value when the threshold is moved to the margin testing levels.

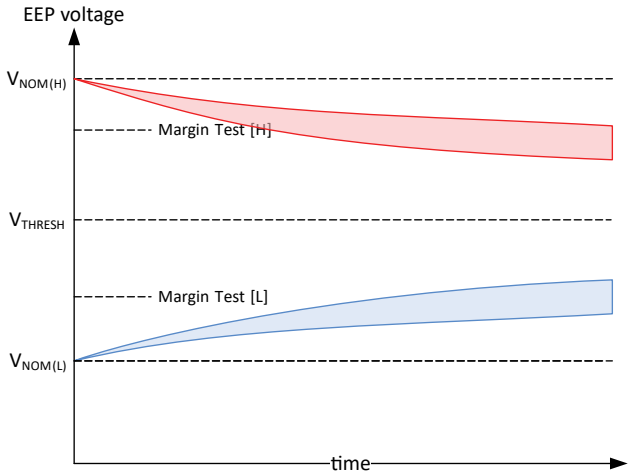

Figure 30: Example of Passing Programming Voltages

In Figure 31, the high and low voltage levels at the time of programming are further from their target. The drift over time results in these values crossing V_{THRESH} and becoming corrupted. At time 0 when the margin test is run, these values fail and are reported as errors to be reprogrammed.

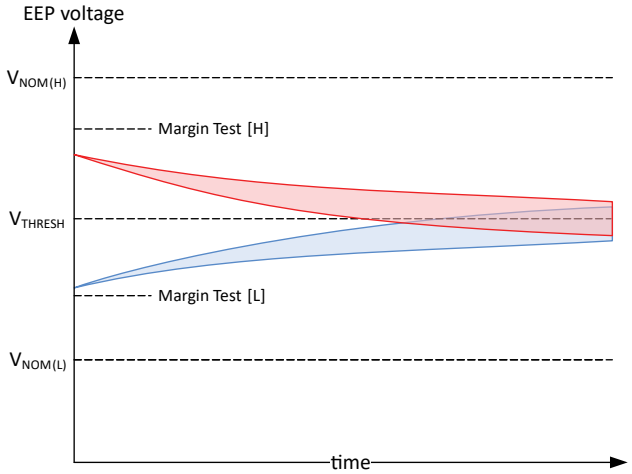

Figure 31: Example of Failing Programming Voltages

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Margining is shown below as a list of high-level steps. For details about performing individual steps, see the associated sections.

1. Clear the ERR and WARN registers.
   A. Set the CTRL.CLW and CTRL.CLE bits.
2. Enable EEPROM access.
3. Write new data to the EEPROM as desired.
4. Check the following flags for EEPROM errors: ESE, EUE, XEE,IER, CRC, and BSY.
   A. If any are asserted, the EEPROM write may have failed.
   B. A second write attempt is recommended.
5. Set CTRL.SPECIAL to 0001b to enable low-voltage margining.
6. Read all EEPROM addresses changed in step 3 and verify their contents.
   A. Verify the ESE and EUE error flags are clear.
7. Set CTRL.SPECIAL to 0010b to enable high-voltage margining.
8. Read all EEPROM addresses changed in step 3 and verify their contents.
   A. Verify the ESE and EUE error flags are clear.
9. If any EEPROM value read with a low or high threshold differs from the desired EEPROM or if either the ESE or EUE bits are set, EEPROM margining has failed.
   A. One additional write attempt and margin check should be accomplished. If margin failures persist following a second EEPROM write, the device should be discarded.

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Read Transaction from EEPROM and Other Extended Locations

Extended access is provided to additional memory space via the direct registers. This access includes the EEPROM and EEPROM shadow registers. All extended registers are up to 32 bits wide. Invoking an extended read access is a three-step process:

1. Write the extended address to be read into the ERA register (using SPI or Manchester direct access). ERA is the 8-bit extended address that determines which extended memory address is to be accessed.
2. Invoke the extended access by writing the direct ERCS.EXT bit with 1. The address specified in ERA is then read, and the data is loaded into the ERD registers.
3. Read the ERD registers (using SPI or Manchester direct access) to get the extended data. Multiple packets are required to obtain all 32 bits.

EEPROM read accesses may require up to 2 µs to complete. The ERCS.RDN bit can be polled to determine if the read access is complete before reading the data. Shadow register reads complete in one system clock cycle after synchronization. Do not attempt to read the ERD registers if the read access is potentially in process, because it could change during the serial access and result in inconsistent data. Also, if the data changes during the serial read via the SPI interface, detection of an SPI CRC error may result.

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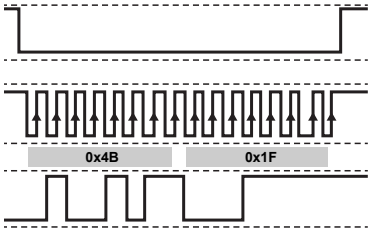
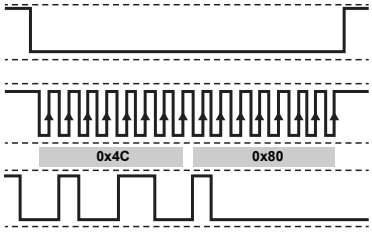
For example, to read location 0x1F in the EEPROM:

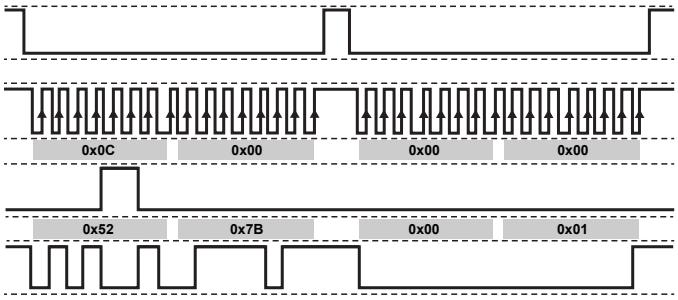
• Write 0x1F to the lower 8 bits of ERA (0x1F to ERA + 1, address 0x0B).



• Write 0x80 to ERCS.

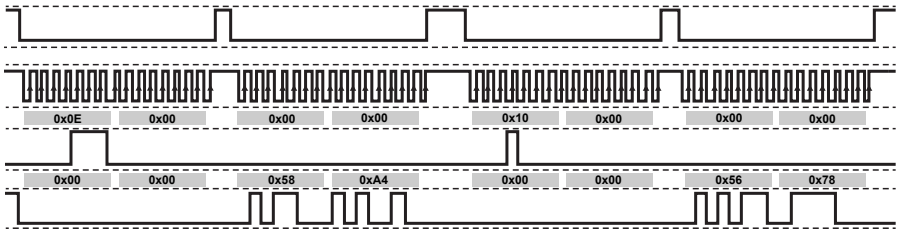


• Read ERCS + 1 until bit 0 (RDN) is set, or wait enough time.
In the example, register 0x0C is read, so that the last bit of the second output byte contains the RDN bit.



• Read ERDH (upper 16 bits of read data).
• Read ERDL (lower 16 bits of read data).
In the example below, the result for the data at address 0x1F is 0x58A45678. In this value,

- □ Bits [31:26] are the EEPROM CRC.
- □ Bits [25:24] are unused and zero.
- □ Bits [23:0] are the EEPROM values that can be used. These are the 24 bits containing the data 0xA45678 that was written in the EEPROM write example.



Note that it would have been possible to pipeline transactions in this example, i.e., send a new command while reading return data from the old command. This way, the transaction could have been performed in five SPI frames instead of eight.

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Shadow Memory Read and Write Transactions

Shadow memory read and write transactions are identical to those for EEPROM. Instead of the EEPROM extended address, the shadow extended memory is addressed. These addresses are located at an offset of 0x40 greater than the EEPROM. For all addresses, refer to the EEPROM and Shadow Register Table.

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SERIAL INTERFACE TABLE

Table 12: Primary Serial Interface Registers Bits Map

Address [1] (0x00)	Register Symbol	Read/ Write	Addressed Byte (MSB)								Addressed Byte + 1 (MSB)								LSB Address
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x02	EWA	RW	0	0	0	0	0	0	0	0	WRITE_ADR								0x03
0x04	EWDH	RW	WRITE_DATA_HI																0x05
0x06	EWDL	RW	WRITE_DATA_LO																0x07
0x08	EWCS	WO/RO	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN	0x09
0x0A	ERA	RW	0	0	0	0	0	0	0	0	READ_ADR								0x0B
0x0C	ERCS	WO/RO	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN	0x0D
0x0E	ERDH	RO	READ_DATA_HI																0x0F
0x10	ERDL	RO	READ_DATA_LO																0x11
0x12 0x14 0x16 0x18 0x1A 0x1C	*Unused*	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x13 0x15 0x17 0x19 0x1B 0x1D
0x1E	CTRL	RW/WO	SPECIAL				0	CLS	CLW	CLE	INITIATE_SPECIAL								0x1F
0x20	ANG	RO	0	EF	UV	P	ANGLE												0x21
0x22	STA	RO	1	0	0	0	0	0	DIEID		ROT	0	SDN	BDN	LBR	CSTR	BIP	AOK	0x23
0x24	ERR	RO	1	0	1	0	WAR	STF	AVG	ABI	PLK	ZIE	EUE	OFE	UVD	UVA	MSL	RST	0x25
0x26	WARN	RO	1	0	1	1	IER	CRC	0	SRW	XEE	TR	ESE	SAT	0	BSY	MSH	0	0x27
0x28	TSEN	RO	1	1	1	1	TEMPERATURE												0x29
0x2A	FIELD	RO	1	1	1	0	GAUSS												0x2B
0x2C	*Unused*	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x2D
0x2E	*Unused*	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x2F
0x30	HANG	RO	0	EF	UV	P	ANGLE_HYS												0x31
0x32	ANG15	RO	0	ANGLE_15															0x33
0x34	ZANG	RO	0	EF	UV	P	ANGLE_ZCD												0x35
0x36	*Unused*	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x37
0x38	*Unused*	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x39
0x3A	*Unused*	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x3B
0x3C	KEY	WO/RO	KEYCODE								0	0	0	0	0	0	0	CUL	0x3D
0x3E	*Unused*	RO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x3F

[1] Addresses that span multiple bytes are addressed by the most significant byte.

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PRIMARY SERIAL INTERFACE REGISTERS REFERENCE

Location 0x02:0x03 (EWA)

EWA.WRITE_ADR

The field WRITE_ADR is a bit field located at address 0x02 [7:0]. This bit field is part of the location EWA.

8-bit address for extended writes. Writes require unlock.

0x00:0x1F—EEPROM (takes about 24 ms)
0x40:0x5F—Shadow

Location 0x04:0x05 (EWDH)

EWDH.WRITE_DATA_HI

The field WRITE_DATA_HI is a bit field located at address 0x04 [15:0]. This bit field is part of the location EWDH.

Upper 16 bits of data for an extended write operation.

Location 0x06:0x07 (EWDL)

EWDL.WRITE_DATA_LO

The field WRITE_DATA_LO is a bit field located at address 0x06 [15:0]. This bit field is part of the location EWDL.

This is the lower 16 bits of data for an extended write operation.

Location 0x08:0x09 (EWCS)

EWCS.WDN

The field WDN is a bit located at address 0x08 [0]. This bit is part of the location EWCS.

Write is complete when WDN = 1; WDN clears when EXW is set to 1.

EWCS.WIP

The field WIP is a bit located at address 0x08 [8]. This bit is part of the location EWCS.

Write in progress when 1.

EWCS.EXW

The field EXW is a bit located at address 0x08 [15]. This bit is part of the location EWCS.

Initiate extended write by writing with 1. Set WIP and clears WDN. Write-only, always reads back 0.

Location 0x0A:0x0B (ERA)

ERA.READ_ADR

The field READ_ADR is a bit field located at address 0x0A [7:0]. This bit field is part of the location ERA.

8-bit address for extended reads.

0x00:0x1F—EEPROM (takes about 2 µs)
0x40:0x5F—Shadow

NOTE: After LBIST or a reload of EEPROM values, the value of READ_ADR is changed.

Location 0x0C:0x0D (ERCS)

ERCS.RDN

The field RDN is a bit located at address 0x0C [0]. This bit is part of the location ERCS.

Read done when 1, clears when EXR set to 1.

ERCS.RIP

The field RIP is a bit located at address 0x0C [8]. This bit is part of the location ERCS.

Read in progress when 1.

ERCS.EXR

The field EXR is a bit located at address 0x0C [15]. This bit is part of the location ERCS.

Initiate extended read by writing with 1. Set RIP and clears RDN. Write-only, always reads back 0.

Location 0x0E:0x0F (ERDH)

ERDH.READ_DATA_HI

The field READ_DATA_HI is a bit field located at address 0x0E [15:0]. This bit field is part of the location ERDH.

Upper 16 bits of data from extended read operation, valid when RDN is set to 1.

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Location 0x10:0x11 (ERDL)

ERDL.READ_DATA_LO

The field READ_DATA_LO is a bit field located at address 0x10 [15:0]. This bit field is part of the location ERDL.

This is the lower 16 bits of data from the extended read operation; it is valid when RDN is set to 1.

Location 0x1E:0x1F (CTRL)

CTRL.INITIATE_SPECIAL

The field INITIATE_SPECIAL is a bit field located at address 0x1E [7:0]. This bit field is part of the location CTRL.

For certain actions from the SPECIAL bit field, a code must be set to INITIATE_SPECIAL. These codes are to be written into this bit field:

- 0xB9 initiates CVH self-test or functional BIST.
- 0xA5 initiates EEPROM margin or EEPROM reload.
- 0x5A initiates hard reset.

Read always returns 0x00.

CTRL.CLE

The field CLE is a bit located at address 0x1E [8]. This bit is part of the location CTRL.

Clear error register ERR when written with 1. Clears bits previously read from the ERR. Unread bits are not cleared; therefore, the user needs to read ERR first. Write-only, always returns 0.

CTRL.CLW

The field CLW is a bit located at address 0x1E [9]. This bit is part of the location CTRL.

Clear warning (WARN) register when set to 1. Clears bits previously read from WARN; therefore, WARN should be read first. Write-only, always returns 0.

CTRL.CLS

The field CLS is a bit located at address 0x1E [10]. This bit is part of the location CTRL.

Clear bits SDN and BDN from STATUS register when set to 1. Write-only, returns 0 when read.

CTRL.SPECIAL

The field SPECIAL is a bit field located at address 0x1E [15:12]. This bit field is part of the location CTRL.

Special actions. Some of the actions are only invoked after the INITIATE_SPECIAL field is written with the correct value. This field returns 0x00 upon completion. Self-tests may be run in parallel.

0000—No action.
0001—Enable EEPROM low-voltage margining.
0010—Enable EEPROM high-voltage margining.
0101—Reload EEPROM. Requires unlock of part. Starts after writing 0xA5 to INITIATE_SPECIAL.
0111—Hard reset. Requires unlock of part. Starts after writing 0x5A to INITIATE_SPECIAL.
1001—Run CVH self-test. Starts after writing 0xB9 to INITIATE_SPECIAL.
1010—Run logic BIST. Starts after writing 0xB9 to INITIATE_SPECIAL.
1011—Run CVH self-test and logic-BIST in parallel. Starts after writing 0xB9 to INITIATE_SPECIAL.

Location 0x20:0x21 (ANG)

ANG.ANGLE

The field ANGLE is a bit field located at address 0x20 [11:0]. This bit field is part of the location ANG.

Angle from PLL after processing. Angle in degrees = unsigned 12-bit value × (360 / 4096).

ANG.P

The field P is a bit located at address 0x20 [12]. This bit is part of the location ANG.

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of ones in the 16-bit word.

ANG.UV

The field UV is a bit located at address 0x20 [13]. This bit is part of the location ANG.

Undervoltage flag (real time). OR of UVA and UVD undervoltage flags. Conditions are real time, but are masked by the shadow mask bits.

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ANG.EF

The field EF is a bit located at address 0x20 [14]. This bit is part of the location ANG.

Error flag—If any unmasked bit in ERR or WARN is set, the value is 1.

Location 0x22:0x23 (STA)

STA.AOK

The field AOK is a bit located at address 0x22 [0]. This bit is part of the location STA.

Angle output OK. PLL is in lock

STA.BIP

The field BIP is a bit located at address 0x22 [1]. This bit is part of the location STA.

Boot in progress.

STA.CSTR

The field CSTR is a bit located at address 0x22 [2]. This bit is part of the location STA.

CVH self-test running.

STA.LBR

The field LBR is a bit located at address 0x22 [3]. This bit is part of the location STA.

LBIST running.

STA.BDN

The field BDN is a bit located at address 0x22 [4]. This bit is part of the location STA.

Boot complete. EEPROM loaded and any startup self-tests are complete.

STA.SDN

The field SDN is a bit located at address 0x22 [5]. This bit is part of the location STA.

Special access (from CTRL register) done. Clears to 0 when SPECIAL triggered, set 1 when complete.

STA.ROT

The field ROT is a bit located at address 0x22 [7]. This bit is part of the location STA.

Rotation direction based on hysteresis
(0 = increasing angle, 1 = decreasing angle).

STA.DIEID

The field DIEID is a bit field located at address 0x22 [9:8]. This bit field is part of the location STA.

DIE ID from EEPROM (for multi-die packages).

Location 0x24:0x25 (ERR)

This is the error register. All errors are latched, meaning an error remains high after a single occurrence. To remove the errors, each must be read, then cleared. It is important that the user clears errors, so that subsequent errors become visible. This is especially important for the RST error flag (reset), which is always enabled after power-on. If the RST error flag is not removed, a subsequent unexpected reset cannot be discovered.

ERR.RST

The field RST is a bit located at address 0x24 [0]. This bit is part of the location ERR.

Reset condition. Sets on power-on reset or on hard reset. Does not set on LBIST.

ERR.MSL

The field MSL is a bit located at address 0x24 [1]. This bit is part of the location ERR.

Magnetic sense low fault. Magnetic sense was below the MAG_THRES_LO limit.

ERR.UVA

The field UVA is a bit located at address 0x24 [2]. This bit is part of the location ERR.

Undervoltage detector tripped. If the undervoltage situation persists after it is cleared, it becomes set again. Based on analog regulator.

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ERR.UVD

The field UVD is a bit located at address 0x24 [3]. This bit is part of the location ERR.

Undervoltage detector tripped. If the undervoltage situation persists after it is cleared, it becomes set again.

ERR.OFE

The field OFE is a bit located at address 0x24 [4]. This bit is part of the location ERR.

Oscillator frequency watchdog tripped.

ERR.EUE

The field EUE is a bit located at address 0x24 [5]. This bit is part of the location ERR.

EEPROM uncorrectable error. A multi-bit EEPROM read occurred.

ERR.ZIE

The field ZIE is a bit located at address 0x24 [6]. This bit is part of the location ERR.

Zero-crossing integrity error. A zero-crossing did not occur within the maximum time expected, likely indicating a missing magnet, an extreme rotation speed, or a sensor defect.

ERR.PLK

The field PLK is a bit located at address 0x24 [7]. This bit is part of the location ERR.

PLL lost lock.

ERR.ABI

The field ABI is a bit located at address 0x24 [8]. This bit is part of the location ERR.

ABI integrity fault. The quadrature integrity of the ABI could not be maintained.

ERR.AVG

The field AVG is a bit located at address 0x24 [9]. This bit is part of the location ERR.

Angle-averaging error. The ORATE is too high for the velocity and the averaging is corrupted.

ERR.STF

The field STF is a bit located at address 0x24 [10]. This bit is part of the location ERR.

Self-test failure.

ERR.WAR

The field WAR is a bit located at address 0x24 [11]. This bit is part of the location ERR.

Warning. Some unmasked error bits are set in the WARN register. If WAR in mask register MSK is set, this bit is forced to 0.

Location 0x26:0x27 (WARN)

WARN.MSH

The field MSH is a bit located at address 0x26 [1]. This bit is part of the location WARN.

Magnetic sense high fault. Magnetic sense has exceeded the MAG_THRES_HI limit.

WARN.BSY

The field BSY is a bit located at address 0x26 [2]. This bit is part of the location WARN.

Extended access overflow. An EXW or EXR was initiated while a previous extended read or write was in progress.

WARN.SAT

The field SAT is a bit located at address 0x26 [4]. This bit is part of the location WARN.

Aggregate saturation flag. Shows that any internal signals are saturated; the likely cause is extremely strong or weak fields.

WARN.ESE

The field ESE is a bit located at address 0x26 [5]. This bit is part of the location WARN.

EEPROM soft error. A correctable (single-bit) EEPROM read occurred.

WARN.TR

The field TR is a bit located at address 0x26 [6]. This bit is part of the location WARN.

Temperature out of range. The temperature sensor calculated a temperature below –60°C or above 180°C. Temperature saturates at those limits.

WARN.XEE

The field XEE is a bit located at address 0x26 [7]. This bit is part of the location WARN.

Extended execute error. A command initiated by an extended write failed. Write failed due to access error (not unlocked) or

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EEPROM write failure.

WARN.SRW

The field SRW is a bit located at address 0x26 [8]. This bit is part of the location WARN.

Slew-rate warning. This warning asserts if the ABI slew-rate limiting is enabled and a condition that requires the limiting to be applied occurs.

WARN.CRC

The field CRC is a bit located at address 0x26 [10]. This bit is part of the location WARN.

Incoming SPI CRC error. Packet was discarded.

WARN.IER

The field IER is a bit located at address 0x26 [11]. This bit is part of the location WARN.

Interface error. Invalid number of bits in SPI packet, or bit 15 of MOSI data = 1. Packet was discarded.

Also Manchester error.

Location 0x28:0x29 (TSEN)

TSEN.TEMPERATURE

The field TEMPERATURE is a bit field located at address 0x28 [11:0]. This bit field is part of the location TSEN.

Current junction temperature from internal temperature sensor relative to 25°C (signed value). Value is in 1/8 of a degree. Temperature °C = (TSEN.TEMPERATURE / 8) + 25.0.

Location 0x2A:0x2B (FIELD)

FIELD.GAUSS

The field GAUSS is a bit field located at address 0x2A [11:0]. This bit field is part of the location FIELD.

Field strength in gauss.

Location 0x30:0x31 (HANG)

HANG.ANGLE_HYS

The field ANGLE_HYS is a bit field located at address 0x30 [11:0]. This bit field is part of the location HANG.

Angle from PLL after processing. Angle in degrees = unsigned 12-bit value × (360 / 4096).

HANG.P

The field P is a bit located at address 0x30 [12]. This bit is part of the location HANG.

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of ones in the 16-bit word.

HANG.UV

The field UV is a bit located at address 0x30 [13]. This bit is part of the location HANG.

Undervoltage flag (real time). OR of analog and digital UV flags. Conditions are in real time but are masked by the shadow mask bits.

HANG.EF

The field EF is a bit located at address 0x30 [14]. This bit is part of the location HANG.

Error flag. If any unmasked bit in ERR or WARN is set, the value of this bit is 1.

Location 0x32:0x33 (ANG15)

ANG15.ANGLE_15

The field ANGLE_15 is a bit field located at address 0x32 [14:0]. This bit field is part of the location ANG15.

15-bit compensated angle (not rounded).

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Location 0x34:0x35 (ZANG)

ZANG.ANGLE_ZCD

The field ANGLE_ZCD is a bit field located at address 0x34 [11:0]. This bit field is part of the location ZANG.

This is the angle from the zero-crossing detector and it is used to verify that the PLL angle is correct.

Angle in degrees = unsigned 12-bit value × (360 / 4096).

ZANG.P

The field P is a bit located at address 0x34 [12]. This bit is part of the location ZANG.

Odd parity computed across all bits of this register. Value is chosen in such a way that there should always be an odd number of ones in the 16-bit word.

ZANG.UV

The field UV is a bit located at address 0x34 [13]. This bit is part of the location ZANG.

Undervoltage flag (real time). OR of analog and digital UV flags. Conditions are in real time but are masked by the shadow mask bits.

ZANG.EF

The field EF is a bit located at address 0x34 [14]. This bit is part of the location ZANG.

Error flag. If any unmasked bit in ERR or WARN is set, the value of this bit is 1.

Location 0x3C:0x3D (KEY)

KEY.CUL

The field CUL is a bit located at address 0x3C [0]. This bit is part of the location KEY.

Customer unlocked if 1.

KEY.KEYCODE

The field KEYCODE is a bit field located at address 0x3C [15:8]. This bit field is part of the location KEY.

Customer access keycode is entered here, using five subsequent write commands with the numbers: 0x00, 0x27, 0x81, 0x1F, and 0x77.

Always reads back 0.

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EEPROM AND SHADOW REGISTER TABLE

The EEPROM register bitmap is shown below. Addresses that span multiple bytes are addressed by the most significant byte.

All EEPROM content can be read by the user. The EEPROM ECC field in bits [31:26] of each word are not shown here. Bits [25:24] of each EEPROM word are unused and not shown here but are included in the ECC.

Table 13: EEPROM / Shadow Memory Map

EEPROM Address	Shadow Memory Address	Register Name	Bits																							
			23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x17	–	CU2	CUSTOMER 2																							
0x18	0x58	PWE	–	–	–	–	–	–	–	–	–	–	–	–	TR	MSH	SAT	ESE	MSL	UV	AVG	ZIE	PLK	STF	EUE	OFE
0x19	0x59	ABI	–	–	ABI_SLEW_TIME						INV	–	–	AHE	–	–	INDEX_MODE		WDH	PLH	IOE	UVW	RESOLUTION_PAIRS			
0x1A	0x5A	MSK	IERM	CRCM	–	SRWM	XEEM	TRM	ESEM	SATM	–	BSYM	MSHM	–	WARM	STFM	AVGM	ABIM	PLKM	ZIEM	EUEM	OFEM	UVDM	UVAM	MSLM	RSTM
0x1B	0x5B	PWI	PEN	PWM_BAND			PWM_FREQ				–	PHE	PEO	PES	ELI	LS	–		ZAL	–			DM	–	S17	SC
0x1C	0x5C	ANG	ORATE				RD	RO	HYSTERESIS						ZERO_OFFSET											
0x1D	0x5D	–	–	–	–	–	–	–	CYCLE_TIME						–	–	–	–	–	–	–	–	–	–	–	–
0x1E	0x5E	COM	LOCK				LBE	CSE	DUR	DEL	–	CUD	DST	DHR	MAG_THRES_HI						MAG_THRES_LO					
0x1F	–	CUS	CUSTOMER																							
0x20	0x60	LIN00	Linearization Error Segment 1												Linearization Error Segment 0											
0x21	0x61	LIN01	Linearization Error Segment 3												Linearization Error Segment 2											
…	…	…	…												---											
0x2E	0x6E	LIN14	Linearization Error Segment 29												Linearization Error Segment 28											
0x2F	0x6F	LIN15	Linearization Error Segment 31												Linearization Error Segment 30											
–	0x80	ALV	Alive counter																							

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EEPROM REFERENCE

Location 0x17 (CU2)

Customer-usable field, intended for storing data.

This word can be written even if EEPROM is locked. Write may be allowed without the unlock code based on COM.DUR and COM.DEL settings (see word 0x1E).

CU2.CUSTOMER 2

The field CUSTOMER 2 is a bit field located at address 0x17 [23:0]. This bit field is part of the location CU2.

Customer-usable field, intended for storing data.

Depending on COM.DUR and COM.DEL settings, this word can be written even if EEPROM is locked. Details are given in the EEPROM Write Lock section.

Location 0x18 (PWE)

PWE.OFE

The field OFE is a bit located at address 0x18 [0]. This bit is part of the location PWE.

PWM oscillator frequency watchdog error enable. Duty cycle output 5% at half the selected PWM frequency.

PWE.EUE

The field EUE is a bit located at address 0x18 [1]. This bit is part of the location PWE.

PWM EEPROM uncorrectable error enable. Duty cycle 10.625% at half the selected PWM frequency.

PWE.STF

The field STF is a bit located at address 0x18 [2]. This bit is part of the location PWE.

PWM self-test failure error enable. Duty cycle 16.25% at half the selected PWM frequency.

PWE.PLK

The field PLK is a bit located at address 0x18 [3]. This bit is part of the location PWE.

PWM PLL lost lock error enable. Duty cycle 21.875% at half the selected PWM frequency.

PWE.ZIE

The field ZIE is a bit located at address 0x18 [4]. This bit is part of the location PWE.

PWM zero-crossing integrity error enable. Duty cycle 27.5% at half the selected PWM frequency.

PWE.AVG

The field AVG is a bit located at address 0x18 [5]. This bit is part of the location PWE.

PWM angle averaging error enable. Duty cycle is 33.125% at half the selected PWM frequency.

PWE.UV

The field UV is a bit located at address 0x18 [6]. This bit is part of the location PWE.

PWM undervoltage fault enable (analog or digital). Duty cycle 38.75% at half the selected PWM frequency.

PWE.MSL

The field MSL is a bit located at address 0x18 [7]. This bit is part of the location PWE.

PWM magnetic sense low fault enable. Duty cycle 44.375% at half the selected PWM frequency.

PWE.ESE

The field ESE is a bit located at address 0x18 [8]. This bit is part of the location PWE.

PWM EEPROM soft error enable. Duty cycle 50% at half the selected PWM frequency.

PWE.SAT

The field SAT is a bit located at address 0x18 [9]. This bit is part of the location PWE.

PWM saturation warning enable. Duty cycle 55.625% at half the selected PWM frequency.

PWE.MSH

The field MSH is a bit located at address 0x18 [10]. This bit is part of the location PWE.

PWM magnetic sense high fault enable. Duty cycle 61.25% at half the selected PWM frequency.

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PWE.TR

The field TR is a bit located at address 0x18 [11]. This bit is part of the location PWE.

PWM temperature sensor out of range error enable. Duty cycle 66.875% at half the selected PWM frequency.

Location 0x19 (ABI)

ABI.RESOLUTION_PAIRS

The field RESOLUTION_PAIRS is a bit field located at address 0x19 [3:0]. This bit field is part of the location ABI.

ABI or UVW resolution.

If ABI is selected, this selects AB cycle counts per rotation. Cycle count = $2^{(14-n)}$, where n is selected code.

If UVW is selected, this is the number of pole pairs minus 1.

ABI.UVW

The field UVW is a bit located at address 0x19 [4]. This bit is part of the location ABI.

Incremental outputs UVW (1), ABI (0).

ABI.IOE

The field IOE is a bit located at address 0x19 [5]. This bit is part of the location ABI.

Incremental output pins enable (see UVW).

ABI.PLH

The field PLH is a bit located at address 0x19 [6]. This bit is part of the location ABI.

Enable ABI all high (before inversions) as error mode if PLL is unlocked.

ABI.WDH

The field WDH is a bit located at address 0x19 [7]. This bit is part of the location ABI.

Enable ABI all high (before inversions) as error mode if high-frequency watchdog trips.

ABI.INDEX_MODE

The field INDEX_MODE is a bit field located at address 0x19 [9:8]. This bit field is part of the location ABI.

ABI index mode, defines width and placement of index pulse.

- Mode 0: Angle = 0
- Mode 1: Angle = –R or 0
- Mode 2: Angle = –R, 0 or +R
- Mode 3: Angle = –2R, –R, 0 or +R

ABI.AHE

The field AHE is a bit located at address 0x19 [12]. This bit is part of the location ABI.

ABI hysteresis enable. If 1, use hysteresis on angle going to ABI.

ABI.INV

The field INV is a bit located at address 0x19 [15]. This bit is part of the location ABI.

Invert ABI or UVW signals.

ABI.ABI_SLEW_TIME

The field ABI_SLEW_TIME is a bit field located at address 0x19 [21:16]. This bit field is part of the location ABI.

ABI slew-rate limit. The value 0 indicates the slew-rate limiter is disabled. Otherwise, (N + 1) × 125 ns (nominal) is the minimum edge-to-edge time for the ABI output. This limits the maximum ABI velocity. Reducing the ABI output resolution may be useful to counteract this effect.

Location 0x1A (MSK)

MSK.RSTM

The field RSTM is a bit located at address 0x1A [0]. This bit is part of the location MSK.

Reset mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.MSLM

The field MSLM is a bit located at address 0x1A [1]. This bit is part of the location MSK.

Magnetic sense low fault mask. If set to 1, the corresponding error does not affect the error flag EF.

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MSK.UVAM

The field UVAM is a bit located at address 0x1A [2]. This bit is part of the location MSK.

Analog undervoltage fault mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.UVDM

The field UVDM is a bit located at address 0x1A [3]. This bit is part of the location MSK.

Digital undervoltage fault mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.OFEM

The field OFEM is a bit located at address 0x1A [4]. This bit is part of the location MSK.

Oscillator frequency watchdog error mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.EUEM

The field EUEM is a bit located at address 0x1A [5]. This bit is part of the location MSK.

EEPROM uncorrectable error mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.ZIEM

The field ZIEM is a bit located at address 0x1A [6]. This bit is part of the location MSK.

Zero-crossing integrity error mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.PLKM

The field PLKM is a bit located at address 0x1A [7]. This bit is part of the location MSK.

PLL lost lock error mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.ABIM

The field ABIM is a bit located at address 0x1A [8]. This bit is part of the location MSK.

ABI integrity fault mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.AVGM

The field AVGM is a bit located at address 0x1A [9]. This bit is part of the location MSK.

Angle averaging fault mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.STFM

The field STFM is a bit located at address 0x1A [10]. This bit is part of the location MSK.

Self-test failure error mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.WARM

The field WARM is a bit located at address 0x1A [11]. This bit is part of the location MSK.

If set to 1, does not set WAR bit in the ERR register when unmasked warnings are present.

MSK.MSHM

The field MSHM is a bit located at address 0x1A [13]. This bit is part of the location MSK.

Magnetic sense high fault mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.BSYM

The field BSYM is a bit located at address 0x1A [14]. This bit is part of the location MSK.

Indirect access busy error mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.SATM

The field SATM is a bit located at address 0x1A [16]. This bit is part of the location MSK.

Aggregate saturation flag mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.ESEM

The field ESEM is a bit located at address 0x1A [17]. This bit is part of the location MSK.

EEPROM soft error mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.TRM

The field TRM is a bit located at address 0x1A [18]. This bit is part of the location MSK.

Temperature sensor out of range error mask. If set to 1, the cor-

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responding error does not affect the error flag EF.

MSK.XEEM

The field XEEM is a bit located at address 0x1A [19]. This bit is part of the location MSK.

Execute error mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.SRWM

The field SRWM is a bit located at address 0x1A [20]. This bit is part of the location MSK.

Slew-rate warning mask. If set to 1, the corresponding error does not affect the error flag EF.

MSK.CRCM

The field CRCM is a bit located at address 0x1A [22]. This bit is part of the location MSK.

CRC error mask (SPI). If set to 1, the corresponding error does not affect the error flag EF.

MSK.IERM

The field IERM is a bit located at address 0x1A [23]. This bit is part of the location MSK.

Interface error mask. If set to 1, the corresponding error does not affect the error flag EF.

Location 0x1B (PWI)

PWI.SC

The field SC is a bit located at address 0x1B [0]. This bit is part of the location PWI.

SPI CRC (incoming) is validated if SC = 1, ignored if SC = 0.

PWI.S17

The field S17 is a bit located at address 0x1B [1]. This bit is part of the location PWI.

SPI ignore 17th clock to allow negative edge host sampling.

PWI.DM

The field DM is a bit located at address 0x1B [3]. This bit is part of the location PWI.

Disable Manchester interface. If 1, any Manchester input on VCC is ignored.

PWI.ZAL

The field ZAL is a bit located at address 0x1B [7]. This bit is part of the location PWI.

Zero offset after linearization:

- 0 = Before linearization and rotation
- 1 = After linearization

PWI.LS

The field LS is a bit located at address 0x1B [10]. This bit is part of the location PWI.

Linearization scale:

- 0 = ±22.5 degrees
- 1 = ±45 degrees

PWI.ELI

The field ELI is a bit located at address 0x1B [11]. This bit is part of the location PWI.

Enable linearization:

- 0 = Disabled
- 1 = Enabled

PWI.PES

The field PES is a bit located at address 0x1B [12]. This bit is

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part of the location PWI.

PWM error select (if PEO = 1).

- 0: PWM tristated, must reset (or set PEO back to 0 in shadow) to release the PWM output.
- 1: PWM carrier frequency halved and highest-priority error output on PWM as selected duty cycle. See PWM Output section for more details.

PWI.PEO

The field PEO is a bit located at address 0x1B [13]. This bit is part of the location PWI.

PWM error output enable. If 1, PES selects the response to an enabled error (see ABE word).

PWI.PHE

The field PHE is a bit located at address 0x1B [14]. This bit is part of the location PWI.

PWM hysteresis enable. If 1, use hysteresis on angle going to PWM.

PWI.PWM_FREQ

The field PWM_FREQ is a bit field located at address 0x1B [19:16]. This bit field is part of the location PWI.

PWM frequency select. See PWM Output section for more details.

PWI.PWM_BAND

The field PWM_BAND is a bit field located at address 0x1B [22:20]. This bit field is part of the location PWI.

PWM frequency band. See PWM Output section for more details.

PWI.PEN

The field PEN is a bit located at address 0x1B [23]. This bit is part of the location PWI.

PWM enable = 1. If 0, PWM is tristate.

Location 0x1C (ANG)

ANG.ZERO_OFFSET

The field ZERO_OFFSET is a bit field located at address 0x1C [11:0]. This bit field is part of the location ANG.

Post-compensation zero offset (or DC adjust) at angle resolution. This value is subtracted from the measured angle.

ANG.HYSTERESIS

The field HYSTERESIS is a bit field located at address 0x1C [17:12]. This bit field is part of the location ANG.

Angle hysteresis threshold, angle resolution × 4 (14 bit). Range is approximately 0 to 1.384 degrees.

ANG.RO

The field RO is a bit located at address 0x1C [18]. This bit is part of the location ANG.

Rotation direction (prelinearization). If set to 0, increasing angle movement is in the clockwise direction when looking down on the top of the die. If set to 1, increasing angle movement is in the counter-clockwise direction.

ANG.RD

The field RD is a bit located at address 0x1C [19]. This bit is part of the location ANG.

Rotate die. Rotates final angle by 180 degrees. This is the last step in the angle-processing algorithm. The sensor is Allegro factory-calibrated to deliver identical field directions for both dies. If the user wants the two outputs to be 180° offset from each other, this setting is a convenient way to do so.

ANG.ORATE

The field ORATE is a bit field located at address 0x1C [23:20]. This bit field is part of the location ANG.

Reduces the output rate by averaging samples. 2^{ORATE} samples are to be averaged. ORATE values greater than 12 are reduced to 12 in the logic, meaning that up to 4096 samples = 4 ms can be selected as averaging time.

Location 0x1D (LPC)

LPC.CYCLE_TIME

The field CYCLE_TIME is a bit field located at address 0x1D [17:12]. This bit field is part of the location LPC.

Alive counter increment rate, in 8.192 ms increments with cycle time = [(N + 1) × 8.192 ms].

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Location 0x1E (COM)

COM.MAG_THRES_LO

The field MAG_THRES_LO is a bit field located at address 0x1E [5:0]. This bit field is part of the location COM.

Magnetic field low comparator value, field value equals low field error threshold in gauss divided by 16.

If set to 0, low threshold is disabled.

00 0000: Low field flag disabled
00 0001: 16 gauss
00 0010: 32 gauss
…
00 1101: 208 gauss (factory setting)
…
11 1111: 1108 gauss

COM.MAG_THRES_HI

The field MAG_THRES_HI is a bit field located at address 0x1E [11:6]. This bit field is part of the location COM.

Magnetic field high comparator value, field value equals maximum field threshold in gauss divided by 32. If set to 0, high threshold is disabled.

00 0000: High field flag disabled
00 0001: 32 gauss
00 0010: 64 gauss
…
10 0101: 1184 gauss (factory setting)
…
11 1111: 2016 gauss

COM.DHR

The field DHR is a bit located at address 0x1E [12]. This bit is part of the location COM.

Disable hard reset in serial CTRL register SPECIAL if 1.

COM.DST

The field DST is a bit located at address 0x1E [13]. This bit is part of the location COM.

Disable self-test initiation in serial CTRL register SPECIAL if 1.

COM.CUD

The field CUD is a bit located at address 0x1E [14]. This bit is part of the location COM.

If 1, the CUSTOMER word 0x1F uses the DUR and DEL configuration in addition to the CUSTOMER2 word 0x17.

COM.DEL

The field DEL is a bit located at address 0x1E [16]. This bit is part of the location COM.

Disable EEPROM lock for CUST2 (EEPROM word 0x17) and, if CUD = 1, CUST word 0x1F. EEPROM lock does not affect writeability of word 0x17 (and 0x1F if enabled).

COM.DUR

The field DUR is a bit located at address 0x1E [17]. This bit is part of the location COM.

Disable unlock requirement for CUST2 (EEPROM word 0x17) and if CUD = 1, CUST word 0x1F.

COM.CSE

The field CSE is a bit located at address 0x1E [18]. This bit is part of the location COM.

Enable CVH self-test at power-up.

COM.LBE

The field LBE is a bit located at address 0x1E [19]. This bit is part of the location COM.

Power-up logic BIST enable.

COM.LOCK

The field LOCK is a bit field located at address 0x1E [23:20]. This bit field is part of the location COM.

Lock options:

1100 Lock EEPROM writes
0011 Lock EEPROM writes AND indirect register writes

Location 0x1F (CUS)

CUS.CUSTOMER

The field CUSTOMER is a bit field located at address 0x1F [23:0]. This bit field is part of the location CUS.

Customer-usable field, intended for storing data.

With certain settings, this word can be written even if EEPROM is locked. Details are provided in the EEPROM Write Lock section.

If COM.CUD = 1, then, depending on COM.DUR and COM.DEL settings, this word can be written even if EEPROM is

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locked. Details are provided in the EEPROM Write Lock section.

Location 0x20 (LIN00)

LIN00.LINEARIZATION_ERROR_SEGMENT_0

The field LINEARIZATION_ERROR_SEGMENT_0 is a bit field located at address 0x20 [11:0]. This bit field is part of the location LIN00.

Correction value at segment boundary. Signed, resolution is based on LS bit. Value is subtracted from sensor angle to produce linearized angle.

- For LS = 0, range is ±22.5 degrees.
- For LS = 1, range is ±45 degrees.

LIN00.LINEARIZATION_ERROR_SEGMENT_1

The field LINEARIZATION_ERROR_SEGMENT_1 is a bit field located at address 0x20 [23:12]. This bit field is part of the location LIN00.

Correction value at segment boundary. Signed, resolution is based on LS bit. Value is subtracted from sensor angle to produce linearized angle.

- For LS = 0, range is ±22.5 degrees.
- For LS = 1, range is ±45 degrees.

NOTE: Linearization segments 2 through 29 are omitted from this datasheet for reasons of brevity.

Location 0x2F (LIN15)

LIN15.LINEARIZATION_ERROR_SEGMENT_30

The field LINEARIZATION_ERROR_SEGMENT_30 is a bit field located at address 0x2F [11:0]. This bit field is part of the location LIN15.

Correction value at segment boundary. Signed, resolution is based on LS bit. Value is subtracted from sensor angle to produce linearized angle.

- For LS = 0, range is ±22.5 degrees.
- For LS = 1, range is ±45 degrees.

LIN15.LINEARIZATION_ERROR_SEGMENT_31

The field LINEARIZATION_ERROR_SEGMENT_31 is a bit field located at address 0x2F [23:12]. This bit field is part of the location LIN15.

Correction value at segment boundary. Signed, resolution is based on LS bit. Value is subtracted from sensor angle to produce linearized angle.

- For LS = 0, range is ±22.5 degrees.
- For LS = 1, range is ±45 degrees.

Location 0x80 (ALV)

ALV.ALIVE_COUNTER

The field ALIVE_COUNTER is a bit field located at address 0x80 [31:0]. This bit field is part of the location ALV.

Alive counter is a 32-bit counter, which increments periodically from zero after power-on or hard reset. The alive increment period is based on the EEPROM CYCLE_TIME, which has a resolution of 8.192 ms. The alive counter can overflow. The counter overflow period is [2^{32} × 8.192 × (CYCLE_TIME + 1)] milliseconds. At CYCLE_TIME = 0, this period is approximately 400 days.

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SAFETY AND DIAGNOSTICS

The AAS33001 was developed in accordance to the ASIL design flow. It incorporates several diagnostics.

Alive Counter

A 32-bit counter increments periodically from zero after power-on or hard reset. It is read via an extended read at address 0x80. The alive increment period is based on the EEPROM CYCLE_TIME, which has a resolution of 8.192 ms.

The alive counter can overflow. The overflow period of the counter is $[2^{32} \times 8.192 \times (\text{LPM\_CYCLE\_TIME} + 1)]$ milliseconds. At LPM_CYCLE_TIME = 0, this period is approximately 400 days.

Oscillator Watchdogs

The watchdogs run constantly. These watchdogs are intended to detect gross failures of either oscillator. Logic running on clocks based on each oscillator effectively counts clock periods produced in the other clock domain and compares the value to the expected limits.

Logic Built-In Self-Test (LBIST)

Logic BIST is implemented to verify the integrity of the AAS33001 logic. It can be executed in parallel with the CVH self-test. LBIST is effectively a form of auto-driven scan. The logic to be tested is broken into 31 scan chains. The chains are fed in parallel by a 31-bit linear feedback shift register (LFSR) to generate pseudo-random data. The output of the scan chains are fed back into a multiple-input shift register (MISR) that accumulates the shifted bits into a 31-bit signature. LBIST typically requires 30 ms to verify.

CVH Self-Test

CVH self-test is a method of verifying the operation of the CVH transducer without applying an external magnetic field. This feature is useful for both manufacturing test and for integration debug. The CVH self-test is implemented by changing the switch configuration from the typical operating mode into a test configuration, allowing a test current to drive the CVH in place of the magnetic field. By changing the direction of the test current and by changing the elements in the CVH that are driven, the self-test circuit emulates a changing angle of magnetic field. The measured angle is monitored to determine a passing or failing device.

CVH self-test typically requires 30 ms to verify.

Self-test can be run on power-up, by setting the EEPROM field COM.CSE = 1

Self-test can also be invoked via the serial control register by issuing the corresponding special command.

The test is complete when either:

- STA.SDN = 1 (special done), or
- STA.CSTR = 0 (CVH self-test not running).

Failure is indicated by:

- ERR.STF = 1 (assuming it was cleared before test was run).

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APPLICATION INFORMATION

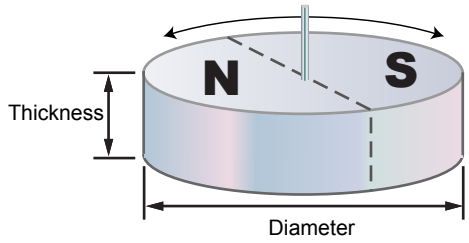
Magnetic Target Requirements

The AAS33001 is designed to operate with magnets constructed with a variety of magnetic materials, geometries, and field strengths. For a list of common magnet dimensions, see Table 14.

The AAS33001 actively measures and adapts to its magnetic environment. This allows operation throughout a large range of field strengths (recommended range is 300 to 1000 G; however, operation beyond this range does not result in long-term damage). Due to the greater signal-to-noise ratio provided at higher field strengths, performance inherently increases with increasing field strength.

Table 14: Target Magnet Parameters

Magnetic Material	Diameter (mm)	Thickness (mm)
Neodymium (Sintered) [1]	10	2.5
Neodymium (Sintered)	8	3
Neodymium/SmCo	6	2.5



[1] A sintered neodymium magnet with 10 mm (or greater) diameter and 2.5 mm thickness is the recommended magnet for redundant applications.

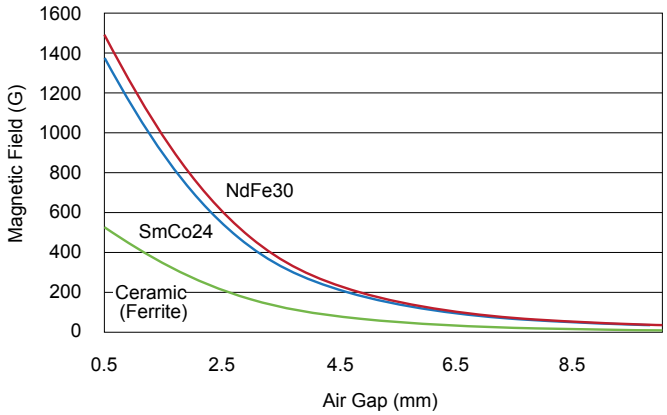


Figure 32: Magnetic Field versus Air Gap for a Magnet 6 mm in Diameter and 2.5 mm Thick.

Allegro can provide similar curves for customer application magnets upon request. Allegro recommends larger magnets for applications that require optimized accuracy performance.

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Typical SPI and ABI/UVW Applications

Below, typical application diagrams for SPI and ABI are given. Programming and controlling are possible using the SPI interface and the Manchester interface. The Manchester programming interface is useful for low-pin-count applications (e.g., ABI). For details about programming with this interface, see the Manchester Interface section.

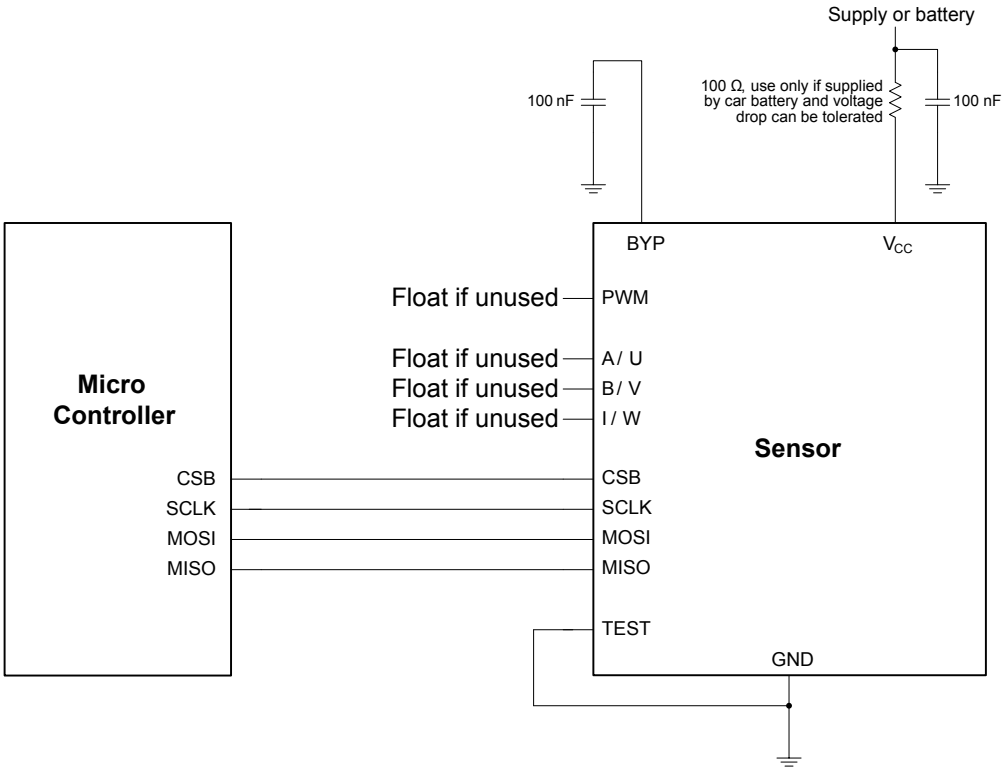

Figure 33: Typical SPI Application Diagram

Notes:

- PWM and ABI/UVW can be used in parallel to the SPI interface.

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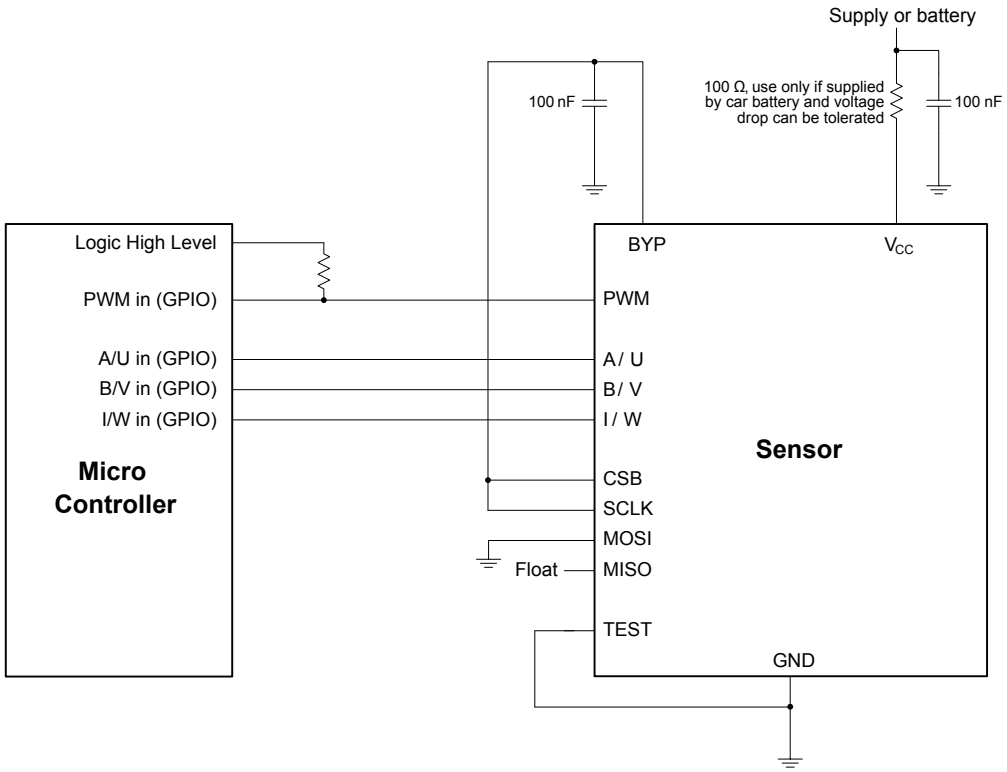

Figure 34: Typical ABI/UVW Application Diagram

Notes:

- PWM output can be left floating if not required. The absolute position is transferred through ABI pins after power-on, so that PWM data is not needed to find the start position. The AAS33001 is different from the A1333 in this regard.
- For programming the sensor, CSB and MOSI determine the peripheral address. For more details, refer to the Manchester Interface section.
- If not needed by the host, any of the ABI outputs can be left floating. For example:
  - □ If only rotational frequency is needed, it is possible to use only pin A.
  - □ If frequency and position is needed, but direction is always the same, it is possible to use only pin B and pin I.

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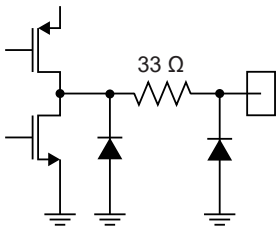
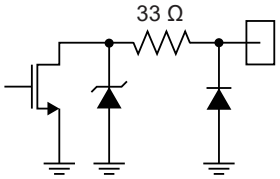
I/O STRUCTURES

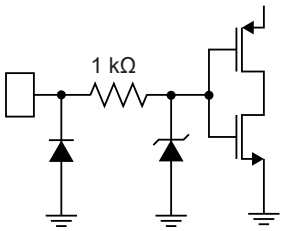
A/U, B/V, I/W, MISO



PWM



SCK/CSN/MOSI



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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use
(Reference MO-153 ADT)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

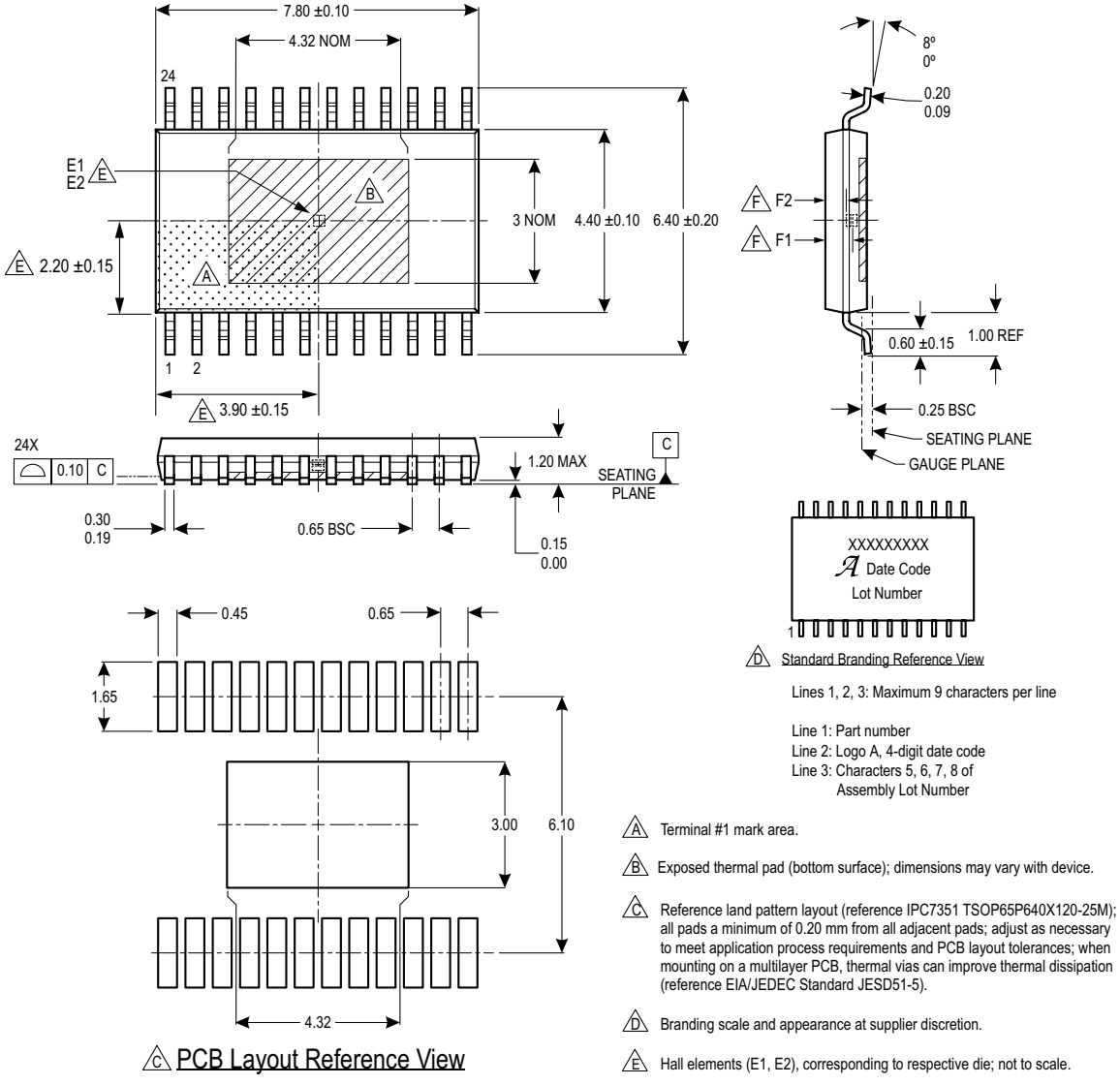

Figure 35: Package LP, 24-Pin TSSOP with Exposed Thermal Pad

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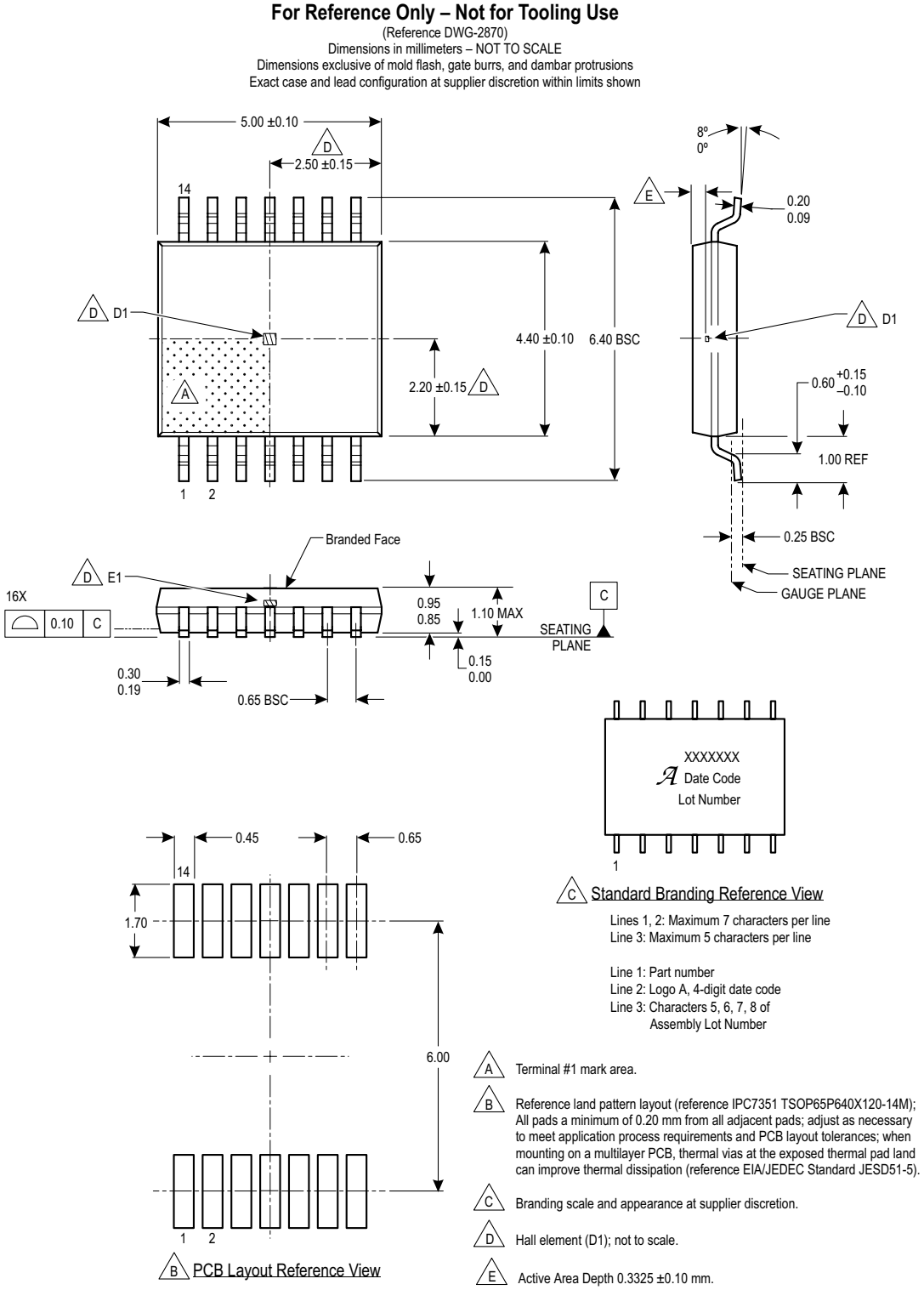

Figure 36: Package LE, 14-Pin TSSOP

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Revision History

Number	Date	Description
–	March 28, 2018	Initial release
1	September 4, 2018	Updated Selection Guide (page 3) and Terminal List table (page 4)
2	October 4, 2019	Updated Selection Guide (page 3), Bypass Pin Output Voltage (page 5), Reverse Battery Current test conditions (page 5), Output High Voltage test conditions (page 5), and minor editorial updates.
3	October 25, 2019	Updated Table 12 (page 41) and I/O Structures (page 60).
4	July 13, 2020	Updated LE-14 and LP-24 package drawing Hall element tolerances (p. 61-62)
5	December 22, 2021	Updated Features and Benefits to indicate completion of ASIL assessment (page 1).
6	January 24, 2024	Updated Table 1 (page 9), Linearization section (page 12), Figure 8 (page 16), Table 13 (page 48), ANG.RO register (page 53), CHV Self-Test section (page 56), and updated all registers to current standard (uppercase).
7	May 14, 2024	Corrected reverse voltage specification (page 3), updated EEPROM margin test (page 37) and made minor editorial corrections throughout (all pages) including: removal of archaic language (master changed to controller, slave changed to peripheral, and normal changed to typical), removal of future tense (“will”) wherever possible, minimization of use of title case (except for headings and captions), removal of trailing zeros to the right of decimal points, and addition of hyperlinks for cross-referenced sections.
8	June 5, 2025	Updated ASIL branding and text (page 1)

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