MT8365 IoT Application Processor Datasheet

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1 Introduction

The MT8365 is a highly integrated solution for wireless connected multimedia systems with the following key features:

- Quad-core Arm® Cortex®-A53 64-bit processor
- Arm Mali™-G52 MC1 3D Graphics Accelerator (GPU) with Vulkan® 1.1, OpenGL ES 3.2 and OpenCL™ 2.0 full profile
- AI Processor Unit (APU) Cadence® Tensilica® VP6 processor, 700 MHz at 0.825 V
- Single-core Cadence HiFi 4 Audio Engine DSP
- Dual MIPI® Camera Serial Interface (CSI)
- Dual display support with MIPI DSI and LVDS/HDMI™ outputs
- Rich audio interfaces to support various microphones and speakers configurations
- Advanced Wi-Fi®/Bluetooth®, GNSS, and FM Radio connectivity
- 10/100 Ethernet MAC with RMII

Figure 1-1 shows the functional block diagram of the device.

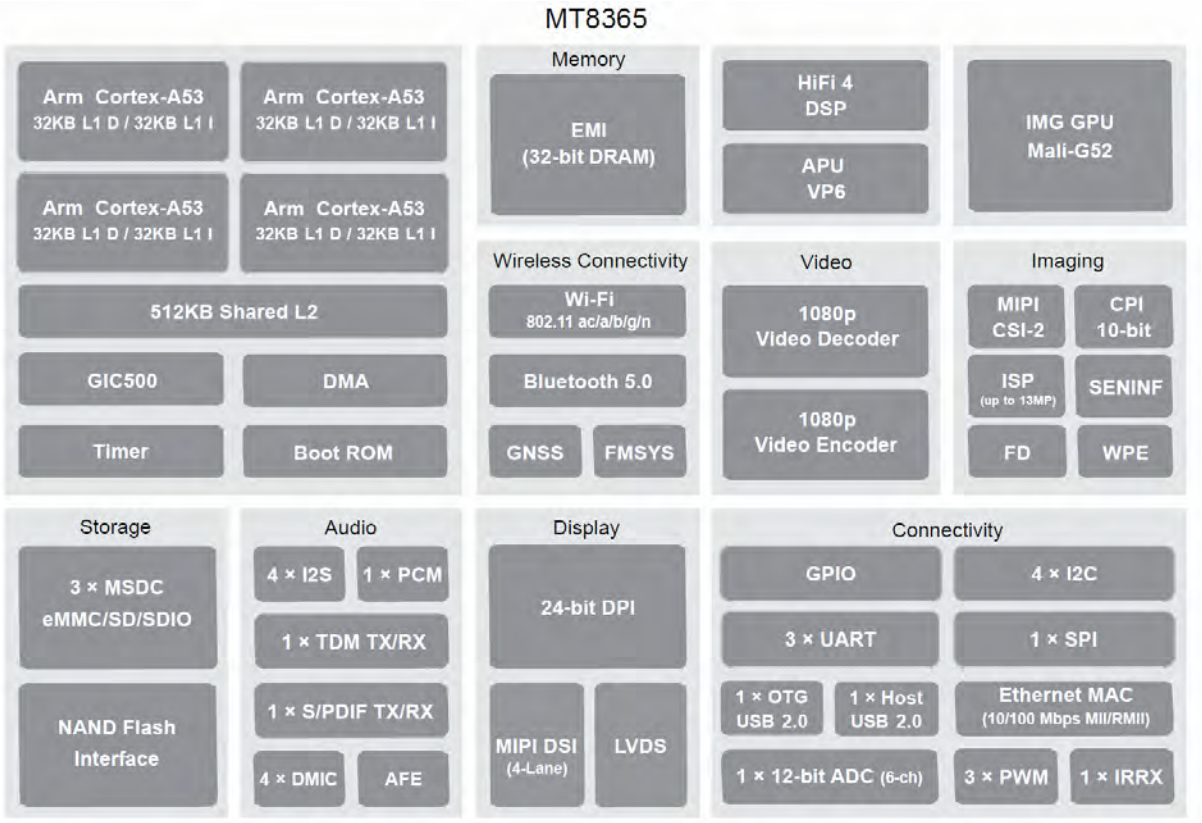

Figure 1-1 Functional Block Diagram

1.1 Features Overview

Table 1-1 shows a summary of the device feature.

Table 1-1 Device Features

Feature		MT8365
Processors		
Quad-core Arm Cortex-A53	CPU	Up to 2000 MHz (see Section 6.1)
Graphics Accelerator	GPU	Up to 800 MHz (see Section 6.1)
AI Processor Unit	APU	Up to 700 MHz (see Section 6.1)
HiFi 4 DSP	DSP	Up to 600 MHz (see Section 6.1)

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Feature		MT8365
Memory		
External Memory Interface (LPDDR3, DDR3/L, DDR4, and LPDDR4/X)	EMI	Up to 4GB DDR-3200 (see Section 6.1)
Storage		
Memory Card Controller eMMC/SD/SDIO	MSDC0	eMMC (8-bit)
	MSDC1	Wi-Fi / SD Card (4-bit)
	MSDC2	Wi-Fi / SD Card (4-bit)
NAND Flash Interface	NFI	Yes
Display		
Display Controller	DISP	Concurrent dual display
Display Parallel Interface	DPI	24-bit(1)
MIPI Display Serial Interface	DSI	4-lane(2)
Low Voltage Differential Signaling	LVDS	Single link (4-lane)(1)
Imaging		
Image Signal Processor	ISP	13MP at 30fps
Camera Parallel Interface	CPI	10-bit
MIPI Camera Serial Interface CSI-2	CSI	2 × 4-lane
Face Detection 5.0	FD	Yes
Warp Engine	WPE	Yes
Sensor Interface	SENINF	Yes
Video		
Video Encoder	VENC	H.264, 1080p at 60fps
JPEG Encoder	JPEG	15 quantization methods
Video Decoder	VDEC	H.264/HEVC, 1080p at 60fps
Audio		
Inter-IC Sound	I2S0	Master/Slave input(3)
	I2S1	Master output
	I2S2	Master input
	I2S3	Master output
Pulse Code Modulation	PCM	1
Pulse Density Modulation	PDM	4
Digital Microphone	DMIC	4
Time Division Multiplexed Interface	TDM_RX	8 RX(4)
	TDM_TX	8 TX(4) 1/2/4 data lane(s)
Sony/Philips Digital Interface	S/PDIF_IN	Yes
	S/PDIF_OUT	Yes
Audio Front-End (AFE)	DAC	2-channel
	ADC	2-channel (3 input ports)
Connectivity		
Inter-Integrated Circuit	I2C	4
Universal Asynchronous Receiver/Transmitter	UART	3
Infrared Receiver	IRRX	1
Serial Peripheral Interface	SPI	Master mode only
Universal Serial Bus, USB2.0	USB0	OTG
	USB1	Host only
10M/100M Ethernet Network Interface Controller	EMAC	MII and RMII
KeyPad Scanner	KeyPad	2 × 2
General Purpose I/O pins	GPIO	145
Pulse Width Modulation	PWM	Up to 3

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Feature		MT8365
Wireless Connectivity		
Wireless Communication Module (WCM)	Wi-Fi	Dual band 2.5 GHz and 5 GHz
	BT	Bluetooth 5.0
	GNSS	Yes
	FMSYS	Yes
Miscellaneous		
JTAG® Interface	JTAG	Yes
PMIC Interface	PWRAP	Yes
Auxiliary ADC	AUXADC	12-bit
Timers	GPT	5 × 32-bit
	SYSTMR	64-bit
	WDT[5]	Yes

1. DPI and LVDS interfaces are not concurrent.
2. LVDS interface is muxed with DSI.
3. Maximum input sampling frequency for slave mode is ≤ 48 kHz.
4. Master mode only.
5. The Watch Dog Timer (WDT) is a part of Top Reset Generation Unit (TOPRGU).

1.2 Ordering Information

Table 1-2 shows the available ordering part numbers.

Table 1-2 Ordering Information

Part Number	Package	Operational Temperature Range
MT8365V/B	VFBGA	See Table 5-3 Recommended Operating Conditions

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2 Preface

2.1 Pin Characteristics and Signal Descriptions Conventions

Table 2-1 describes the column headers in all Pin Characteristic and Signal Description tables in Section 4.2 Pin Characteristics and Chapter 3 Features Description.

Table 2-1 Column Headers Description

Column Name	Explanations
Ball Name	Logical name of the ball
Ball Location	Associated balls. Note that there may be several signals associated with the same ball
Signal Name	The name of the signal for the given aux mode
Type	Pin type when configured for the given aux mode: • AI: Analog input • AO: Analog output • AIO: Analog bi-directional pin • DI: Digital input • DO: Digital output • DIO: Digital bi-directional pin • P: Power • G: Ground
Description	Description of the signal
Aux. Function	Auxiliary function mode number: • 0 through 7 are possible alternative functions • An empty box means Not Applicable
Reset State	Shows the Aux. function configured at the release of the SYSRSTB signal
Buffer Type	Describes the associated input/output buffer type
Power Domain	Indicates the voltage supply that powers the terminal IO buffers
PU/PD	Indicates the state of an internal pull-up or pull-down resistor at the release of the SYSRSTB signal: • OFF: Internal pull-up and pull-down are disabled • PU: Pull-up is enabled • PD: Pull-down is enabled • No: Pull-up and pull-down not available • Blank cell means "No"
IO Reset Value	Shows the IO state at the release of the SYSRSTB signal

2.2 Timing Conventions, Parameters, and Information

This section provides a general description of used symbols, adopted standards and terminology, and test process. All timing characteristics are valid over the represented operating conditions unless otherwise specified.

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The interface clock frequency documented in this datasheet is the maximum clock frequency, which corresponds to the maximum programmable frequency on the particular output clock. The frequency defines the maximum limit supported by the device and does not consider into account any system limitation (layouts, connectors, and so forth).
The system designer should take into account these system considerations and the device timing characteristics as well and should determine properly the maximum frequency supported to transfer the data on the corresponding interface.

The timing parameter values do not include delays by board routes. Timing values may be adjusted by increasing/decreasing such delays. If needed, external logic hardware such as buffers may be used to compensate any timing differences.

2.2.1 Timing Parameters and Information

Table 2-2 represents timing parameter symbols and descriptions used in the timing characteristic tables.

Table 2-2 Timing Parameters

Symbol	Description
f_{op}	Operating frequency
t_p	Period (cycle time)
t_d	Delay time
t_{dis}	Disable time
t_{en}	Enable time
t_h	Hold time
t_{su}	Setup time
Start	Start bit
t_t	Transition time
t_v	Valid time
t_w	Pulse duration
t_{FALL}	Fall time
t_{RISE}	Rise time
V_{OH}	High level output voltage
V_{OL}	Low level output voltage
V_{IH}	High level input voltage
V_{IL}	Low level input voltage
V_{REF}	Reference voltage

2.2.2 Parameter Information

This datasheet provides timing values at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be also taken into account.

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

All rise and fall transition timing parameters are referenced correspondingly to 90% and 10% of the signal logical levels, unless otherwise specified.

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2.3 Abbreviations

3

3GPP
3rd Generation Partnership Project

A

A-GPS
Assisted GPS
ACCDET
Accessory Detector
AI
Artificial Intelligence
ALE
Address Latch Enable
APB
Advanced Peripheral Bus
API
Application Programming Interface
APU
AI Processor Unit
AXI
Advanced eXtensible Interface

B

BLE
Bluetooth Low Energy
bps
Bits Per Second
BT
Bluetooth
BTA
Bus Turnaround
BW
BandWidth

C

CABC
Content Adaptive Backlight Control
CCK
Complementary Code Keying
CDM
Charged Device Model
CE
Chip Enable
CLE
Command Latch Enable
CLK
Clock

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CPHA

Clock Phase

CPOL

Clock Polarity

CRC

Cyclic Redundancy Check

CSI

Camera Serial Interface

CTI

Cross Trigger Interface

CTM

Cross Trigger Matrix

CV

Computer Vision

D

DE

Data Enable

DISM

Digital Interface Standard for Monitor

DISP

Display Controller

DISP_AAL

Display Adaptive Ambient Light

DISP_CCORR

Display Color Correction

DISP_COLOR

Display Color

DISP_DITHER

Display Dither

DISP_GAMMA

Display GAMMA

DISP_MUTEX

Display MUTEX

DISP_OVL

Display Overlay

DISP_PWM

Display Pulse Width Modulation

DISP_RDMA

Display Data Path Read DMA

DISP_RSZ

Display Resizer

DISP_WDMA

Display Write Direct Memory Access

DL

Downlink

DMA

Direct Memory Access

DMEM

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Data Memory

DPI

Display Parallel Interface

DQS

Data Strobe

DRAM

Dynamic Random Access Memory

DRE

Dark Region Enhancement

DSI

Display Serial Interface

DTCM

Data Tightly Coupled Memory

DVFS

Dynamic Voltage and Frequency Scaling

E

EAV

End of Active Video

ECC

Error Correcting Code

EEE

Energy Efficient Ethernet

EMAC

Ethernet Network Interface Controller

EMI

External Memory Interface

EPO

Extended Prediction Orbit

F

FCS

Frame Check Sequence

FD

Face Detection

FIFO

First In First Out

FIR

Finite Impulse Response

FM

Frequency Modulation

FMSYS

Frequency Modulation System

fps

Frames Per Second

G

GIC

Generic Interrupt Controller

GNSS

Global Navigation Satellite System

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GPIO

General-Purpose Input/Output

GPS

Global Positioning System

GPU

Graphics Processor Unit

H

HBM

Human Body Model

HDMI

High-Definition Multimedia Interface

HEIF

High Efficiency Image File Format

HEVC

High Efficiency Video Coding

HNP

Host Negotiation Protocol

HS

High-Speed

HSYNC/HSync

Horizontal Synchronization

HW

Hardware

I

I2C

Inter-Integrated Circuit

I2S

Inter-IC Sound

IMEM

Instruction Memory

IP

Internet Protocol

IRRX

Infrared Receiver

ISP

Image Signal Processor

ITCM

Instruction Tightly Coupled Memory

J

JTAG

Joint Test Action Group

JTAG-AP

JTAG Access Port

L

LCM

Liquid Crystal Monitor

LDC

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Lens Distortion Compensation

LDO

Low Dropout

LFSR

Linear Feedback Shift Register

LP

Low-Power

LPF

Low-Pass Filter

LPM

Lower Power Management

LSB

Least Significant Bit

LTE

Long-Term Evolution

LVDS

Low-Voltage Differential Signaling

M

MACs

Multiply-Accumulate operations

MCDI

MultiCore Deep Idle

MCLK

Master Clock

MCS

Modulation and Coding Set

MCUSYS

Microcontroller Unit System

MDIO

Management Data Input/Output

MDP

Multimedia Data Path

MDP_CCORR

Multimedia Data Path Color Correction

MDP_RDMA

Multimedia Data Path Read DMA

MDP_RSZ

Multimedia Data Path Resizer

MDP_TDSHP

Multimedia Data Path 2D Sharpness

MDP_WROT

Multimedia Data Path Rotation

MFG

MFlexGraphics

MHL

Mobile High-Definition Link

MISO

Master Input to Slave Output

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MLC

Multi-Level Cell

MMD

MediaTek Module Design

MMsys

Multimedia Subsystem

MMU

Memory Management Unit

MOSI

Master Output to Slave Input

mSBC

modified Sub-Band Codec

MSDC

MMC and SD Controller

MUX

Multiplexer

N

NFI

NAND Flash Interface

O

OFDM

Orthogonal Frequency Division Multiplexing

ONFI

Open NAND Flash Interface

OTG

On-The-Go

P

PA

Power Ampilifier

PBC

Peaking by Color

PCB

Printed Circuit Board

PCM

Pulse Code Modulation

PCO

Phased Coexistence Operation

PDM

Pulse Density Modulation

PIO

Programmed Input/Output

PLC

Packet Loss Concealment

PSMP

Power-Save Multi-Poll

PTPOD

Performance Thermal Power Over Drive

PWM

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Pulse Width Modulation

PWRAP

PMIC Wrapper

Q

QoS

Quality of Service

R

RBDS

Radio Broadcast Data System

RDMA

Read Direct Memory Access

RDS

Radio Data System

RE

Read Enable

RF

Radio Frequency

RH

Relative Humidity

RIFS

Reduced Interframe Space

ROI

Region-of-Interest

RTC

Real-Time Counter

RX

Receiver

S

S/PDIF

Sony/Philips Digital Interface Format

SAR

Successive Approximation Register

SAV

Start of Active Video

SBAS

Satellite-Based Augmentation Systems

SBC

Sub-Band Codec

SCK

Serial Clock

SCPSYS

System Companion Processor + System Power Manager

SDM

Sigma-Delta Modulation

SENINF

Sensor Interface

SIMD

Single Instruction Multiple Data

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SLC

Single-Level Cell

SMI

Smart Multimedia Interface

SPI

Serial Peripheral Interface

SPM

System Power Management

SRP

Session Request Protocol

SSC

Spread-Spectrum Clocking

STBC

Space-Time Block Code

SW

Software

T

TAP

Test Access Port

TCP

Transmission Control Protocol

TCXO

Temperature Compensated Crystal Oscillator

TDM

Time-Division Multiplexing

TE

Tearing Effect

TLB

Translation Lookaside Buffer

TLC

Triple-Level Cell

TMS

Thermistor Crystal

TOPRGU

Top Reset Generation Unit

TSENSE

Temperature Sensor

TX

Transmitter

U

UART

Universal Asynchronous Receiver/Transmitter

UDP

User Datagram Protocol

UI

Unit Interval

UL

Uplink

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USB

Universal Serial Bus

UTMI

USB Transceiver Macrocell Interface

V

VAD

Voice Activity Detection

VDEC

Video Decoder

VENC

Video Encoder

VESA

Video Electronics Standards Association

VLIW

Very Long Instruction Word

VSYNC/VSync

Vertical Synchronization

W

WBG

Wi-Fi, Bluetooth, and GNSS

WDMA

Write DMA

WDT

Watchdog Timer

WE

Write Enable

WMT

Wireless Management Task

WoWLAN

Wake on Wireless LAN

WPE

Warp Engine

X

xHCI

eXtensible Host Controller Interface

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3 Features Description

The MT8365 architecture is a highly integrated mobile computing platform incorporating application processing, APU, DSP and connectivity subsystems to enable smart mobile applications. This high-performance and low power platform features advanced implementation of Quad-core Arm Cortex-A53 operating at up to 2.0 GHz and powerful multi-standard video accelerator. The device features NAND flash memory, LPDDR3, DDR3/L, LPDDR4/X, DDR4 for optimal performance and also supports booting from eMMC to minimize the overall BOM cost. In addition, an extensive set of interfaces is included to connect to cameras, touch screen displays, and MMC/SD cards.

The Quad-core Arm Cortex-A53 MPCore equipped with Arm Neon™ engine, offers necessary processing power to support the latest OpenOS along with demanding applications such as web browsing, email, GPS navigation and games. This content can be enhanced by the 2D/3D graphics accelerator and then visualized on a high resolution touch screen display. To provide advanced multimedia applications and services such as streaming audio and video, the device features a multi-standard video accelerator with multitude of decoders and encoders such as HEVC and H.264, and an advanced audio subsystem.

The device also features wireless connectivity functions, such as 2.4 GHz and 5 GHz WLAN, 2.4 GHz Bluetooth, and 1.575 GHz GPS, all sharing single antenna, and thus providing the best and most convenient wireless connectivity solution among the industry with enhanced overall quality achieved for simultaneous voice, data, and audio/video transmission solutions on Artificial Intelligence (AI) embedded devices. The device implements hardware mechanism to support advanced and sophisticated radio coexistence algorithms. It also supports single antenna sharing among 2.4 GHz Bluetooth, 2.4 GHz / 5 GHz WLAN and 1.575 GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on AI embedded devices. The small footprint with low-power consumption greatly reduces the PCB layout resource.

3.1 Processor

The Quad-core Arm Cortex-A53 (CPU) MPCore with Arm Neon extension is a general purpose and highly efficient processor and together with the Generic Interrupt Controller (GIC) forms the MCU Subsystem (MCUSYS). It is responsible for running an operating system and many different application programs. A 128-bit AXI bus is directly connected to External Memory Interface (EMI) to minimize the access latency to DRAM thus providing sufficient memory bandwidth. The peripheral system and on-chip storage are bridged through an AXI bus, and the outstanding capability of AXI protocol, allowing the system to exploit its maximum performance.

The device supports Dynamic Voltage and Frequency Scaling (DVFS) technology, which allows the CPU to run at different frequency and voltage configurations for different application requirements. The MCUSYS can be completely shut down to save further power consumption and optimizes battery usage on mobile devices.

The CPU supports the following key features:

- Neon processing engine with SIMDv2/VFPv4 ISA
- Full compliance with Armv8-A architecture:
  - AArch32 and AArch64 execution states at all Exception Levels (EL0 to EL3)
  - A64 instruction set
  - A32 instruction set (Arm instruction set in pre-Armv8 architectures)
  - T32 instruction set (Arm Thumb instruction set in pre-Armv8 architectures)
- In-order pipeline with direct and indirect branch prediction
- Generic timers supporting 64-bit count input from SYSTMR
- Level 1 (L1) and Level 2 (L2) cache memory with cache line length of 64 bytes:

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  - Separate L1 instruction cache: 32KB L1 I-cache
  - Separate L1 data cache: 32KB L1 D-cache
  - 512KB unified L2 cache
- Memory Management Unit (MMU):
  - 10-entry, fully-associative, L1 instruction micro Translation Lookaside Buffer (TLB)
  - 10-entry, fully-associative, L1 data micro TLB
  - 4-way, set-associative, 512-entry unified main TLB
- Security:
  - TrustZone®
  - Secure boot (refer to Section 3.14 Boot Modes)
- Debug:
  - Armv8 debug logic
  - Arm CoreSight™ architecture
- 128-bit AXI master interface

3.2 Graphics Accelerator

The device graphics accelerator (GPU) is based on Arm Mali-G52 MC1 core. It is used to process extremely complicated graphics and perform general processing tasks assigned by the main application processor.

The GPU supports the following key features:

- An enhanced API feature set with high-performance support for both shader-based and fixed-function graphics APIs. The supported API graphics industry standards are:
  - OpenGL ES 1.1, 2.0, 3.2
  - Vulkan® 1.0, 1.1
  - OpenCL™ 2.0 Full Profile Specification
- Anti-aliasing capabilities
- An effective core for General Purpose computing on GPU (GPGPU) applications
- High memory bandwidth and low-power consumption for 3-Dimentional (3D) graphics content
- Frame buffer compression
- Bus protocol
  - 1 × 128-bit master AXI4 bus with support of 64 read and 32 write outstanding transactions
  - Slave AXI4 bus
- Level-2 cache
  - 1 × 128KB
- Performance
  - Fill rate: 1600MP/sec
  - Shader rate: 57.6 GFLOPS

3.3 Digital Signal Processor

The HiFi 4 Audio Engine Digital Signal Processor (DSP) is a highly optimized audio processor designed for efficient execution of audio and voice codecs and pre- and post-processing modules.

The HiFi 4 is a Single Instruction Multiple Data (SIMD) processor with ability to work in parallel on two 32-bit data items or

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four 16-bit data items. The Very Long Instruction Word (VLIW) architecture supports the execution up to four operations in parallel.

The HiFi 4 DSP supports the following key features:

- CPU architecture:
  - Four 32 × 32-bit Multiply-Accumulate operations (MACs) per cycle
  - Limited support for 72-bit accumulators
  - Limited support for eight 32 × 16-bit MACs
  - Four VLIW slots
  - Ability to issue two 64-bit loads per cycle
- 32KB L1 I-cache
- 32KB L1 D-cache
- 480KB Local SRAM (Tightly Coupled Memory – TCM), with programmable size of the Instruction TCM (ITCM) and Data TCM (DTCM) sections:
  - 96KB ITCM and 384KB DTCM, or
  - 64KB ITCM and 416KB DTCM, or
  - 32KB ITCM and 448KB DTCM
- Data retention support for local ITCM and DTCM
- No data retention support for pre-fetch buffer, I-cache, D-cache, ITag, and DTag
- Legacy JTAG Access Port (JTAG-AP)
- Support for 25 interrupts
- Supports System Power Management (SPM) to control power sequence
- Mathematic co-processors for high-performance computing
- Dedicated UART (DSP_UART)

3.4 AI Processor Unit

The AI Processor Unit (APU) is a highly efficient computing processor that is best suited for AI and Computer Vision (CV) algorithms. It is based on the Cadence Vision P6 (VP6) core and together with the integrated eDMA engine for data movement between an external DRAM and the VP6 internal memory forms the AI Processor Unit System (APUSYS). The operation frequency of APU can be adjusted dynamically for various application scenarios.

The APUSYS main features:

- eDMA to reduce extra time for data transfer. It can copy data between external DRAM and VP6 internal memory Instruction Memory (IMEM) and Data memory (DMEM)
- eDMA can run concurrently with iDMA inside VP6
- 128 bits read data and 128 bits write data bus for data transferring respectively from and to external DRAM

The APU supports the following key features:

- Support of iDMA for data transfer between VP6 internal Data Memory (DMEM) and external DRAM
- L1 instruction memory per core: 64KB + 128KB Cache
- L1 data memory per core: 128KB + 128KB
- Top performance:
  - Fix 8: Up to 160 GMACs
  - Fix 16: Up to 40 GMACs
- TrustZone security support

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- Data protection to avoid slaves from being accessed by unexpected masters
- Dynamic Voltage and Frequency Scaling

3.5 Memory

The device connects to external memories using External Memory Interface (EMI) controller and Dynamic Random-Access Memory Controller (DRAMC) with DDR PHY. EMI is a sophisticated communication interface between external memories and the device.

The EMI controller processes requests from the device masters and issues commands to the DRMAC. It has the following key features:

- Prevents DRAM stall, data overflow, and underflow
- Gates its clock when no transactions occurred to reduce power
- Organizes the schedule options for the device master commands:
  - Starvation control
  - Bandwidth limiter
  - Priority control
  - Page hit control
  - Read and write turn around prevent control
- Dedicated AXI connection ports:
  - 128-bit read and write port to the CPU system
  - 128-bit read and write port to the multimedia modules
  - 128-bit read and write port to the GPU
  - 128-bit read and write port to the peripheral modules
  - 128-bit read and write port to the wireless connectivity modules
  - 64-bit read and write port to the DSP
- Supports connecting to two rank DRAM devices

The DRAMC processes EMI commands and controls the external memory. It has the following key features:

- Contains integrated DDR PHY
- Supports the following DDR memory types:
  - 16-bit and 32-bit DDR3 at 1600 MT/s
  - 16-bit and 32-bit DDR4 at 3200 MT/s
  - 32-bit LPDDR3 at 1600 MT/s
  - 32-bit LPDDR4 at 3200 MT/s
- Schedules and issues DRAM bus commands
- Keeps the integrity of DRAM bus timings
- Raises the DRAM bus utilization rate

The DDR PHY connects the DRAMC to the external memory and has the following key features:

- Processes the DRAM commands
- Reads from and writes to the DRAM
- Contains PLL that provides clock for EMI, DRAMC, and DDR PHY

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3.5.1 EMI Signal Descriptions

Table 3-1 presents EMI signal descriptions.

Table 3-1 EMI Signal Descriptions

Signal Name	Type	Description	Ball Location
EMI_EXTR[1]	AIO	DRAM output driving calibration resistor	J1
EMI_RESET_N	AIO	DRAM reset output	F14
EMI_TN	AIO	Not used. Leave unconnected.	G28
EMI_TP[2]	AIO	DRAM voltage reference 2, connected to ½ AVDDQ_EMI0	F28
EMI0 Address Bus—EMI0_A[13:0]			
EMI0_A0	AIO	DRAM address output 0	C14
EMI0_A1	AIO	DRAM address output 1	G6
EMI0_A2	AIO	DRAM address output 2	F3
EMI0_A3	AIO	DRAM address output 3	J6
EMI0_A4	AIO	DRAM address output 4	J12
EMI0_A5	AIO	DRAM address output 5	F6
EMI0_A6	AIO	DRAM address output 6	D14
EMI0_A7	AIO	DRAM address output 7	E6
EMI0_A8	AIO	DRAM address output 8	G3
EMI0_A9	AIO	DRAM address output 9	D3
EMI0_A10	AIO	DRAM address output 10	E12
EMI0_A11	AIO	DRAM address output 11	H3
EMI0_A12	AIO	DRAM address output 12	H12
EMI0_A13	AIO	DRAM address output 13	C3
EMI0 Data Bus—EMI0_DQ[15:0]			
EMI0_DQ0	AIO	DRAM data pin 0	C11
EMI0_DQ1	AIO	DRAM data pin 1	A2
EMI0_DQ2	AIO	DRAM data pin 2	B12
EMI0_DQ3	AIO	DRAM data pin 3	B4
EMI0_DQ4	AIO	DRAM data pin 4	B11
EMI0_DQ5	AIO	DRAM data pin 5	B3
EMI0_DQ6	AIO	DRAM data pin 6	B13
EMI0_DQ7	AIO	DRAM data pin 7	B5
EMI0_DQ8	AIO	DRAM data pin 8	B7
EMI0_DQ9	AIO	DRAM data pin 9	E1
EMI0_DQ10	AIO	DRAM data pin 10	B8
EMI0_DQ11	AIO	DRAM data pin 11	F2
EMI0_DQ12	AIO	DRAM data pin 12	B9
EMI0_DQ13	AIO	DRAM data pin 13	G2
EMI0_DQ14	AIO	DRAM data pin 14	C9
EMI0_DQ15	AIO	DRAM data pin 15	H2
EMI0 System Bus—Bank, Data Mask, Data Strobe, Clock, Reset Signals			
EMI0_BA0	AIO	DRAM banks address	K12
EMI0_BA1	AIO	DRAM banks address	K6
EMI0_ACT_N	AIO	DRAM cmd activation command input	F12
EMI0_BG0	AIO	DRAM cmd bank group input	G14

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Signal Name	Type	Description	Ball Location
EMI0_CAS_N	AIO	DRAM cmd column strobe output	J9
EMI0_CK_C	AIO	DRAM clock 0 output, invert	D8
EMI0_CK_T	AIO	DRAM clock 0 output	E8
EMI0_CKE0	AIO	DRAM command output clock enable 0	K14
EMI0_CKE1	AIO	DRAM command output clock enable 1	J14
EMI0_CS0_N	AIO	DRAM chip select 0, invert	G9
EMI0_CS1_N	AIO	DRAM chip select 1, invert	F9
EMI0_DM0	AIO	DRAM DQM 0	B1
EMI0_DM1	AIO	DRAM DQM 1	C10
EMI0_DQS0_C	AIO	DRAM DQS 0	C7
EMI0_DQS0_T	AIO	DRAM DQS 0, invert	C6
EMI0_DQS1_C	AIO	DRAM DQS 1	C2
EMI0_DQS1_T	AIO	DRAM DQS 1, invert	D2
EMI0_ODT	AIO	DRAM cmd on die termination	G12
EMI0_RAS_N	AIO	DRAM cmd row strobe output	H9
EMI0_WE_N	AIO	DRAM cmd write enable	H14
EMI1 Address Bus—EMI1_A[13:0]			
EMI1_A0	AIO	DRAM address output 0	J28
EMI1_A1	AIO	DRAM address output 1	H20
EMI1_A2	AIO	DRAM address output 2	B16
EMI1_A3	AIO	DRAM address output 3	G20
EMI1_A4	AIO	DRAM address output 4	F24
EMI1_A5	AIO	DRAM address output 5	J20
EMI1_A6	AIO	DRAM address output 6	H28
EMI1_A7	AIO	DRAM address output 7	D18
EMI1_A8	AIO	DRAM address output 8	B15
EMI1_A9	AIO	DRAM address output 9	C17
EMI1_A10	AIO	DRAM address output 10	J24
EMI1_A11	AIO	DRAM address output 11	A14
EMI1_A12	AIO	DRAM address output 12	D20
EMI1_A13	AIO	DRAM address output 13	C18
EMI1 Data Bus—EMI1_DQ[15:0]			
EMI1_DQ0	AIO	DRAM data pin 16	E30
EMI1_DQ1	AIO	DRAM data pin 17	B24
EMI1_DQ2	AIO	DRAM data pin 18	G29
EMI1_DQ3	AIO	DRAM data pin 19	A26
EMI1_DQ4	AIO	DRAM data pin 20	F29
EMI1_DQ5	AIO	DRAM data pin 21	B25
EMI1_DQ6	AIO	DRAM data pin 22	H29
EMI1_DQ7	AIO	DRAM data pin 23	A27
EMI1_DQ8	AIO	DRAM data pin 24	A29
EMI1_DQ9	AIO	DRAM data pin 25	A21
EMI1_DQ10	AIO	DRAM data pin 26	B30
EMI1_DQ11	AIO	DRAM data pin 27	B20
EMI1_DQ12	AIO	DRAM data pin 28	C30

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Signal Name	Type	Description	Ball Location
EMI1_DQ13	AIO	DRAM data pin 29	B19
EMI1_DQ14	AIO	DRAM data pin 30	D29
EMI1_DQ15	AIO	DRAM data pin 31	B18
EMI1 System Bus—Bank, Data Mask, Data Strobe, Clock, Reset Signals			
EMI1_ACT_N	AIO	DRAM cmd activation command input	H24
EMI1_BA0	AIO	DRAM banks address	E24
EMI1_BA1	AIO	DRAM banks address	E20
EMI1_BG0	AIO	DRAM cmd bank group input	D28
EMI1_CAS_N	AIO	DRAM cmd column strobe output	E18
EMI1_CK_C	AIO	DRAM clock 0 output, invert	K18
EMI1_CK_T	AIO	DRAM clock 0 output	J18
EMI1_CKE0	AIO	DRAM command output clock enable 0	D24
EMI1_CKE1	AIO	DRAM command output clock enable 1	C24
EMI1_CS0_N	AIO	DRAM chip select 0, invert	F18
EMI1_CS1_N	AIO	DRAM chip select 1, invert	G18
EMI1_DM0	AIO	DRAM DQM 2	A24
EMI1_DM1	AIO	DRAM DQM 3	E29
EMI1_DQS0_C	AIO	DRAM DQS 2	B29
EMI1_DQS0_T	AIO	DRAM DQS 2, invert	B28
EMI1_DQS1_C	AIO	DRAM DQS 3	B23
EMI1_DQS1_T	AIO	DRAM DQS 3, invert	B22
EMI1_ODT	AIO	DRAM cmd on die termination	G24
EMI1_RAS_N	AIO	DRAM cmd row strobe output	C20
EMI1_WE_N	AIO	DRAM cmd write enable	C28

1. Connect this pin through an external resistor to GND. An external voltage should be applied.
2. This pin should be connected via 100-nF capacitors to the corresponding EMI power supply and GND. If not used, it can be left unconnected.

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3.5.2 EMI Signal Mapping

Table 3-2 presents EMI signals mapping per device memory type.

Table 3-2 EMI Signals Mapping

Ball Location	Ball Name	Pin-Mux 1 PCDDR4 2 × 16-bit	Pin-Mux 2 PCDDR4 1 × 16-bit	Pin-Mux 3 LPDDR4 eMCP 2 × 16-bit	Pin-Mux 4 LPDDR4 DSC 2 × 16-bit	Pin-Mux 5 LPDDR4 DSC 1 × 16-bit	Pin-Mux 6 PCDDR3 2 × 16-bit	Pin-Mux 7 PCDDR3 1 × 16-bit	Pin-Mux 8 PCDDR3 4 × 8-bit	Pin-Mux 9 LPDDR3 eMCP 1 × 32-bit	Pin-Mux 10 LPDDR3 DSC 1 × 32-bit
C14	EMI0_A0	A0	A0	DVSS	DVSS	DVSS	A7	A7	A3	CA8	CA5
G6	EMI0_A1	A1	A1	DVSS	DVSS	DVSS	BA1	BA1	A9	CA4	DVSS
F3	EMI0_A2	A2	A2	DVSS	DVSS	DVSS	A14	A14	A8	CA3	CA1
J6	EMI0_A3	A3	A3	CA2	CA4	CA4	A10	A10	A11	CA1	DVSS
J12	EMI0_A4	A4	A4	CA3	CA3	CA3	A5	A5	BA0	DVSS	DVSS
F6	EMI0_A5	A5	A5	DVSS	DVSS	DVSS	A12	A12	A14	DVSS	CA3
D14	EMI0_A6	A6	A6	DVSS	DVSS	DVSS	A13	A13	A1	CA9	CA7
E6	EMI0_A7	A7	A7	DVSS	DVSS	DVSS	A4	A4	A7	DVSS	CA4
G3	EMI0_A8	A8	A8	DVSS	DVSS	DVSS	A11	A11	A4	CA0	CA0
D3	EMI0_A9	A9	A9	DVSS	DVSS	DVSS	A8	A8	A6	DVSS	DVSS
E12	EMI0_A10	A10	A10	DVSS	DVSS	DVSS	BA2	BA2	WE#	CA6	CA6
H3	EMI0_A11	A11	A11	DVSS	DVSS	DVSS	A1	A1	A5	CA2	CA2
H12	EMI0_A12	A12	A12	CA0	CA2	CA2	CAS#	CAS#	BA2	DVSS	DVSS
C3	EMI0_A13	A13	A13	DVSS	DVSS	DVSS	A6	A6	A13	DVSS	DVSS
F12	EMI0_ACT_N	ACT_n	ACT_n	CA1	CA1	CA1	BA0	BA0	A15	DVSS	DVSS
K12	EMI0_BA0	BA0	BA0	CA5	CA5	CA5	A2	A2	A12	DVSS	DVSS
K6	EMI0_BA1	BA1	BA1	DVSS	DVSS	DVSS	A15	A15	A2	DVSS	DVSS
G14	EMI0_BG0	BG0	BG0	DVSS	DVSS	DVSS	A9	A9	BA1	CA7	CA8
J9	EMI0_CAS_N	CAS_n	CAS_n	DVSS	DVSS	DVSS	A0	A0	CAS#	DVSS	DVSS
D8	EMI0_CK_C	CK_c	CK_c	CK_c	CK_c	CK_c	CK0#	CK0#	CK0#	CK_c	CK_c
E8	EMI0_CK_T	CK_t	CK_t	CK_t	CK_t	CK_t	CK0	CK0	CK0	CK_t	CK_t
K14	EMI0_CKE0	CKE0	CKE0	CKE0	CKE0	CKE0	CKE0	CKE0	CKE0	CKE0	CKE0
J14	EMI0_CKE1	DVSS	DVSS	CKE1	CKE1	CKE1	CKE1	CKE1	DVSS	CKE1	CKE1
G9	EMI0_CS0_N	CS0_n	CS0_n	CS0_n	CS0_n	CS0_n	CS0#	CS0#	CS0#	CS0_n	CS0_n
F9	EMI0_CS1_N	DVSS	DVSS	CS1_n	CS1_n	CS1_n	CS1#	CS1#	DVSS	CS1_n	CS1_n

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Ball Location	Ball Name	Pin-Mux 1 PCDDR4 2 × 16-bit	Pin-Mux 2 PCDDR4 1 × 16-bit	Pin-Mux 3 LPDDR4 eMCP 2 × 16-bit	Pin-Mux 4 LPDDR4 DSC 2 × 16-bit	Pin-Mux 5 LPDDR4 DSC 1 × 16-bit	Pin-Mux 6 PCDDR3 2 × 16-bit	Pin-Mux 7 PCDDR3 1 × 16-bit	Pin-Mux 8 PCDDR3 4 × 8-bit	Pin-Mux 9 LPDDR3 eMCP 1 × 32-bit	Pin-Mux 10 LPDDR3 DSC 1 × 32-bit
B1	EMI0_DM0	DM0	DM0	DM0	DM1	DM1	DM0	DM0	DM1	DM2	DM2
C10	EMI0_DM1	DM1	DM1	DM1	DM0	DM0	DM1	DM1	DM0	DM0	DM0
C11	EMI0_DQ0	DQ0	DQ0	DQ11	DQ2	DQ2	DQ0	DQ0	DQ4	DQ4	DQ2
A2	EMI0_DQ1	DQ1	DQ1	DQ1	DQ8	DQ8	DQ3	DQ3	DQ8	DQ20	DQ16
B12	EMI0_DQ2	DQ2	DQ2	DQ8	DQ5	DQ5	DQ6	DQ6	DQ2	DQ6	DQ7
B4	EMI0_DQ3	DQ3	DQ3	DQ3	DQ10	DQ10	DQ5	DQ5	DQ14	DQ23	DQ17
B11	EMI0_DQ4	DQ4	DQ4	DQ10	DQ3	DQ3	DQ2	DQ2	DQ0	DQ5	DQ3
B3	EMI0_DQ5	DQ5	DQ5	DQ2	DQ9	DQ9	DQ1	DQ1	DQ10	DQ19	DQ20
B13	EMI0_DQ6	DQ6	DQ6	DQ9	DQ4	DQ4	DQ4	DQ4	DQ6	DQ7	DQ6
B5	EMI0_DQ7	DQ7	DQ7	DQ6	DQ11	DQ11	DQ7	DQ7	DQ12	DQ22	DQ21
B7	EMI0_DQ8	DQ8	DQ8	DQ15	DQ7	DQ7	DQ15	DQ15	DQ5	DQ0	DQ18
E1	EMI0_DQ9	DQ9	DQ9	DQ0	DQ12	DQ12	DQ12	DQ12	DQ9	DQ16	DQ0
B8	EMI0_DQ10	DQ10	DQ10	DQ12	DQ6	DQ6	DQ9	DQ9	DQ7	DQ1	DQ22
F2	EMI0_DQ11	DQ11	DQ11	DQ5	DQ13	DQ13	DQ14	DQ14	DQ11	DQ17	DQ1
B9	EMI0_DQ12	DQ12	DQ12	DQ13	DQ0	DQ0	DQ13	DQ13	DQ3	DQ2	DQ19
G2	EMI0_DQ13	DQ13	DQ13	DQ4	DQ14	DQ14	DQ10	DQ10	DQ15	DQ21	DQ4
C9	EMI0_DQ14	DQ14	DQ14	DQ14	DQ1	DQ1	DQ11	DQ11	DQ1	DQ3	DQ23
H2	EMI0_DQ15	DQ15	DQ15	DQ7	DQ15	DQ15	DQ8	DQ8	DQ13	DQ18	DQ5
C7	EMI0_DQS0_C	DQS0_c	DQS0_c	DQS1_c	DQS0_c	DQS0_c	DQS0#	DQS0#	DQS0#	DQS0_c	DQS0_c
C6	EMI0_DQS0_T	DQS0_t	DQS0_t	DQS1_t	DQS0_t	DQS0_t	DQS0	DQS0	DQS0	DQS0_t	DQS0_t
C2	EMI0_DQS1_C	DQS1_c	DQS1_c	DQS0_c	DQS1_c	DQS1_c	DQS1#	DQS1#	DQS1#	DQS2_c	DQS2_c
D2	EMI0_DQS1_T	DQS1_t	DQS1_t	DQS0_t	DQS1_t	DQS1_t	DQS1	DQS1	DQS1	DQS2_t	DQS2_t
G12	EMI0_ODT	ODT	ODT	CA4	CA0	CA0	WE#	WE#	A10	DVSS	DVSS
H9	EMI0_RAS_N	RAS_n	RAS_n	DVSS	DVSS	DVSS	A3	A3	RAS#	DVSS	DVSS
H14	EMI0_WE_N	WE_n	WE_n	DVSS	DVSS	DVSS	RAS#	RAS#	A0	CA5	CA9
J28	EMI1_A0	A0	DVSS	CA2	CA4	DVSS	RAS#	DVSS	A5	DVSS	DVSS
H20	EMI1_A1	A1	DVSS	CA1	CA3	DVSS	A11	DVSS	BA0	DVSS	DVSS
B16	EMI1_A2	A2	DVSS	DVSS	DVSS	DVSS	A4	DVSS	A2	DVSS	DVSS
G20	EMI1_A3	A3	DVSS	CA4	CA2	DVSS	A14	DVSS	RAS#	DVSS	DVSS
F24	EMI1_A4	A4	DVSS	DVSS	DVSS	DVSS	A7	DVSS	A7	DVSS	DVSS

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Ball Location	Ball Name	Pin-Mux 1 PCDDR4 2 × 16-bit	Pin-Mux 2 PCDDR4 1 × 16-bit	Pin-Mux 3 LPDDR4 eMCP 2 × 16-bit	Pin-Mux 4 LPDDR4 DSC 2 × 16-bit	Pin-Mux 5 LPDDR4 DSC 1 × 16-bit	Pin-Mux 6 PCDDR3 2 × 16-bit	Pin-Mux 7 PCDDR3 1 × 16-bit	Pin-Mux 8 PCDDR3 4 × 8-bit	Pin-Mux 9 LPDDR3 eMCP 1 × 32-bit	Pin-Mux 10 LPDDR3 DSC 1 × 32-bit
J20	EMI1_A5	A5	DVSS	CA0	CA5	DVSS	A10	DVSS	BA2	DVSS	DVSS
H28	EMI1_A6	A6	DVSS	DVSS	DVSS	DVSS	CAS#	DVSS	A4	DVSS	DVSS
D18	EMI1_A7	A7	DVSS	DVSS	DVSS	DVSS	A12	DVSS	A0	DVSS	DVSS
B15	EMI1_A8	A8	DVSS	DVSS	DVSS	DVSS	A6	DVSS	A11	DVSS	DVSS
C17	EMI1_A9	A9	DVSS	DVSS	DVSS	DVSS	A1	DVSS	A1	DVSS	DVSS
J24	EMI1_A10	A10	DVSS	DVSS	DVSS	DVSS	BA2	DVSS	WE#	DVSS	DVSS
A14	EMI1_A11	A11	DVSS	DVSS	DVSS	DVSS	A8	DVSS	A9	DVSS	DVSS
D20	EMI1_A12	A12	DVSS	DVSS	DVSS	DVSS	A3	DVSS	A10	DVSS	DVSS
C18	EMI1_A13	A13	DVSS	DVSS	DVSS	DVSS	BA1	DVSS	A3	DVSS	DVSS
H24	EMI1_ACT_N	ACT_n	DVSS	CA3	CA0	DVSS	A2	DVSS	A15	DVSS	DVSS
E24	EMI1_BA0	BA0	DVSS	DVSS	DVSS	DVSS	A9	DVSS	A6	DVSS	DVSS
E20	EMI1_BA1	BA1	DVSS	DVSS	DVSS	DVSS	A13	DVSS	A12	DVSS	DVSS
D28	EMI1_BG0	BG0	DVSS	DVSS	DVSS	DVSS	WE#	DVSS	A13	DVSS	DVSS
E18	EMI1_CAS_N	CAS_n	DVSS	DVSS	DVSS	DVSS	A15	DVSS	BA1	DVSS	DVSS
K18	EMI1_CK_C	CK_c	NC	CK_c	CK_c	NC	CK0#	NC	CK0#	NC	NC
J18	EMI1_CK_T	CK_t	DVSS	CK_t	CK_t	DVSS	CK0	DVSS	CK0	DVSS	DVSS
D24	EMI1_CKE0	CKE0	DVSS	CKE0	CKE0	DVSS	CKE0	DVSS	CKE0	DVSS	DVSS
C24	EMI1_CKE1	DVSS	DVSS	CKE1	CKE1	DVSS	CKE1	DVSS	DVSS	DVSS	DVSS
F18	EMI1_CS0_N	CS0_n	DVSS	CS0_n	CS0_n	DVSS	CS0#	DVSS	CS0#	DVSS	DVSS
G18	EMI1_CS1_N	DVSS	DVSS	CS1_n	CS1_n	DVSS	CS1#	DVSS	DVSS	DVSS	DVSS
A24	EMI1_DM0	DM0	DVSS	DM1	DM0	DVSS	DM0	DVSS	DM1	DM1	DM1
E29	EMI1_DM1	DM1	DVSS	DM0	DM1	DVSS	DM1	DVSS	DM0	DM3	DM3
E30	EMI1_DQ0	DQ0	DVSS	DQ0	DQ12	DVSS	DQ0	DVSS	DQ4	DQ31	DQ15
B24	EMI1_DQ1	DQ1	DVSS	DQ14	DQ1	DVSS	DQ3	DVSS	DQ12	DQ12	DQ24
G29	EMI1_DQ2	DQ2	DVSS	DQ4	DQ14	DVSS	DQ6	DVSS	DQ0	DQ26	DQ10
A26	EMI1_DQ3	DQ3	DVSS	DQ12	DQ6	DVSS	DQ5	DVSS	DQ8	DQ13	DQ25
F29	EMI1_DQ4	DQ4	DVSS	DQ5	DQ13	DVSS	DQ2	DVSS	DQ6	DQ30	DQ14
B25	EMI1_DQ5	DQ5	DVSS	DQ13	DQ0	DVSS	DQ1	DVSS	DQ14	DQ14	DQ28
H29	EMI1_DQ6	DQ6	DVSS	DQ7	DQ15	DVSS	DQ4	DVSS	DQ2	DQ29	DQ11
A27	EMI1_DQ7	DQ7	DVSS	DQ15	DQ7	DVSS	DQ7	DVSS	DQ10	DQ15	DQ29

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Ball Location	Ball Name	Pin-Mux 1 PCDDR4 2 × 16-bit	Pin-Mux 2 PCDDR4 1 × 16-bit	Pin-Mux 3 LPDDR4 eMCP 2 × 16-bit	Pin-Mux 4 LPDDR4 DSC 2 × 16-bit	Pin-Mux 5 LPDDR4 DSC 1 × 16-bit	Pin-Mux 6 PCDDR3 2 × 16-bit	Pin-Mux 7 PCDDR3 1 × 16-bit	Pin-Mux 8 PCDDR3 4 × 8-bit	Pin-Mux 9 LPDDR3 eMCP 1 × 32-bit	Pin-Mux 10 LPDDR3 DSC 1 × 32-bit
A29	EMI1_DQ8	DQ8	DVSS	DQ6	DQ11	DVSS	DQ15	DVSS	DQ5	DQ25	DQ26
A21	EMI1_DQ9	DQ9	DVSS	DQ11	DQ2	DVSS	DQ12	DVSS	DQ9	DQ11	DQ13
B30	EMI1_DQ10	DQ10	DVSS	DQ3	DQ10	DVSS	DQ9	DVSS	DQ7	DQ24	DQ30
B20	EMI1_DQ11	DQ11	DVSS	DQ10	DQ3	DVSS	DQ14	DVSS	DQ11	DQ10	DQ12
C30	EMI1_DQ12	DQ12	DVSS	DQ2	DQ9	DVSS	DQ13	DVSS	DQ3	DQ28	DQ27
B19	EMI1_DQ13	DQ13	DVSS	DQ8	DQ5	DVSS	DQ10	DVSS	DQ15	DQ9	DQ8
D29	EMI1_DQ14	DQ14	DVSS	DQ1	DQ8	DVSS	DQ11	DVSS	DQ1	DQ27	DQ31
B18	EMI1_DQ15	DQ15	DVSS	DQ9	DQ4	DVSS	DQ8	DVSS	DQ13	DQ8	DQ9
B29	EMI1_DQS0_C	DQS0_c	DVSS	DQS0_c	DQS1_c	DVSS	DQS0#	DVSS	DQS0#	DQS3_c	DQS3_c
B28	EMI1_DQS0_T	DQS0_t	DVSS	DQS0_t	DQS1_t	DVSS	DQS0	DVSS	DQS0	DQS3_t	DQS3_t
B23	EMI1_DQS1_C	DQS1_c	DVSS	DQS1_c	DQS0_c	DVSS	DQS1#	DVSS	DQS1#	DQS1_c	DQS1_c
B22	EMI1_DQS1_T	DQS1_t	DVSS	DQS1_t	DQS0_t	DVSS	DQS1	DVSS	DQS1	DQS1_t	DQS1_t
G24	EMI1_ODT	ODT	DVSS	CA5	CA1	DVSS	A5	DVSS	A8	DVSS	DVSS
C20	EMI1_RAS_N	RAS_n	DVSS	DVSS	DVSS	DVSS	A0	DVSS	CAS#	DVSS	DVSS
C28	EMI1_WE_N	WE_n	DVSS	DVSS	DVSS	DVSS	BA0	DVSS	A14	DVSS	DVSS
F14	EMI_RESET_N	RESET_N	RESET_N	RESET_N	RESET_N	RESET_N	RESET#	RESET#	RESET#	NC	NC
J1	EMI_EXTR	EMI_EXTR	EMI_EXTR	EMI_EXTR	EMI_EXTR	EMI_EXTR	EMI_EXTR	EMI_EXTR	EMI_EXTR	EMI_EXTR	EMI_EXTR
G28	EMI_TN	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
F28	EMI_TP	EMI_VREF	EMI_VREF	NC	NC	NC	EMI_VREF	EMI_VREF	EMI_VREF	EMI_VREF	EMI_VREF

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3.5.3 DDR Parameter Requirements and Skew Tolerances

This section describes the parameter requirements and skew tolerances for the supported memory types.

Table 3-3 DDR Parameter Requirements at Component Pin

Parameter	Comment	Min	Typ	Max	Unit
On-chip dynamic skew span between DQ/DQS	WRITE mode			40	ps
On-chip dynamic skew span between CMD/CLK				40	ps
On-chip static skew within DQ byte	If per-bit deskew is not available			40	ps
On-chip static skew within CA bus	If training is not available			40	ps
Max allowed DQ/DQS byte skew span	READ mode, if per-bit deskew is not available			100	ps
Max allowed DQ/DQS single-bit skew span	READ mode, if per-bit deskew is available			165	ps
Required type (aperture-based)	DQ READ, skew between DQ/DQS			120	ps
Required V_{IH_DC}/V_{IL_DC}	DDR3/L		90		mV
	DDR4		75		mV
	LPDDR3		100		mV
Required V_{IH_AC}/V_{IL_AC}	DDR3/L		135		mV
	DDR4		100		mV
	LPDDR3		150		mV
Max allowed overshoot/undershoot value; see Figure 3-1.	DDR3/L		0.4		V
	DDR4		0.3		V
	LPDDR3		0.35		V
Max allowed overshoot/undershoot area; see Figure 3-1.	DDR3/L		0.33		V × ns
	DDR4		0.25		V × ns
	LPDDR3		0.1		V × ns

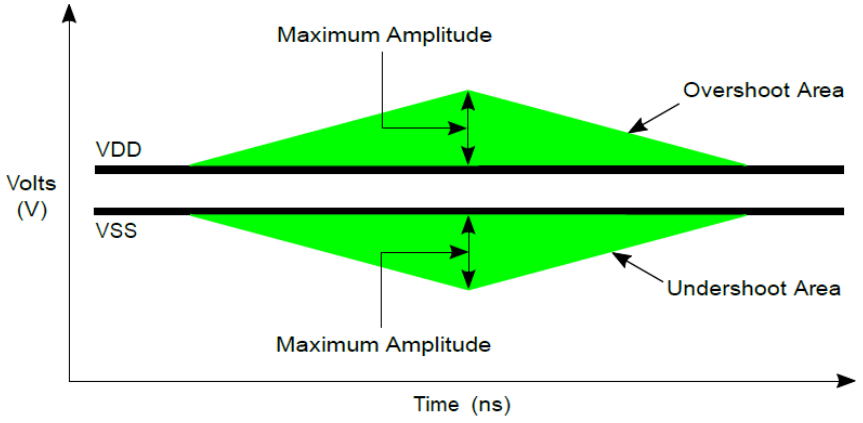

Figure 3-1 Control Overshoot and Undershoot Definition Block

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3.5.4 DDR3/L Interface

3.5.4.1 DDR3/L Timing Characteristics

The EMI DDR3/L timing characteristics are compliant with JEDEC Standard—JESD79-3D.

3.5.4.2 DDR3/L Application Guidelines

Table 3-4 presents supported DDR3/L device combinations.

Table 3-4 DDR3/L Device Combinations

Number of Devices	Device Data Width	Mirrored	EMI Width
4	8-bit	Yes	32-bit
4	8-bit	No	32-bit
2	16-bit	No	32-bit
1	16-bit	No	16-bit

Figure 3-2 shows the schematic connections for a 32-bit interface using 2 × 16-bit devices.

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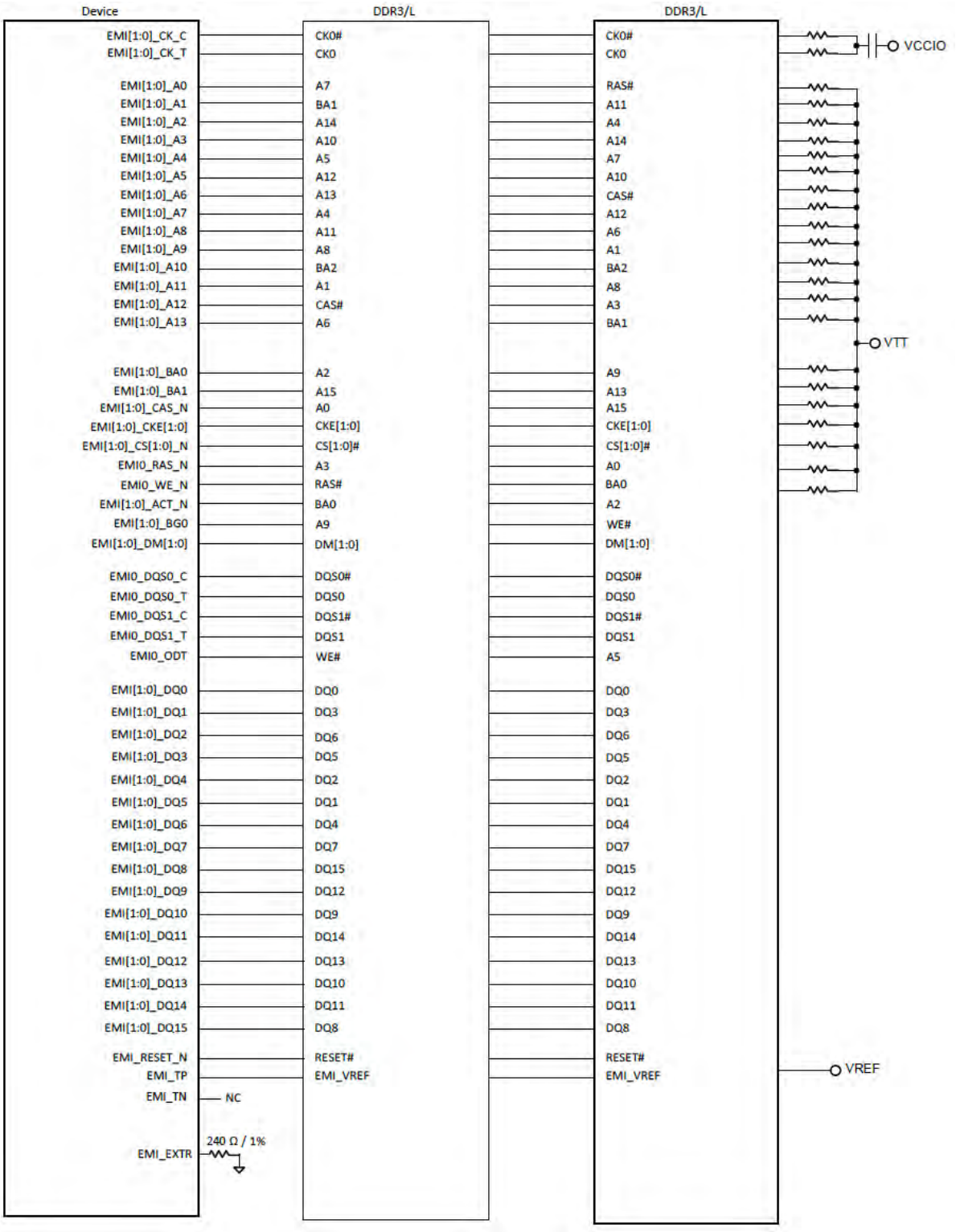

Figure 3-2 DDR3/L Basic Schematic for 2 × 16-bit

3.5.5 DDR4 Interface

3.5.5.1 DDR4 Timing Characteristics

The EMI DDR4 timing characteristics are compliant with JEDEC Standard—JESD79-4A.

Table 3-5 and Figure 3-3 present the EMI clock timing characteristics when DDR4 type of memory is used.

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Table 3-5 DDR4 Timing Characteristics

Parameter		Min	Max	Unit
t_{CK}	Cycle time, CK	0.625	1.67	ns

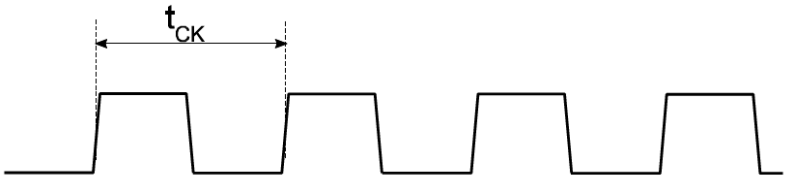

Figure 3-3 DDR4 Clock Timing Diagram

3.5.5.2 DDR4 Application Guidelines

Table 3-6 presents supported DDR4 device combinations.

Table 3-6 DDR4 Device Combinations

Number of Devices	Device Data Width	Mirrored	EMI Width
2	16-bit	No	32-bit
1	16-bit	No	16-bit

Figure 3-4 shows the schematic connections for a 32-bit interface using 2 × 16-bit devices.

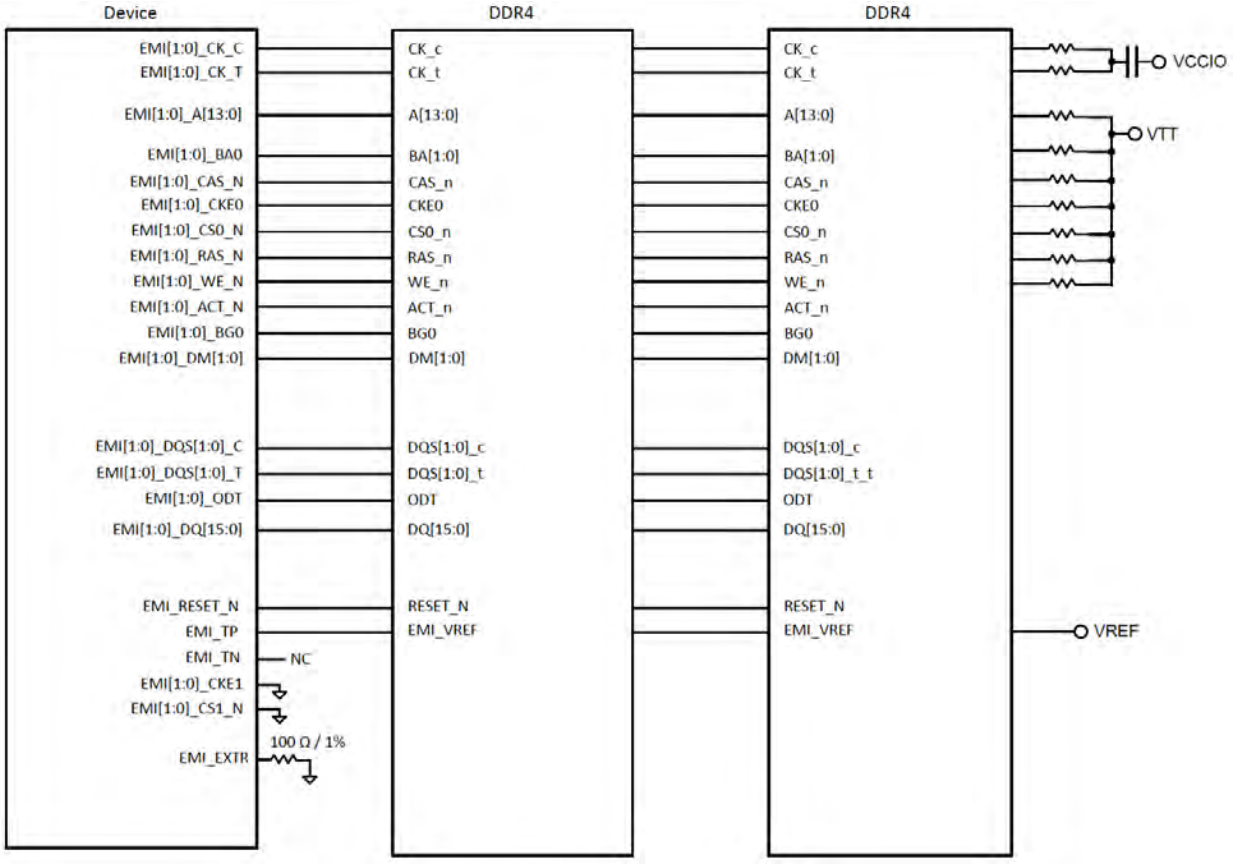

Figure 3-4 DDR4 Basic Schematic for 2 × 16-bit

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3.5.6 LPDDR3 Interface

3.5.6.1 LPDDR3 Timing Characteristics

The EMI LPDDR3 timing characteristics are compliant with JEDEC Standard—JESD209-3C.

3.5.6.2 LPDDR3 Application Guidelines

Table 3-7 presents supported LPDDR3 device combinations.

Table 3-7 LPDDR3 Device Combinations

Number of Devices	Device Data Width	Mirrored	EMI Width
1 × 178 pins	32-bit	No	32-bit
1 × 221 pins (eMCP)	32-bit	No	32-bit

Figure 3-5 shows the schematic connections for a 32-bit interface using 1 × 32-bit devices.

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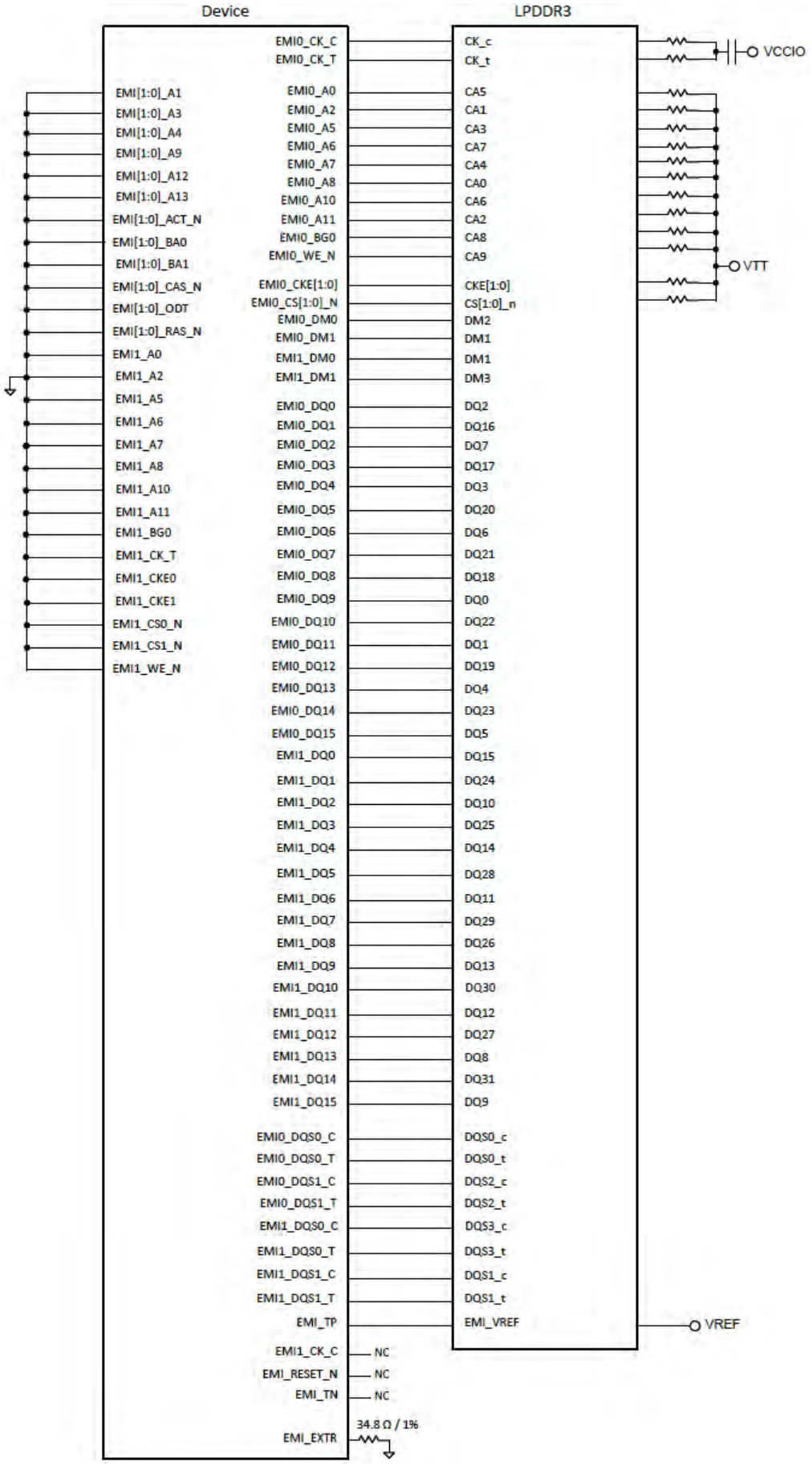

Figure 3-5 LPDDR3 Basic Schematic for 1 × 32-bit

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3.5.7 LPDDR4/X Interface

3.5.7.1 LPDDR4/X Timing Characteristics

The EMI LPDDR4 timing characteristics are compliant with JEDEC Standard—JESD209-4B.

3.5.7.2 LPDDR4/X Application Guidelines

Table 3-8 presents supported LPDDR4/X device combinations.

Table 3-8 LPDDR4/X Device Combinations

Number of Devices	Device Data Width	Mirrored	EMI Width
2 × 200 pins	16-bit	No	32-bit
1 × 200 pins	16-bit	No	16-bit
1 × 254 pins (eMCP)	2 × 16-bit	No	32-bit

Figure 3-6 shows the schematic connections for a 32-bit interface using 2 × 16-bit device.

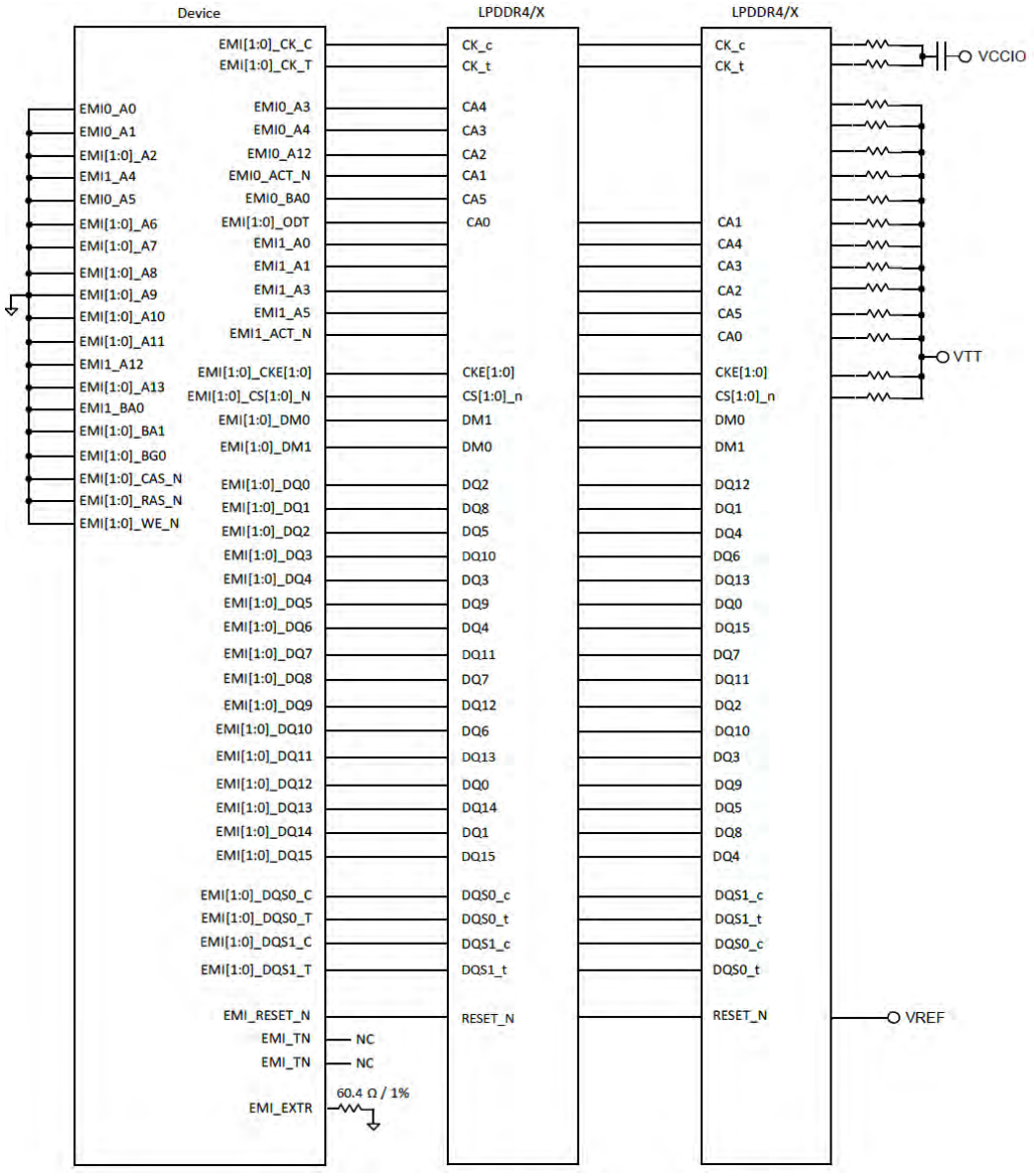

Figure 3-6 LPDDR4/X Basic Schematic for 2 × 16-bit

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3.6 Storage

3.6.1 Memory Card Controller (MSDC)

The Memory Stick and Secure Digital (SD®) card Controller (MSDC) offers a high throughput data transfers while power consumption and data security between device local hosts and memory cards are taken into consideration.

The MSDC interface fully supports:

- SD3.0 (Secure Digital) memory card specification
- SDIO3.0+ (Secure Digital Input Output) card specification
- eMMC5.1 (embedded MultiMediaCard) specification

The device has integrated 3 MSDC modules. Each MSDC module supports the following key features:

- 32-bit access on AHB bus
- Built-in CRC circuit
- Basic DMA mode and descriptor mode
- Interrupt capabilities

The MSDC0 controller fully supports:

- 1-, 4-, 8-bit data bus width for eMMC
- Backwards compatibility with legacy MMC card
- High Speed Single Data Rate (SDR) mode
- High Speed Dual Data Rate (DDR) mode
- HS200 mode, SDR up to 200 MBps
- HS400 mode, DDR up to 400 MBps
- eMMC Boot up mode
- Command Queuing

The MSDC1 and MSDC2 controllers fully support:

- 1-, 4-bit data bus for SD card interface or SDIO interface
- Default Speed mode, data rate up to 12 MBps
- High Speed mode, data rate up to 25 MBps
- SDR12 mode, data rate up to 12 MBps
- SDR25 mode, data rate up to 25 MBps
- SDR50 mode, data rate up to 50 MBps
- SD3.0 SDR104 mode, data rate up to 100 MBps
- SD3.0 DDR50 mode, data rate up to 50 MBps
- SD3.0+ HS400 mode, data rate up to 200 MBps (MDSC2 only)

3.6.1.1 MSDC Signal Descriptions

Table 3-9 presents MSDC signal descriptions.

Table 3-9 MSDC Signal Descriptions

Signal Name	Type	Description	Ball Location
MSDC0			

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Signal Name	Type	Description	Ball Location
MSDC0_CLK	DO	MSDC0 clock output/NWEB	M28
MSDC0_CMD	DIO	MSDC0 command pin/NALE	M26
MSDC0_DAT0	DIO	MSDC0 data0 pin/NLD2	L28
MSDC0_DAT1	DIO	MSDC0 data1 pin/NDQS	M29
MSDC0_DAT2	DIO	MSDC0 data2 pin/NLD5	L29
MSDC0_DAT3	DIO	MSDC0 data3 pin/NLD1	L27
MSDC0_DAT4	DIO	MSDC0 data4 pin/NLD3	N29
MSDC0_DAT5	DIO	MSDC0 data5 pin/NLD4	L30
MSDC0_DAT6	DIO	MSDC0 data6 pin/NLD6	N30
MSDC0_DAT7	DIO	MSDC0 data7 pin/NLD7	P30
MSDC0_DSL	DI	MSDC0 data strobe input	N26
MSDC0_RSTB	DO	MSDC0 reset output/NLD0	M27
MSDC1			
MSDC1_CLK	DO	MSDC1 clock output	M3
MSDC1_CMD	DIO	MSDC1 command pin	M6
MSDC1_DAT0	DIO	MSDC1 data0 pin	L3
MSDC1_DAT1	DIO	MSDC1 data1 pin	L2
MSDC1_DAT2	DIO	MSDC1 data2 pin	M4
MSDC1_DAT3	DIO	MSDC1 data3 pin	M5
MSDC2			
MSDC2_CLK	DO	MSDC2 clock output	AC13
MSDC2_CMD	DIO	MSDC2 command pin	AE13
MSDC2_DAT0	DIO	MSDC2 data0 pin	AF14
MSDC2_DAT1	DIO	MSDC2 data1 pin	AF13
MSDC2_DAT2	DIO	MSDC2 data2 pin	AD13
MSDC2_DAT3	DIO	MSDC2 data3 pin	AF12
MSDC2_DSL	DI	MSDC2 data strobe input	AE14

3.6.1.2 MSDC Signal Mapping

The communication protocol between controller and device is implemented through an advanced 11-signal or 6-signal bus. Details are provided in Table 3-10.

Table 3-10 MSDC Signal Mapping

No.	Name[1][2]	Type	MMC	SD/SDHC	SDIO	Description
1	MSDC0/1/2_CLK	DO	CLK	CLK	SCLK	Clock
2	MSDC0_RSTB	DO	RCLK			Reset output
3	MSDC0/1/2_DAT0	DIO	DAT0	DAT0	DAT0	Serial data line bit 0
4	MSDC0/1/2_DAT1	DIO	DAT1	DAT1	DAT1	Serial data line bit 1
5	MSDC0/1/2_DAT2	DIO	DAT2	DAT2	DAT2	Serial data line bit 2
6	MSDC0/1/2_DAT3	DIO	DAT3	DAT3	DAT3	Serial data line bit 3
7	MSDC0_DAT4	DIO	DAT4			Serial data line bit 4
8	MSDC0_DAT5	DIO	DAT5			Serial data line bit 5
9	MSDC0_DAT6	DIO	DAT6			Serial data line bit 6
10	MSDC0_DAT7	DIO	DAT7			Serial data line bit 7
11	MSDC0/1/2_CMD	DIO	CMD	CMD	BS	Command/bus state

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No.	Name[1][2]	Type	MMC	SD/SDHC	SDIO	Description
12	SD_WP[3]	I		WP		Write protection
13	SD_INS[3]	I	VSS2	VSS2	INS	Card insertion

1. All MSDC I/O pads include both pull-up and pull-down resistors because they are shared by both the Memory Stick and SD/MMC memory card. Pull-down resistor for these pins can be used for power saving.
2. All embedded pull-up and pull-down resistors can be disabled by programming the corresponding control registers if optimal pull-up or pull-down resistors are required on the system board.
3. SD_WP and SD_INS signals are not provided by MSDC controller. These functions can be accomplished using GPIO pins, if needed.

3.6.1.3 eMMC Interface

Table 3-11 through Table 3-16 present timing characteristics for eMMC interface in the device.

Table 3-11 eMMC Timing Characteristics (backward-compatible device interface)

No.	Parameter		Min	Max	Unit
CLK output from host					
MMC1	f_{OP_CLK}	Operating frequency		26	MHz
MMC2	$t_{w_CLK_L}$	Pulse duration, CLK low	12		ns
MMC3	$t_{w_CLK_H}$	Pulse duration, CLK high	12		ns
MMC4	t_{RISE_CLK}	Rise time, CLK		4	ns
MMC5	t_{FALL_CLK}	Fall time, CLK		4	ns
Host CMD/DAT output (refer to CLK)					
MMC6	$t_{su_DAT/CMD}$	Setup time, DAT/CMD output	10		ns
MMC7	$t_{h_DAT/CMD}$	Hold time, DAT/CMD output	10		ns
Host CMD/DAT input (refer to CLK)					
MMC8	$t_{su_DAT/CMD}$	Setup time, DAT/CMD input	3		ns
MMC9	$t_{h_DAT/CMD}$	Hold time, DAT/CMD input	18		ns

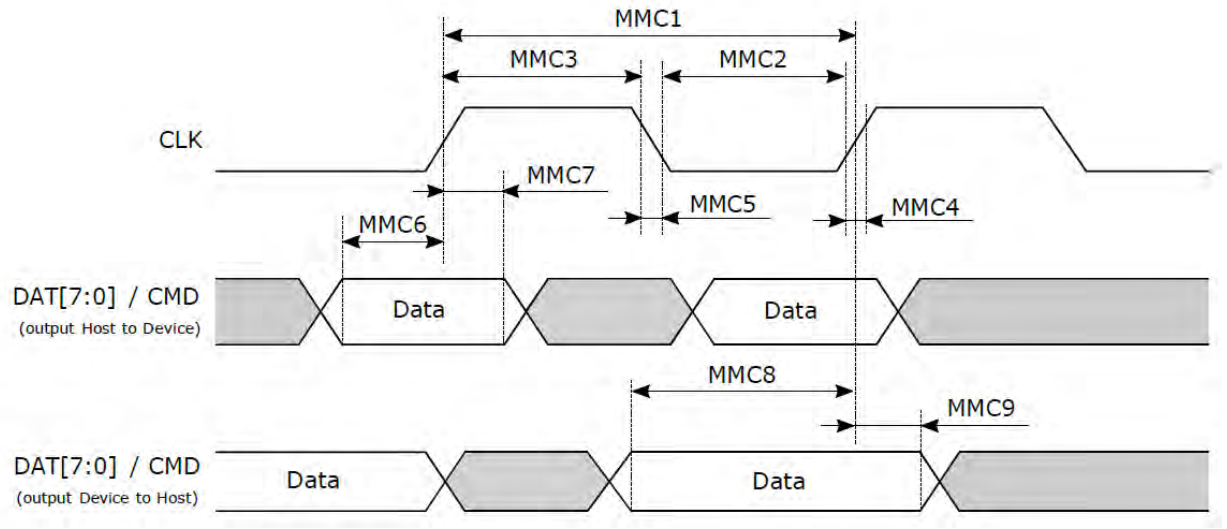

Figure 3-7 eMMC Timing Diagram (backward-compatible device interface)

Table 3-12 eMMC Timing Characteristics (High Speed mode)

No.	Parameter	Min	Max	Unit
CLK output from host				

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No.	Parameter		Min	Max	Unit
HS1	f_{OP_CLK}	Operating frequency		50	MHz
HS2	$t_{w_CLK_L}$	Pulse duration, CLK low	7.5		ns
HS3	$t_{w_CLK_H}$	Pulse duration, CLK high	7.5		ns
HS4	t_{RISE_CLK}	Rise time, CLK		2	ns
HS5	t_{FALL_CLK}	Fall time, CLK		2	ns
Host CMD/DAT output (refer to CLK)					
HS6	$t_{su_DAT/CMD}$	Setup time, DAT/CMD output	7		ns
HS7	$t_{h_DAT/CMD}$	Hold time, DAT/CMD output	7		ns
Host CMD/DAT input (refer to CLK)					
HS8	$t_{d_DAT/CMD}$	Delay time, DAT/CMD input		5[1]	ns
HS9	$t_{h_DAT/CMD}$	Hold time, DAT/CMD input	2		ns

1. Simulation result.

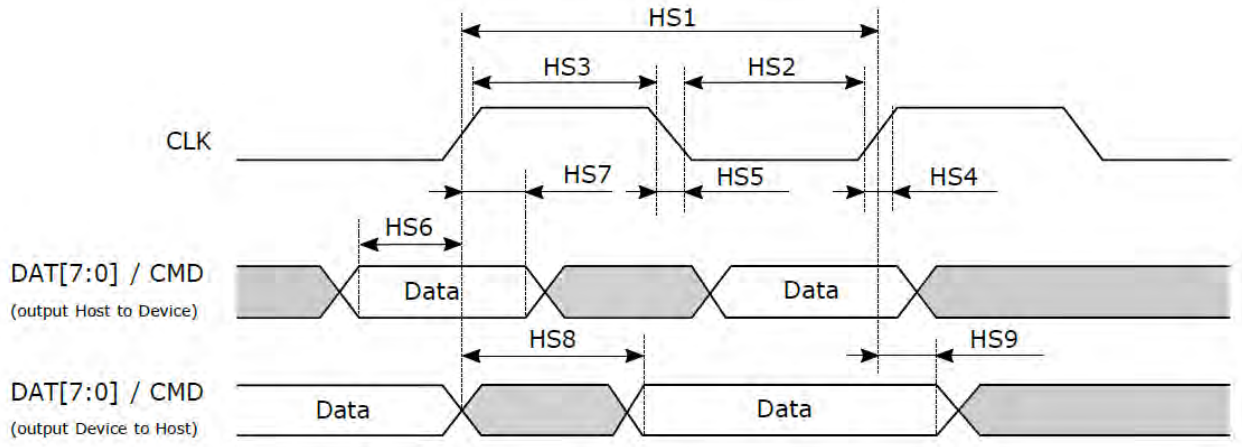

Figure 3-8 eMMC5.1 Timing Diagram (High Speed mode)

Table 3-13 eMMC Timing Characteristics (High Speed DDR mode)

No.	Parameter		Min	Max	Unit
CLK output from host					
HSDR1	t_C	Cycle time, CLK		20	ns
	D	Duty cycle, CLK	47	53	%
Host DATA output (refer to CLK)[1]					
HSDR3	t_{su_DATA}	Setup time, DATA output	3		ns
HSDR4	t_{h_DATA}	Hold time, DATA output	3		ns
Host DATA input (refer to CLK)[1]					
HSDR5	t_{su_DATA}	Setup time, DATA input	6[2]		ns
HSDR6	t_{h_DATA}	Hold time, DATA input	1		ns

1. High Speed DDR mode CMD timing is the same as High Speed mode.
2. Simulation result.

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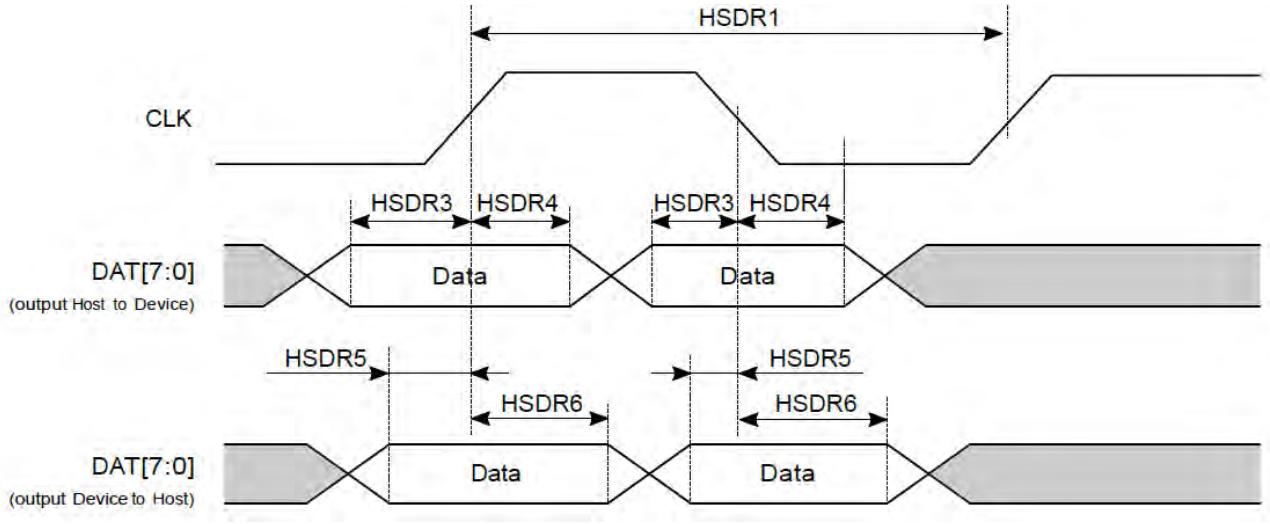

Figure 3-9 eMMC Timing Diagram (High Speed DDR mode)

Table 3-14 eMMC Timing Characteristics (HS200 mode)

No.	Parameter		Min	Max	Unit
CLK output from host					
HS2001	f_{OP_CLK}	Operating frequency		200	MHz
HS2002	t_{RISE_CLK}	Rise time, CLK		0.6	ns
HS2003	t_{FALL_CLK}	Fall time, CLK		0.6	ns
	D	Duty cycle, CLK	40	60	%
Host CMD/DAT output (refer to CLK)					
HS2005	$t_{su_DAT/CMD}$	Setup time, DAT/CMD output	1.8		ns
HS2006	$t_{h_DAT/CMD}$	Hold time, DAT/CMD output	1.5		ns
Host CMD/DAT input (refer to CLK)					
HS2007	$t_{dm_DAT/CMD}$	Input data momentary from CLK output to DAT or CMD input	0	3	UI[1]
HS2008	$t_{dv_DAT/CMD}$	Input data valid window	2.6		ns

1. Unit Interval (UI) is one bit nominal time. For example, UI = 5 ns at 200 MHz.

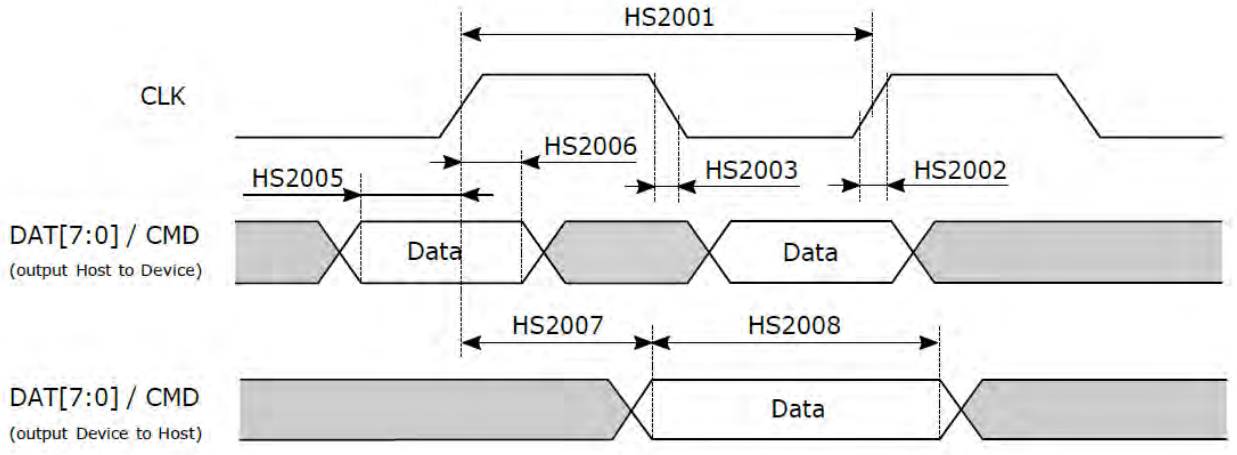

Figure 3-10 eMMC5.1 Timing Diagram (HS200 mode)

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Table 3-15 eMMC Timing Characteristics (HS400 mode host output)

No.	Parameter		Min	Max	Unit
CLK output from host					
HSHO1	t_C	Cycle time, CLK	5		ns
HSHO2	t_{dd}	Duty distortion, CLK		0.2	ns
HSHO3		Minimum pulse width	2.3		ns
Host DAT output (reference to CLK)[1]					
HSHO4	t_{su_DATA}	Setup time, DATA output	0.7[2]		ns
HSHO5	t_{h_DATA}	Hold time, DATA output	0.7[2]		ns

1. HS400 mode CMD timing is the same as HS200 mode.
2. Simulation result.

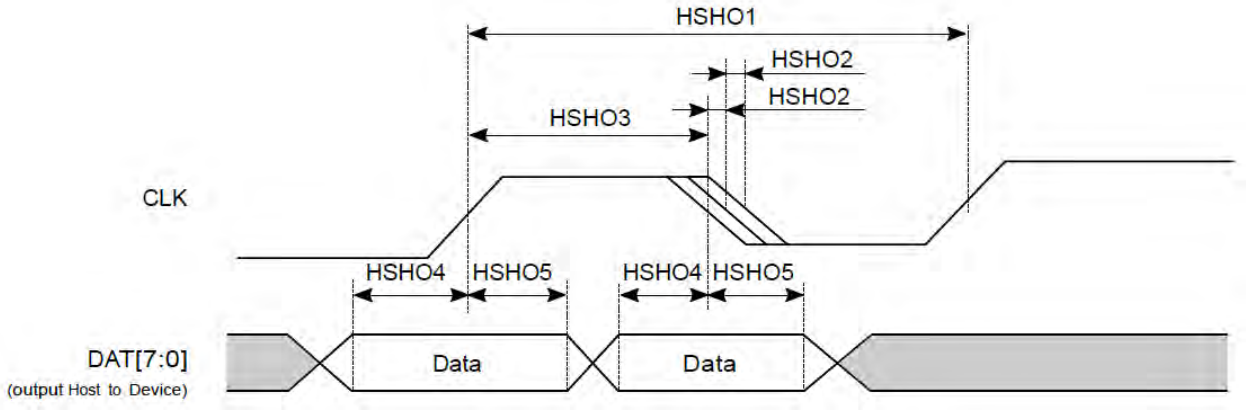

Figure 3-11 eMMC Timing Diagram (HS400 mode host output)

Table 3-16 eMMC Timing Characteristics (HS400 mode host input)

No.	Parameter		Min	Max	Unit
Data strobe output from device					
HSHI1		Data strobe period	5		ns
HSHI2		Data strobe duty distortion		0.3	ns
HSHI3		Minimum pulse width	1.9		ns
Host DAT input (refer to data strobe)					
HSHI4	t_{sk_DATA}	Input skew		0.5	ns
HSHI5	t_{skh_DATA}	Input hold skew		0.5	ns

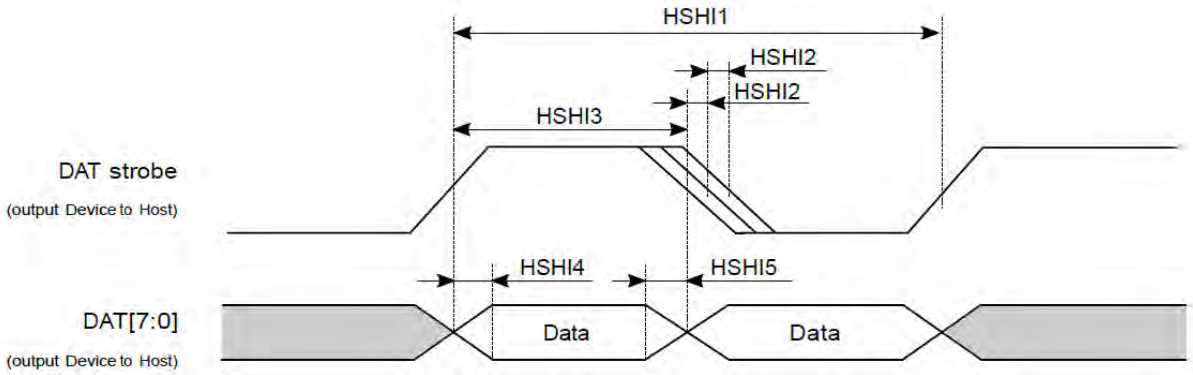

Figure 3-12 eMMC Timing Diagram (HS400 mode host input)

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3.6.1.4 SD3.0/SDIO3.0 Interface

Table 3-17 through Table 3-21 present timing characteristics for SDIO interface in the device.

Table 3-17 SD Timing Characteristics (Default Speed mode)

No.	Parameter		Min	Max	Unit
CLK output from host					
DS1	f_{OP_CLK}	Operating frequency		25	MHz
DS2	$t_{w_CLK_L}$	Pulse duration, CLK low	12		ns
DS3	$t_{w_CLK_H}$	Pulse duration, CLK high	12		ns
DS4	t_{RISE_CLK}	Rise time, CLK		4	ns
DS5	t_{FALL_CLK}	Fall time, CLK		4	ns
Host CMD/DAT output (refer to CLK)					
DS6	$t_{su_DAT/CMD}$	Setup time, DAT/CMD output	10		ns
DS7	$t_{h_DAT/CMD}$	Hold time, DAT/CMD output	10		ns
Host CMD/DAT input (refer to CLK)					
DS8	$t_{su_DAT/CMD}$	Setup time, DAT/CMD input	3		ns
DS9	$t_{h_DAT/CMD}$	Hold time, DAT/CMD input	18		ns

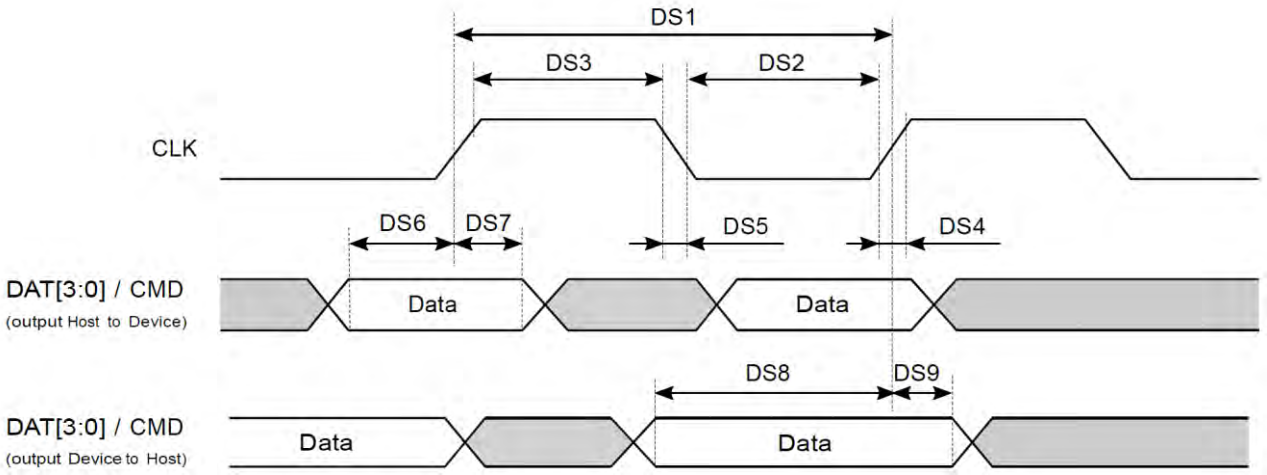

Figure 3-13 SD Timing Diagram (Default Speed mode)

Table 3-18 SD Timing Characteristics (High Speed / SDR12 / SDR25 mode)

No.	Parameter		Min	Max	Unit
CLK output from host					
SDR121	f_{OP_CLK}	Operating frequency		50[(1)]	MHz
SDR122	$t_{w_CLK_L}$	Pulse duration, CLK low	7.5		ns
SDR123	$t_{w_CLK_H}$	Pulse duration, CLK high	7.5		ns
SDR124	t_{RISE_CLK}	Rise time, CLK		2	ns
SDR125	t_{FALL_CLK}	Fall time, CLK		2	ns
Host CMD/DAT output (refer to CLK)					
SDR126	$t_{su_DAT/CMD}$	Setup time, DAT/CMD output	7		ns
SDR127	$t_{h_DAT/CMD}$	Hold time, DAT/CMD output	4		ns
Host CMD/DAT input (refer to CLK)					
SDR128	$t_{su_DAT/CMD}$	Setup time, DAT/CMD input	5[(2)]		ns
SDR129	$t_{h_DAT/CMD}$	Hold time, DAT/CMD input	2		ns

1. Maximum CLK frequency of SDR12 mode is 25 MHz.

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2. Simulation result.

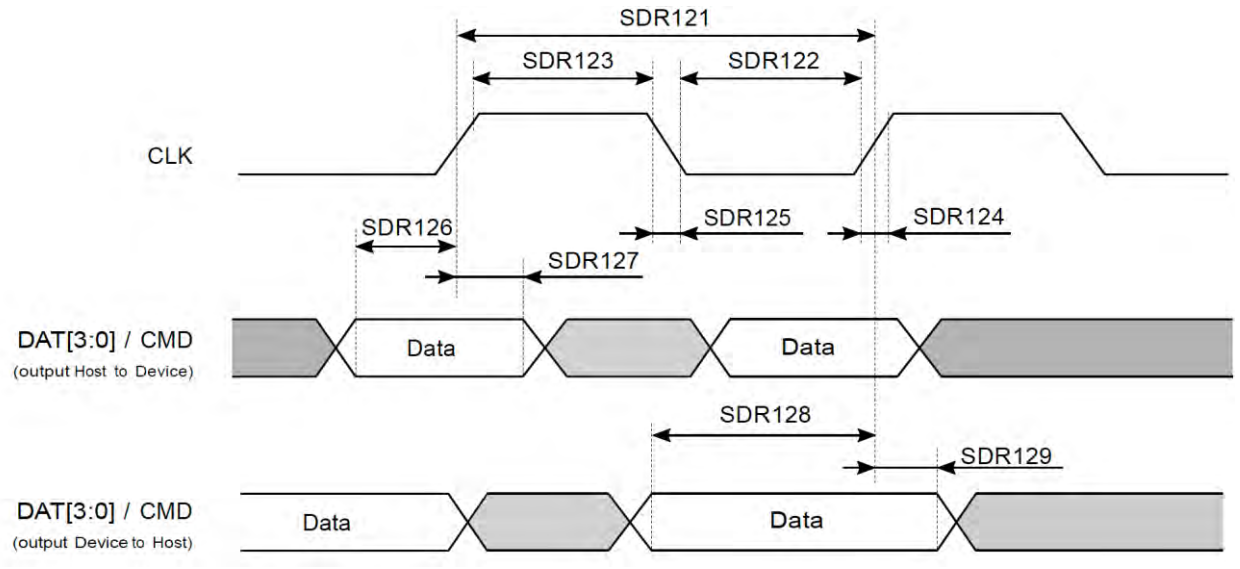

Figure 3-14 SD Timing Diagram (High Speed / SDR12 / SDR25 mode)

Table 3-19 SD Timing Characteristics (SDR50 mode)

No.	Parameter		Min	Max	Unit
CLK output from host					
SDR501	f_{OP_CLK}	Operating frequency		100	MHz
SDR502	$t_{w_CLK_L}$	Pulse duration, CLK low	3		ns
SDR503	$t_{w_CLK_H}$	Pulse duration, CLK high	3		ns
SDR504	t_{RISE_CLK}	Rise time, CLK		1.5	ns
SDR505	t_{FALL_CLK}	Fall time, CLK		1.5	ns
Host CMD/DAT output (refer to CLK)					
SDR506	$t_{su_DAT/CMD}$	Setup time, DAT/CMD output	3.3		ns
SDR507	$t_{h_DAT/CMD}$	Hold time, DAT/CMD output	3		ns
Host CMD/DAT input (refer to CLK)					
SDR508	$t_{su_DAT/CMD}$	Setup time, DAT/CMD input	2[(1)]		ns
SDR509	$t_{h_DAT/CMD}$	Hold time, DAT/CMD input	4[(1)]		ns

1. Simulation result.

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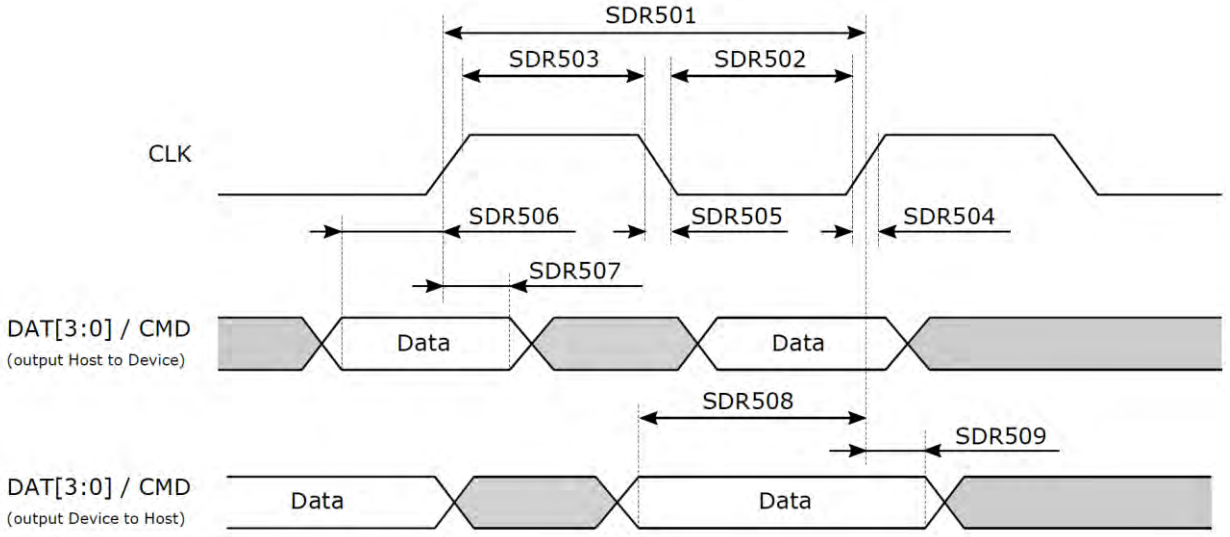

Figure 3-15 SD Timing Diagram (SDR50 mode)

Table 3-20 SD Timing Characteristics (DDR50 mode)

No.	Parameter		Min	Max	Unit
CLK output from host					
DDR501	t_C	Cycle time, CLK	-	20	ns
	D	Duty cycle, CLK	47	53	%
Host DAT output (refer to CLK)(1)					
DDR503	t_{su_DATA}	Setup time, DATA output	3	-	ns
DDR504	t_{h_DATA}	Hold time, DATA output	3	-	ns
Host DAT input (refer to CLK)(1)					
DDR505	t_{su_DATA}	Setup time, DATA input	7(2)	-	ns
DDR506	t_{h_DATA}	Hold time, DATA input	1	-	ns

1. DDR50 CMD timing is the same as High Speed mode.
2. Simulation result.

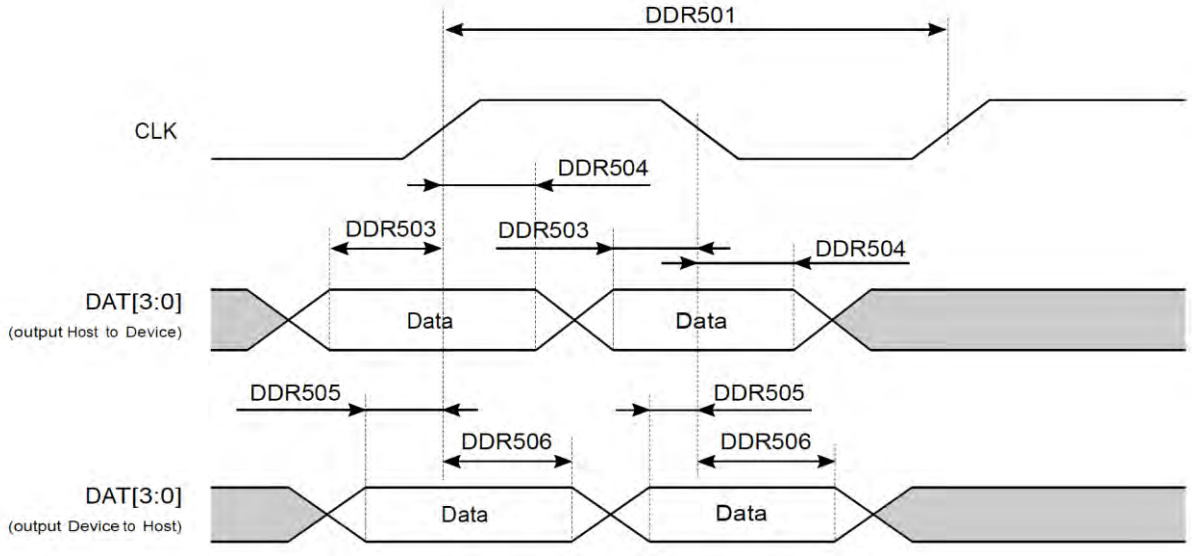

Figure 3-16 SD Timing Diagram (DDR50 mode)

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Table 3-21 SD Timing Characteristics (SDR104 mode)

No.	Parameter		Min	Max	Unit
CLK output from host					
SDR1041	f_{OP_CLK}	Operating frequency		200	MHz
SDR1042	t_{RISE_CLK}	Rise time, CLK		0.7	ns
SDR1043	t_{FALL_CLK}	Fall time, CLK		0.7	ns
	D	Duty cycle, CLK	40	60	%
Host CMD/DAT output (refer to CLK)					
SDR1045	$t_{su_DAT/CMD}$	Setup time, DAT/CMD output	1.6		ns
SDR1046	$t_{h_DAT/CMD}$	Hold time, DAT/CMD output	1.8		ns
Host CMD/DAT input (refer to CLK)					
SDR1047	$t_{dm_DAT/CMD}$	Input data momentary from CLK output to DAT or CMD input		3	UI
SDR1048	$t_{dv_DAT/CMD}$	Input data valid window	2.6		ns

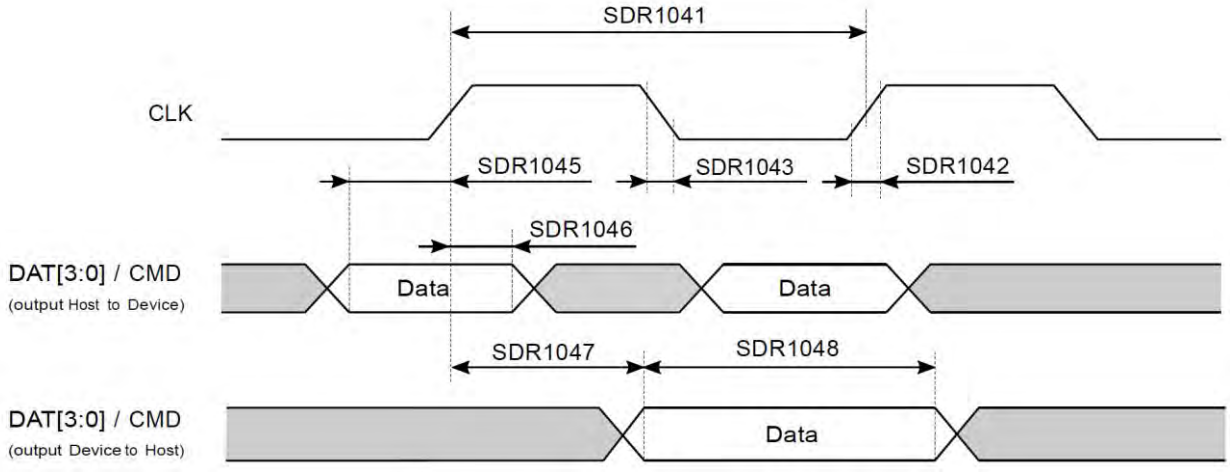

Figure 3-17 SD Timing Diagram (SDR104 mode)

3.6.1.5 SDIO3.0+ Interface

Table 3-22 presents timing characteristics for SDIO3.0+ interface in the device.

Table 3-22 SDIO3.0+ Timing Characteristics (HS400 mode host output)

No.	Parameter		Min	Max	Unit
CLK output from host					
SDIO1	t_C	Cycle time, CLK	5		ns
SDIO2	t_{dd}	CLK duty distortion		0.2	ns
SDIO3	t_{pw}	Minimum pulse width	2.3		ns
Host DAT output (refer to CLK)[1]					
SDIO4	t_{su_DATA}	Setup time, DATA output	0.7[2]		ns
SDIO5	t_{h_DATA}	Hold time, DATA output	0.7[2]		ns

1. HS400 mode CMD timing is the same as SDR104 mode.
2. Simulation result.

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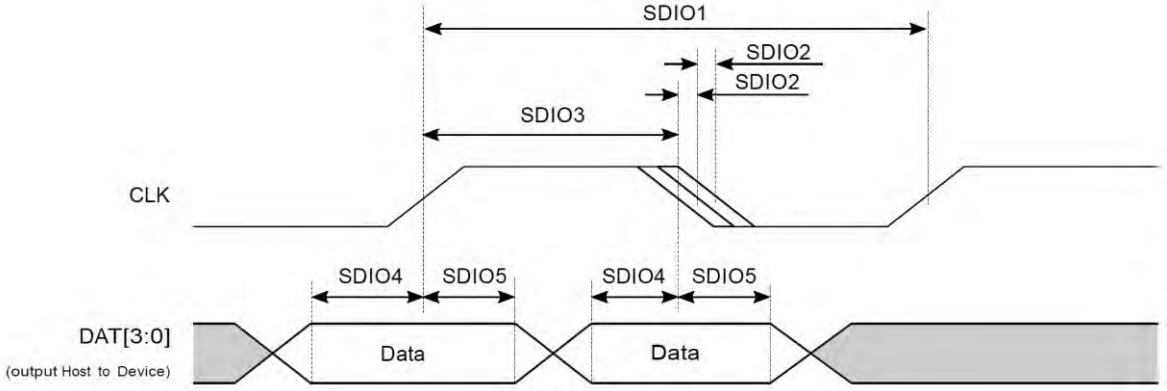

Figure 3-18 SDIO3.0+ Timing Diagram (HS400 mode host output)

Table 3-23 SDIO3.0+ Timing Characteristics (HS400 mode host input)

No.	Parameter		Min	Max	Unit
Data strobe output from device					
HSHI1		Data strobe period	5		ns
HSHI2		Data strobe duty distortion		0.3	ns
HSHI3		Minimum pulse width	1.9		ns
Host DAT input (refer to data strobe)					
HSHI4	t_{sk_DATA}	Input skew		0.5	ns
HSHI5	t_{skh_DATA}	Input hold skew		0.5	ns

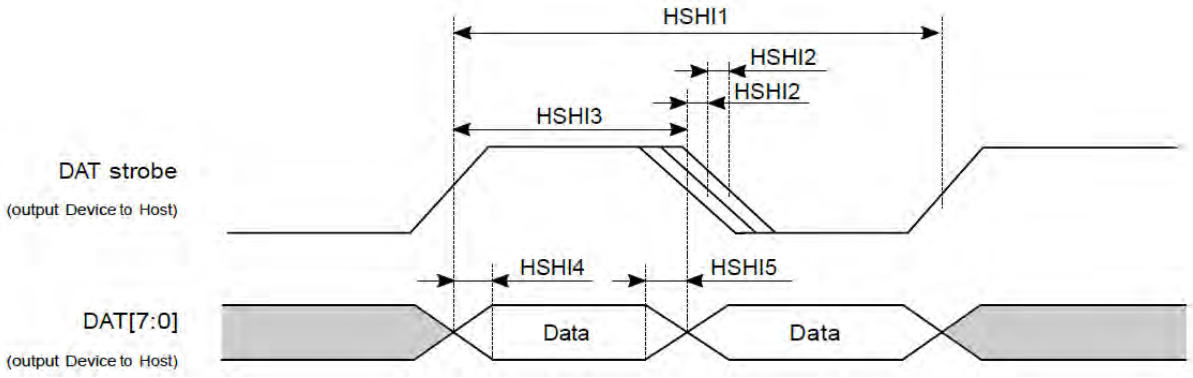

Figure 3-19 SDIO3.0+ Timing Diagram (HS400 mode host input)

3.6.2 NAND Flash Interface (NFI)

The device has integrated NAND flash interface controller for connection to SLC/MLC/TLC NAND flash memories.

The NFI controller supports the following key features:

- Legacy NAND flash timing control
- Toggle NAND v1.0 flash timing control
- Open NAND Flash Interface (ONFI) v2.x flash timing control
- ECC engine with BCH code capable of correcting up to 80-bit errors within one sector
- Programmable page size and spare size
- Programmable FDM data size and protected FDM data size
- Word and byte access through APB bus
- DMA for massive data transfer

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- Latch sensitive interrupt indicating ready state for read, program, and erase operations
- Programmable:
  - Wait states
  - Command and address setup and hold time
  - Read enable hold time
  - Write enable recovery time
- 2-chip selects
- 8-bit Toggle and ONFI NAND I/O interface
- Randomizer (TOSHIBA or SAMSUNG)

3.6.2.1 NFI Signal Descriptions

Table 3-24 presents NFI signal descriptions.

Table 3-24 NFI Signal Descriptions

Signal Name	Type	Description	Ball Location
NFI Port Bus -NLD[7:0]			
NLD0	DIO	Input/Output Port bit 0	M27
NLD1	DIO	Input/Output Port bit 1	L27
NLD2	DIO	Input/Output Port bit 2	L28
NLD3	DIO	Input/Output Port bit 3	N29
NLD4	DIO	Input/Output Port bit 4	L30
NLD5	DIO	Input/Output Port bit 5	L29
NLD6	DIO	Input/Output Port bit 6	N30
NLD7	DIO	Input/Output Port bit 7	P30
NFI Command and Control Signals			
NREB	DO	Read enable, active low	R28
NRNB	DI	Ready/Busy	R27
NWEB	DO	Write enable, active low	M28
NALE	DO	Address latch enable	M26
NCEB0	DO	Chip enable 0, active low	P28
NCEB1	DO	Chip enable 1, active low	P27
NCLE	DO	Command latch enable	P29
NDQS	DIO	Data strobe complement	M29

3.6.2.2 NFI Timing Characteristics

3.6.2.2.1 ONFI1.0 Timing Characteristics

Table 3-25 and Figure 3-20 through Figure 3-22 present the output timing characteristics for ONFI1.0 mode—write access.

Table 3-25 NFI ONFI1.0 Command/Address/Data Write Access Timing

No	Parameter	Description	Min	Max	Unit
DS	t_{DS}	Write data setup time	11.8		ns
DH	t_{DH}	Write data hold time	11.8		ns
WP	t_{WP}	Write low pulse time	12.8		ns

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No	Parameter	Description	Min	Max	Unit
WH	t_{WH}	Write high pulse time	12.8		ns
CS	t_{CS}	CE setup time	50.2		ns
CH	t_{CH}	CE hold time	101.5		ns
CLS	t_{CLS}	Command latch enable setup time	50.2		ns
CLH	t_{CLH}	Command latch enable hold time	24.6		ns
ALS	t_{ALS}	Address latch enable setup time	50.2		ns
ALH	t_{ALH}	Address latch enable hold time	24.6		ns
WC	t_{WC}	Write cycle time	25.6		ns

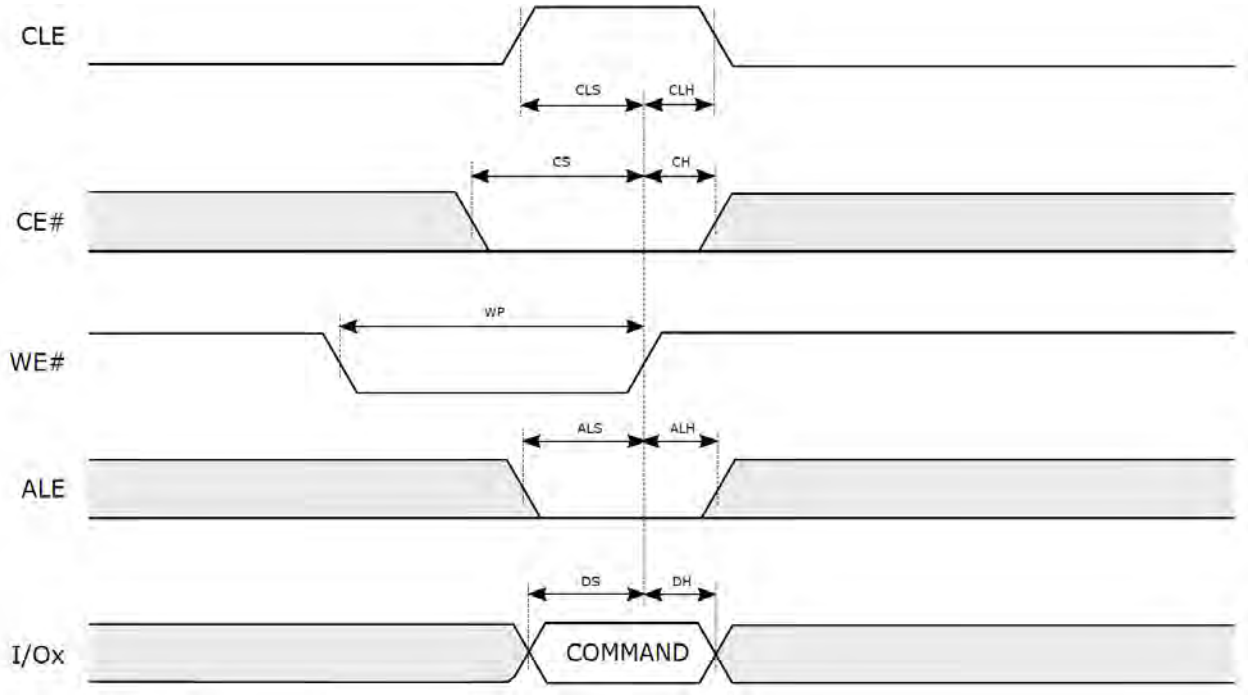

Figure 3-20 NFI ONFI1.0 Command Input Cycle

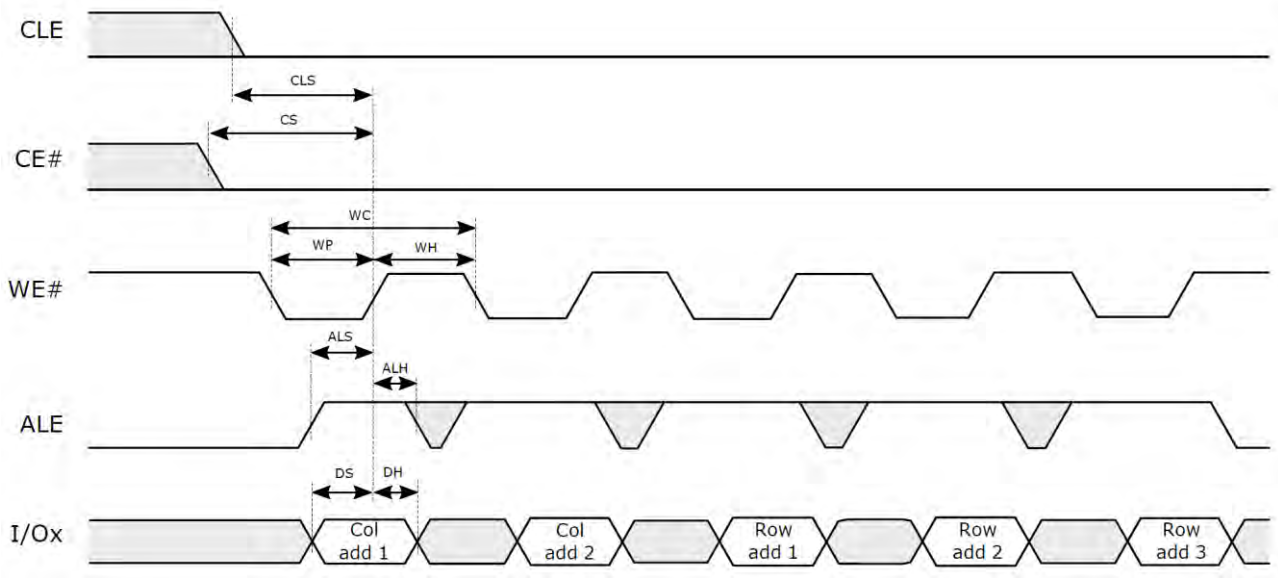

Figure 3-21 NFI ONFI1.0 Address Input Cycle

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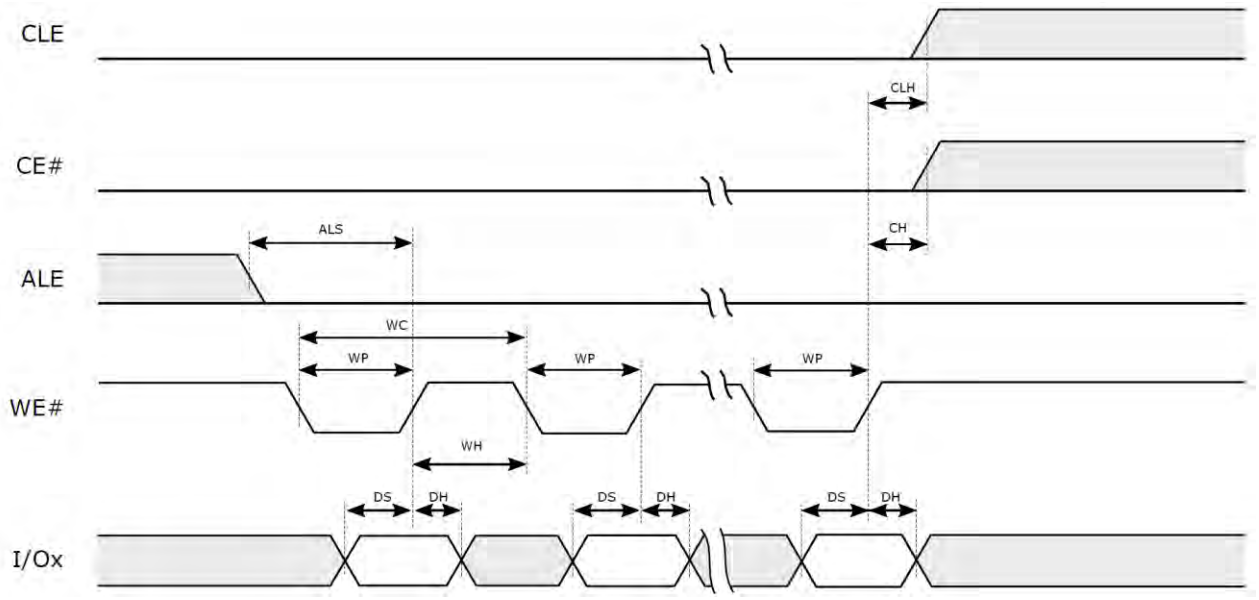

Figure 3-22 NFI ONFI1.0 Consecutive Data Write Cycles

Table 3-26 and Figure 3-23 present the input timing characteristics for ONFI1.0 mode—read access.

Table 3-26 NFI ONFI1.0 Read Access Timing

No	Parameter	Description	Min	Max	Unit
REA	t_{REA}	RE access required time	0	34.3	ns
RP	t_{RP}	Read low pulse time	12.8		ns
REH	t_{REH}	Read high pulse time	12.8		ns
RHZ	t_{RHZ}	RE high to output Hi-Z required time		t_{REA}+ t_{REH}	ns
RC	t_{RC}	Read cycle time	25.6		ns

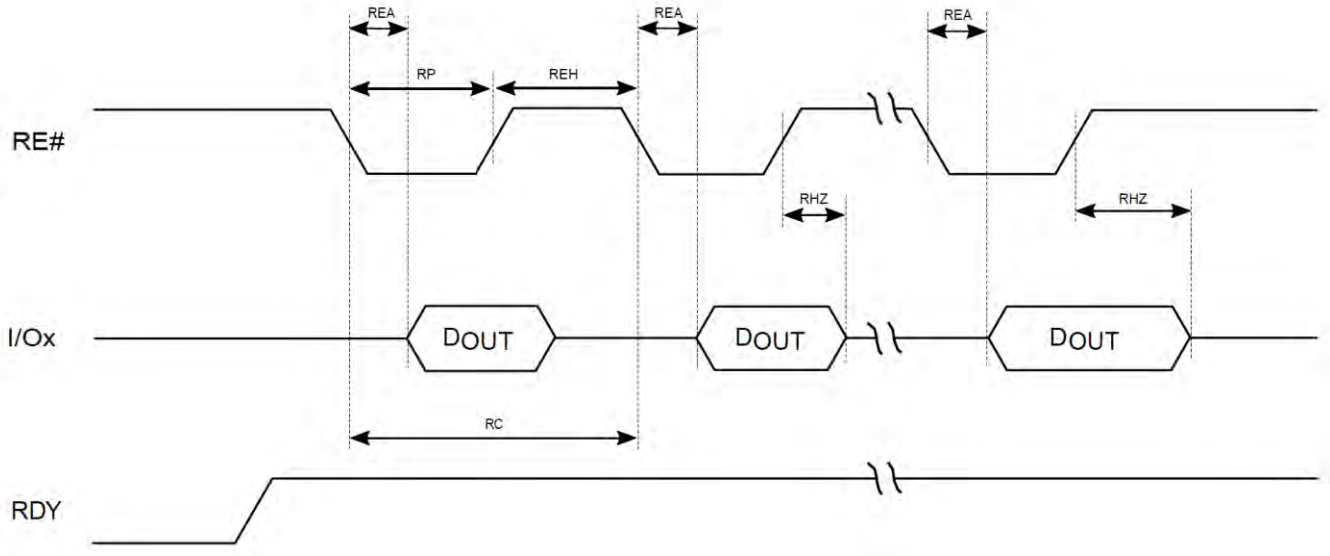

Figure 3-23 NFI ONFI1.0 Serial Read Cycle

3.6.2.2.2 NAND (Toggle1.0) Timing Characteristics

Table 3-27 and Figure 3-24 through Figure 3-26 present the output timing characteristics for NFI Toggle1.0 mode—write access.

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Table 3-27 NFI Toggle1.0 Write Access Timing

No	Parameter	Description	Min	Max	Unit
CS	t_{CS}	CE setup time	191		ns
CH	t_{CH}	CE hold time	178		ns
CALS	t_{CALS}	CLE/ALE setup time	191		ns
CALH	t_{CALH}	CLE/ALE hold time	24		ns
WP	t_{WP}	WE low pulse time	24		ns
CAS	t_{CAS}	CMD/ADR setup time	24		ns
CAH	t_{CAH}	CMD/ADR hold time	12		ns
WH	t_{WH}	WE high pulse time	12		ns
DS	t_{DS}	Data setup time	3		ns
DH	t_{DH}	Data hold time	2.5		ns
DQSH	t_{DQSH}	DQS high pulse	6		ns
DQSL	t_{DQSL}	DQS low pulse	6		ns
DSC	t_{DSC}	Data strobe cycle time	12.8		ns

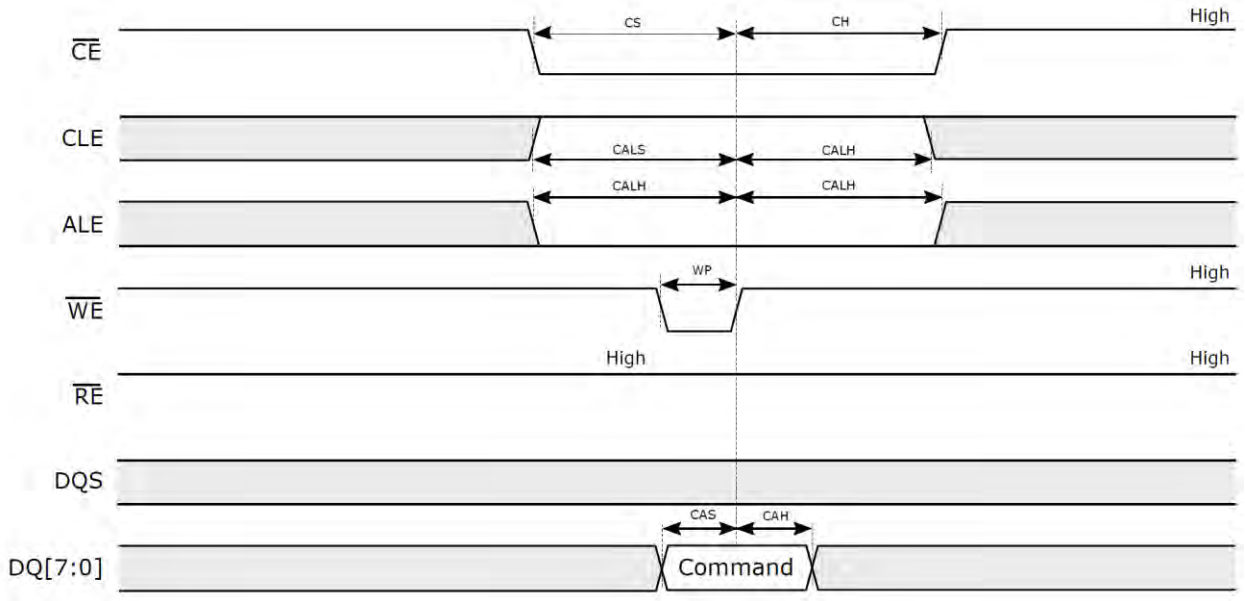

Figure 3-24 NFI Toggle1.0 Command Input Cycle

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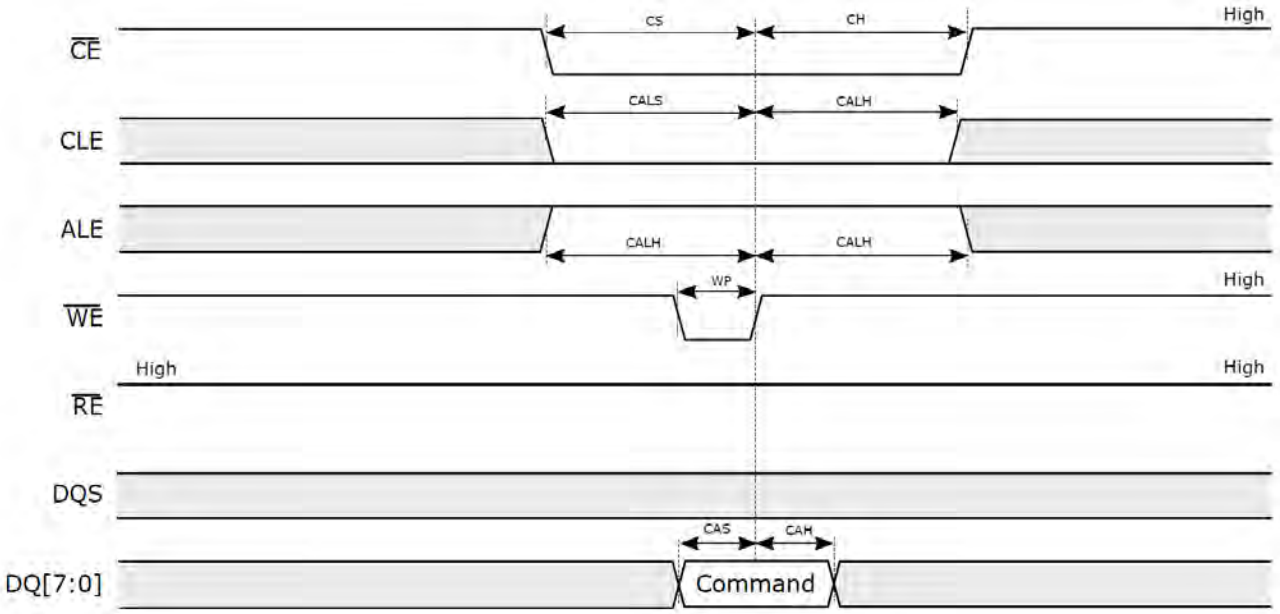

Figure 3-25 NFI Toggle1.0 Address Input Cycle

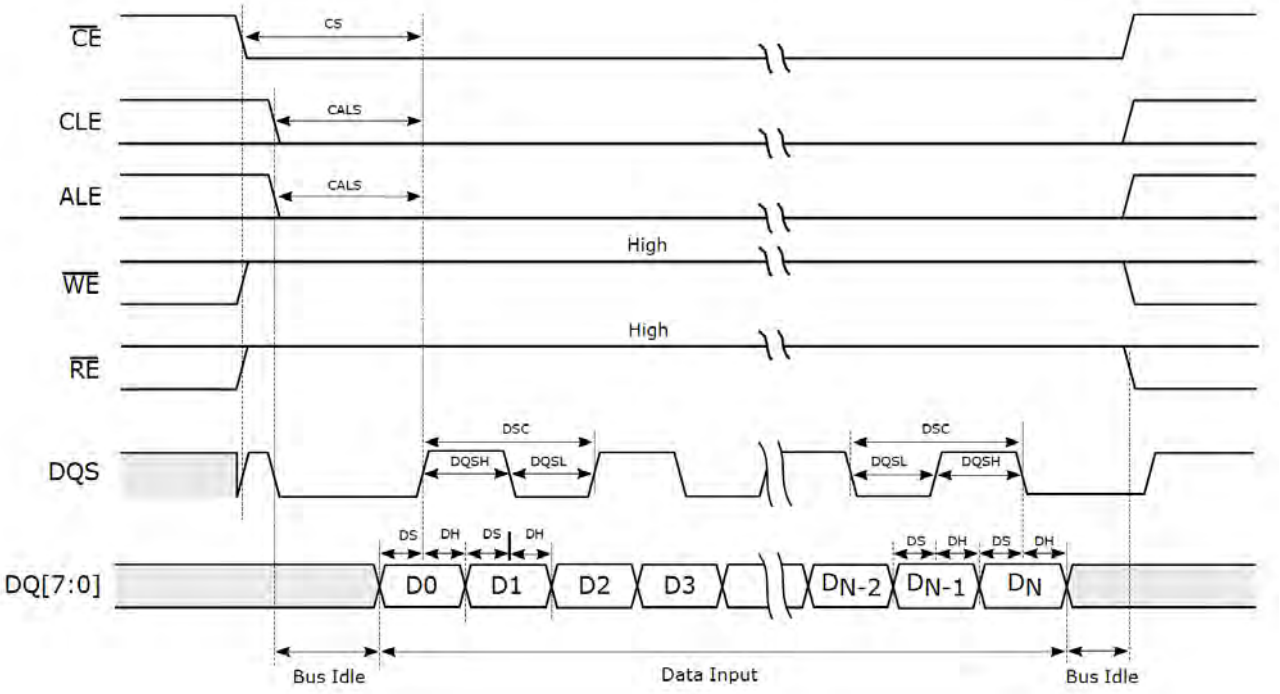

Figure 3-26 NFI Toggle1.0 Data Write Cycle

Table 3-28 and Figure 3-27 present the input timing characteristics for NFI Toggle1.0 mode—read access.

Table 3-28 NFI Toggle1.0 Read Access Timing

No	Parameter	Description	Min	Max	Unit
REH	t_{REH}	RE high pulse time	6		ns
RP	t_{RP}	RE low pulse time	6		ns
RC	t_{RC}	RE read cycle time	12.8		ns
DQSRE	t_{DQSRE}	RE to DQS/DQ delay	0	30	ns
DQSQ	t_{DQSQ}	Output skew among DQ and DQS		800	ps

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No	Parameter	Description	Min	Max	Unit
QH	t_{QH}	Output hold time from DQS	min(t_{REH}, t_{RP}) - t_{QHS}		ns
QHS	t_{QHS}	DQS hold skew factor (up to device)		800	ps
DVW	t_{DVW}	Output data valid window (up to device)	t_{QH} - t_{DQSQ}		ns

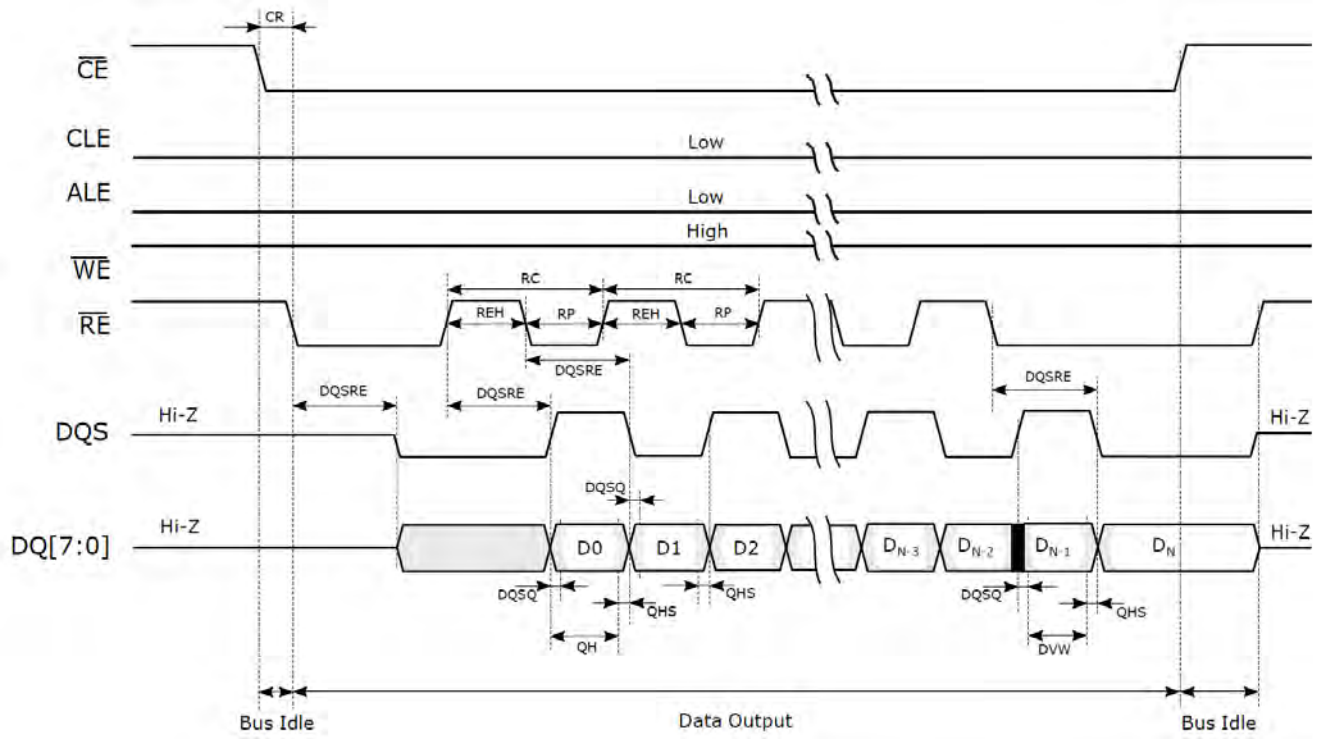

Figure 3-27 NFI Toggle1.0 Data Read Cycle

3.6.2.2.3 ONFI2.x Timing Characteristics

Table 3-29 and Figure 3-28 through Figure 3-30 present the output timing characteristics for ONFI2.x Sync mode—write.

Table 3-29 NFI ONFI2.x Sync Mode Write Timing

No	Parameter	Description	Min	Max	Unit
CS	t_{CS}	CE setup time	14		ns
CH	t_{CH}	CE hold time	4		ns
CAD	t_{CAD}	Command, address data delay	34		ns
CALS	t_{CALS}	CLE/ALE setup time	4		ns
CALH	t_{CALH}	CLE/ALE hold time	4		ns
CKL	t_{CKL}	CLK cycle high	4.5		ns
CKH	t_{CKH}	CLK cycle low	4.5		ns
CK	t_{CK}	CLK cycle time	10		ns
CAS	t_{CAS}	CMD/ADR setup time	4		ns
CAH	t_{CAH}	CMD/ADR hold time	4		ns
DSS	t_{DSS}	Data setup time	4		ns
DSH	t_{DSH}	Data hold time	4		ns
DQSH	t_{DQSH}	DQS high pulse	4		ns
DQSL	t_{DQSL}	DQS low pulse	4		ns
DQSS	t_{DQSS}	Data input	10		ns
DS	t_{DS}	Data setup time	1.8		ns

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No	Parameter	Description	Min	Max	Unit
DH	t_{DH}	Data hold time	2.8		ns

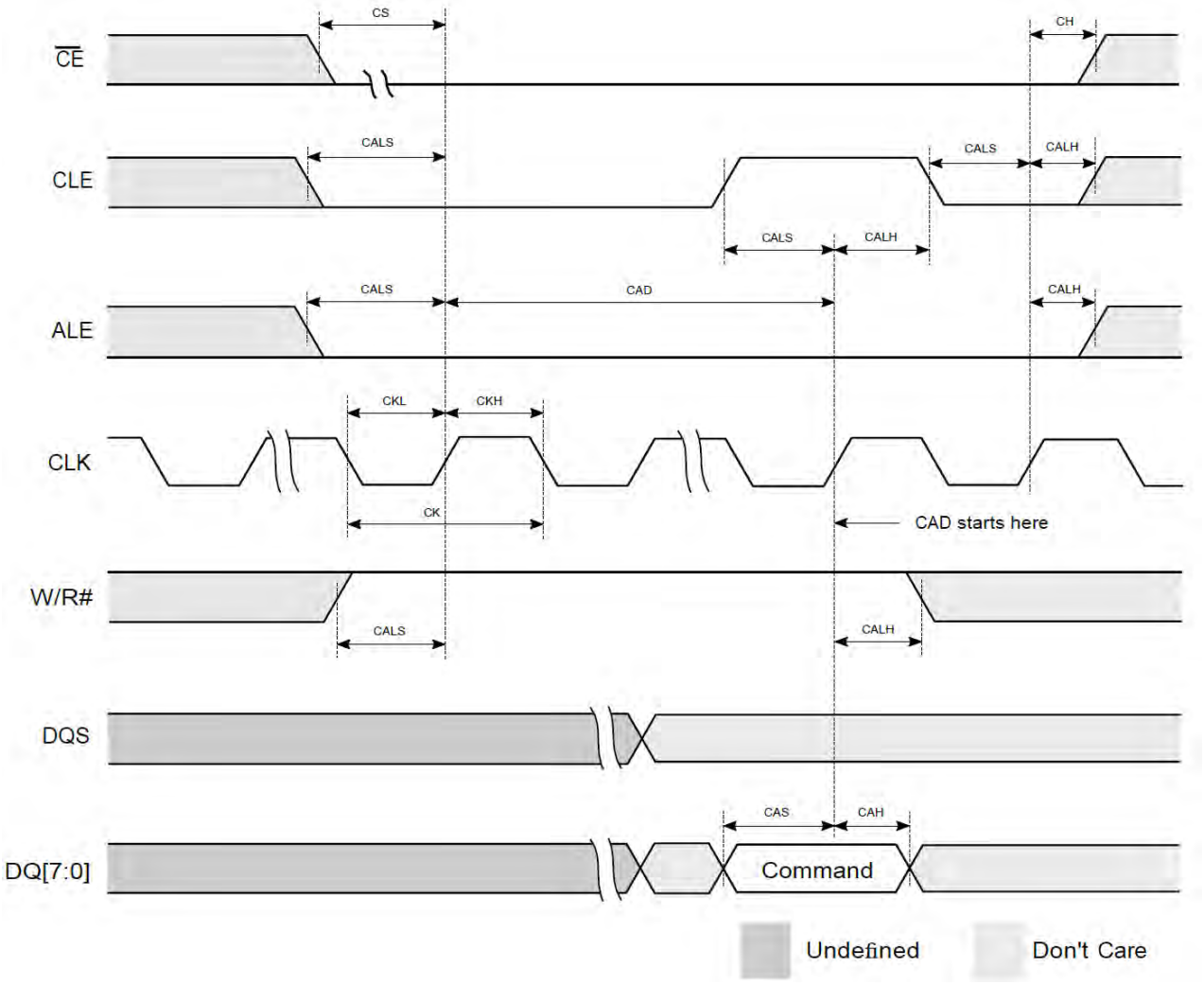

Figure 3-28 NFI ONFI2.x Command Input Cycle

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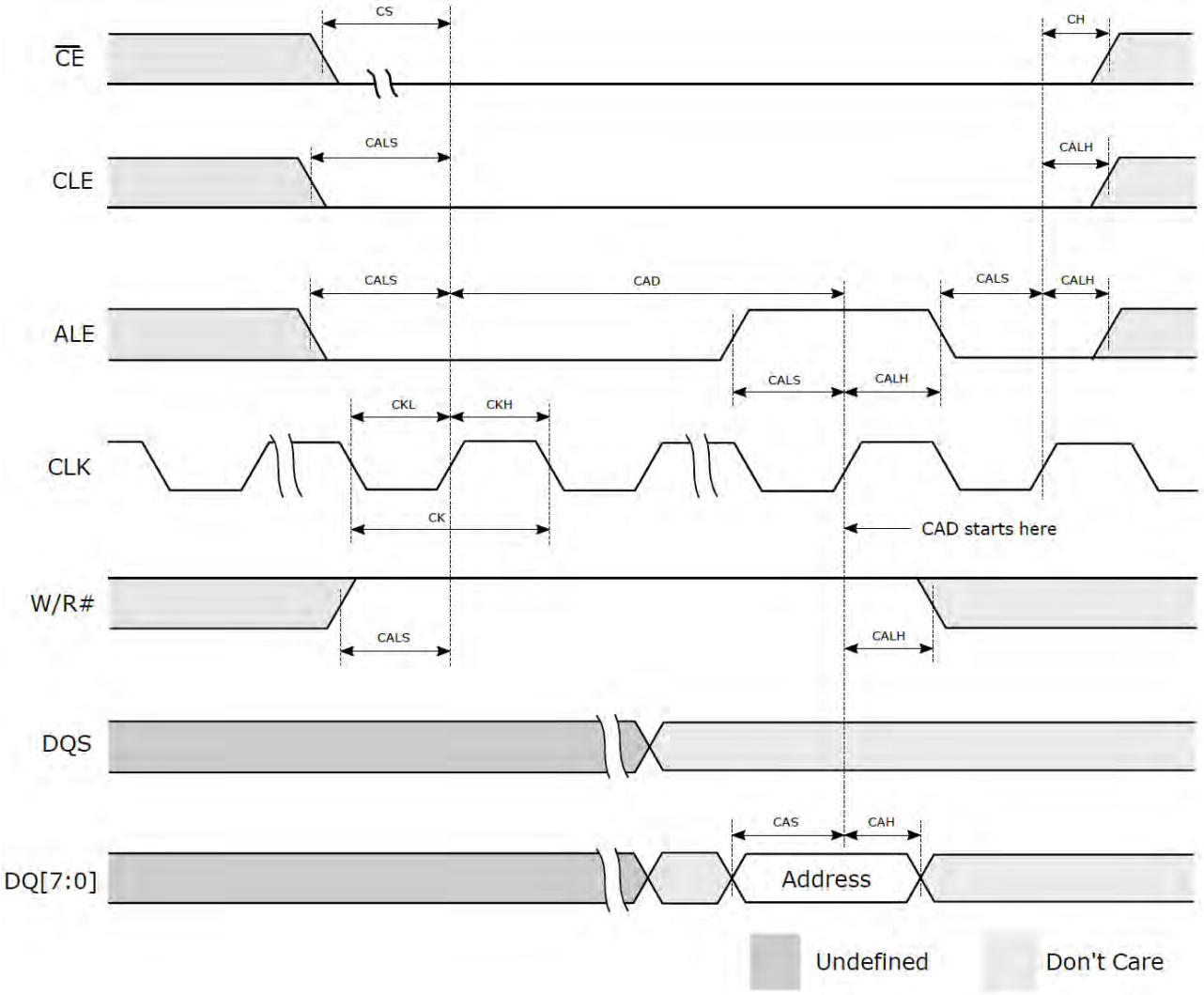

Figure 3-29 NFI ONFI2.x Address Input Cycle

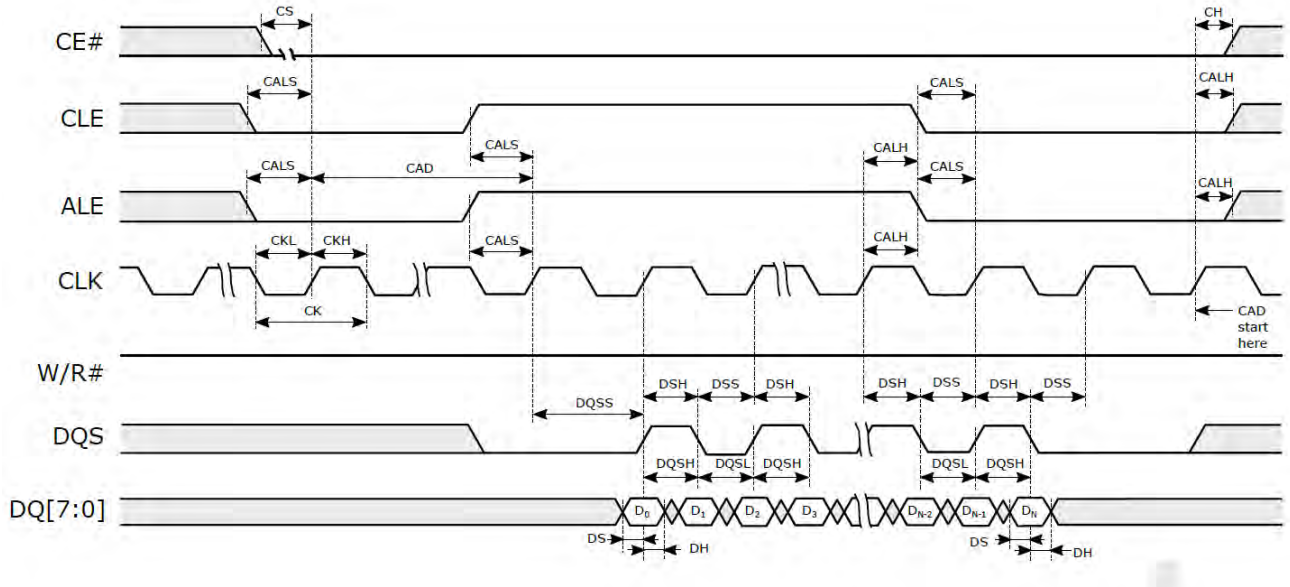

Figure 3-30 NFI ONFI2.x Data Write Cycle

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Table 3-30 and Figure 3-31 present the input timing characteristics for ONFI2.x Sync mode—read.

Table 3-30 NFI ONFI2.x Sync Mode Read Timing

No	Parameter	Description	Min	Max	Unit
CK	t_C	Cycle time, CLK	9		ns
CKL	$t_{w_CLK_L}$	Pulse duration, CLK low	4.5		ns
CKH	$t_{w_CLK_L}$	Pulse duration, CLK high	4.5		ns
HP	t_{HP}	Half clock period	4.5		ns
DQSQ	t_{DQSQ}	DQS-DQ skew	0	800	ps
DVW	t_{DVW}	Data valid window	t_{QH} - t_{DQSQ}		ns
DQSCK	t_{DQSCK}	Access window of DQS from CLK	0	30	ns
QH	t_{QH}	DQ-DQS hold, DQS to first DQ to go non-valid, per access	4		ns

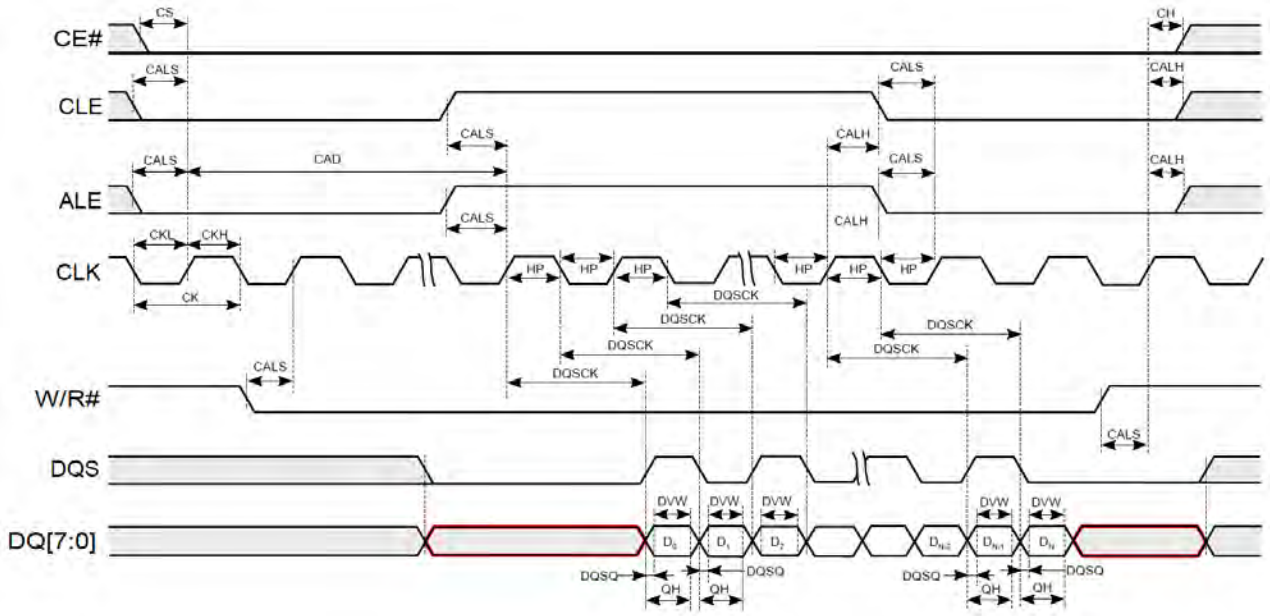

Figure 3-31 NFI ONFI2.x Data Read Cycle

3.7 Display

The display subsystem consists of two distinctive components:

- Multimedia Data Path (MDP) is a time-sharing pipeline data flow controller performing resizing and rotation operations for memory-to-memory pixel data transfers.
- Display Controller Data Path (DISP) is a set of read/write DMA engines and various pixel data processing cores. The processed data can be either stored back in memory and/or delivered to display interface controllers like DSI and DPI.

  The DPI port can output the data either directly on device pads, or deliver it either to the LVDS encoder or to an HDMI transmitter (through external bridge).

3.7.1 Multimedia Data Path (MDP)

The MDP is a set of DMA and image processing cores, the main purpose of which is generating images for display, video codec, JPEG codec and face detection.

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3.7.1.1 MDP Read DMA (MDP_RDMA)

The MDP_RDMA is used to read images of multiple source formats in memory and output in scan line sequence. The MDP_RDMA is fully tile mode ready and can fulfil the single or the tile modes of operation, in order to support larger image size.

The MDP_RDMA supports several functions:

- Multiple formats of input images
- Input image cropping/clipping
- Tile mode ready; supports source width up to 131,072 pixels
- Multiple formats of input images:
  - YUV420 and YUV422 scan line 1/2/3 planes
  - RGB 16/24/32-bit
- Arbitrary byte swap for YUV or RGB source
- 3 × 3 color space conversion from RGB to YUV
- Chroma upsample to YUV444 for cosited or non-cosited YUV420 and YUV422 source data

Figure 3-32 shows the internal pipeline of MDP_RDMA. The input data is fetched from an external memory via SMI read port, while the output is directly linked to the next processing engine depending on the multimedia data path setting, for example MDP_RSZ. There is also an APB interface for software control.

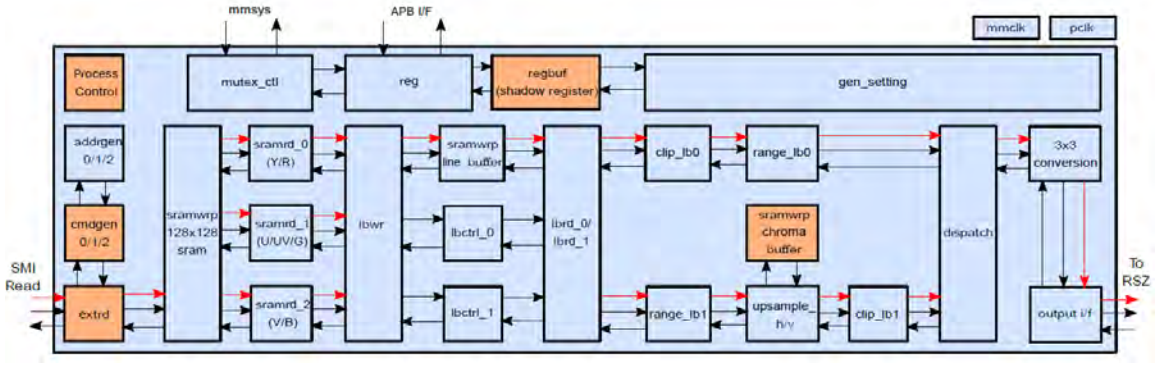

Figure 3-32 MDP_RDMA Block Diagram

3.7.1.2 MDP Color Correction (MDP_CCORR)

The MDP color correction engine changes the overall mixture of RGB colors to fit the characteristics of the target display panel.

The MDP_CCORR supports the following features:

- YUV to RGB and RGB to YUV conversions
- Fixed-coefficient inverse gamma correction
- Programmable 3 × 3 conversion matrix

3.7.1.3 MDP Resizer (MDP_RSZ)

There are two resizer modules within the MDP: MDP_RSZ0 and MDP_RSZ1.

Each resizer supports the following key features:

- Three scaling algorithms (depending on the scaling ratio) including 6-tap FIR, 4n-tap cubic accumulation, and n-tap source accumulation

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- 8-bit YUV444 (unsigned) input and output data format
- Scaling ratio between 1/128× and 64×
- Crop and digital zoom functions
- Maximum width of 544 pixels (tile mode)
- Edge-preserving interpolation
- Signal enhancer (pre-scaler sharpness)

3.7.1.4 MDP 2D Sharpness Engine (MDP_TDSHP)

The sharpness function provides better picture quality for panel display by restoring the image details, sharpening the edge and delivering a vivid feeling for pictures and videos.

The MDP_TDSHP supports the following functions:

- 2-dimensional sharpness filter
- Peaking by Color (PBC)
- Gain curve control
- Content analyzer

3.7.1.5 MDP Rotation DMA (MDP_WROT)

There are two write rotate DMA agents within the MDP, MDP_WROT0 and MDP_WROT1, each supporting 8 rotation/flip options.

Each MDP_WROT provides the following key features:

- Rotation angles: 0°, 0° + H_Flip, 90°, 90° + H_Flip, 180°, 180° + H_Flip, 270°, and 270° + H_Flip
- Formats and footprints: YUV422 1/2/3 plane(s), YUV420 2/3 plane(s), RGB888, ARGB8888, RGB565, Y only
- Programmable RGB color matrix
- Dither function

3.7.2 Display Data Path (DISP)

The DISP consists of two display pipelines. One display pipeline fetches pixel data from memory, performs various processing operations and outputs the data either to multiple display interface controllers or writes it back to memory. The other pipeline fetches pixel data from memory and directly provides it to the display interface controllers.

3.7.2.1 DISP Read DMA (DISP_RDMA)

The DISP_RDMA engine reads out the data in the display pipeline from either DRAM or from upstream engines within the display pipeline, applies processing operations and delivers the data to the display interface engines like DSI and DPI.

The DISP_RDMA supports the following key features:

- Direct link input mode
- Memory input mode
  - Input formats: YUYV422, UYVY422, YVYU422, UYVY422, RGB565, RGB888, ARGB8888
  - Input footprints: Raster-scan mode, 64 byte-aligned tile mode
  - Slow down mode

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- Output control
  - Byte swap, RGB swap
  - Progressive and interlace modes
  - Programmable YUV to RGB conversion matrix
  - Non-stop output mode, if the data buffer is under-running
- Buffer control
  - 384 × 16 bytes data buffer (1920 pixels with RGB888 format)
  - Programmable request, pre-ultra, and ultra control mechanisms

3.7.2.2 DISP Write DMA (DISP_WDMA)

The DISP_WDMA writes out the data in display pipeline into the DRAM.

The DISP_WDMA provides the following key features:

- Input color format: YUV444/RGB888
- Dither function
- Programmable parameter color transformation
- 3-tap filter in horizontal and 2-tap filter in vertical direction for YUV420 down sample
- Byte swap, color swap, and UV swap functions
- Output color formats: RGB565/RGB888/ARGB8888/UYVY/YV12/NV12/NV21

3.7.2.3 DISP Overlay (DISP_OVL)

The DISP_OVL manager does alpha blending of pixel data layers. The source pixel data is fetched from DRAM by a dedicated read DMA for each layer. The pixel data is processed depending on pixel characteristics and the display requirements.

There are two DISP_OVL managers in the DISP: DISP_OVL0 and DISP_OVL0_2L.

Each DISP_OVL supports the following key features:

- Layers of blending:
  - Up to 4 layers for DISP_OVL0
  - Up to 2 layers for DISP_OVL0_2L
- Input resolution:
  - Full HD+ (2400p × 1080p) for DISP_OVL0
  - Full HD (1920p × 1080p) for DISP_OVL0_2L
- Memory source formats: RGB565/RGB888/ARGB8888/PARGB8888/XRGB/YUV422
- Swap control:
  - RGB swap and byte swap control (RGB/BGR/xARGB/xABGR/RGBxA/BGRxA)
  - UYVY swap (UYVY/VYUY/YUYV/YVYU)
- Interleaving of left and right images for 3D display in landscape and portrait modes (supported by DISP_OVL0_2L only)
- One common color conversion set with fixed coefficients (BT.T601/BT.T709/JPEG) that serves all layers and processes one pixel per clock cycle.
- Source color key or destination color key
- Pixel alpha with PARGB/ARGB and constant alpha or surface flinger alpha blending
- Flexible Region-of-Interest (ROI) system, supporting individual color depth, window size, vertical and horizontal offsets
- Vertical, horizontal, and 180-degree flip function

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3.7.2.4 DISP Color Engine (DISP_COLOR)

The DISP_COLOR is a multi-stage processing engine that is used for achieving better picture quality and making one display panel resemble another in their output characteristics. It provides color space conversion functions and various hue/luma/saturation adjustments.

The DISP_COLOR supports the following key features:

- Input (RGB to YUV) and output (YUV to RGB) color space conversion
- Hue engine functions:
  - Partial hue: modifies hue angle of specific hue phase
- Luma engine functions:
  - Adaptive luma: adaptively adjusts Y curve according to image content
  - Global contrast and brightness adjustment
  - Chroma boost: compensates saturation value due to Y change
- Saturation engine functions:
  - Partial S: modifies saturation value of specific hue phase
  - Global saturation adjustment
- Histogram statistics: includes chroma histogram

3.7.2.5 DISP Color Correction (DISP_CCORR)

The DISP_CCORR engine changes the overall mixture of RGB colors to fit the characteristics of target display panel.

The DISP_CCORR supports the following key features:

- Fixed-coefficient inverse gamma table
- Fixed-coefficient gamma table
- Programmable 3×3 matrix

3.7.2.6 DISP Adaptive Ambient Light Controller (DISP_AAL)

The DSIP_AAL controller includes content adaptive and ambient light adaptive functions. It is responsible for backlight power saving and sunlight visibility improvement.

The DISP_AAL provides the following key features:

- 33-bin weighted histogram
- Dark Region Enhancement (DRE) function for sunlight visibility
- Content Adaptive Backlight Control (CABC) compensation for backlight power saving

3.7.2.7 DISP Gamma Engine (DISP_GAMMA)

The DISP_GAMMA engine provides gamma correction by changing the overall mixture of RGB colors to fit the characteristics of the display panel.

The DISP_GAMMA supports the following key features:

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- 10-bit gamma table with 512 entries
- Non-block gamma LUT programming

3.7.2.8 DISP Dither Engine (DISP_DITHER)

The DISP_DITHER engine is used to reduce effect of quantization errors while decreasing the RGB depth.

The DISP_DITHER supports the following key features:

- Ordered dithering: Running order dither frame phase control
- Linear Feedback Shift Register (LFSR) dithering
- Rounding

3.7.2.9 Display Resizer (DISP_RSZ)

The DISP_RSZ is the resizer module in the display data path.

The DISP_RSZ supports the following key features:

- Input and output format: ARGB8888
- Up-scaling only
- Scaling ratio between 1× and 64×
- 4-tap FIR
- Maximum width of 736 pixels

3.7.2.10 DISP Mutex (DISP_MUTEX)

The DISP_MUTEX is used to synchronize the start trigger signal of each submodule in the display data path. This enables the composition of up to two independent real-time display paths, or multiple soft paths, which can perform multi-tasking between several software processes.

The DISP_MUTEX supports the following key features:

- Up to 10 mutex cores in parallel
- Each submodule in the display data path can be assigned to any one of the 10 mutex cores
- Start trigger signal selection for each mutex core: driven either from SW or from a display interface (DSI, DPI)

The start trigger method determines the operation mode of the display data path:

- Single mode (SW trigger):
  - Single frame processing upon every SW trigger
  - Memory in-memory out path (not always being single mode)
  - Memory in and direct link to command mode display output (for example, DSI command mode)
- Refresh mode (display interface trigger):
  - Frame-by-frame processing after start
  - Memory in and direct link to video mode display output (for example, DSI video mode, DPI, LVDS, HDMI)

3.7.3 Display Parallel Interface (DPI)

The DPI controller provides data to the companion chip, such as HDMI, MHL, or other bridge chips.

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The DPI controller supports the following key features:

- Progressive/interlaced timing generator
- Programmable EAV and SAV embedded synchronization timing
- Fixed-coefficient color space transformation
- Supports RGB888 without VSync, HSync, de/ YUV444 8-bit without VSync, HSync, de/ RGB666/YUV444 6-bit/YUV422 8-bit output data formats
- Supports YC MUX (CCIR656-like) output format
- Supports dual edge output format
- 3-tap chroma Low-Pass Filter (LPF)
- YUV444 to YUV422 chroma resampling
- Internal pattern generator

3.7.3.1 DPI Signal Descriptions

Table 3-31 presents DPI signal descriptions.

Table 3-31 DPI Signal Descriptions

Signal Name	Type	Description	Ball Location
Display Pixel Data Bus—DPI_D[23:0]			
DPI_D0	DO	Display pixel data 0	AE20
DPI_D1	DO	Display pixel data 1	AE21
DPI_D2	DO	Display pixel data 2	AF21
DPI_D3	DO	Display pixel data 3	AG22
DPI_D4	DO	Display pixel data 4	AF19
DPI_D5	DO	Display pixel data 5	AH19
DPI_D6	DO	Display pixel data 6	AF18
DPI_D7	DO	Display pixel data 7	AG21
DPI_D8	DO	Display pixel data 8	AJ19
DPI_D9	DO	Display pixel data 9	AG18
DPI_D10	DO	Display pixel data 10	AJ18
DPI_D11	DO	Display pixel data 11	AH18
DPI_D12	DO	Display pixel data 12	AH17
DPI_D13	DO	Display pixel data 13	AH16
DPI_D14	DO	Display pixel data 14	AJ16
DPI_D15	DO	Display pixel data 15	AB13
DPI_D16	DO	Display pixel data 16	AB14
DPI_D17	DO	Display pixel data 17	AD14
DPI_D18	DO	Display pixel data 18	AC14
DPI_D19	DO	Display pixel data 19	AE13
DPI_D20	DO	Display pixel data 20	AC13
DPI_D21	DO	Display pixel data 21	AF14
DPI_D22	DO	Display pixel data 22	AF13
DPI_D23	DO	Display pixel data 23	AD13
DPI Command and Clock Signals			
DPI_CK	DO	Display pixel clock	AF17

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Signal Name	Type	Description	Ball Location
DPI_DE	DO	Display pixel data enable	AE17
DPI_HSYNC	DO	Display horizontal sync	AG17
DPI_VSYNC	DO	Display vertical sync	AE16

Table 3-32 presents the DPI signal mapping.

Table 3-32 DPI Signal Mapping

Ball Number	Ball Name	RGB-888	RGB-666	DPI-12Bit	
				1st edge	2nd edge
AE20	DPI_D0	B0	N/A	B0	G4
AE21	DPI_D1	B1	N/A	B1	G5
AF21	DPI_D2	B2	B0	B2	G6
AG22	DPI_D3	B3	B1	B3	G7
AF19	DPI_D4	B4	B2	B4	R0
AH19	DPI_D5	B5	B3	B5	R1
AF18	DPI_D6	B6	B4	B6	R2
AG21	DPI_D7	B7	B5	B7	R3
AJ19	DPI_D8	G0	N/A	G0	R4
AG18	DPI_D9	G1	N/A	G1	R5
AJ18	DPI_D10	G2	G0	G2	R6
AH18	DPI_D11	G3	G1	G3	R7
AH17	DPI_D12	G4	G2	N/A	N/A
AH16	DPI_D13	G5	G3	N/A	N/A
AJ16	DPI_D14	G6	G4	N/A	N/A
AB13	DPI_D15	G7	G5	N/A	N/A
AB14	DPI_D16	R0	N/A	N/A	N/A
AD14	DPI_D17	R1	N/A	N/A	N/A
AC14	DPI_D18	R2	R0	N/A	N/A
AE13	DPI_D19	R3	R1	N/A	N/A
AC13	DPI_D20	R4	R2	N/A	N/A
AF14	DPI_D21	R5	R3	N/A	N/A
AF13	DPI_D22	R6	R4	N/A	N/A
AD13	DPI_D23	R7	R5	N/A	N/A
AF17	DPI_CK	DPI_CK			
AE17	DPI_DE	DPI_DE			
AG17	DPI_HSYNC	DPI_HSYNC			
AE16	DPI_VSYNC	DPI_VSYNC			

3.7.3.2 DPI Timing Characteristics

Table 3-33 and Figure 3-33 present timing characteristics for DPI in the device.

Table 3-33 DPI Timing Characteristics

No.	Parameter		Min	Max	Unit
DPI01	t_c	Cycle time	13.47[1]		ns
DPI02	D	Duty cycle, DPI_CK	45	55	%
DPI03	t_{RISE}	Rise time		2.69	ns

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No.	Parameter		Min	Max	Unit
DPI04	t_{FALL}	Fall time		2.69	ns
DPI05	t_d	Delay time, other signals to DPI_CK	3.69		ns

1. For maximum operating clock frequency refer to Table 6-1.

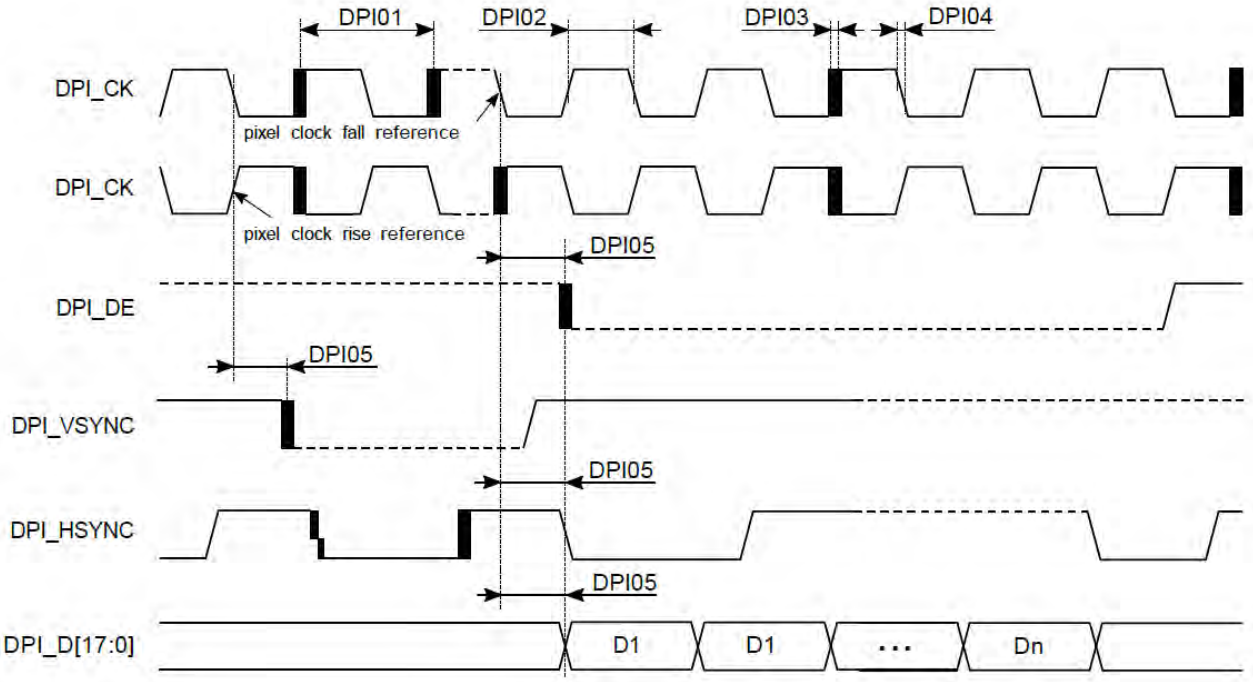

Figure 3-33 DPI Timing Diagram

3.7.4 Display Serial Interface (DSI)

The DSI is based on MIPI Alliance Specification, supporting high-speed serial data transfer between host processor and peripheral devices such as display modules.

The DSI module receives frame pixels from memory, performs frames packing and lane distribution, and then sends the data to the MIPI D-PHY TX core for serializing.

Figure 3-34 shows DSI functional block diagram.

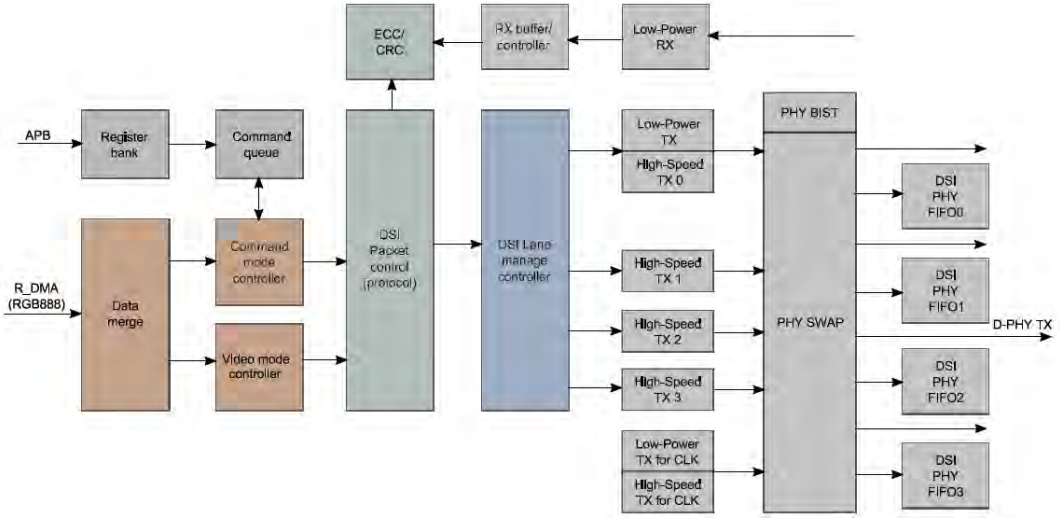

Figure 3-34 DSI Block Diagram

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The DSI module has the following key features for display serial interface:

- Supports video and command mode data transfers
- 1 clock lane and up to 4 data lanes
- Throughput up to 1.2 Gbps per data lane
- Bi-directional data transmission in Low-Power mode in data lane 0
- Uni-directional data transmission in High-Speed mode in data lanes 0 through 3
- Non-continuous high-speed transmission in clock and data lanes
- Pixel formats supported: RGB565 / RGB666 / loosely RGB666 / RGB888
- 128-entry command queue for command transmission
- 3 types of video modes: sync-event, sync-pulse, and burst modes
- Limited high-speed command transmission during video mode blanking period
- Ultra-low power mode control
- Low-Power Escape mode for low-speed asynchronous data communication
- Peripheral and external Tearing Effect (TE) signals detection
- Ability to receive peripheral TE signals via Bus Turnaround (BTA) procedure
- Limited reverse direction bandwidth (one-fourth of the forward direction) for half-duplex operation
- Link communication:
  - Token passing support for control of the direction
  - High-Speed signaling mode for fast-data traffic
  - Low-Power signaling mode for control purposes

The D-PHY TX core provides the following main features:

- Fractional-N PLL
- Spread Spectrum Clocking (SSC) control
- Lane and output pads control
- Lane swap for clock and data lanes

3.7.4.1 DSI Signal Descriptions

Table 3-34 presents DSI signal descriptions.

Table 3-34 DSI and LVDS Signal Descriptions

Signal Name	Type	Description	Ball Location
DSI_CKN	AIO	DSI0 negative clock lane / LVDSTX negative data lane2	Y3
DSI_CKP	AIO	DSI0 positive clock lane / LVDSTX positive data lane2	AA3
DSI_D0N	AIO	DSI0 negative data lane0 / LVDSTX negative data lane1	W4
DSI_D0P	AIO	DSI0 positive data lane0 / LVDSTX positive data lane1	W5
DSI_D1N	AIO	DSI0 negative data lane1 / LVDSTX negative clock data lane	AA2
DSI_D1P	AIO	DSI0 positive data lane1 / LVDSTX positive clock data lane	AB2
DSI_D2N	AIO	DSI0 negative data lane2 / LVDSTX negative data lane0	Y6
DSI_D2P	AIO	DSI0 positive data lane2 / LVDSTX positive data lane0	W6
DSI_D3N	AIO	DSI0 negative data lane3 / LVDSTX negative data lane3	AC2
DSI_D3P	AIO	DSI0 positive data lane3 / LVDSTX positive data lane3	AC3
DSI_TE	DI	DSI tearing effect control	AA5

Table 3-35 presents the DSI to LVDS interface signal mapping.

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Table 3-35 DSI to LVDS Signal Mapping

Ball Number	Ball Name	MIPI DSI	LVDS
W6	DSI_D2P	DSI_D2P	LVDS_A0P
Y6	DSI_D2N	DSI_D2N	LVDS_A0N
W5	DSI_D0P	DSI_D0P	LVDS_A1P
W4	DSI_D0N	DSI_D0N	LVDS_A1N
AA3	DSI_CKP	DSI_CKP	LVDS_A2P
Y3	DSI_CKN	DSI_CKN	LVDS_A2N
AB2	DSI_D1P	DSI_D1P	LVDS_ACKP
AA2	DSI_D1N	DSI_D1N	LVDS_ACKN
AC3	DSI_D3P	DSI_D3P	LVDS_A3P
AC2	DSI_D3N	DSI_D3N	LVDS_A3N

3.7.4.2 DSI Timing Characteristics

The DSI timing and electrical characteristics are compliant with MIPI DSI Specification v01-02-00 and MIPI D-PHY Specification v1-1.

3.7.5 Low Voltage Differential Signaling (LVDS)

The LVDS encoder is used to generate LVDS format data for Liquid Crystal Monitor (LCM). The LVDS encoder can encode RGB data into VESA or DISM formats, and then send it to the analog LVDS PHY core.

The LVDS encoder supports the following key features:

- Single-link interface with 4 data lanes
- Maximal resolution of 1366p × 768p
- VESA standard 8-bit and 6-bit
- DISM standard 8-bit
- Built-in test pattern
- Bit select for RGB
- Channel swap

3.7.5.1 LVDS Signal Descriptions

The LVDS signals are presented in Table 3-34.

3.7.5.2 LVDS Timing Characteristics

Table 3-36 and Figure 3-35 present timing characteristics for LVDS interfaces in the device.

Table 3-36 LVDS Timing Characteristics

No.	Parameter		Min	Max	Unit
LVDS01	t_c	Cycle time, CLK	13.33[1]		ns
LVDS02	t_w	Pulse duration, CLK	6.67		ns

1. For maximum operating clock frequency refer to Table 6-1.

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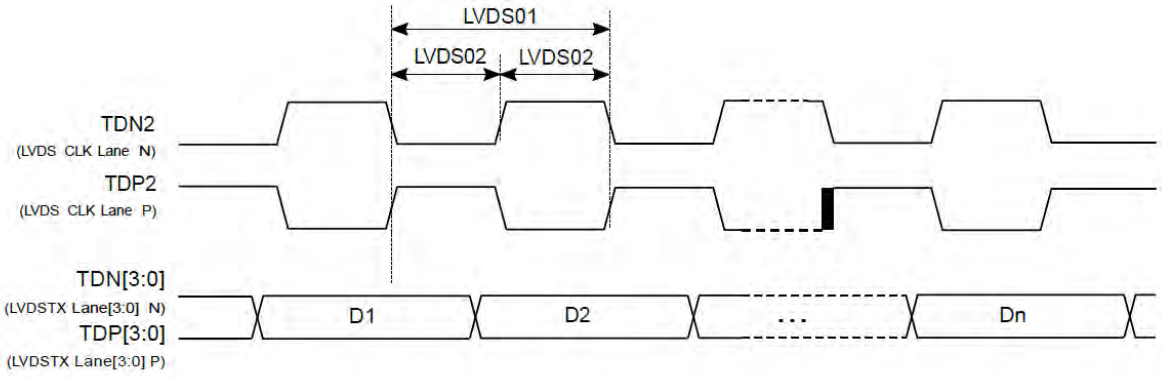

Figure 3-35 LVDS Timing Diagram

3.7.6 Display Pulse Width Modulation (DISP_PWM) and Reset

The DISP_PWM module provides a PWM signal for the LED driver of an LCM in order to reduce its backlight power consumption.

The DISP_PWM supports the following features:

- Gradual PWM control
- Operating clock: 26 MHz (default) or 104 MHz

Additionally, the device provides the LCM_RST signal that can be used to reset an external LCM.

Table 3-37 presents the DISP_PWM and reset signal descriptions.

Table 3-37 DISP_PWM and Reset Signal Descriptions

Signal Name	Type	Description	Ball Location
DISP_PWM	DO	Display PWM output	AB5
LCM_RST	DO	Display reset	AB4

3.8 Imaging

The imaging subsystem is built around a feature-rich Image Signal Processor (ISP) that processes data received from camera sensors through either MIPI CSI-2 or parallel camera interface, and ancillary engines for face detection and image warping.

3.8.1 Camera Image Signal Processor (ISP)

The ISP consists of timing generation unit, a lens and sensor compensation unit, and an image processing unit. The ISP works on image data received either from one of the camera interfaces or from system DRAM, and outputs the processed data back into DRAM.

Figure 3-36 shows the ISP internal block diagram.

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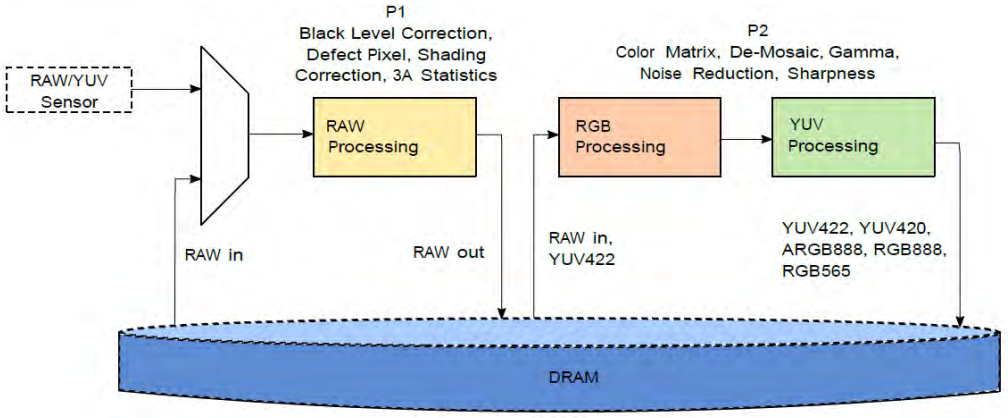

Figure 3-36 Image Signal Processor Block Diagram

The following list highlights the ISP features:

- Camera interfaces:
  - Primary camera: MIPI CSI-2 with 4 data lanes
  - Secondary camera: MIPI CSI-2 with 4 data lanes
  - Optional camera: 10-bit parallel interface
- Raw dump frame rate: 13MP at 30fps
- Lens and sensor compensation and image processing units:
  - Bad pixel correction/compensation
  - Lens shading correction/compensation
  - De-mosaic
  - Color clipping
  - Gamma correction
  - Edge enhancement
  - Noise reduction with large kernel
  - Preference color adaptation
  - 3A statistics and correction
  - Flicker detection
  - Digital image stabilization for video
  - High quality resizer engines with 90° and 180° image rotation

3.8.2 Face Detection (FD)

The device has an integrated FD 5.0 module, the main purpose of which is to detect a face on the source image and to output the detected coordinates of the face windows and landmarks into DRAM.

The FD supports the following key features:

- YUV to RGB format conversion
- Image down-scaling (maximum resize width of 400 pixels)
- Handling the convolutional neural network sequence
- YUV422 format:
  - 2 planes (Y/UV, Y/VU)
  - 1 plane (YUYV, YVYU, UYVY, VYUY)

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3.8.3 Warp Engine (WPE)

The WPE module offloads CPU and GPU loading on the Lens Distortion Compensation (LDC) feature. WPE is dedicated to real-time image warping. The engine has lower power consumption and a smaller silicon area compared with GPU. The WPE reads image data from DRAM and outputs image data to DRAM.

Table 3-38 shows the supported main features of the WPE module.

Table 3-38 WPE Main Features

Parameter	Description
Input/Output Color Format	YUV422 8-bit
Input/Output Color Range	Full (0-255)
Frame Rate	30fps
Input Max Size	3840p × 2160p
Output Max Size	3840p × 2160p
WarpMap Size	2 × 2 ~ 640p × 480p
Latency	33 ms (one frame delay)
Line Buffer Design	NA
Interpolation	WarpMap: Bi-linear interpolation Image: Bi-cubic filtering

3.8.4 Sensor Interface (SENINF)

The SENINF module supports data reception from either MIPI CSI-2 compliant camera sensor or parallel sensor. The SENINF includes two CSI controllers, CSI0 and CSI1, that are based on the MIPI Alliance specification and provide high-speed serial data transfer between the ISP and external camera modules. The data from camera modules can be transferred to different virtual channels of the ISP depending on the format of the data. There is a dedicated MIPI D-PHY physical layer for each CSI controller that is configurable to meet different throughput requirements of camera modules.

The SENINF engine supports the following features:

- Flexible configuration of the MIPI D-PHY physical layers providing support for one of the following options:
  - Four data lanes and one clock lane for CSI0 (primary camera) and CSI1 (secondary camera)
  - Two setups with two data lanes and one clock lane for CSI0 only (split mode)
- Throughput of up to 1.5 Gbps per lane
- Compliant with electrical characteristics of MIPI D-PHY Version 1.2
- Sensor clock (MCLK): 6/12/13/18/24/26/27/48/52 MHz
- Pixel formats: RAW8/RAW10/RAW12/RAW14
- Four Virtual Channels
- l Low Power (LP) command mode and Bus Turnaround are not supported

3.8.5 Camera Serial Interface (CSI)

The device features two MIPI CSI-2 modules (4-data lanes for primary and secondary cameras, respectively) that are fully compliant with MIPI CSI-2 specification. The MIPI D-PHY layer of each interface acts as a physical link between the CSI controllers and the image sensors.

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The D-PHY layer primarily feeds in the CSI data and clock lanes. The D-PHY layer provides high-speed clock as a primary clock to the CSI controller, which can achieve up to 1.5 Gbps throughput. Half-speed, 768-MHz clock is also supported.

The following functions of MIPI D-PHY layer are SW controllable:

- Bandgap control
- LDO core power and configuration
- Sigma-Delta Modulator (SDM) PLL configuration
- Spread-Spectrum Clocking
- Analog function related settings and status
- Output pads control and electronic features
- GPI pads control
- Software-control mode for each lane
- Lane swap for clock and data

3.8.5.1 CSI Signal Descriptions

Table 3-39 presents CSI signal descriptions.

Table 3-39 CSI Signal Descriptions

Signal Name	Type	Description	Ball Location
MIPI CSI0			
CSI0A_L0N	AIO	Channel input CSI0A lane0, negative	R3
CSI0A_L0P	AIO	Channel input CSI0A lane0, positive	R4
CSI0A_L1N	AIO	Channel input CSI0A lane1, negative	P4
CSI0A_L1P	AIO	Channel input CSI0A lane1, positive	P5
CSI0A_L2N	AIO	Channel input CSI0A lane2, negative	P6
CSI0A_L2P	AIO	Channel input CSI0A lane2, positive	P7
CSI0B_L0N	AIO	Channel input CSI0B lane0, negative	U1
CSI0B_L0P	AIO	Channel input CSI0B lane0, positive	T1
CSI0B_L1N	AIO	Channel input CSI0B lane1, negative	T2
CSI0B_L1P	AIO	Channel input CSI0B lane1, positive	R2
CSI0B_L2N	AIO	Channel input CSI0B lane2, negative	P2
CSI0B_L2P	AIO	Channel input CSI0B lane2, positive	P1
MIPI CSI1			
CSI1A_L0N	AIO	Channel input CSI1A lane0, negative	U5
CSI1A_L0P	AIO	Channel input CSI1A lane0, positive	U6
CSI1A_L1N	AIO	Channel input CSI1A lane1, negative	T3
CSI1A_L1P	AIO	Channel input CSI1A lane1, positive	T4
CSI1A_L2N	AIO	Channel input CSI1A lane2, negative	R6
CSI1A_L2P	AIO	Channel input CSI1A lane2, positive	R7
CSI1B_L0N	AIO	Channel input CSI1B lane0, negative	W1
CSI1B_L0P	AIO	Channel input CSI1B lane0, positive	W2
CSI1B_L1N	AIO	Channel input CSI1B lane1, negative	V2
CSI1B_L1P	AIO	Channel input CSI1B lane1, positive	U2

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3.8.6 Camera Parallel Interface (CPI)

The 10-bit CPI gives an optional (in addition to the CSI-2 receivers) uni-directional connection to the camera sensor for image data reception by the ISP. The connection is uni-directional. That is, all parallel signals are transmitted by the interface and received by the ISP.

The CPI has the following key features:

- Provides master clock for the image sensor
- Provides two types of synchronization when data is sampled at pixel clock:
  - Vertical synchronization
  - Horizontal line synchronization

3.8.6.1 CPI Signal Descriptions

Table 3-40 presents CPI signal descriptions.

Table 3-40 CPI Signal Descriptions

Signal Name	Type	Description	Ball Location
CPI Data Bus—CMDAT[6:0]			
CMDAT0	DI	Camera pixel data 0	AF1
CMDAT1	DI	Camera pixel data 1	AF2
CMDAT2	DI	Camera pixel data 2	AG2
CMDAT3	DI	Camera pixel data 3	AH2
CMDAT4	DI	Camera pixel data 4	AF3
CMDAT5	DI	Camera pixel data 5	AG3
CMDAT6	DI	Camera pixel data 6	AH3
CMDAT7	DI	Camera pixel data 7	AJ2
CMDAT8	DI	Camera pixel data 8	AH1
CMDAT9	DI	Camera pixel data 9	AJ3
CPI Clock and Sync Signals			
CMPCLK	DI	Camera pixel clock	AE3
CMVSYNC	DI	Camera vertical frame sync	AG4
CMHSYNC	DI	Camera horizontal frame sync	AF4
CMMCLK0	DO	CPI master clock	AD4, AE4
CMMCLK1	DO	CPI master clock	AE4, AD4

3.8.6.2 CPI Timing Characteristics

Table 3-41 and Figure 3-37 present timing characteristics for CPI in the device.

Table 3-41 CPI Timing Characteristics

No.	Parameter		Min	Max	Unit
CPI01	t_c	Cycle time, MCLK	10.4[(1)]		ns
CPI02	t_w	Pulse duration, MCLK	2		ns
CPI03	t_{su}	Setup time, input VSYNC valid before PCLK	2		ns
CPI04	t_h	Hold time, input VSYNC valid after PCLK	2		ns
CPI05	t_{su}	Setup time, input HSYNC valid before PCLK	2		ns

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No.	Parameter		Min	Max	Unit
CPI06	t_h	Hold time, input HSYNC valid after PCLK	2		ns
CPI07	t_{su}	Setup time, input DATA valid before PCLK	2		ns
CPI08	t_h	Hold time, input DATA valid after PCLK	2		ns

1. For maximum operating clock frequency refer to Table 6-1.

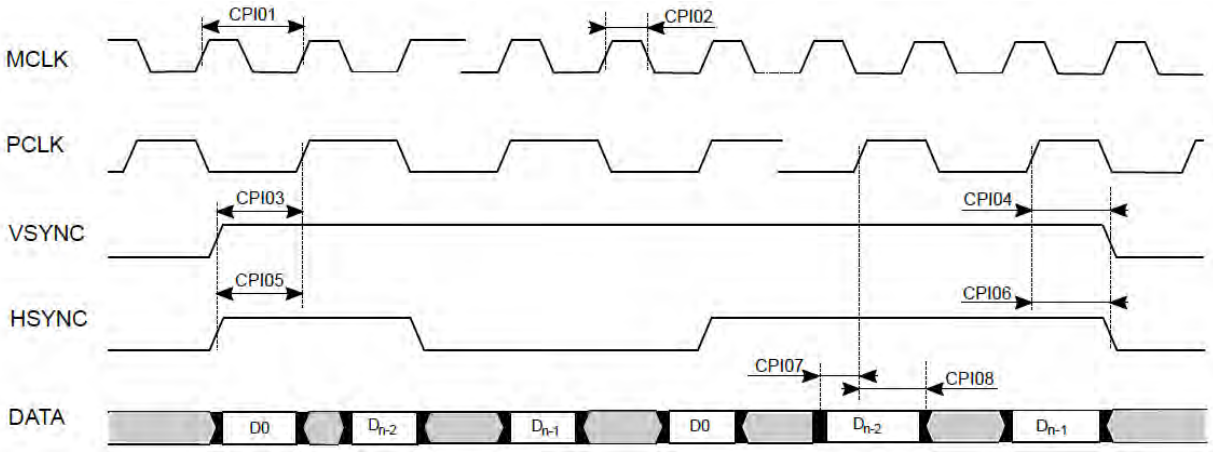

Figure 3-37 CPI Timing Diagram

3.9 Video

There are two video accelerators in the device—the Video Encoder (VENC) and the Video Decoder (VDEC).

3.9.1 Video Encoder (VENC)

The VENC accelerator supports main stream H.264 and HEVC video encoding. It is capable of encoding 1080p video at 60fps superior video quality. The VENC supports various encoding methods that satisfy basic requirements of easy software controllability. The VENC brings astonishing high quality and low memory bandwidth requirements, with advanced encoding technology. The accelerator also considers the usage of portable devices and provides several power saving capabilities.

The VENC has the following main features:

- Uses DRAM as an input, output, and working buffer
- Reads input frame buffers, executes video encoding and writes encoded bitstream to the output buffer
- Support of H.264 and HEVC encoding formats
- Support of YUV420 two plane scan line (NV12/NV21) and YUV420 three plane scan line (YV12/I420) color spaces

Table 3-42 shows the supported video formats and their capabilities.

Table 3-42 VENC Supported Formats

Format	Feature	Details
H.264 Encoding	Profile	Main profile
	Level	4.1
	Speed	1920p × 1088p @ 60fps
HEVC Encoding	Profile	Main profile
	Level	4.1
	Speed	1920p × 1088p @ 60fps

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3.9.2 JPEG Encoder

The device has a baseline JPEG Encoder, which supports 15 quantization methods that satisfy the basic requirement of video quality. The JPEG Encoder takes DRAM as input and output. It reads input frame buffers, executes JPEG encoding, and writes encoded bit stream to the output buffer.

The JPEG Encoder supports the following key features:

- Baseline JPEG encoding
- Color format: YUV420, YUV422
- Quantization level: 15
- Standard Huffman table
- Supports restart marker insertion
- Supports JFIF, EXIF, and JPEG format
- Full-frame encoding (non-stop)
- Support YUV420 two plane scan line (NV12/NV21)

3.9.3 Video Decoder (VDEC)

The VDEC accelerator provides multi-standard video decoding feature. The main purpose of the accelerator is to greatly relieve the CPU usage while providing high performance video. The input to VDEC is a compressed video bitstream. After decoding process, the reconstructed video is sent to thedisplay.

The VDEC supports various multimedia video formats, including:

- HEVC decoder:
  - Main profile 1080p @ 60fps (40 Mbps at L4)
- H.264 decoder:
  - Constrained Baseline profile @ 60fps (40 Mbps)
  - Main/High profile 1080p @ 60fps (40 Mbps)
- MPEG-4 decoder:
  - H.263 @ 60fps (40 Mbps)
  - SP/ASP 1080p @ 60fps (40 Mbps)
- MPEG-1/MPEG-2
- VP8
- VP9
- High Efficiency Image File Format (HEIF)
- Adaptive MPEG de-blocking filter
- Error handling

The VDEC supports Full HD at 60fps under the limitation of picture size > Full HD (it does not support picture width > 1960p or picture height > 1080p).

3.10 Audio

The device includes one audio subsystem providing audio data exchange features.

The audio subsystem includes the following key features:

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- Master or slave I2S input interface with FM radio Sampling Rate Converter (SRC)
- 2 × Master I2S outputs
- Master I2S input
- S/PDIF-input
- S/PDIF-output
- Master TDM TX
- Master TDM RX
- PCM master/slave interface
- 4 × PDM interfaces
- Audio Front-End

Figure 3-38 shows the Audio interfaces block diagram.

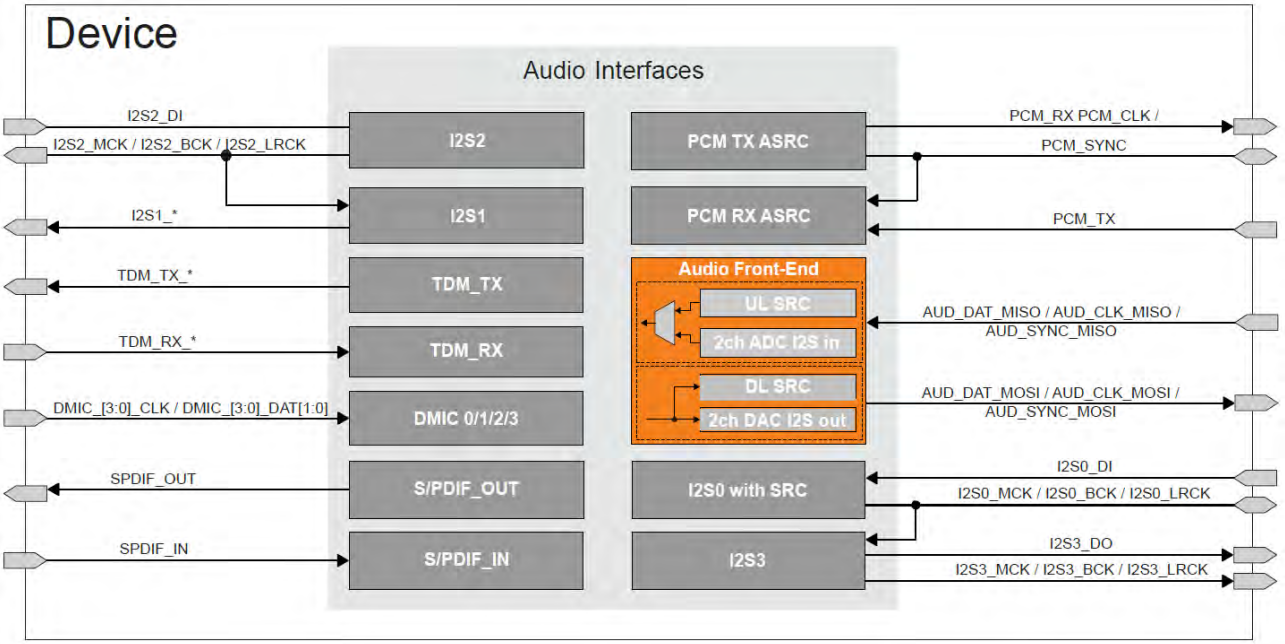

Figure 3-38 Audio Interfaces Block Diagram

3.10.1 Inter-IC Sound (I2S)

The device includes four I2S modules with the following key features:

- I2S0 with SRC supports master and slave input modes
- I2S1 and I2S3 support master output mode
- I2S2 supports master input mode
- Support of 16-, 24-bit stereo data
- Support of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz sampling rates in master mode
- Support of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, and 48 kHz sampling rates in slave mode
- Support of EIAJ and I2S protocol formats
- Support of I2S input/output with the same sampling rate at the same time
- Support of MCLK frequency range from 1.024 MHz to 49.152 MHz

3.10.1.1 I2S Signal Descriptions

Table 3-43 presents I2S signal descriptions.

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Table 3-43 I2S Signal Descriptions

Signal Name	Type	Description	Ball Location
I2S0			
I2S0_BCK	DIO	I2S0 master/slave serial bit clock	AJ19, AE3, AB13, AJ27
I2S0_DI	DI	I2S0 serial data input	AH18, AG2, AD14, AJ29
I2S0_LRCK	DIO	I2S0 word select	AG18, AF1, AB14, AJ28
I2S0_MCK	DO	I2S0 master clock	AJ18, AF22, AF2, AC14
I2S1			
I2S1_BCK	DO	I2S1 master serial bit clock	AF19, Y27, AJ27, AF30
I2S1_DO	DO	I2S1 serial data output	AG21, W26, AJ29, AH29
I2S1_LRCK	DO	I2S1 word select	AH19, AA26, AJ28, AF28
I2S1_MCK	DO	I2S1 master clock	AF18, AF23, Y26, AF29
I2S2			
I2S2_BCK	DO	I2S2 master serial bit clock	AE20, AA29, AJ27, AD29
I2S2_DI	DI	I2S2 serial data input	AG22, AB29, AJ29, AC29
I2S2_LRCK	DO	I2S2 word select	AE21, Y29, AJ28, AE30
I2S2_MCK	DO	I2S2 master clock	AF21, AE24, Y30, AE29
I2S3			
I2S3_BCK	DO	I2S3 master serial bit clock	AE17, AF3, AB13, AJ27, AF26
I2S3_DO	DO	I2S3 serial data output	AG17, AJ2, AC14, AJ29, AH25
I2S3_LRCK	DO	I2S3 word select	AE16, AG3, AB14, AJ28, AF27
I2S3_MCK	DO	I2S3 master clock	AF17, AE23, AH3, AD14, AJ25

1. I2S1 signals are internally muxed with TDM transmit. Refer to Table 3-47, TDM Signal Descriptions.

3.10.1.2 I2S Timing Characteristics

Table 3-44, Figure 3-39, and Figure 3-40 present timing characteristics for I2S modules in the device.

Table 3-44 I2S Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
	f_S	Sampling frequency	8		192	kHz
IIS01	f_{c_MCK}	Cycle time, MCK (master clock)	0.768		49.152	MHz
	f_{OP_BCK}	Operation frequency, BCK (serial clock)	32 × f_S		64 × f_S	MHz
IIS03	t_{c_BCK}	Cycle time, BCK (serial clock)	81		3906	ns
IIS04	$t_{w_BCK_H}$	Pulse duration, BCK high		0.5		$1/t_{c_BCK}$
IIS05	$t_{w_BCK_L}$	Pulse duration, BCK low		0.5		$1/t_{c_BCK}$
IIS06	$t_{d_BCK_LRCK}$	Delay time, output BCK low to LRCK valid			16	ns
IIS07	$t_{d_BCK_DO}$	Delay time, output BCK low to DO valid			16	ns
IIS08	t_{su}	Setup time, DI master mode	16			ns
IIS09	t_{su}	Setup time, DI slave mode	16			ns
IIS10	t_h	Hold time, DI master mode	16			ns
IIS11	t_h	Hold time, DI slave mode	16			ns

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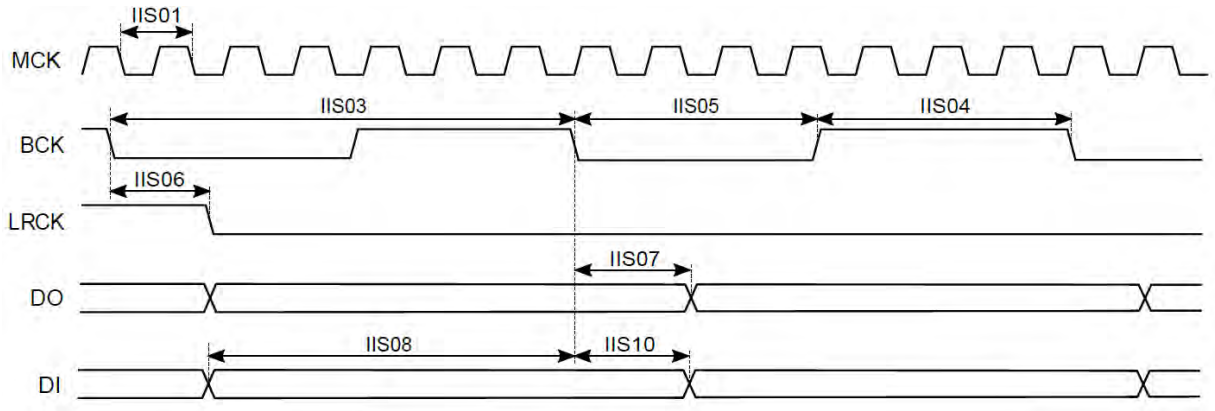

Figure 3-39 I2S Master Mode Timing Diagram

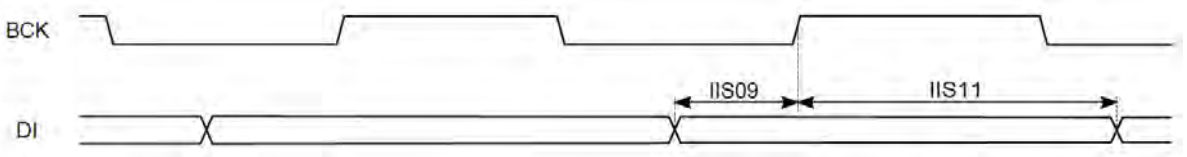

Figure 3-40 I2S Slave Mode Timing Diagram

3.10.2 Pulse Code Modulation (PCM)

The device includes one PCM interface with the following key features:

- Support of master/slave mode
- 4-pin interface for concurrently supporting I2S and PCM
- Support of 8, 16, 32, and 48 kHz sampling rates

3.10.2.1 PCM Signal Descriptions

Table 3-45 presents PCM signal descriptions.

Table 3-45 PCM Signal Descriptions

Signal Name	Type	Description	Ball Location
PCM_CLK	DIO	PCM clock	AH1, AB13
PCM_RX	DI	PCM data input	AF4, AD14
PCM_SYNC	DIO	PCM sync	AJ3, AB14
PCM_TX	DO	PCM data output	AG4, AC14

3.10.2.2 PCM Timing Characteristics

Table 3-46, Figure 3-41 and Figure 3-42 present timing characteristics for PCM interfaces in the device.

Table 3-46 PCM Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
	f_S	Sampling frequency	8		48	kHz
PCM1	f_{CLK}	Serial clock frequency	32 × f_S		64 × f_S	MHz
	t_{SYNC}	Sync period	32		64	$1/f_{BCK}$
PCM2	$t_{w_CLK_H}$	Pulse duration, CLK high		0.5		$1/f_{BCK}$
PCM3	$t_{w_CLK_L}$	Pulse duration, CLK low		0.5		$1/f_{BCK}$

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No.	Parameter		Min	Typ	Max	Unit
PCM4	$t_{d_CLK_SYNC}$	Delay time, output CLK low to SYNC valid			65	ns
PCM5	$t_{d_CLK_TX}$	Delay time, output CLK low to TX valid			65	ns
PCM6	t_{su}	Setup time, RX master mode	65			ns
PCM7	t_h	Hold time, RX master mode	65			ns
PCM8	t_{su}	Setup time, RX slave mode	65			ns
PCM9	t_h	Hold time, RX slave mode	65			ns

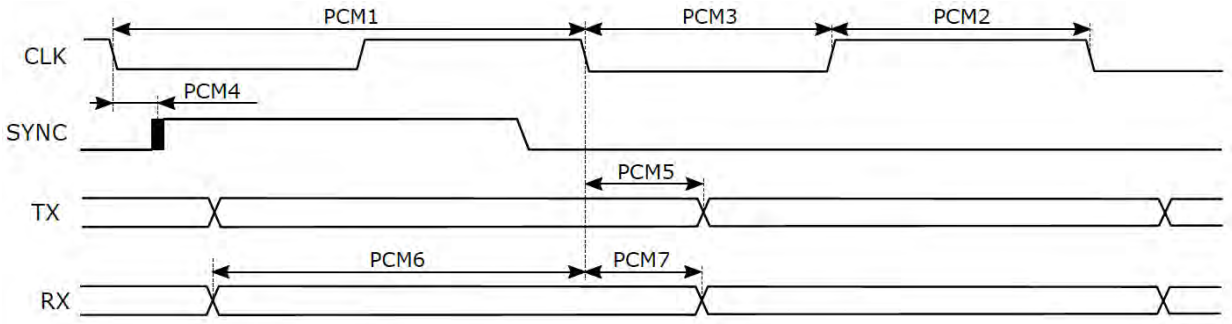

Figure 3-41 PCM Master Mode Timing Diagram

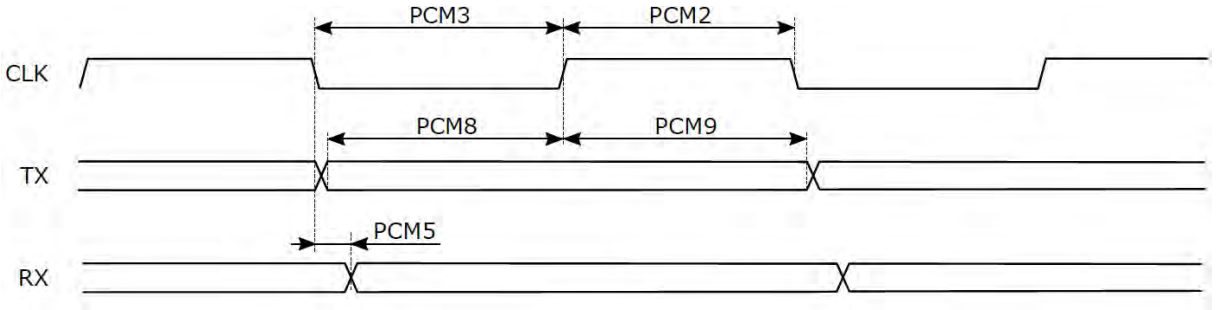

Figure 3-42 PCM Slave Mode Timing Diagram

3.10.3 Time Division Multiplexed (TDM) Interface

The TDM Interface is a digital multiplexing technique for combining several low-rate digital channels into a high-rate one. The device features one TDM RX and one TDM TX interfaces with independent clock signals.

The TDM TX includes the following key features:

- TDM I2S output (master mode only)
- 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, and 192 kHz sampling rates
- 2, 4, or 8 channels in 1, 2, or 4 data pins correspondingly
- Dedicated pins for TDM TX

The TDM RX includes the following key features:

- TDM I2S and EIAJ modes input
- 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, and 192 kHz sampling rates
- 2, 4, or 8 channels in 1 serial data pin
- Dedicated pin for TDM RX
- Channel width: 16 or 32 BCK cycles

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3.10.3.1 TDM Signal Descriptions

Table 3-47 presents TDM signal descriptions.

Table 3-47 TDM Signal Descriptions

Signal Name	Type	Description	Ball Location
TDM Transmit			
TDM_TX_BCK	DO	TDM clock	AC13, AF26
TDM_TX_DATA0	DO	TDM data0 output	AF14, AF25
TDM_TX_DATA1	DO	TDM data1 output	AF13, AG25
TDM_TX_DATA2	DO	TDM data2 output	AD13, AE25
TDM_TX_DATA3	DO	TDM data3 output	AF12, AF25
TDM_TX_LRCK	DO	TDM LRCK	AE13, AF27
TDM_TX_MCK	DO	TDM master clock	AE14, AJ25
TDM Receive			
TDM_RX_BCK	DO	TDM receive clock output	AE3, P27, AG29
TDM_RX_DI	DI	TDM receive data input	AG2, R28, AG27
TDM_RX_LRCK	DO	TDM receive frame sync output	AF1, P28, AH28
TDM_RX_MCK	DO	TDM receive master clock output	AF2, P29, AG28

1. TDM transmit signals are internally muxed with I2S1. Refer to Table 3-42, I2S Signal Descriptions.

3.10.3.2 TDM Timing Characteristics

Table 3-48 and Figure 3-43 present timing characteristics for TDM interfaces in the device.

Table 3-48 TDM Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
	f_S	Sampling frequency	8		192	kHz
TDM1	f_{MCK}	Master clock frequency	0.768		49.152	MHz
TDM2	f_{BCK}	Serial clock frequency	32 × f_S		256 × f_S	MHz
TDM3	$t_{w_BCK_H}$	Pulse duration, BCK high		0.5		1/f_{BCK}
TDM4	$t_{w_BCK_L}$	Pulse duration, BCK low		0.5		1/f_{BCK}
TDM5	$t_{d_BCLK_WS}$	Delay time, output BCLK low to WS valid			8	ns
TDM6	$t_{d_BCLK_SDOUT}$	Delay time, output BCLK low to SDOUT valid			8	ns
TDM7	t_{su_DI}	Setup time, DI	8			ns
TDM8	t_{h_DI}	Hold time, DI	8			ns

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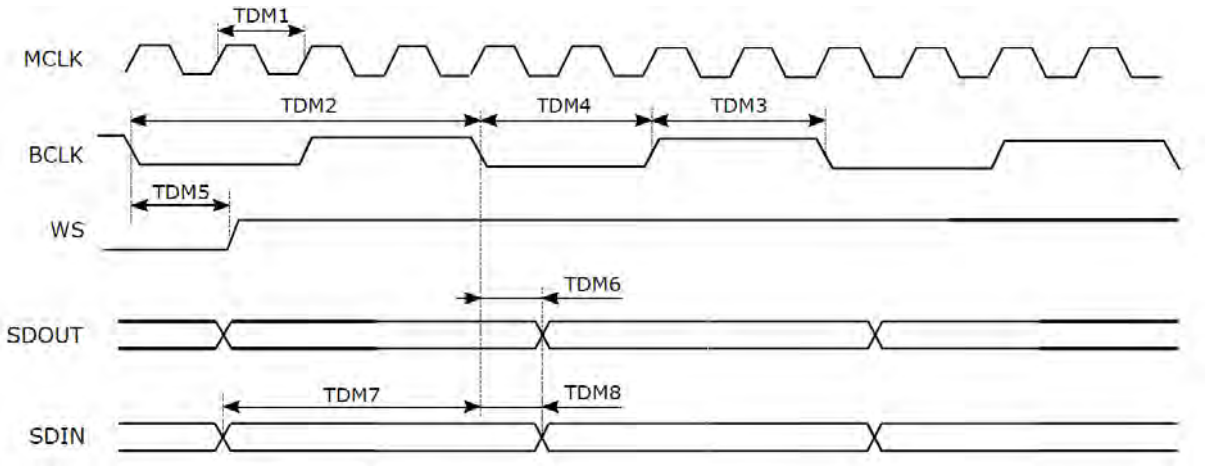

Figure 3-43 TDM Master Mode Timing Diagram

3.10.4 Digital Microphone (DMIC)

3.10.4.1 DMIC Signal Descriptions

Table 3-49 presents DMIC signal descriptions.

Table 3-49 DMIC Signal Descriptions

Signal Name	Type	Description	Ball Location
DMIC0_CLK	DO	DMIC0 PDM clock	AD29
DMIC0_DAT0	DI	DMIC0 PDM data0 input	AC29
DMIC0_DAT1	DI	DMIC0 PDM data1 input	AE30
DMIC1_CLK	DO	DMIC1 PDM clock	AE29
DMIC1_DAT0	DI	DMIC1 PDM data0 input	AF30
DMIC1_DAT1	DI	DMIC1 PDM data1 input	AF28
DMIC2_CLK	DO	DMIC2 PDM clock	AF29
DMIC2_DAT0	DI	DMIC2 PDM data0 input	AH29
DMIC2_DAT1	DI	DMIC2 PDM data1 input	AG29
DMIC3_CLK	DO	DMIC3 PDM clock	AH28
DMIC3_DAT0	DI	DMIC3 PDM data0 input	AG27
DMIC3_DAT1	DI	DMIC3 PDM data1 input	AG28

3.10.4.2 DMIC Filter Characteristics

Table 3-50 presents filter characteristics for DMIC interface in the device.

Table 3-50 DMIC Filter Characteristics

Parameter		Min	Typ	Max	Unit
f_{OP}	Operating frequency		3.25		MHz
			1.625		
			0.8125		
			0.40625		
D	Duty cycle, CLK	40		60	%
t_{RISE}	Rise time, CLK (Max C_L = 80 pF)		10		ns
t_{FALL}	Fall time, CLK (Max C_L = 80 pF)		10		ns

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Parameter		Min	Typ	Max	Unit
f_S	Sampling rate	8		48	kHz

3.10.5 Pulse Density Modulation (PDM)

The PDM module includes the following key features:

- Supports one or two wire modes
- Supports sampling rates of 8, 16, 32, 48 KHz

3.10.5.1 PDM Timing Characteristics

Table 3-51 and Figure 3-44 present timing characteristics for PDM interface in the device.

Table 3-51 PDM Timing Characteristics

No.	Parameter	Description	Min	Typ	Max	Unit
PDM1	f_{OP}	Operating frequency, PDM CLK	0.40625	-	3.25	MHz
PDM2	$t_{W_CLK_H}$	Pulse duration, CLK high	-	0.5	-	1 / f_{CLK}
PDM3	$t_{W_CLK_L}$	Pulse duration, CLK low	-	0.5	-	1 / f_{CLK}
PDM4	t_{SU_DAT}	Setup time, DAT	20	-	-	ns
PDM5	t_{H_DAT}	Hold time, DAT	20	-	-	ns

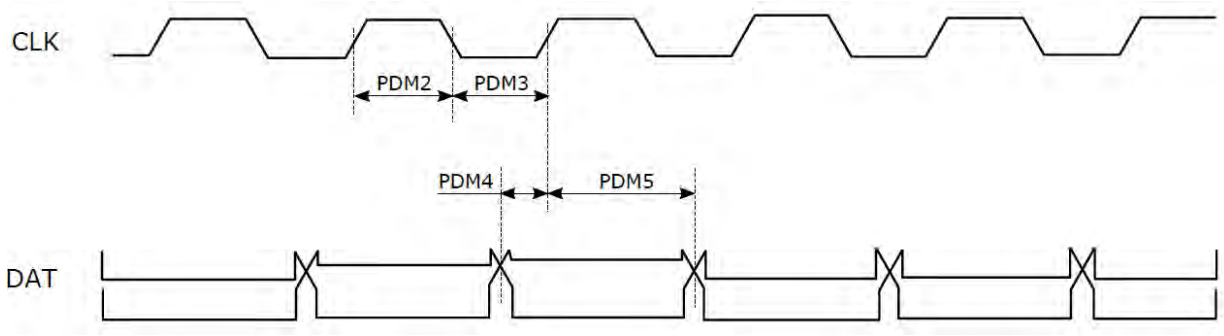

Figure 3-44 PDM Timing Diagram

3.10.6 Sony/Philips Digital Interface (S/PDIF)

The device includes one S/PDIF input and one S/PDIF output, which provide serial and uni-directional transmission of digital audio through a single transmission line.

The S/PDIF-In main features are:

- Support of S/PDIF input decode
- Support of 32, 44.1, 48, 88.2, 96, 176, 192 kHz sampling rates

The S/PDIF-Out main features are:

- Support of S/PDIF output encode
- Support of 32, 44.1, 48, 88.2, 96, 176, 192 kHz sampling rates

3.10.6.1 S/PDIF Signal Descriptions

Table 3-52 presents S/PDIF signal descriptions.

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Table 3-52 S/PDIF Signal Descriptions

Signal Name	Type	Description	Ball Location
SPDIF_IN	DI	S/PDIF decoder input	AE16, L2, AB13, AJ29
SPDIF_OUT	DO	S/PDIF encoder output	AF17, M4, AB14, AJ28

3.10.7 Audio Front-End (AFE)

The AFE system provides Audio Uplink (UL) and Downlink (DL) paths.

The Audio UL path includes the following key features:

- Programmable Gain Amplifier (PGA)
- Stereo Audio ADC
- Accessory Detector (ACCDET) with two types of external accessories support—microphone and hook-switch.

The Audio DL path includes the following key features:

- Stereo audio DAC

3.10.7.1 PMIC Signal Descriptions

Table 3-53 presents PMIC signal descriptions.

Table 3-53 PMIC Signal Descriptions

Signal Name	Type	Description	Ball Location
AUD_CLK_MISO	DI	PMIC audio interface clock master input / slave output	Y26, Y30
AUD_CLK_MOSI(1)	DO	PMIC audio interface clock master output / slave input	Y26, Y30
AUD_DAT_MISO0	DI	PMIC audio interface data master input / slave output	AA26, Y29
AUD_DAT_MISO1	DI	PMIC audio interface data master input / slave output	W26, AB29
AUD_DAT_MOSI0(1)	DO	PMIC audio interface data master output / slave input	AA26, Y29
AUD_DAT_MOSI1(1)	DO	PMIC audio interface data master output / slave input	W26, AB29
AUD_SYNC_MISO	DI	PMIC audio interface sync master input / slave output	Y27, AA29
AUD_SYNC_MOSI(1)	DO	PMIC audio interface sync master output / slave input	Y27, AA29

1. These pins should be connected to GND through an external pull resistor when unused.

3.10.7.2 ADC Characteristics

Table 3-54 presents ADC characteristics.

Table 3-54 ADC Characteristics

Parameter		Min	Typ	Max	Unit
N	Resolution		12		Bit
f_S	Sampling rate at N-bit		4/(N+4)		MSPS
IN_{SW}	Input swing	0		1.5	V
C_{IN}	Input capacitance unselected channel		50		fF
	Input capacitance selected channel		4		pF
R_{IN}	Input resistance unselected channel	400			MΩ
$F_{cycle_latency}$	Cycle latency		N+4		$1/f_{OP}$
INL	Integral Non-Linearity		+2.0/-2.0		LSB

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Parameter		Min	Typ	Max	Unit
DNL	Differential Non-Linearity		+1.0/-1.0		LSB
SNR+D	Signal to noise and distortion ratio (1 kHz full swing input and 1.0833 MHz clock rate)	60	67		dB
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD	Analog power supply	1.7	1.8	1.9	V

3.11 Connectivity

3.11.1 Inter-Integrated Circuit (I2C)

The device contains four I2C controllers, which provide interface between internal hosts and any I^{2}C™ bus compatible devices. Each can be configured to work as a master or slave I^{2}C-compatible device.

Each I2C module supports the following key features:

- Compliant with Philips I2C-bus specification version 2.1
- Standard (LS) communication mode (up to 100 Kbps)
- Fast-Speed (FS) communication mode (up to 400 Kbps)
- Fast-Speed plus (FS+) communication mode (1 Mbps)
- 7-bit I2C addressing mode
- START/STOP/REPEATED START conditions
- Clock stretching (synchronization) mode
- Adjustable clock speed for FS+ mode operation
- I2C compliant master mode operation
- Manual transfer mode with built-in 16-byte FIFO
- Multi-write per transfer
- Multi-read per transfer
- Multi-transfer per transaction
- Combined format transfer with length change capability
- DMA transfer mode

3.11.1.1 I2C Signal Descriptions

Table 3-55 presents I2C signal descriptions.

Table 3-55 I2C Signal Descriptions

Signal Name	Type	Description	Ball Location
I2C0[(1)]			
SCL0_0	DIO	I2C0 serial clock (input/output)	AH26
SDA0_0	DIO	I2C0 serial data (input/output)	AH27
I2C1[(1)]			
SCL1_0	DIO	I2C1 serial clock (input/output)	AH24
SDA1_0	DIO	I2C1 serial data (input/output)	AJ24
I2C2[(1)]			
SCL2_0	DIO	I2C2 serial clock (input/output)	AH4
SDA2_0	DIO	I2C2 serial data (input/output)	AJ4

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Signal Name	Type	Description	Ball Location
I2C3[1]			
SCL3_0	DIO	I2C3 serial clock (input/output)	AC5
SDA3_0	DIO	I2C3 serial data (input/output)	AD5

1. The internal pull-up resistance after reset for all I2C* pins is set to 75 kΩ by default. It is software programmable and can be adjusted to 1 kΩ, 5 kΩ, 15 kΩ, or no pull-up.

3.11.1.2 I2C Timing Characteristics

Table 3-56 and Figure 3-45 present timing characteristics for I2C interfaces in the device.

Table 3-56 I2C Timing Characteristics

No.	Parameter		LS		FS		FS+		Unit
			Min	Max	Min	Max	Min	Max	
IIC1	t_c	Cycle time		10000		2500		1000	ns
IIC2	$t_{w\ high}$	Pulse duration, SCL high	4.0		0.6		0.26		µs
IIC3	$t_{w\ low}$	Pulse duration, SCL low	4.7		1.3		0.5		µs
IIC4	t_{RISE}	Rise time of SDA and SCL signals		1000	20	300		120	ns
IIC5	t_{FALL}	Fall time of SDA and SCL signals		300	20 × (VDD/5.5V)	300	20 × (VDD/5.5V)	120	ns
IIC6	t_{su}	Setup time, SDA to SCL	250		100		50		ns
IIC7	t_h	Hold time, SDA to SCL	0		0		0		ns
IIC8	$t_{su\ start}$	Setup time, SCL to start condition	4.7		0.6		0.26		µs
IIC9	$t_{h\ start}$	Hold time, start condition to SCL	4.0		0.6		0.26		µs
IIC10	$t_{h\ stop}$	Setup time, SCL to stop condition	4.0		0.6		0.26		ns
IIC11	$t_{(BUF)}$	Bus free time between stop and start condition	4.7		1.3		0.5		ns
IIC12	t_{DV}	Data valid time		3.45		0.9		0.45	µs
IIC13	t_{DV_ACK}	Data valid acknowledge time		3.45		0.9		0.45	µs
	C_b	Capacitive load for each bus line		400		400		550	pF

NOTE: The maximum allowable bus capacitance may vary from Cb value depending on the actual operating voltage and frequency of the application.

NOTE: I2C t_{RISE} and t_{FALL} transition timing parameters are referenced correspondingly to 70% and 30% of the signal logical level.

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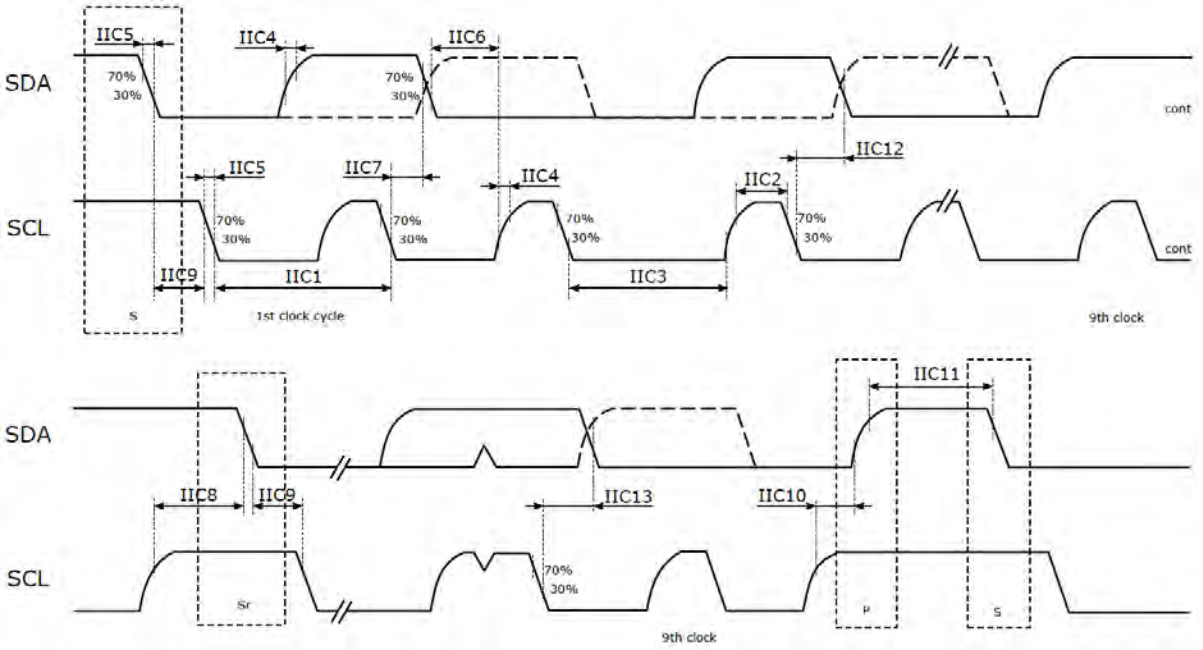

Figure 3-45 I2C Timing Diagram

3.11.2 Universal Asynchronous Receiver/Transmitter (UART)

The device supports three UART modules, which provide full-duplex serial communication with external devices. UART1 and UART2 are 4-pin channels (TX, RX, CTS, RTS) while UART0 and DSP_UART are 2-pin channels (TX, RX).

Each UART module supports the following key features:

- 16C450-compatible
- 16C550A-compatible
- Fully programmable by an 8-bit CPU interface
- Configurable data formats:
  - 5, 6, 7, or 8 data bits
  - Optional parity bit
  - 1 or 2 stop bits
- Internal 16-bit programmable baud rate generator
- 8-bit scratch register
- Separate transmit and receive FIFOs
- Baud rates from 110 bps up to 961,200 bps
- Baud rate auto detection function
- Two modem control lines
- Two DMA handshake lines
- Internal diagnostic capabilities with loopback
- Polling, DMA and interrupt modes of operation
- Hardware flow control (RTS/CTS)

3.11.2.1 UART Signal Descriptions

Table 3-57 presents UART signal descriptions.

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Table 3-57 UART Signal Descriptions

Signal Name	Type	Description	Ball Location
UART0			
URXD0	DI	UART0 receive data	AH22, AH23
UTXD0	DO	UART0 transmit data	AH22, AH23
UART1			
UCTS1	DI	UART1 clear to send (active low)	AE17, AE24
URTS1	DO	UART1 request to send (active low)	AE16, AE23
URXD1	DI	UART1 receive data	AF22, AF23, AC13
UTXD1	DO	UART1 transmit data	AF22, AF23, AE13
UART2			
UCTS2	DI	UART2 clear to send (active low)	AF17, AF22
URTS2	DO	UART2 request to send (active low)	AG17, AF23
URXD2	DI	UART2 receive data	AE24, AE23, AF13
UTXD2	DO	UART2 transmit data	AE24, AE23, AF14

3.11.3 Infrared Receiver (IRRX)

The device has one IRRX module, which serves as a receiver for Infrared (IR) assistive applications.

The IRRX module supports the following key features:

- Decoding of various IR transmission protocols divided into two groups:
  - Pulse width coding (NEC)
  - Bi-phase coding (RC5, RC6, and RC-MM)
- Decoding the signal by the length of pulse width
- Decoding the signal by a constant period sampling pulse

3.11.3.1 IRRX Signal Descriptions

Table 3-58 presents IRRX signal descriptions.

Table 3-58 IRRX Signal Descriptions

Signal Name	Type	Description	Ball Location
IRRX	DI	Infrared receiver module input	AG17, M5, AD14, AJ27

3.11.4 Serial Peripheral Interface (SPI)

The SPI is a four-pin synchronous serial interface used for short-distance communication, primarily in embedded systems. The device features one SPI master controller.

The SPI supports the following key features:

- Two configurable transmit modes:
  - TX DMA mode—the SPI controller automatically fetches the transmitted data (to be put on the MOSI line) from memory
  - TX FIFO mode—the data to be transmitted on the MOSI line is written to FIFO before the start of the transaction.
- Two configurable receive modes:

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  - RX DMA mode—the SPI controller automatically stores the received data (from MISO line) to memory.
  - RX FIFO mode—the received data is kept in RX FIFO of the SPI controller. The processor must read back the data by itself.
- Configurable chip-select setup time, hold time and idle time
- Programmable serial clock (SCK) high time and low time
- Configurable transmit and receive bit order
- Adjustable endian order from/to memory system
- Programmable byte length for transmission
- Unlimited length for transmission using dedicated pause mode
- Configurable option to control chip-select de-assertion between byte transfers
- Supports all clock polarity and phase modes

3.11.4.1 SPI Signal Descriptions

Table 3-59 presents SPI signal descriptions.

Table 3-59 SPI Signal Descriptions

Signal Name	Type	Description	Ball Location
SPI_CLK	DO	SPI serial clock	AJ19, AF6
SPI_CSB	DO	SPI chip select	AG18, AE5
SPI_MI	DI	SPI master input / slave output	AJ18, AE6, AG5
SPI_MO	DO	SPI master output / slave input	AH18, AE6, AG5

3.11.4.2 SPI Timing Characteristics

Table 3-60 and Figure 3-46 present timing characteristics for SPI in the device.

Table 3-60 SPI Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
SPI01	f_{OP_MCK}	SPI HW module clock frequency (MCK)—chip internal clock		104		MHz
SPI02	t_c	Cycle time, SPI_CLK	19.1[(1)]			ns
SPI03	t_{RISE_SCK}	Rise time, SPI_CLK			1.2	ns
SPI04	t_{FALL_SCK}	Fall time, SPI_CLK			1.6	ns
SPI05	$t_{w_CLK_L}$	Pulse duration, SPI_CLK low	8.2			ns
SPI06	$t_{w_CLK_H}$	Pulse duration, SPI_CLK high	8.1			ns
SPI07	t_{su_cs}	Setup time, SPI_CSB—register adjustable			2.5	ns
SPI08	t_{h_cs}	Hold time, SPI_CSB—register adjustable			2.5	ns
SPI09	t_{su_MOSI}	Setup time, SPI_MO to SPI_CLK	9.5			ns
SPI10	t_{h_MOSI}	Hold time, SPI_MO to SPI_CLK	8.5			ns

1. For maximum operating clock frequency refer to Table 6-1.

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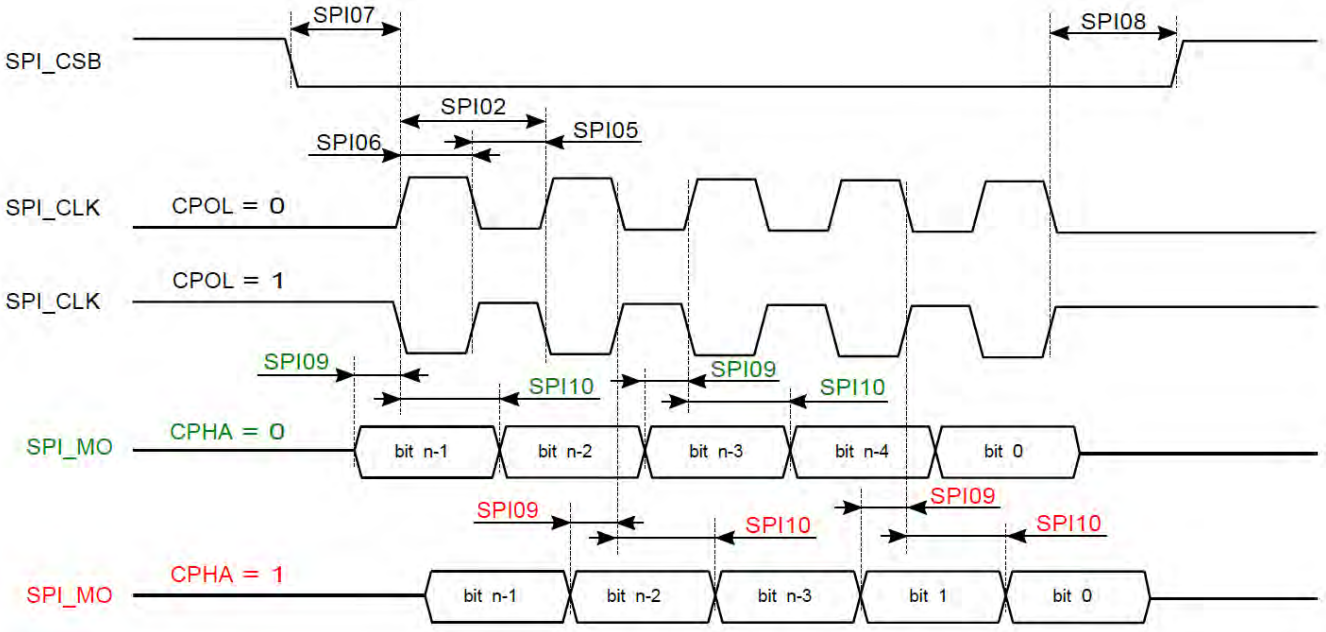

Figure 3-46 SPI Master Timing Diagram

3.11.5 Universal Serial Bus (USB)

The device features two USB2.0 controllers with integrated PHY—one USB (USB0) On-The-Go (OTG) and one USB as host only (USB1).

The USB controllers support the following key features:

- Capability to operate in Host or Device (Peripheral) mode
- Host mode features:
  - High-Speed, Full-Speed, or Low-Speed operation, USB2.0
  - Full-Speed or Low-Speed operation, USB1.1
  - xHCI specification implemented host controller
  - Compatible with connection to USB2.0 hub
  - Support of up to 15 devices
  - Support of up to 64 endpoints
  - Support of smart scheduling algorithm
- Device (Peripheral) mode features:
  - High-Speed or Full-Speed operation
  - Support of up to 8 transmit and 8 receive endpoints
  - 8KB on-chip data RAM for endpoint FIFOs
  - Configurable number of packet slots (up to 4) for each endpoint separately
  - Configurable FIFOs size allocation for each endpoint separately
  - Configurable transfer type to Bulk/Interrupt/Isochronous for each endpoint
  - Embedded queue management function with scatter/gather DMA capability
- 16-bit, 30-MHz UTMI+ level 2 transceiver interface to embedded USB2.0 PHY
- Lower Power Management (LPM) with local and remote wake-up capability
- Point-to-point communication with High-Speed/Full-Speed OTG host/peripheral (compliant with OTG Supplement Version 2.0)
- Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)

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3.11.5.1 USB Signal Descriptions

Table 3-61 presents USB signal descriptions.

Table 3-61 USB Signal Descriptions

Signal Name	Type	Description	Ball Location
CHD_DM_P0	AIO	BC1.1 charger mode detection D- differential data line	R26
CHD_DP_P0	AIO	BC1.1 charger mode detection D+ differential data line	R25
IDDIG	DI	USB OTG ID	AH16, AB24, AE24
USB_DM_P0	AIO	USB port0 D- differential data line	T29
USB_DM_P1	AIO	USB port1 D- differential data line	T25
USB_DP_P0	AIO	USB port0 D+ differential data line	T30
USB_DP_P1	AIO	USB port1 D+ differential data line	T26
USB_DRVVBUS	DO	USB VBUS enable output	AH17, AC24, AE23
USB_VBUS_P0	AI	Power for connected device	V30

3.11.6 Ethernet Network Interface Controller (EMAC)

The device features one 10/100 Mbps EMAC compliant with 802.3 Standard. The EMAC supports the following key features:

- Dynamically configurable to support 10/100 Mbps with MII/RMII
- Energy Efficient Ethernet (EEE) MII signaling according to the IEEE802.3az Specification
- Flow control for half-duplex and full-duplex modes
- 32-bit CRC with optional Frame Check Sequence (FCS) field forwarding to the user application
- 32-bit CRC generation and append on transmit or forwarding of user application provided FCS
- Operational Ethernet Pause Frame generation from FIFO congestion thresholds
- Transmit and receive VLAN tagged frames according to IEEE 802.1q Specification
- Transmit and receive IPv4/UDP/TCP checksum offload
- Clause 22 and Clause 45 MDIO master interface for PHY configuration and management
- Optional MAC address comparison on receive and overwrite on transmit with programmable promiscuous mode operation
- Optional multicast address filtering with 512-bin hash code lookup table on receive
- Optional Ethernet Pause Frame (802.3 Annex 31A) termination providing fully automated flow control without any user application overhead
- Optional Magic Packet detection

3.11.6.1 EMAC Signal Descriptions

Table 3-62 presents EMAC signal descriptions.

Table 3-62 EMAC Signal Descriptions

Signal Name	Type	Description	Ball Location
EMAC Receive Data Bus—EXT_RXD[3:0]			
EXT_RXD0	DI	Receive data 0	AJ19
EXT_RXD1	DI	Receive data 1	AG18
EXT_RXD2	DI	Receive data 2	AJ18

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Signal Name	Type	Description	Ball Location
EXT_RXD3	DI	Receive data 3	AH18
EMAC Transmit Data Bus—EXT_TXD[3:0]			
EXT_TXD0	DO	Transmit data 0	AE20
EXT_TXD1	DO	Transmit data 1	AE21
EXT_TXD2	DO	Transmit data 2	AF21
EXT_TXD3	DO	Transmit data 3	AG22
EMAC Command, Status and Clock Signals			
EXT_TXEN	DO	Transmit enable	AE17
EXT_RXDV	DI	Receive data valid	AG21
EXT_RXER	DI	Receive error	AH19
EXT_TXC	DI	Transmit clock	AF19
EXT_COL	DIO	Collision detect	AE16
EXT_FRAME_SYNC	DI	Frame synchronization	AG17, AJ16, AB24, AF12
EXT_RXC	DI	Receive clock	AF18
EMAC Management Bus			
EXT_MDC	DO	Management data clock	AG17
EXT_MDIO	DIO	Management data	AF17

3.11.6.2 EMAC Timing Characteristics

Table 3-63 and Figure 3-47 present timing characteristics for EMAC MII in the device.

Table 3-63 EMAC MII Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
MII1	$t_{c_TXC_RXC}$	Cycle time, TXC/RXC		40		ns
MII2	t_{d_TX}	Delay time, TX			18	ns
MII7	t_{su_RX}	Setup time, RX	2			ns
MII8	t_{h_RX}	Hold time, RX	2			ns
MII9	D	Duty cycle, TXC/RXC	40	50	60	%
II10	t_{RISE}	Rise time, TXC/RXC (20% ~ 80%)			0.75	ns
MII11	t_{FALL}	Fall time, TXC/RXC (20% ~ 80%)			0.75	ns

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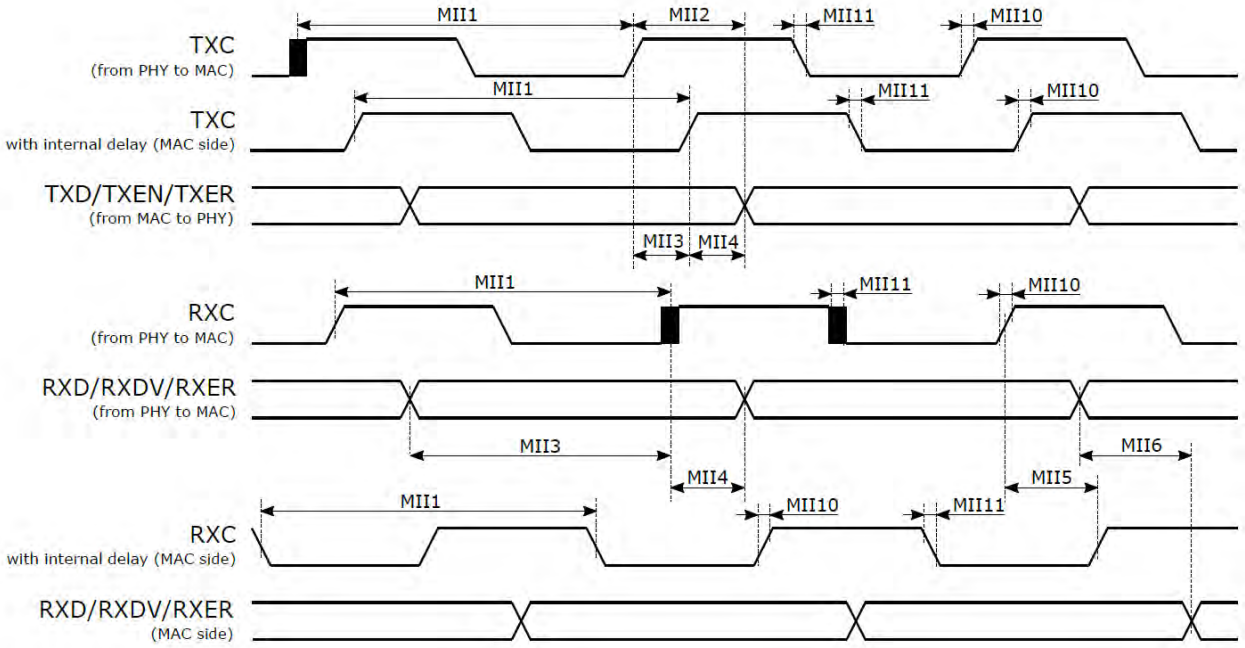

Figure 3-47 EMAC MII Timing Diagram

Table 3-64 and Figure 3-48 present timing characteristics for EMAC RMII in the device.

Table 3-64 EMAC RMII Timing Characteristics

No.	Parameter		Min	Typ	Max	Unit
RMII1	t_{c_REFCLK}	Cycle time, REFCLK		20		ns
RMII2	t_{d_TX}	Delay time, TX			18	ns
RMII7	t_{su_RX}	Setup time, RX	2			ns
RMII8	t_{h_RX}	Hold time, RX	2			ns
RMII9	D	Duty cycle, REFCLK	45	50	55	%
RMII10	t_{RISE}	Rise time, REFCLK (20%~80%)			0.75	ns
RMII11	t_{FALL}	Fall time, REFCLK (20%~80%)			0.75	ns

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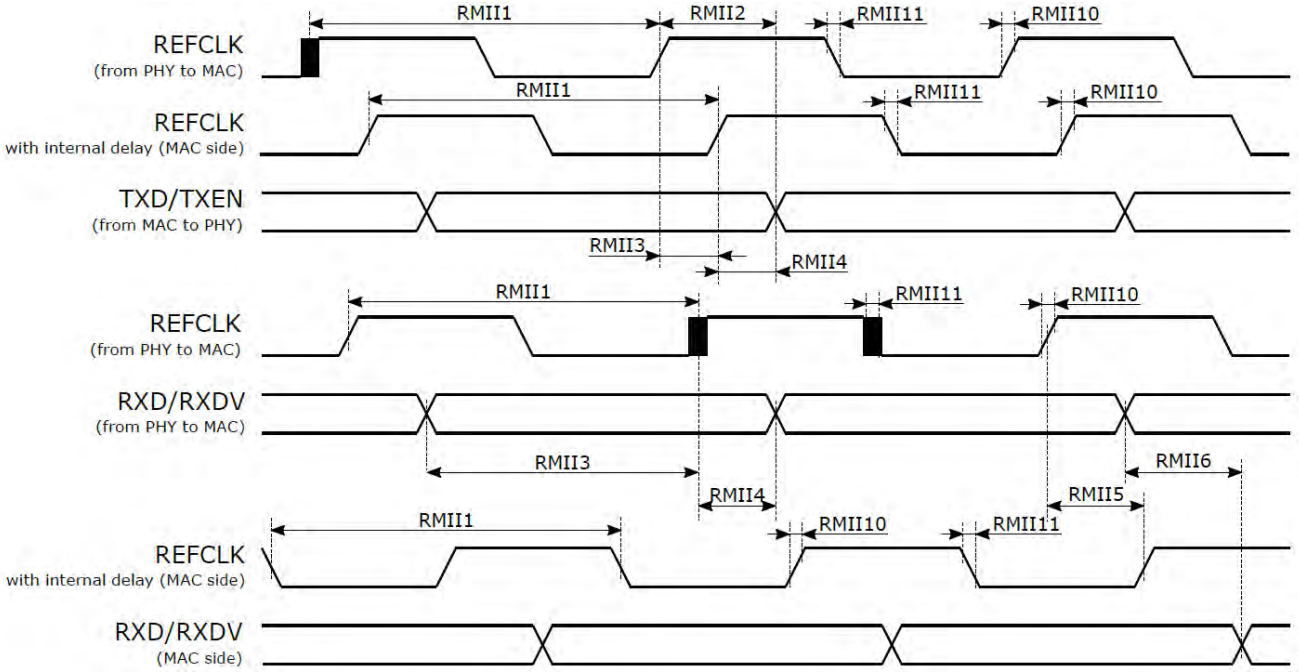

Figure 3-48 EMAC RMII Timing Diagram

3.11.7 KeyPad Scanner (KeyPad)

The KeyPad module implements scanning algorithm for hardware-based key-press decoding and reduces overhead to the CPU.

The KeyPad supports the following key features:

- Two types of keyboards:
  - 2 × 2 single keys
  - 2 × 2 configurable double keys
- Double KeyPad supports 8 keys matrix divided into four subgroups of 2 keys and a 20 Ω resistor
- Key detection block providing key pressed, key released and de-bounce mechanisms
- Interrupt event detection of key press and key release
- Detection of one or two keys pressed simultaneously with any combination

3.11.7.1 KeyPad Signal Descriptions

Table 3-65 presents KeyPad signal descriptions.

Table 3-65 KeyPad Signal Descriptions

Signal Name	Type	Description	Ball Location
KPCOL0	DIO	KeyPad column 0	AA24
KPCOL1	DIO	KeyPad column 1	AC24
KPROW0	DIO	KeyPad row 0	AD24
KPROW1	DIO	KeyPad row 1	AB24

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3.11.7.2 KeyPad Applications

The 2 × 2 double KeyPad supports a 2 × 2 × 2 = 8 keys matrix. The eight keys are divided into four subgroups, and each group consists of 2 keys and a 20 Ω resistor.

NOTE: KeyPad does not support detection of simultaneously pressed keys on the same column and row.

Figure 3-49 represents 2 × 2 double KeyPad matrix (8 keys) example configuration.

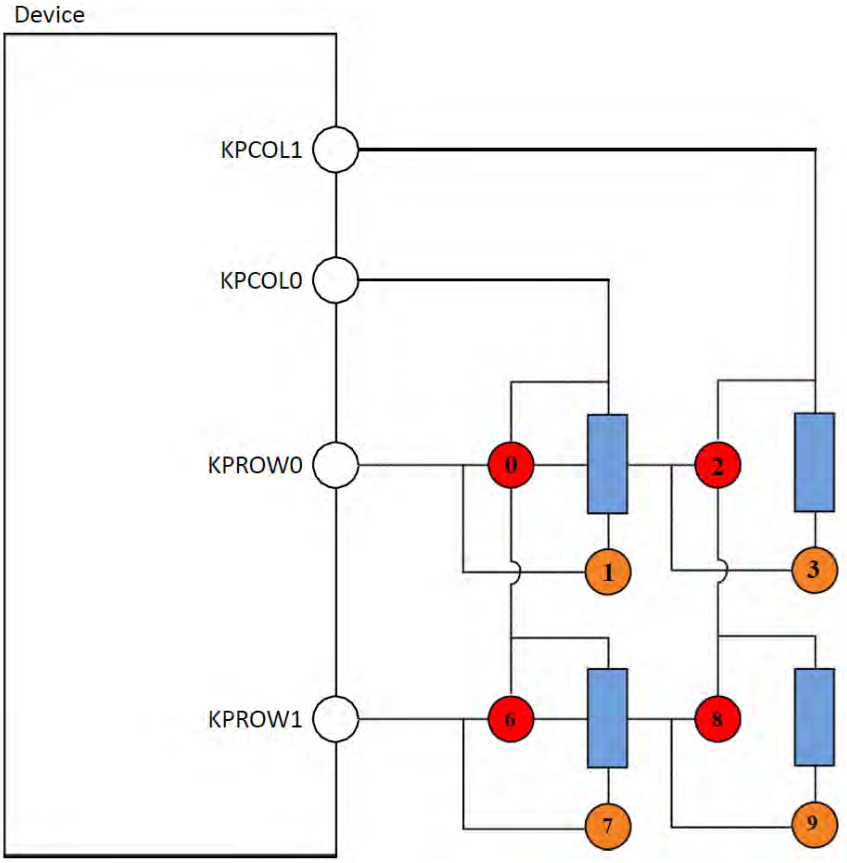

Figure 3-49 2 × 2 KeyPad Matrix (8 Keys)

3.11.8 General Purpose I/O (GPIO)

The GPIO peripheral provides 145 dedicated GPIO pins that are multiplexed with other functions to reduce the pin count.

Each GPIO pin has the following key functions:

- Configurable direction: input or output
- Control of the state driven on the output pin when GPIO is configured as an output
- Detection of the state of the pin when GPIO is configured as an input
- Configurable interrupt event generation

3.11.8.1 GPIO Signal Descriptions

Table 3-66 presents GPIO signal descriptions.

Table 3-66 GPIO Signal Descriptions

Signal Name	Type	Description	Ball Location
GPIO0	DIO	General purpose input and output	AE20
GPIO1	DIO	General purpose input and output	AE21

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Signal Name	Type	Description	Ball Location
GPIO2	DIO	General purpose input and output	AF21
GPIO3	DIO	General purpose input and output	AG22
GPIO4	DIO	General purpose input and output	AF19
GPIO5	DIO	General purpose input and output	AH19
GPIO6	DIO	General purpose input and output	AF18
GPIO7	DIO	General purpose input and output	AG21
GPIO8	DIO	General purpose input and output	AJ19
GPIO9	DIO	General purpose input and output	AG18
GPIO10	DIO	General purpose input and output	AJ18
GPIO11	DIO	General purpose input and output	AH18
GPIO12	DIO	General purpose input and output	AE17
GPIO13	DIO	General purpose input and output	AE16
GPIO14	DIO	General purpose input and output	AF17
GPIO15	DIO	General purpose input and output	AG17
GPIO16	DIO	General purpose input and output	AH17
GPIO17	DIO	General purpose input and output	AH16
GPIO18	DIO	General purpose input and output	AJ16
GPIO19	DIO	General purpose input and output	AB5
GPIO20	DIO	General purpose input and output	AB4
GPIO21	DIO	General purpose input and output	AA5
GPIO22	DIO	General purpose input and output	AD24
GPIO23	DIO	General purpose input and output	AB24
GPIO24	DIO	General purpose input and output	AA24
GPIO25	DIO	General purpose input and output	AC24
GPIO26	DIO	General purpose input and output	AE5
GPIO27	DIO	General purpose input and output	AF6
GPIO28	DIO	General purpose input and output	AE6
GPIO29	DIO	General purpose input and output	AG5
GPIO30	DIO	General purpose input and output	AG15
GPIO31	DIO	General purpose input and output	AJ15
GPIO32	DIO	General purpose input and output	AH15
GPIO33	DIO	General purpose input and output	AE15
GPIO34	DIO	General purpose input and output	AG14
GPIO35	DIO	General purpose input and output	AH22
GPIO36	DIO	General purpose input and output	AH23
GPIO37	DIO	General purpose input and output	AF22
GPIO38	DIO	General purpose input and output	AF23
GPIO39	DIO	General purpose input and output	AE24
GPIO40	DIO	General purpose input and output	AE23
GPIO41	DIO	General purpose input and output	AC27
GPIO42	DIO	General purpose input and output	AE28
GPIO43	DIO	General purpose input and output	AD27
GPIO44	DIO	General purpose input and output	AD28
GPIO45	DIO	General purpose input and output	Y28
GPIO46	DIO	General purpose input and output	AB30

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Signal Name	Type	Description	Ball Location
GPIO47	DIO	General purpose input and output	AB27
GPIO48	DIO	General purpose input and output	AB28
GPIO49	DIO	General purpose input and output	Y26
GPIO50	DIO	General purpose input and output	Y27
GPIO51	DIO	General purpose input and output	AA26
GPIO52	DIO	General purpose input and output	W26
GPIO53	DIO	General purpose input and output	Y30
GPIO54	DIO	General purpose input and output	AA29
GPIO55	DIO	General purpose input and output	Y29
GPIO56	DIO	General purpose input and output	AB29
GPIO57	DIO	General purpose input and output	AH27
GPIO58	DIO	General purpose input and output	AH26
GPIO59	DIO	General purpose input and output	AJ24
GPIO60	DIO	General purpose input and output	AH24
GPIO61	DIO	General purpose input and output	AJ4
GPIO62	DIO	General purpose input and output	AH4
GPIO63	DIO	General purpose input and output	AD5
GPIO64	DIO	General purpose input and output	AC5
GPIO65	DIO	General purpose input and output	AD4
GPIO66	DIO	General purpose input and output	AE4
GPIO67	DIO	General purpose input and output	AE3
GPIO68	DIO	General purpose input and output	AF1
GPIO69	DIO	General purpose input and output	AF2
GPIO70	DIO	General purpose input and output	AG2
GPIO71	DIO	General purpose input and output	AH2
GPIO72	DIO	General purpose input and output	AF3
GPIO73	DIO	General purpose input and output	AG3
GPIO74	DIO	General purpose input and output	AH3
GPIO75	DIO	General purpose input and output	AJ2
GPIO76	DIO	General purpose input and output	AH1
GPIO77	DIO	General purpose input and output	AJ3
GPIO78	DIO	General purpose input and output	AF4
GPIO79	DIO	General purpose input and output	AG4
GPIO80	DIO	General purpose input and output	AE13
GPIO81	DIO	General purpose input and output	AC13
GPIO82	DIO	General purpose input and output	AF14
GPIO83	DIO	General purpose input and output	AF13
GPIO84	DIO	General purpose input and output	AD13
GPIO85	DIO	General purpose input and output	AF12
GPIO86	DIO	General purpose input and output	AE14
GPIO87	DIO	General purpose input and output	M6
GPIO88	DIO	General purpose input and output	M3
GPIO89	DIO	General purpose input and output	L3
GPIO90	DIO	General purpose input and output	L2
GPIO91	DIO	General purpose input and output	M4

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Signal Name	Type	Description	Ball Location
GPIO92	DIO	General purpose input and output	M5
GPIO93	DIO	General purpose input and output	P30
GPIO94	DIO	General purpose input and output	N30
GPIO95	DIO	General purpose input and output	L30
GPIO96	DIO	General purpose input and output	N29
GPIO97	DIO	General purpose input and output	M27
GPIO98	DIO	General purpose input and output	M26
GPIO99	DIO	General purpose input and output	M28
GPIO100	DIO	General purpose input and output	L27
GPIO101	DIO	General purpose input and output	L29
GPIO102	DIO	General purpose input and output	M29
GPIO103	DIO	General purpose input and output	L28
GPIO104	DIO	General purpose input and output	N26
GPIO105	DIO	General purpose input and output	P29
GPIO106	DIO	General purpose input and output	P27
GPIO107	DIO	General purpose input and output	P28
GPIO108	DIO	General purpose input and output	R28
GPIO109	DIO	General purpose input and output	R27
GPIO110	DIO	General purpose input and output	AB13
GPIO111	DIO	General purpose input and output	AB14
GPIO112	DIO	General purpose input and output	AD14
GPIO113	DIO	General purpose input and output	AC14
GPIO114	DIO	General purpose input and output	AJ29
GPIO115	DIO	General purpose input and output	AJ28
GPIO116	DIO	General purpose input and output	AJ27
GPIO117	DIO	General purpose input and output	AD29
GPIO118	DIO	General purpose input and output	AC29
GPIO119	DIO	General purpose input and output	AE30
GPIO120	DIO	General purpose input and output	AE29
GPIO121	DIO	General purpose input and output	AF30
GPIO122	DIO	General purpose input and output	AF28
GPIO123	DIO	General purpose input and output	AF29
GPIO124	DIO	General purpose input and output	AH29
GPIO125	DIO	General purpose input and output	AG29
GPIO126	DIO	General purpose input and output	AH28
GPIO127	DIO	General purpose input and output	AG27
GPIO128	DIO	General purpose input and output	AG28
GPIO129	DIO	General purpose input and output	AF26
GPIO130	DIO	General purpose input and output	AF27
GPIO131	DIO	General purpose input and output	AJ25
GPIO132	DIO	General purpose input and output	AH25
GPIO133	DIO	General purpose input and output	AG25
GPIO134	DIO	General purpose input and output	AE25
GPIO135	DIO	General purpose input and output	AF25
GPIO136	DIO	General purpose input and output	AE9

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Signal Name	Type	Description	Ball Location
GPIO137	DIO	General purpose input and output	AD9
GPIO138	DIO	General purpose input and output	AC9
GPIO139	DIO	General purpose input and output	AB9
GPIO140	DIO	General purpose input and output	AD8
GPIO141	DIO	General purpose input and output	AC8
GPIO142	DIO	General purpose input and output	AE8
GPIO143	DIO	General purpose input and output	AF7
GPIO144	DIO	General purpose input and output	AB8

3.11.9 Pulse Width Modulation (PWM)

The device features three generic PWM modules to generate pulse sequences with programmable frequency and duration for variety of applications.

Each PWM module supports the following key features:

- Programmable duty cycle, high time and low time of pulse signals
- Programmable clock sources to support a wide range of output pulse frequencies
- Old mode, FIFO mode
- Periodical memory and random modes
- Sequential output mode and 3D LCM mode

3.11.9.1 PWM Signal Descriptions

Table 3-67 presents PWM signal descriptions.

Table 3-67 PWM Signal Descriptions

Signal Name	Type	Description	Ball Location
PWM_A	DO	PWM output A	AE20, AH17, AB5, AD13, M5, AJ29
PWM_B	DO	PWM output B	AE21, AH16, AB4, AF12, AC14, AJ28
PWM_C	DO	PWM output C	AF21, AJ16, AA5, AE14, L3, AJ27

3.11.9.2 PWM Timing Characteristics

Table 3-68 and Figure 3-50 present timing characteristics for PWM interfaces in the device.

Table 3-68 PWM Timing Characteristics

No.	Parameter		Min	Max	Unit
PWM01	t_c	Cycle time	76.92		ns
PWM02	t_w	Pulse duration, PWM	38.46		ns

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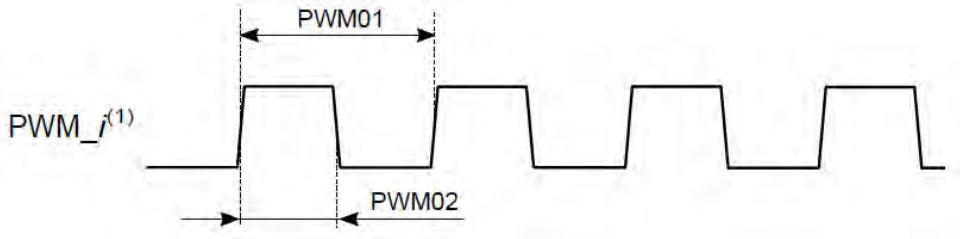

Figure 3-50 PWM Timing Diagram

1. In this diagram, *i* stands for A, B, or C.

3.12 Wireless Connectivity

The device supports four wireless connectivity functions, WLAN, BT, GPS, and FM, with RF parts integrated in the companion chips (MT6631, MT7663). With the built-in advanced and sophisticated radio coexistence algorithms and hardware mechanisms, the device provides the best and most convenient connectivity solution among the industry. The small footprint with low-power consumption greatly reduces the PCB layout resource.

The Wireless Communication Module (WCM) supports the following key features:

- Single shared antenna for BT, WLAN, and GPS
- Intelligent BT/WLAN/LTE coexistence scheme
- Enhanced overall quality for simultaneous voice, data and audio/video transmission on AI embedded devices

The WCM is programmed only by CPU internal API, WMT (Wireless Management Task). Therefore the user doesn't need to individually set-up the WCM.

3.12.1 WCM Signal Descriptions

Table 3-69 presents WCM signal descriptions.

Table 3-69 WCM Signal Descriptions

Signal Name	Type	Description	Ball Location
CONN_BT_CLK	DIO	Connectivity BT 2-wire interface	AD8
CONN_BT_DATA	DIO	Connectivity BT 2-wire interface	AC8
CONN_HRST_B	DO	Connectivity reset	AC9
CONN_TOP_CLK	DO	Connectivity TOP 2-wire interface	AE9
CONN_TOP_DATA	DIO	Connectivity TOP 2-wire interface	AD9
CONN_WB_PTA	DIO	Connectivity Wi-Fi/BT PTA	AB9
CONN_WF_CTRL0	DIO	Connectivity Wi-Fi 3-wire interface	AE8
CONN_WF_CTRL1	DIO	Connectivity Wi-Fi 3-wire interface	AF7
CONN_WF_CTRL2	DIO	Connectivity Wi-Fi 3-wire interface	AB8
BT_IN	AIO	BT I-channel negative input	AH9
BT_IP	AIO	BT I-channel positive input	AJ9
BT_QN	AIO	BT Q-channel negative input	AH11
BT_QP	AIO	BT Q-channel positive input	AH10
GPS_I	AIO	GPS I-channel input	AJ11
GPS_Q	AIO	GPS Q-channel input	AH12
WF_IN	AIO	Wi-Fi I-channel negative input	AJ7
WF_IP	AIO	Wi-Fi I-channel positive input	AJ6

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Signal Name	Type	Description	Ball Location
WF_QN	AIO	Wi-Fi Q-channel negative input	AH8
WF_QP	AIO	Wi-Fi Q-channel positive input	AH7
XIN_WBG	AIO	Crystal Clock Input	Y13

3.12.2 Wireless Local Area Network (WLAN)

The WLAN module includes the following key features:

- Dual-band (2.4 GHz and 5 GHz) single stream 802.11 ac/a/b/g/n MAC/BB/RF
- Compliance with 802.11 d/e/h/i/j/k/r/v
- Security: WFA WPA/WPA2 personal, AES-CCMP, WPI-SMS4, GCMP, WPS2.0, WAPI (hardware)
- Support of 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20 and 40 MHz Phased Coexistence Operation (PCO), unscheduled Power-Save Multi-Poll (PSMP)
- Support of 802.11w protected managed frames
- Support for 802.11ac STBC TX/RX, 4T1R beamformee, MU-MIMO RX, WoWLAN
- Support for MediaTek proprietary low power Green AP mode for portable hotspot operation
- Support of Wi-Fi DIRECT® (peer-to-peer wireless connection) and Wi-Fi Miracast® (Wi-Fi Display)
- Support of HotSpot 2.0 (HS2)
- Integrated 2.4 GHz PA with maximum 23 dBm CCK output power and 5 GHz PA with maximum 18.5 dBm OFDM 54 Mbps output power
- RX sensitivity at IEEE 802.11n HT20 MCS7 mode and -62 dBm at 5 GHz RX sensitivity at IEEE 802.11ac VHT80 MCS9 mode
- Support for 32 multicast address filters and TCP/UDP/IP checksum offload
- Support of per packet transmit power control
- QoS: WFA WMM, WMM PS

For more details refer to MT6631 and MT7663 documentation.

3.12.3 Bluetooth (BT)

The BT module supports the following key features:

- Bluetooth 5 dual mode for LE 2 Mbps, LE long range, and advertise extension
- Integrated PA with 9 dBm (class 1) transmit power or 12 dBm boost mode via Wi-Fi PA.
- Receiver sensitivity:
  - GFSK: -95 dBm
  - DQPSK: -94.5 dBm
  - 8-DPSK: -88 dBm
  - BLE_1M: -98.5 dBm
  - BLE_2M: -95 dBm
  - o BLE_500K: -101.5 dBm
  - BLE_125K: -104 dBm
- BT/Wi-Fi/LTE coexistence
- 7 BT links and 16 BLE links
- Packet Loss Concealment (PLC) function for better voice quality
- Wideband speech
- mSBC and SBC including mono and stereo
- Secure connection with AES-128 and ECC256

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- Adaptive Frequency Hopping with built-in channel assessment method For more details refer to MT6631 and MT7663 documentation.

3.12.4 Global Navigation Satellite System (GNSS)

The GNSS module includes the following key features:

- Support for GPS/Glonass/Beidou/Galileo/QZSS tri-band reception concurrently
  - GPS/Galileo only (GPS only)
  - GPS/Galileo—GLONASS (G+G)
  - GPS/Beidou (G+B)
  - GPS/GLONASS/Beidou (G+G+B)
  - GPS/Galileo/GLONASS (G+G+G)
  - GPS/Galileo/GLONASS/Beidou (G+G+G+B)
- Support for Satellite-Based Augmentation Systems (SBAS): WAAS/MSAS/EGNOS/GAGAN
- Best-in-class sensitivity performance
  - -165 dBm tracking sensitivity
  - -163 dBm hot start sensitivity
  - -148 dBm cold start sensitivity
  - -151 dBm warm start sensitivity
- A-GPS sensitivity is 8 dB design margin over 3GPP
- Full A-GPS capability (EPO/HotStill)
- Active interference cancellation for up to 12 in-band tones
- Support for both Temperature-Compensated Crystal Oscillator (TCXO) and Thermistor Crystal (TMS) clock sources
- 5 Hz update rate

For more details refer to MT6631 documentation.

3.12.5 FM System (FMSYS)

FMSYS is an FM radio module, which includes the following key features:

- Broadcast band from 65 to 108 MHz with 50 kHz tune increment
- RDS/RBDS
- Digital stereo demodulator
- Simplified digital audio interface (I2S)
- Stereo noise reduction
- Audio sensitivity 2 dBµVemf (SINAD = 26 dB)
- Audio SINAD 60 dB
- Anti-jamming

For more details refer to MT6631 documentation.

3.13 Miscellaneous

3.13.1 JTAG Interface (JTAG)

The device supports legacy JTAG interfaces available for emulation. The interface connects to an external Test Access Port (TAP) that implements a stateful protocol to access a set of test registers that present chip logic levels and device capabilities of various parts.

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3.13.1.1 JTAG Signal Descriptions

Table 3-70 presents JTAG signal descriptions.

Table 3-70 JTAG Signal Descriptions

Signal Name	Type	Description	Ball Location
JTCK	DI	JTAG test clock input	AJ15
JTDI	DI	JTAG test data input	AH15
JTDO	DO	JTAG test data output	AE15
JTMS	DI	JTAG test mode select input	AG15
JTRST	DI	JTAG test reset	AG14

3.13.1.2 JTAG Timing Characteristics

Table 3-71 presents timing characteristics for JTAG interfaces in the device.

Table 3-71 JTAG Timing Characteristics

No.	Parameter		Min	Max	Unit
JTG01	t_c	Cycle time, TCK		100	ns
JTG02	$t_{w_TCK_high}$	Pulse duration, TCK high	50		ns
JTG03	$t_{w_TCK_low}$	Pulse duration, TCK low	50		ns
JTG04	t_{s_TDI/TMS_TCK}	Setup time, TDI/TMS valid before TCK rising edge	50		ns
JTG05	t_{h_TDI/TMS_TCK}	Hold time, TDI/TMS valid after TCK rising edge	50		ns
JTG06	t_{d_TDO}	Delay time, TDO valid after TCK falling edge		10.399	ns
JTG07	$t_{h_TDO_TCK}$	Hold time, TDO valid after TCK rising edge	60.319		ns

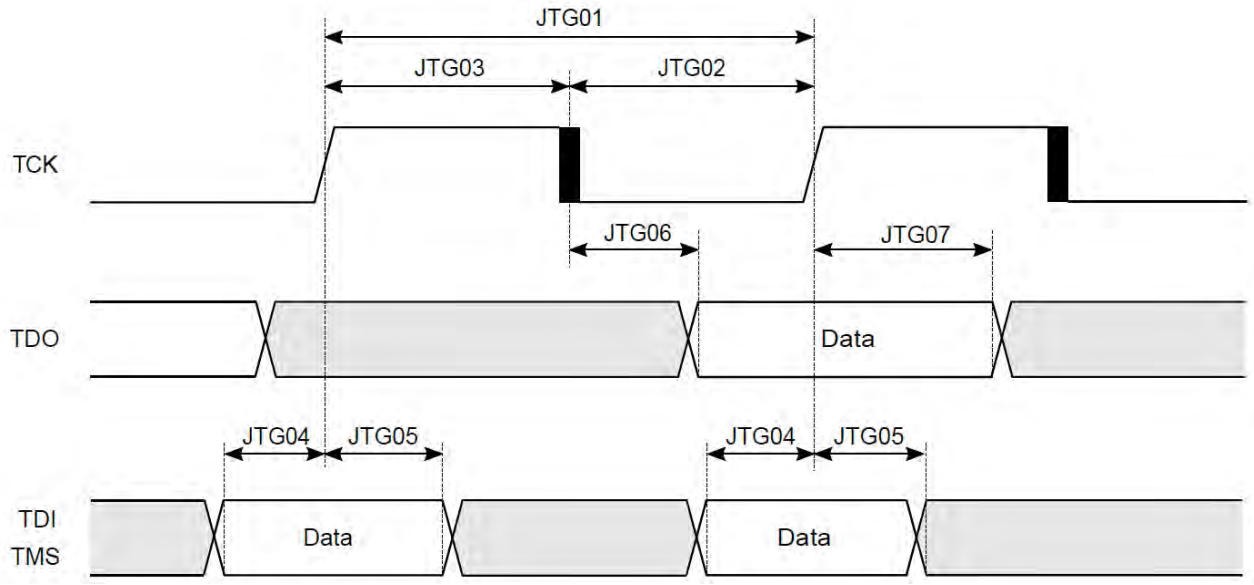

Figure 3-51 JTAG Timing Diagram

3.13.2 Timers and Counters

3.13.2.1 System Timer (SYSTMR)

The device has dedicated universal 64-bit always-on up-counter SYSTMR. The counter value of SYSTMR is passed to CPU, SCPSYS, GPU, and other processors to provide uniform system timestamps for operating systems like Android, Linux, and RTOS.

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The SYSTMR supports the following key features:

- Enabled by default to tick with 13 MHz clock period
- Clock divider to allow the timer to tick with 26/13/6.5 MHz clock period
- HW counter incremented compensation when switching to 32 kHz clock source
- 4 x 32-bit counter timeout value (read as 32-bit down counter)
- Security access permission control for each control register (with one-time lock bit)

3.13.2.2 General-Purpose Timer (GPT)

The device has one GPT module that includes five 32-bit and one 64-bit timers. Each GPT can operate on one of the two clock sources, RTC clock (32.768 kHz) or system clock (13 MHz).

Each GPT supports:

- ONE-SHOT mode
- REPEAT mode
- KEEP-GO mode
- FREERUN mode

3.13.2.3 Watchdog Timer (WDT)

The WDT module is a part of TOPRGU. For more information refer to Section 5.5 Reset.

3.13.3 PMIC Wrapper (PWRAP)

The PWRAP serves as a bridge for the communication between CPU and PMIC.

The PWRAP supports the following key features:

- Fast auto SPI format generator for PMIC registers read/write
- APB3.0 bus lock scheme when SPI is busy
- Manual SPI format generator
- Dual I/O SPI mode
- Separated frequency between controller and SPI

3.13.3.1 PWRAP Signal Descriptions

Table 3-72 presents PWRAP signal descriptions.

Table 3-72 PWRAP Signal Descriptions

Signal Name	Type	Description	Ball Location
PWRAP_SPI0_CK	DO	PWRAP serial clock	AD27
PWRAP_SPI0_CSN	DO	PWRAP chip select	AD28
PWRAP_SPI0_MI	DIO	PWRAP master input / slave output	AC27, AE28
PWRAP_SPI0_MO	DIO	PWRAP master output / slave input	AC27, AE28

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3.13.4 Auxiliary Analog-to-Digital Converter (AUXADC)

The device features one AUXADC module. It is used to identify the plugged peripherals and perform temperature measurements.

The AUXADC module key features are:

- 12-bit Successive Approximation Register (SAR) ADC architecture
- 16 input channels operating in immediate mode
- Configurable auto-sampling function per channel
- Sequential channel serving from high to low channel
- Immediate analog-digital conversion with auto-set option
- Background detection and interrupt
- Temperature measurement

3.13.4.1 AUXADC Signal Descriptions

Table 3-73 shows the AUXADC channels descriptions.

Table 3-73 AUXADC Signal Descriptions

Signal Name	Type	Description	Ball Location
AUXIN0[1][2]	AIO	AUXADC external input channel 0	W18
AUXIN1[1][2]	AIO	AUXADC external input channel 1	Y18
AUXIN2[1][2]	AIO	AUXADC external input channel 2	AA18
AUXIN3[1][2]	AIO	AUXADC external input channel 3	AB18
AUXIN4[1][2]	AIO	AUXADC external input channel 4	AC18
AUXIN5[1][2]	AIO	AUXADC external input channel 5	AD18
REFP[3]	AIO	Positive reference voltage for internal circuit	AD19

1. This pin should be connected to GND when unused.
2. All AUXIN* pins should be connected via a 0.1-µF capacitor to GND, as close as possible to the device, when used.
3. The REFP pin should be connected via a 1-µF capacitor to GND, as close as possible to the device, when used.

3.13.4.2 AUXADC Channel Mapping

Table 3-74 presents definitions of AUXADC channels.

Table 3-74 AUXADC Channel Mapping

AUXADC Channel ID	Description
Channel 0	External use (AUXIN0)
Channel 1	External use (AUXIN1)
Channel 2	External use (AUXIN2)
Channel 3	External use (AUXIN3)
Channel 4	External use (AUXIN4)
Channel 5	External use (AUXIN5)
Channel 6	NA[1]
Channel 7	NA[1]
Channel 8	NA[1]
Channel 9	NA[1]
Channel 10	Internal use (thermal sensor)
Channel 11	Internal use (thermal sensor)

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AUXADC Channel ID	Description
Channel 12	NA[1]
Channel 13	NA[1]
Channel 14	NA[1]
Channel 15	NA[1]

1. NA in this table = Not Applicable.

3.13.4.3 AUXADC Timing and Functional Characteristics

Table 3-75 presents timing and functional characteristics for auxiliary AUXADC interface in the device.

Table 3-75 AUXADC Specifications

Parameter		Min	Typ	Max	Unit
f_{OP}	Operating frequency		4		MHz
N	Resolution		12		Bit
f_S	Sampling rate at N-bit		4 / (N+4)		MSPS
IN_{SW}	Input swing	0		1.5	V
C_{IN}	Input capacitance unselected channel		50		fF
	Input capacitance selected channel		4		pF
R_{IN}	Input resistance unselected channel	400			MΩ
$F_{cycle_latency}$	Cycle latency		N+4		$1/f_{OP}$
D_{NL}	Differential non-linearity		±1		LSB
I_{NL}	Integral non-linearity		±2		LSB
SNR+D	Signal-to-noise and distortion ratio (1 kHz full swing input and 1.0833 MHz clock rate)	60	67		dB
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD	Analog power supply	1.7	1.8	1.9	V

3.13.5 Thermal Controller

The device thermal controller is based on several temperature sensors in the hot spots on the die. The thermal controller executes a periodic measurement for each hot spot. The temperature values are readable by software. In order to minimize the software effort to monitor temperature, the thermal controller generates interrupts to inform microprocessors of any abnormal condition.

The thermal controller supports the following key features:

- Up to four thermal sensors
- Periodic temperature measurement
- Temperature monitoring
- Different types of low pass filters for thermal sensor reading

Table 3-76 presents the Temperature Sensor (TSENSE) specifications.

Table 3-76 TSENSE Specifications

Parameter	Min	Typ	Max	Unit
Resolution		0.15		°C
Temperature range	0		85	°C
Accuracy	±5			°C

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Parameter	Min	Typ	Max	Unit
Active current		700		µA
Quiescent current		30		µA

3.14 Boot Modes

The device supports the following boot modes:

- eMMC boot
- Boot ROM power down mode

The Boot ROM power down mode is used in the following scenarios:

- After system boot, boot ROM will be powered down and prevented from any probe of ROM content.
- In MultiCore Deep Idle (MCDI), the Boot ROM is the bootstrap for suspend/resume CPU.

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4 Ball Map

Figure 4-1 presents simplified diagram of the ball location on the package.

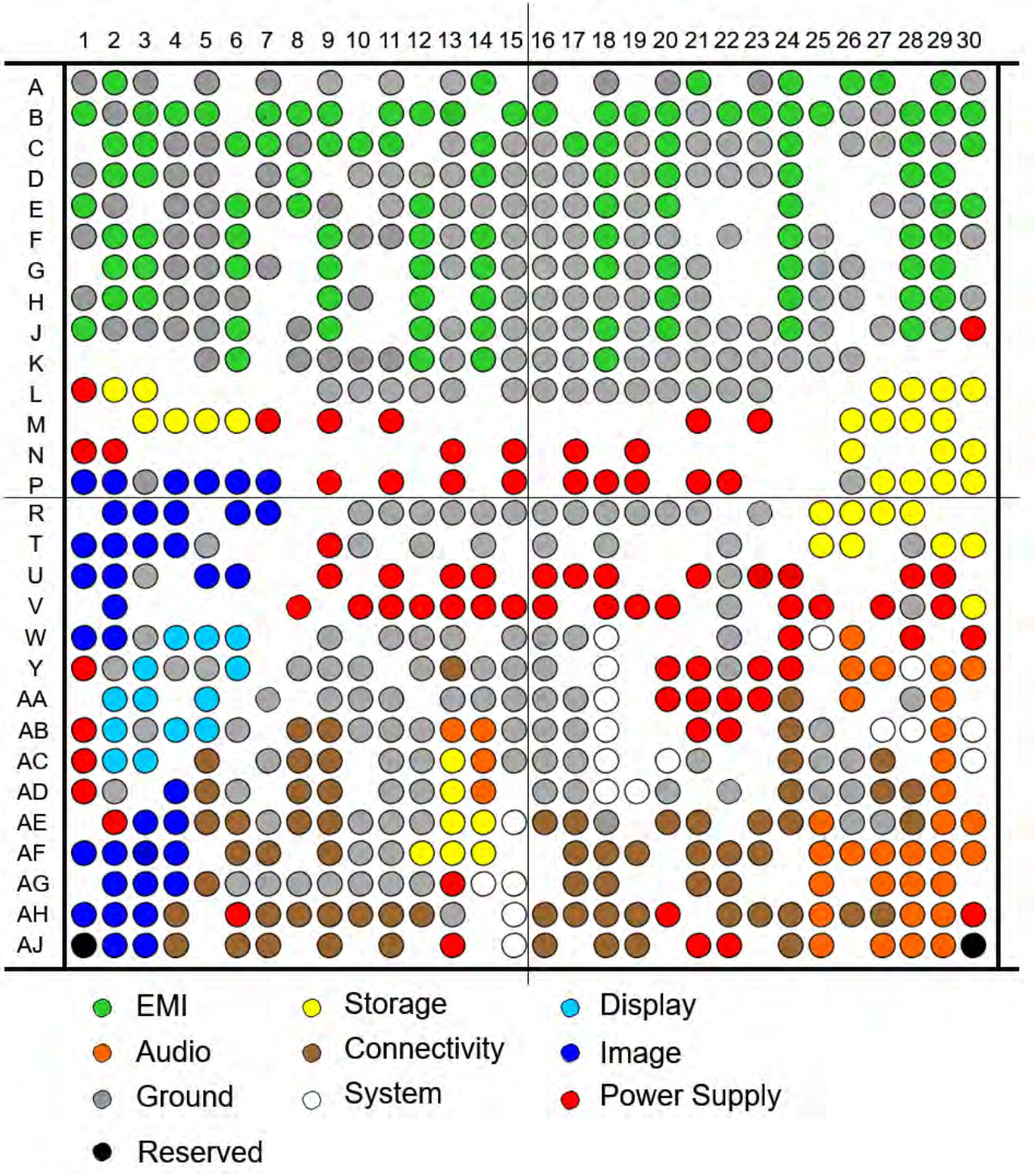

Figure 4-1 Ball Map Diagram

For detailed information about package outlines, thermal characteristics, and markings, see Section 7 Package Information.

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4.1 Quadrant Pinout

Table 4-1 shows pin mapping on the top left part of the package.

Table 4-1 Ball Map-Top Left

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DVSS	EMI0_ DQ1	DVSS		DVSS		DVSS		DVSS		DVSS		DVSS	EMI1_A11	
B	EMI0_ DM0	DVSS	EMI0_ DQ5	EMI0_ DQ3	EMI0_DQ7		EMI0_DQ8	EMI0_ DQ10	EMI0_DQ12		EMI0_DQ4	EMI0_DQ2	EMI0_DQ6		EMI1_A8
C		EMI0_ DQS1_C	EMI0_ A13	DVSS	DVSS	EMI0_DQS0_T	EMI0_DQS0_C	DVSS	EMI0_DQ14	EMI0_ DM1	EMI0_DQ0		DVSS	EMI0_A0	DVSS
D	DVSS	EMI0_ DQS1_T	EMI0_ A9	DVSS	DVSS		DVSS	EMI0_CK_C		DVSS	DVSS	DVSS	DVSS	EMI0_A6	DVSS
E	EMI0_ DQ9	DVSS		DVSS	DVSS	EMI0_A7	DVSS	EMI0_CK_T	DVSS		DVSS	EMI0_A10	DVSS	DVSS	DVSS
F	DVSS	EMI0_ DQ11	EMI0_ A2	DVSS	DVSS	EMI0_A5			EMI0_CS1_N	DVSS	DVSS	EMI0_ACT_N	DVSS	EMI_RESET_N	DVSS
G		EMI0_ DQ13	EMI0_ A8	DVSS	DVSS	EMI0_A1	DVSS		EMI0_CS0_N			EMI0_ODT	DVSS	EMI0_BG0	DVSS
H	DVSS	EMI0_ DQ15	EMI0_ A11	DVSS	DVSS	DVSS			EMI0_RAS_N	DVSS		EMI0_A12		EMI0_WE_N	DVSS
J	EMI_ EXTR	DVSS	DVSS	DVSS	DVSS	EMI0_A3		DVSS	EMI0_CAS_N			EMI0_A4	DVSS	EMI0_CKE1	DVSS
K					DVSS	EMI0_BA1		DVSS	DVSS	DVSS	DVSS	EMI0_BA0	DVSS	EMI0_CKE0	DVSS
L	DVDD28_ MSDC1	MSDC1_ DAT1	MSDC1_ DAT0						DVSS	DVSS	DVSS	DVSS	DVSS		DVSS
M			MSDC1_ CLK	MSDC1_ DAT2	MSDC1_ DAT3	MSDC1_CMD	AVDD18_ RDDR		AVDDQ_ EMI0		AVDDQ_EMI0				
N	AVDD12_ CSI0	AVDD12_ CSI1											AVDD2_EMI		AVDD2_EMI
P	CSI0B_L2P	CSI0B_L2N	DVSS	CSI0A_L1N	CSI0A_L1P	CSI0A_L2N	CSI0A_L2P		DVDD_TOP		DVDD_TOP		DVDD_TOP		DVDD_TOP

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Table 4-2 shows pin mapping on the top right part of the package.

Table 4-2 Ball Map-Top Right

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
DVSS		DVSS		DVSS	EMI1_DQ9		DVSS	EMI1_DM0		EMI1_DQ3	EMI1_DQ7		EMI1_DQ8	DVSS	A
EMI1_A2		EMI1_DQ15	EMI1_DQ13	EMI1_DQ11	DVSS	EMI1_DQS1_T	EMI1_DQS1_C	EMI1_DQ1	EMI1_DQ5	DVSS	DVSS	EMI1_DQS0_T	EMI1_DQS0_C	EMI1_DQ10	B
DVSS	EMI1_A9	EMI1_A13	DVSS	EMI1_RAS_N	DVSS	DVSS	DVSS	EMI1_CKE1		DVSS	DVSS	EMI1_WE_N	DVSS	EMI1_DQ12	C
DVSS	DVSS	EMI1_A7	DVSS	EMI1_A12	DVSS	DVSS	DVSS	EMI1_CKE0				EMI1_BG0	EMI1_DQ14		D
DVSS	DVSS	EMI1_CAS_N	DVSS	EMI1_BA1				EMI1_BA0			DVSS	DVSS	EMI1_DM1	EMI1_DQ0	E
DVSS	DVSS	EMI1_CS0_N	DVSS	DVSS		DVSS		EMI1_A4	DVSS			EMI_TP	EMI1_DQ4	DVSS	F
DVSS	DVSS	EMI1_CS1_N	DVSS	EMI1_A3	DVSS			EMI1_ODT	DVSS	DVSS		EMI_TN	EMI1_DQ2		G
DVSS	DVSS	DVSS	DVSS	EMI1_A1	DVSS			EMI1_ACT_N	DVSS	DVSS		EMI1_A6	EMI1_DQ6	DVSS	H
DVSS	DVSS	EMI1_CK_T	DVSS	EMI1_A5	DVSS	DVSS	DVSS	EMI1_A10	DVSS		DVSS	EMI1_A0	DVSS	DVDD18_MSDC0	J
DVSS	DVSS	EMI1_CK_C	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS					K
DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS				MSDC0_DAT3	MSDC0_DAT0	MSDC0_DAT2	MSDC0_DAT5	L
					AVDDQ_EMI0		AVDDQ_EMI0			MSDC0_CMD	MSDC0_RSTB	MSDC0_CLK	MSDC0_DAT1		M
	AVDD2_EMI		AVDD2_EMI							MSDC0_DSL			MSDC0_DAT4	MSDC0_DAT6	N
	DVDD_TOP	DVDD_TOP	DVDD_TOP		DVDD_TOP	DVDD_TOP				DVSS	NCEB1	NCEB0	NCLE	MSDC0_DAT7	P

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Table 4-3 shows pin mapping on the bottom left part of the package.

Table 4-3 Ball Map-Bottom Left

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R		CSI0B_L1P	CSI0A_L0N	CSI0A_L0P		CSI1A_L2N	CSI1A_L2P			DVSS	DVSS	DVSS	DVSS	DVSS	DVSS
T	CSI0B_L0P	CSI0B_L1N	CSI1A_L1N	CSI1A_L1P	DVSS				DVDD_SRAM	DVSS		DVSS		DVSS	
U	CSI0B_L0N	CSI1B_L1P	DVSS		CSI1A_L0N	CSI1A_L0P			DVDD_TOP		DVDD_TOP		DVDD_TOP	DVDD_TOP	
V		CSI1B_L1N						DVDD_TOP		DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP	DVDD_TOP
W	CSI1B_L0N	CSI1B_L0P	DVSS	DSI_D0N	DSI_D0P	DSI_D2P			DVSS		DVSS	DVSS	DVSS		DVSS
Y	AVDD18_CSI	DVSS	DSI_CKN	DVSS	DVSS	DSI_D2N		DVSS	DVSS	DVSS		DVSS	XIN_WBG	DVSS	DVSS
AA		DSI_D1N	DSI_CKP		DSI_TE		DVSS		DVSS	DVSS	DVSS		DVSS	DVSS	DVSS
AB	AVDD04_DSI	DSI_D1P	DVSS	LCM_RST	DISP_PWM	DVSS		CONN_WF_CTRL2	CONN_WB_PTA	DVSS	DVSS	DVSS	PCM_CLK	PCM_SYNC	DVSS
AC	AVDD12_DSI	DSI_D3N	DSI_D3P		SCL3		DVSS	CONN_BT_DATA	CONN_HRST_B		DVSS	DVSS	MSDC2_CLK	PCM_TX	DVSS
AD	AVDD18_DSI	DVSS		CMMCLK0	SDA3	DVSS		CONN_BT_CLK	CONN_TOP_DATA		DVSS	DVSS	MSDC2_DAT2	PCM_RX	
AE		DVDD18_IO3	CMPCLK	CMMCLK1	SPI_CS	SPI_MI	DVSS	CONN_WF_CTRL0	CONN_TOP_CLK	DVSS	DVSS	DVSS	MSDC2_CMD	MSDC2_DSL	JTDO
AF	CMDAT0	CMDAT1	CMDAT4	CMHSYNC		SPI_CK	CONN_WF_CTRL1		DVSS	DVSS	DVSS	MSDC2_DAT3	MSDC2_DAT1	MSDC2_DAT0	
AG		CMDAT2	CMDAT5	CMVSYNC	SPI_MO	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD18_MSDC2	JTRST	JTMS
AH	CMDAT8	CMDAT3	CMDAT6	SCL2		AVDD12_WBG	WF_QP	WF_QN	BT_IN	BT_QP	BT_QN	GPS_Q	DVSS		JTDI
AJ	DUMMY	CMDAT7	CMDAT9	SDA2		WF_IP	WF_IN		BT_IP		GPS_I		AVDD18_WBG		JTCK

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Table 4-4 shows pin mapping on the bottom right part of the package.

Table 4-4 Ball Map-Bottom Right

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		DVSS		CHD_DP_P0	CHD_DM_P0	NRNB	NREB			R
DVSS		DVSS				DVSS			USB_DM_P1	USB_DP_P1		DVSS	USB_DM_P0	USB_DP_P0	T
DVDD_TOP	DVDD_TOP	DVDD_SRAM			DVDD_DVFS	DVSS	DVDD_DVFS	DVDD_DVFS				DVDD_DVFS	AVDD18_USB_P0		U
DVDD_TOP		DVDD_TOP	DVDD_MCUSYS_SRAM	DVDD_DVFS		DVSS		DVDD_DVFS	DVDD_DVFS		DVDD_DVFS	DVSS	AVDD18_USB_P1	USB_VBUS_P0	V
DVSS	DVSS	AUXIN0				DVSS		DVDD_DVFS	TESTMODE	AUD_DAT_MOSI1		AVDD33_USB		AVDD12_USB	W
DVSS		AUXIN1		DVDD_DVFS	DVDD_DVFS	DVSS	DVDD_DVFS	DVDD_DVFS		AUD_CLK_MOSI	AUD_SYNC_MOSI	RTC32K_CK	AUD_DAT_MISO0	AUD_CLK_MISO	Y
DVSS	DVSS	AUXIN2		DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	DVDD_DVFS	KPCOL0		AUD_DAT_MOSI0		DVSS	AUD_SYNC_MISO		AA
DVSS	DVSS	AUXIN3			DVDD18_IO1	DVDD_VQPS		KPROW1	DVSS		SRCLKENA0	SRCLKENA1	AUD_DAT_MISO1	WATCHDOG	AB
DVSS	DVSS	AUXIN4		26M_CLKSQ	DVSS			KPCOL1	DVSS	DVSS	PWRAP_SPI0_MI		DMIC0_DAT0	SYSRSTB	AC
DVSS	DVSS	AUXIN5	REFP	DVSS		DVSS		KPROW0	DVSS	DVSS	PWRAP_SPI0_CK	PWRAP_SPI0_CSN	DMIC0_CLK		AD
GPIO13	GPIO12	DVSS		GPIO0	GPIO1		UTXD2	URXD2	TDM_TX_DATA2	DVSS	DVSS	PWRAP_SPI0_MO	DMIC1_CLK	DMIC0_DAT1	AE
	GPIO14	GPIO6	GPIO4		GPIO2	URXD1	UTXD1		TDM_TX_DATA3	TDM_TX_BCK	TDM_TX_LRCK	DMIC1_DAT1	DMIC2_CLK	DMIC1_DAT0	AF
	GPIO15	GPIO9			GPIO7	GPIO3			TDM_TX_DATA1		DMIC3_DAT0	DMIC3_DAT1	DMIC2_DAT1		AG
GPIO17	GPIO16	GPIO11	GPIO5	AVDD18_AP		URXD0	UTXD0	SCL1	TDM_TX_DATA0	SCL0	SDA0	DMIC3_CLK	DMIC2_DAT0	DVDD18_IO0	AH
GPIO18		GPIO10	GPIO8		AVDD12_PLLGP	AVDD18_PLLGP		SDA1	TDM_TX_MCK		I2S_BCK	I2S_LRCK	I2S_DATA_IN	DUMMY	AJ

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4.2 Pin Characteristics

Table 4-5 describes the pin characteristics and the multiplexed signals on each ball.

Table 4-5 Pin Characteristics

Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
GPIO0	AE20	GPIO0	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_D0	DO	1					
		PWM_A	DO	2					
		I2S2_BCK	DO	3					
		EXT_TXD0	DO	4					
GPIO1	AE21	GPIO1	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_D1	DO	1					
		PWM_B	DO	2					
		I2S2_LRCK	DO	3					
		EXT_TXD1	DO	4					
GPIO2	AF21	GPIO2	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_D2	DO	1					
		PWM_C	DO	2					
		I2S2_MCK	DO	3					
		EXT_TXD2	DO	4					
GPIO3	AG22	GPIO3	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_D3	DO	1					
		I2S2_DI	DI	3					
		EXT_TXD3	DO	4					
GPIO4	AF19	GPIO4	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_D4	DO	1					
		I2S1_BCK	DO	3					
		EXT_TXC	DI	4					

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Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
GPIO5	AH19	GPIO5	DIO	0	0	KP200KIO	DVDD18_IO0	PD	I
		DPI_D5	DO	1					
		I2S1_LRCK	DO	3					
		EXT_RXER	DI	4					
GPIO6	AF18	GPIO6	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_D6	DO	1					
		I2S1_MCK	DO	3					
		EXT_RXC	DI	4					
GPIO7	AG21	GPIO7	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_D7	DO	1					
		I2S1_DO	DO	3					
		EXT_RXDV	DI	4					
GPIO8	AJ19	GPIO8	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_D8	DO	1					
		SPI_CLK	DO	2					
		I2S0_BCK	DIO	3					
		EXT_RXD0	DI	4					
GPIO9	AG18	GPIO9	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_D9	DO	1					
		SPI_CSB	DO	2					
		I2S0_LRCK	DIO	3					
		EXT_RXD1	DI	4					
GPIO10	AJ18	GPIO10	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_D10	DO	1					
		SPI_MI	DI	2					
		I2S0_MCK	DO	3					
		EXT_RXD2	DI	4					

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Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
GPIO11	AH18	GPIO11	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_D11	DO	1					
		SPI_MO	DO	2					
		I2S0_DI	DI	3					
		EXT_RXD3	DI	4					
GPIO12	AE17	GPIO12	DIO	0	0	I2C18IO	DVDD18_IO0	PD	I
		DPI_DE	DO	1					
		UCTS1	DI	2					
		I2S3_BCK	DO	3					
		EXT_TXEN	DO	4					
GPIO13	AE16	GPIO13	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_VSYNC	DO	1					
		URTS1	DO	2					
		I2S3_LRCK	DO	3					
		EXT_COL	DIO	4					
		SPDIF_IN	DI	5					
GPIO14	AF17	GPIO14	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_CK	DO	1					
		UCTS2	DI	2					
		I2S3_MCK	DO	3					
		EXT_MDIO	DIO	4					
		SPDIF_OUT	DO	5					
GPIO15	AG17	GPIO15	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		DPI_HSYNC	DO	1					
		URTS2	DO	2					
		I2S3_DO	DO	3					
		EXT_MDC	DO	4					
		IRRX	DI	5					
		EXT_FRAME_SYNC	DI	6					

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Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
GPIO16	AH17	GPIO16	DIO	0	0	MSDC0IO	DVDD18_IO0	PD	I
		DPI_D12	DO	1					
		USB_DRVVBUS	DO	2					
		PWM_A	DO	3					
GPIO17	AH16	GPIO17	DIO	0	0	MSDC1IO	DVDD18_IO0	PD	I
		DPI_D13	DO	1					
		IDDIG	DI	2					
		PWM_B	DO	3					
GPIO18	AJ16	GPIO18	DIO	0	0	MSDC0IO	DVDD18_IO0	PD	I
		DPI_D14	DO	1					
		EXT_FRAME_SYNC	DI	2					
		PWM_C	DO	3					
DISP_PWM	AB5	GPIO19	DIO	0	0	MSDC0IO	DVDD18_IO3	PD	I
		DISP_PWM	DO	1					
		PWM_A	DO	2					
LCM_RST	AB4	GPIO20	DIO	0	0	MSDC0IO	DVDD18_IO3	PD	I
		LCM_RST	DO	1					
		PWM_B	DO	2					
DSI_TE	AA5	GPIO21	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		DSI_TE	DI	1					
		PWM_C	DO	2					
KPROW0	AD24	GPIO22	DIO	0	1	GPIO18	DVDD18_IO1	PD	OL
		KPROW0	DIO	1					
KPROW1	AB24	GPIO23	DIO	0	0	GPIO18	DVDD18_IO1	PU	I
		KPROW1	DIO	1					
		IDDIG	DI	2					
		EXT_FRAME_SYNC	DI	6					
KPCOL0	AA24	GPIO24	DIO	0	1	GPIO18	DVDD18_IO1	PU	I
		KPCOL0	DIO	1					

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Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
KPCOL1	AC24	GPIO25	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		KPCOL1	DIO	1					
		USB_DRVVBUS	DO	2					
SPI_CS	AE5	GPIO26	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		SPI_CSB	DO	1					
SPI_CK	AF6	GPIO27	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		SPI_CLK	DO	1					
SPI_MI	AE6	GPIO28	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		SPI_MI	DI	1					
		SPI_MO	DO	2					
SPI_MO	AG5	GPIO29	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		SPI_MO	DO	1					
		SPI_MI	DI	2					
JTMS	AG15	GPIO30	DIO	0	1	GPIO18	DVDD18_IO1	PU	I
		JTMS	DIO	1					
JTCK	AJ15	GPIO31	DIO	0	1	GPIO18	DVDD18_IO1	PU	I
		JTCK	DI	1					
JTDI	AH15	GPIO32	DIO	0	1	GPIO18	DVDD18_IO1	PU	I
		JTDI	DI	1					
JTDO	AE15	GPIO33	DIO	0	1	GPIO18	DVDD18_IO1	PD	OL
		JTDO	DO	1					
JTRST	AG14	GPIO34	DIO	0	1	GPIO18	DVDD18_IO1	PU	I
		JTRST	DI	1					
URXD0	AH22	GPIO35	DIO	0	1	GPIO18	DVDD18_IO1	PU	I
		URXD0	DI	1					
		UTXD0	DO	2					
UTXD0	AH23	GPIO36	DIO	0	1	GPIO18	DVDD18_IO1	PU	OH
		UTXD0	DO	1					
		URXD0	DI	2					

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URXD1	AF22	GPIO37	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		URXD1	DI	1					
		UTXD1	DO	2					
		UCTS2	DI	3					
		I2S0_MCK	DO	6					
UTXD1	AF23	GPIO38	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		UTXD1	DO	1					
		URXD1	DI	2					
		URTS2	DO	3					
		I2S1_MCK	DO	6					
URXD2	AE24	GPIO39	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		URXD2	DI	1					
		UTXD2	DO	2					
		UCTS1	DI	3					
		IDDIG	DI	4					
		I2S2_MCK	DO	6					
UTXD2	AE23	GPIO40	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		UTXD2	DO	1					
		URXD2	DI	2					
		URTS1	DO	3					
		USB_DRVVBUS	DO	4					
		I2S3_MCK	DO	6					
PWRAP_SPI0_MI	AC27	GPIO41	DIO	0	1	GPIO18	DVDD18_IO0	PD	I
		PWRAP_SPI0_MI	DIO	1					
		PWRAP_SPI0_MO	DIO	2					
PWRAP_SPI0_MO	AE28	GPIO42	DIO	0	1	GPIO18	DVDD18_IO0	PD	I
		PWRAP_SPI0_MO	DIO	1					
		PWRAP_SPI0_MI	DIO	2					
PWRAP_SPI0_CK	AD27	GPIO43	DIO	0	1	GPIO18	DVDD18_IO0	PD	OL
		PWRAP_SPI0_CK	DO	1					

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PWRAP_SPI0_CSN	AD28	GPIO44	DIO	0	1	GPIO18	DVDD18_IO0	PU	OH
		PWRAP_SPI0_CSN	DO	1					
RTC32K_CK	Y28	GPIO45	DIO	0	1	GPIO18	DVDD18_IO0	PD	I
		RTC32K_CK	DI	1					
WATCHDOG	AB30	GPIO46	DIO	0	1	GPIO18	DVDD18_IO0	PU	OH
		WATCHDOG	DO	1					
SRCLKENA0	AB27	GPIO47	DIO	0	1	GPIO18	DVDD18_IO0	PU	OH
		SRCLKENA0	DO	1					
		SRCLKENA1	DO	2					
SRCLKENA1	AB28	GPIO48	DIO	0	1	I2C18IO	DVDD18_IO0	PD	OL
		SRCLKENA1	DO	1					
AUD_CLK_MOSI	Y26	GPIO49	DIO	0	0	I2C18IO	DVDD18_IO0	PD	I
		AUD_CLK_MOSI	DO	1					
		AUD_CLK_MISO	DI	2					
		I2S1_MCK	DO	3					
AUD_SYNC_MOSI	Y27	GPIO50	DIO	0	0	I2C18IO	DVDD18_IO0	PD	I
		AUD_SYNC_MOSI	DO	1					
		AUD_SYNC_MISO	DI	2					
		I2S1_BCK	DO	3					
AUD_DAT_MOSI0	AA26	GPIO51	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		AUD_DAT_MOSI0	DO	1					
		AUD_DAT_MISO0	DI	2					
		I2S1_LRCK	DO	3					
AUD_DAT_MOSI1	W26	GPIO52	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		AUD_DAT_MOSI1	DO	1					
		AUD_DAT_MISO1	DI	2					
		I2S1_DO	DO	3					

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AUD_CLK_MISO	Y30	GPIO53	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		AUD_CLK_MISO	DI	1					
		AUD_CLK_MOSI	DO	2					
		I2S2_MCK	DO	3					
AUD_SYNC_MISO	AA29	GPIO54	DIO	0	0	MSDC0IO	DVDD18_IO1	PD	I
		AUD_SYNC_MISO	DI	1					
		AUD_SYNC_MOSI	DO	2					
		I2S2_BCK	DO	3					
AUD_DAT_MISO0	Y29	GPIO55	DIO	0	0	MSDC0IO	DVDD18_IO1	PD	I
		AUD_DAT_MISO0	DI	1					
		AUD_DAT_MOSI0	DO	2					
		I2S2_LRCK	DO	3					
AUD_DAT_MISO1	AB29	GPIO56	DIO	0	0	MSDC1IO	DVDD18_IO1	PD	I
		AUD_DAT_MISO1	DI	1					
		AUD_DAT_MOSI1	DO	2					
		I2S2_DI	DI	3					
SDA0	AH27	GPIO57	DIO	0	1	MSDC1IO	DVDD18_IO1	PU	I
		SDA0_0	DIO	1					
SCL0	AH26	GPIO58	DIO	0	1	MSDC0IO	DVDD18_IO1	PU	I
		SCL0_0	DIO	1					
SDA1	AJ24	GPIO59	DIO	0	1	MSDC0IO	DVDD18_IO1	PU	I
		SDA1_0	DIO	1					
SCL1	AH24	GPIO60	DIO	0	1	MSDC0IO	DVDD18_IO1	PU	I
		SCL1_0	DIO	1					
SDA2	AJ4	GPIO61	DIO	0	1	MSDC0IO	DVDD18_IO3	PU	I
		SDA2_0	DIO	1					
SCL2	AH4	GPIO62	DIO	0	1	MSDC0IO	DVDD18_IO3	PU	I
		SCL2_0	DIO	1					
SDA3	AD5	GPIO63	DIO	0	1	MSDC0IO	DVDD18_IO3	PU	I
		SDA3_0	DIO	1					

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SCL3	AC5	GPIO64	DIO	0	1	MSDC0IO	DVDD18_IO3	PU	I
		SCL3_0	DIO	1					
CMMCLK0	AD4	GPIO65	DIO	0	0	MSDC0IO	DVDD18_IO3	PD	I
		CMMCLK0	DO	1					
		CMMCLK1	DO	2					
CMMCLK1	AE4	GPIO66	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMMCLK1	DO	1					
		CMMCLK0	DO	2					
CMPCLK	AE3	GPIO67	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMPCLK	DI	1					
		TDM_RX_BCK	DO	4					
		I2S0_BCK	DIO	5					
CMDAT0	AF1	GPIO68	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMDAT0	DI	1					
		TDM_RX_LRCK	DO	4					
		I2S0_LRCK	DIO	5					
CMDAT1	AF2	GPIO69	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMDAT1	DI	1					
		TDM_RX_MCK	DO	4					
		I2S0_MCK	DO	5					
CMDAT2	AG2	GPIO70	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMDAT2	DI	1					
		TDM_RX_DI	DI	4					
		I2S0_DI	DI	5					
CMDAT3	AH2	GPIO71	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMDAT3	DI	1					
CMDAT4	AF3	GPIO72	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMDAT4	DI	1					
		I2S3_BCK	DO	5					

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CMDAT5	AG3	GPIO73	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMDAT5	DI	1					
		I2S3_LRCK	DO	5					
CMDAT6	AH3	GPIO74	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMDAT6	DI	1					
		I2S3_MCK	DO	5					
CMDAT7	AJ2	GPIO75	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMDAT7	DI	1					
		I2S3_DO	DO	5					
CMDAT8	AH1	GPIO76	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMDAT8	DI	1					
		PCM_CLK	DIO	5					
CMDAT9	AJ3	GPIO77	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMDAT9	DI	1					
		PCM_SYNC	DIO	5					
CMHSYNC	AF4	GPIO78	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMHSYNC	DI	1					
		PCM_RX	DI	5					
CMVSYNC	AG4	GPIO79	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CMVSYNC	DI	1					
		PCM_TX	DO	5					
MSDC2_CMD	AE13	GPIO80	DIO	0	0	GPIO18	DVDD18_MSDC2	PU	I
		MSDC2_CMD	DIO	1					
		TDM_TX_LRCK	DO	2					
		UTXD1	DO	3					
		DPI_D19	DO	4					

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MSDC2_CLK	AC13	GPIO81	DIO	0	0	KP200KIO	DVDD18_MSDC2	PD	I
		MSDC2_CLK	DO	1					
		TDM_TX_BCK	DO	2					
		URXD1	DI	3					
		DPI_D20	DO	4					
MSDC2_DAT0	AF14	GPIO82	DIO	0	0	GPIO18	DVDD18_MSDC2	PU	I
		MSDC2_DAT0	DIO	1					
		TDM_TX_DATA0	DO	2					
		UTXD2	DO	3					
		DPI_D21	DO	4					
MSDC2_DAT1	AF13	GPIO83	DIO	0	0	GPIO18	DVDD18_MSDC2	PU	I
		MSDC2_DAT1	DIO	1					
		TDM_TX_DATA1	DO	2					
		URXD2	DI	3					
		DPI_D22	DO	4					
MSDC2_DAT2	AD13	GPIO84	DIO	0	0	GPIO18	DVDD18_MSDC2	PU	I
		MSDC2_DAT2	DIO	1					
		TDM_TX_DATA2	DO	2					
		PWM_A	DO	3					
		DPI_D23	DO	4					
MSDC2_DAT3	AF12	GPIO85	DIO	0	0	GPIO18	DVDD18_MSDC2	PU	I
		MSDC2_DAT3	DIO	1					
		TDM_TX_DATA3	DO	2					
		PWM_B	DO	3					
		EXT_FRAME_SYNC	DI	5					
MSDC2_DSL	AE14	GPIO86	DIO	0	0	GPIO18	DVDD18_MSDC2	PD	I
		MSDC2_DSL	DI	1					
		TDM_TX_MCK	DO	2					
		PWM_C	DO	3					

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MSDC1_CMD	M6	GPIO87	DIO	0	1	GPIO18	DVDD28_MSDC1	PU	I
		MSDC1_CMD	DIO	1					
MSDC1_CLK	M3	GPIO88	DIO	0	1	GPIO18	DVDD28_MSDC1	PD	OL
		MSDC1_CLK	DO	1					
MSDC1_DAT0	L3	GPIO89	DIO	0	1	I2C18IO	DVDD28_MSDC1	PU	I
		MSDC1_DAT0	DIO	1					
		PWM_C	DO	2					
MSDC1_DAT1	L2	GPIO90	DIO	0	1	I2C18IO	DVDD28_MSDC1	PU	I
		MSDC1_DAT1	DIO	1					
		SPDIF_IN	DI	2					
MSDC1_DAT2	M4	GPIO91	DIO	0	1	I2C18IO	DVDD28_MSDC1	PU	I
		MSDC1_DAT2	DIO	1					
		SPDIF_OUT	DO	2					
MSDC1_DAT3	M5	GPIO92	DIO	0	1	GPIO18	DVDD28_MSDC1	PU	I
		MSDC1_DAT3	DIO	1					
		IRRX	DI	2					
		PWM_A	DO	3					
MSDC0_DAT7	P30	GPIO93	DIO	0	1	GPIO18	DVDD18_MSDC0	PU	I
		MSDC0_DAT7	DIO	1					
		NLD7	DIO	2					
MSDC0_DAT6	N30	GPIO94	DIO	0	1	GPIO18	DVDD18_MSDC0	PU	I
		MSDC0_DAT6	DIO	1					
		NLD6	DIO	2					
MSDC0_DAT5	L30	GPIO95	DIO	0	1	GPIO18	DVDD18_MSDC0	PU	I
		MSDC0_DAT5	DIO	1					
		NLD4	DIO	2					
MSDC0_DAT4	N29	GPIO96	DIO	0	1	MSDC0IO	DVDD18_MSDC0	PU	I
		MSDC0_DAT4	DIO	1					
		NLD3	DIO	2					

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MSDC0_RSTB	M27	GPIO97	DIO	0	1	MSDC0IO	DVDD18_MSDC0	PU	OH
		MSDC0_RSTB	DO	1					
		NLD0	DIO	2					
MSDC0_CMD	M26	GPIO98	DIO	0	1	MSDC0IO	DVDD18_MSDC0	PU	I
		MSDC0_CMD	DIO	1					
		NALE	DO	2					
MSDC0_CLK	M28	GPIO99	DIO	0	1	MSDC1IO	DVDD18_MSDC0	PD	OL
		MSDC0_CLK	DO	1					
		NWEB	DO	2					
MSDC0_DAT3	L27	GPIO100	DIO	0	1	MSDC1IO	DVDD18_MSDC0	PU	I
		MSDC0_DAT3	DIO	1					
		NLD1	DIO	2					
MSDC0_DAT2	L29	GPIO101	DIO	0	1	MSDC0IO	DVDD18_MSDC0	PU	I
		MSDC0_DAT2	DIO	1					
		NLD5	DIO	2					
MSDC0_DAT1	M29	GPIO102	DIO	0	1	MSDC0IO	DVDD18_MSDC0	PU	I
		MSDC0_DAT1	DIO	1					
		NDQS	DIO	2					
MSDC0_DAT0	L28	GPIO103	DIO	0	1	MSDC0IO	DVDD18_MSDC0	PU	I
		MSDC0_DAT0	DIO	1					
		NLD2	DIO	2					
MSDC0_DSL	N26	GPIO104	DIO	0	1	MSDC0IO	DVDD18_MSDC0	PD	I
		MSDC0_DSL	DI	1					
NCLE	P29	GPIO105	DIO	0	1	MSDC0IO	DVDD18_MSDC0	PD	OL
		NCLE	DO	1					
		TDM_RX_MCK	DO	2					
NCEB1	P27	GPIO106	DIO	0	1	MSDC0IO	DVDD18_MSDC0	PU	OH
		NCEB1	DO	1					
		TDM_RX_BCK	DO	2					

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NCEB0	P28	GPIO107	DIO	0	1	GPIO18	DVDD18_MSDC0	PU	OH
		NCEB0	DO	1					
		TDM_RX_LRCK	DO	2					
NREB	R28	GPIO108	DIO	0	1	GPIO18	DVDD18_MSDC0	PU	OH
		NREB	DO	1					
		TDM_RX_DI	DI	2					
NRNB	R27	GPIO109	DIO	0	1	GPIO18	DVDD18_MSDC0	PU	I
		NRNB	DI	1					
PCM_CLK	AB13	GPIO110	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		PCM_CLK	DIO	1					
		I2S0_BCK	DIO	2					
		I2S3_BCK	DO	3					
		SPDIF_IN	DI	4					
		DPI_D15	DO	5					
PCM_SYNC	AB14	GPIO111	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		PCM_SYNC	DIO	1					
		I2S0_LRCK	DIO	2					
		I2S3_LRCK	DO	3					
		SPDIF_OUT	DO	4					
		DPI_D16	DO	5					
PCM_RX	AD14	GPIO112	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		PCM_RX	DI	1					
		I2S0_DI	DI	2					
		I2S3_MCK	DO	3					
		IRRX	DI	4					
		DPI_D17	DO	5					

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PCM_TX	AC14	GPIO113	DIO	0	0	GPIO18	DVDD18_IO0	PD	I
		PCM_TX	DO	1					
		I2S0_MCK	DO	2					
		I2S3_DO	DO	3					
		PWM_B	DO	4					
		DPI_D18	DO	5					
I2S_DATA_IN	AJ29	GPIO114	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		I2S0_DI	DI	1					
		I2S1_DO	DO	2					
		I2S2_DI	DI	3					
		I2S3_DO	DO	4					
		PWM_A	DO	5					
		SPDIF_IN	DI	6					
I2S_LRCK	AJ28	GPIO115	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		I2S0_LRCK	DIO	1					
		I2S1_LRCK	DO	2					
		I2S2_LRCK	DO	3					
		I2S3_LRCK	DO	4					
		PWM_B	DO	5					
		SPDIF_OUT	DO	6					
I2S_BCK	AJ27	GPIO116	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		I2S0_BCK	DIO	1					
		I2S1_BCK	DO	2					
		I2S2_BCK	DO	3					
		I2S3_BCK	DO	4					
		PWM_C	DO	5					
		IRRX	DI	6					
DMIC0_CLK	AD29	GPIO117	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		DMIC0_CLK	DO	1					
		I2S2_BCK	DO	2					

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DMIC0_DAT0	AC29	GPIO118	DIO	0	0	KP2KIO	DVDD18_IO1	PD	I
		DMIC0_DAT0	DI	1					
		I2S2_DI	DI	2					
DMIC0_DAT1	AE30	GPIO119	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		DMIC0_DAT1	DI	1					
		I2S2_LRCK	DO	2					
DMIC1_CLK	AE29	GPIO120	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		DMIC1_CLK	DO	1					
		I2S2_MCK	DO	2					
DMIC1_DAT0	AF30	GPIO121	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		DMIC1_DAT0	DI	1					
		I2S1_BCK	DO	2					
DMIC1_DAT1	AF28	GPIO122	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		DMIC1_DAT1	DI	1					
		I2S1_LRCK	DO	2					
DMIC2_CLK	AF29	GPIO123	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		DMIC2_CLK	DO	1					
		I2S1_MCK	DO	2					
DMIC2_DAT0	AH29	GPIO124	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		DMIC2_DAT0	DI	1					
		I2S1_DO	DO	2					
DMIC2_DAT1	AG29	GPIO125	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		DMIC2_DAT1	DI	1					
		TDM_RX_BCK	DO	2					
DMIC3_CLK	AH28	GPIO126	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		DMIC3_CLK	DO	1					
		TDM_RX_LRCK	DO	2					
DMIC3_DAT0	AG27	GPIO127	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		DMIC3_DAT0	DI	1					
		TDM_RX_DI	DI	2					

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DMIC3_DAT1	AG28	GPIO128	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		DMIC3_DAT1	DI	1					
		TDM_RX_MCK	DO	2					
		VAD_CLK	DI	3					
TDM_TX_BCK	AF26	GPIO129	DIO	0	0	I2C18IO	DVDD18_IO1	PD	I
		TDM_TX_BCK	DO	1					
		I2S3_BCK	DO	2					
TDM_TX_LRCK	AF27	GPIO130	DIO	0	0	I2C18IO	DVDD18_IO1	PD	I
		TDM_TX_LRCK	DO	1					
		I2S3_LRCK	DO	2					
TDM_TX_MCK	AJ25	GPIO131	DIO	0	0	I2C18IO	DVDD18_IO1	PD	I
		TDM_TX_MCK	DO	1					
		I2S3_MCK	DO	2					
TDM_TX_DATA0	AH25	GPIO132	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		TDM_TX_DATA0	DO	1					
		I2S3_DO	DO	2					
TDM_TX_DATA1	AG25	GPIO133	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		TDM_TX_DATA1	DO	1					
TDM_TX_DATA2	AE25	GPIO134	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		TDM_TX_DATA2	DO	1					
TDM_TX_DATA3	AF25	GPIO135	DIO	0	0	GPIO18	DVDD18_IO1	PD	I
		TDM_TX_DATA3	DO	1					
CONN_TOP_CLK	AE9	GPIO136	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CONN_TOP_CLK	DO	1					
CONN_TOP_DATA	AD9	GPIO137	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CONN_TOP_DATA	DIO	1					
CONN_HRST_B	AC9	GPIO138	DIO	0	0	GPIO18	DVDD18_IO3	PD	I
		CONN_HRST_B	DO	1					

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Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
CONN_WB_PTA	AB9	GPIO139	DIO	0	0	MSDC0IO	DVDD18_IO3	PD	I
		CONN_WB_PTA	DIO	1					
CONN_BT_CLK	AD8	GPIO140	DIO	0	0	MSDC0IO	DVDD18_IO3	PD	I
		CONN_BT_CLK	DIO	1					
CONN_BT_DATA	AC8	GPIO141	DIO	0	0	MSDC0IO	DVDD18_IO3	PD	I
		CONN_BT_DATA	DIO	1					
CONN_WF_CTRL0	AE8	GPIO142	DIO	0	0	MSDC1IO	DVDD18_IO3	PD	I
		CONN_WF_CTRL0	DIO	1					
CONN_WF_CTRL1	AF7	GPIO143	DIO	0	0	MSDC1IO	DVDD18_IO3	PD	I
		CONN_WF_CTRL1	DIO	1					
CONN_WF_CTRL2	AB8	GPIO144	DIO	0	0	MSDC1IO	DVDD18_IO3	PD	I
		CONN_WF_CTRL2	DIO	1					
EMI0_CK_C	D8	EMI0_CK_C	AIO			DDRIO	AVDDQ_EMI0		
EMI0_CK_T	E8	EMI0_CK_T	AIO			DDRIO	AVDDQ_EMI0		
EMI0_CKE0	K14	EMI0_CKE0	AIO			DDRIO	AVDD2_EMI		
EMI0_CKE1	J14	EMI0_CKE1	AIO			DDRIO	AVDD2_EMI		
EMI0_CS0_N	G9	EMI0_CS0_N	AIO			DDRIO	AVDDQ_EMI0		
EMI0_CS1_N	F9	EMI0_CS1_N	AIO			DDRIO	AVDDQ_EMI0		
EMI0_CAS_N	J9	EMI0_CAS_N	AIO			DDRIO	AVDDQ_EMI0		
EMI0_RAS_N	H9	EMI0_RAS_N	AIO			DDRIO	AVDDQ_EMI0		
EMI0_WE_N	H14	EMI0_WE_N	AIO			DDRIO	AVDDQ_EMI0		
EMI0_ODT	G12	EMI0_ODT	AIO			DDRIO	AVDDQ_EMI0		
EMI0_ACT_N	F12	EMI0_ACT_N	AIO			DDRIO	AVDDQ_EMI0		
EMI0_BG0	G14	EMI0_BG0	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A0	C14	EMI0_A0	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A1	G6	EMI0_A1	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A2	F3	EMI0_A2	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A3	J6	EMI0_A3	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A4	J12	EMI0_A4	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A5	F6	EMI0_A5	AIO			DDRIO	AVDDQ_EMI0		

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Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
EMI0_A6	D14	EMI0_A6	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A7	E6	EMI0_A7	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A8	G3	EMI0_A8	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A9	D3	EMI0_A9	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A10	E12	EMI0_A10	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A11	H3	EMI0_A11	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A12	H12	EMI0_A12	AIO			DDRIO	AVDDQ_EMI0		
EMI0_A13	C3	EMI0_A13	AIO			DDRIO	AVDDQ_EMI0		
EMI0_BA0	K12	EMI0_BA0	AIO			DDRIO	AVDDQ_EMI0		
EMI0_BA1	K6	EMI0_BA1	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DM0	B1	EMI0_DM0	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DM1	C10	EMI0_DM1	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQS0_C	C7	EMI0_DQS0_C	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQS0_T	C6	EMI0_DQS0_T	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQS1_C	C2	EMI0_DQS1_C	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQS1_T	D2	EMI0_DQS1_T	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ0	C11	EMI0_DQ0	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ1	A2	EMI0_DQ1	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ2	B12	EMI0_DQ2	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ3	B4	EMI0_DQ3	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ4	B11	EMI0_DQ4	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ5	B3	EMI0_DQ5	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ6	B13	EMI0_DQ6	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ7	B5	EMI0_DQ7	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ8	B7	EMI0_DQ8	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ9	E1	EMI0_DQ9	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ10	B8	EMI0_DQ10	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ11	F2	EMI0_DQ11	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ12	B9	EMI0_DQ12	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ13	G2	EMI0_DQ13	AIO			DDRIO	AVDDQ_EMI0		

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Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
EMI0_DQ14	C9	EMI0_DQ14	AIO			DDRIO	AVDDQ_EMI0		
EMI0_DQ15	H2	EMI0_DQ15	AIO			DDRIO	AVDDQ_EMI0		
EMI1_CK_C	K18	EMI1_CK_C	AIO			DDRIO	AVDDQ_EMI0		
EMI1_CK_T	J18	EMI1_CK_T	AIO			DDRIO	AVDDQ_EMI0		
EMI1_CKE0	D24	EMI1_CKE0	AIO			DDRIO	AVDD2_EMI		
EMI1_CKE1	C24	EMI1_CKE1	AIO			DDRIO	AVDD2_EMI		
EMI1_CS0_N	F18	EMI1_CS0_N	AIO			DDRIO	AVDDQ_EMI0		
EMI1_CS1_N	G18	EMI1_CS1_N	AIO			DDRIO	AVDDQ_EMI0		
EMI1_CAS_N	E18	EMI1_CAS_N	AIO			DDRIO	AVDDQ_EMI0		
EMI1_RAS_N	C20	EMI1_RAS_N	AIO			DDRIO	AVDDQ_EMI0		
EMI1_WE_N	C28	EMI1_WE_N	AIO			DDRIO	AVDDQ_EMI0		
EMI1_ODT	G24	EMI1_ODT	AIO			DDRIO	AVDDQ_EMI0		
EMI1_ACT_N	H24	EMI1_ACT_N	AIO			DDRIO	AVDDQ_EMI0		
EMI1_BG0	D28	EMI1_BG0	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A0	J28	EMI1_A0	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A1	H20	EMI1_A1	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A2	B16	EMI1_A2	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A3	G20	EMI1_A3	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A4	F24	EMI1_A4	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A5	J20	EMI1_A5	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A6	H28	EMI1_A6	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A7	D18	EMI1_A7	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A8	B15	EMI1_A8	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A9	C17	EMI1_A9	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A10	J24	EMI1_A10	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A11	A14	EMI1_A11	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A12	D20	EMI1_A12	AIO			DDRIO	AVDDQ_EMI0		
EMI1_A13	C18	EMI1_A13	AIO			DDRIO	AVDDQ_EMI0		
EMI1_BA0	E24	EMI1_BA0	AIO			DDRIO	AVDDQ_EMI0		
EMI1_BA1	E20	EMI1_BA1	AIO			DDRIO	AVDDQ_EMI0		

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Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
EMI1_DM0	A24	EMI1_DM0	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DM1	E29	EMI1_DM1	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQS0_C	B29	EMI1_DQS0_C	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQS0_T	B28	EMI1_DQS0_T	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQS1_C	B23	EMI1_DQS1_C	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQS1_T	B22	EMI1_DQS1_T	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ0	E30	EMI1_DQ0	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ1	B24	EMI1_DQ1	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ2	G29	EMI1_DQ2	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ3	A26	EMI1_DQ3	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ4	F29	EMI1_DQ4	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ5	B25	EMI1_DQ5	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ6	H29	EMI1_DQ6	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ7	A27	EMI1_DQ7	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ8	A29	EMI1_DQ8	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ9	A21	EMI1_DQ9	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ10	B30	EMI1_DQ10	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ11	B20	EMI1_DQ11	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ12	C30	EMI1_DQ12	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ13	B19	EMI1_DQ13	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ14	D29	EMI1_DQ14	AIO			DDRIO	AVDDQ_EMI0		
EMI1_DQ15	B18	EMI1_DQ15	AIO			DDRIO	AVDDQ_EMI0		
EMI_RESET_N	F14	EMI_RESET_N	AIO			DDRIO	AVDD2_EMI		
EMI_EXTR	J1	EMI_EXTR	AIO			DDRIO	AVDDQ_EMI0		
EMI_TN	G28	EMI_TN	AIO			DDRIO	AVDD18_RDDR		
EMI_TP	F28	EMI_TP	AIO			DDRIO	AVDD18_RDDR		
DSI_D3N	AC2	DSI_D3N	AIO				AVDD18_DSI		
DSI_D3P	AC3	DSI_D3P	AIO				AVDD18_DSI		
DSI_D2N	Y6	DSI_D2N	AIO				AVDD18_DSI		
DSI_D2P	W6	DSI_D2P	AIO				AVDD18_DSI		

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Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
DSI_CKN	Y3	DSI_CKN	AIO				AVDD18_DSI		
DSI_CKP	AA3	DSI_CKP	AIO				AVDD18_DSI		
DSI_D1N	AA2	DSI_D1N	AIO				AVDD18_DSI		
DSI_D1P	AB2	DSI_D1P	AIO				AVDD18_DSI		
DSI_D0N	W4	DSI_D0N	AIO				AVDD18_DSI		
DSI_D0P	W5	DSI_D0P	AIO				AVDD18_DSI		
CSI1A_L0N	U5	CSI1A_L0N	AIO				AVDD12_CSI1		
CSI1A_L0P	U6	CSI1A_L0P	AIO				AVDD12_CSI1		
CSI1A_L1N	T3	CSI1A_L1N	AIO				AVDD12_CSI1		
CSI1A_L1P	T4	CSI1A_L1P	AIO				AVDD12_CSI1		
CSI1A_L2N	R6	CSI1A_L2N	AIO				AVDD12_CSI1		
CSI1A_L2P	R7	CSI1A_L2P	AIO				AVDD12_CSI1		
CSI1B_L0N	W1	CSI1B_L0N	AIO				AVDD12_CSI1		
CSI1B_L0P	W2	CSI1B_L0P	AIO				AVDD12_CSI1		
CSI1B_L1N	V2	CSI1B_L1N	AIO				AVDD12_CSI1		
CSI1B_L1P	U2	CSI1B_L1P	AIO				AVDD12_CSI1		
CSI0A_L0N	R3	CSI0A_L0N	AIO				AVDD12_CSI0		
CSI0A_L0P	R4	CSI0A_L0P	AIO				AVDD12_CSI0		
CSI0A_L1N	P4	CSI0A_L1N	AIO				AVDD12_CSI0		
CSI0A_L1P	P5	CSI0A_L1P	AIO				AVDD12_CSI0		
CSI0A_L2N	P6	CSI0A_L2N	AIO				AVDD12_CSI0		
CSI0A_L2P	P7	CSI0A_L2P	AIO				AVDD12_CSI0		
CSI0B_L0N	U1	CSI0B_L0N	AIO				AVDD12_CSI0		
CSI0B_L0P	T1	CSI0B_L0P	AIO				AVDD12_CSI0		
CSI0B_L1N	T2	CSI0B_L1N	AIO				AVDD12_CSI0		
CSI0B_L1P	R2	CSI0B_L1P	AIO				AVDD12_CSI0		
CSI0B_L2N	P2	CSI0B_L2N	AIO				AVDD12_CSI0		
CSI0B_L2P	P1	CSI0B_L2P	AIO				AVDD12_CSI0		
USB_DP_P0	T30	USB_DP_P0	AIO				AVDD33_USB		
USB_DM_P0	T29	USB_DM_P0	AIO				AVDD33_USB		

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Ball Name	Ball Location	Signal Name	Signal Type	Aux. Function	Reset Function	Buffer Type	Power Domain	PU/PD Reset	IO Reset
CHD_DP_P0	R25	CHD_DP_P0	AIO				AVDD33_USB		
CHD_DM_P0	R26	CHD_DM_P0	AIO				AVDD33_USB		
USB_VBUS_P0	V30	USB_VBUS_P0	AI				AVDD18_USB_P0		
USB_DP_P1	T26	USB_DP_P1	AIO				AVDD33_USB		
USB_DM_P1	T25	USB_DM_P1	AIO				AVDD33_USB		
XIN_WBG	Y13	XIN_WBG	AIO				AVDD18_WBG		
GPS_Q	AH12	GPS_Q	AIO				AVDD18_WBG		
GPS_I	AJ11	GPS_I	AIO				AVDD18_WBG		
BT_QN	AH11	BT_QN	AIO				AVDD18_WBG		
BT_QP	AH10	BT_QP	AIO				AVDD18_WBG		
BT_IN	AH9	BT_IN	AIO				AVDD18_WBG		
BT_IP	AJ9	BT_IP	AIO				AVDD18_WBG		
WF_QN	AH8	WF_QN	AIO				AVDD18_WBG		
WF_QP	AH7	WF_QP	AIO				AVDD18_WBG		
WF_IN	AJ7	WF_IN	AIO				AVDD18_WBG		
WF_IP	AJ6	WF_IP	AIO				AVDD18_WBG		
REFP	AD19	REFP	AIO				AVDD18_AP		
AUXIN0	W18	AUXIN0	AIO				AVDD18_AP		
AUXIN1	Y18	AUXIN1	AIO				AVDD18_AP		
AUXIN2	AA18	AUXIN2	AIO				AVDD18_AP		
AUXIN3	AB18	AUXIN3	AIO				AVDD18_AP		
AUXIN4	AC18	AUXIN4	AIO				AVDD18_AP		
AUXIN5	AD18	AUXIN5	AIO				AVDD18_AP		
26M_CLKSQ	AC20	26M_CLKSQ	AIO				AVDD18_PLLGP		
SYSRSTB	AC30	SYSRSTB	DI				DVDD18_IO0		
TESTMODE	W25	TESTMODE	DI				DVDD18_IO0		

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4.3 Power Rails

Table 4-6 lists the device power rails.

Table 4-6 Power Rails

Ball Name	Ball Location	Type	Description
AVDD04_DSI	AB1	P	Analog power for DSI
AVDD12_CSI0	N1	P	Analog power input 1.2 V for CSI0
AVDD12_CSI1	N2	P	Analog power input 1.2 V for DSI1
AVDD12_DSI	AC1	P	Analog power input 1.2 V for DSI
AVDD12_PLLGP	AJ21	P	Analog power input 1.2 V for PLL and oscillator
AVDD12_USB	W30	P	Analog power 1.2 V for USB
AVDD12_WBG	AH6	P	Analog power 1.2 V for wireless connectivity
AVDD18_AP	AH20	P	Analog power input 1.8 V for AUXADC and internal Temperature Sensor (TSENSE)
AVDD18_CSI	Y1	P	Analog power input 1.8 V for CSI
AVDD18_DSI	AD1	P	Analog power input 1.8 V for DSI
AVDD18_RDDR	M7	P	Analog power input 1.8 V for DDR
AVDD18_USB_P0	U29	P	Analog power 1.8 V for USB port0
AVDD18_USB_P1	V29	P	Analog power 1.8 V for USB port1
AVDD18_WBG	AJ13	P	Analog power 1.8 V for wireless connectivity
AVDD2_EMI	N13, N15, N17, N19	P	Analog power input for 1.1/1.2/1.5 V DDR
AVDDQ_EMI0	M9, M11, M21, M23	P	Analog power input for 0.6/1.1/1.2/1.5 V EMI
DVDD_DVFS	V20, Y20, AA20, U21, Y21, AA21, AA22, U23, Y23, AA23, U24, V24, W24, Y24, V25, V27, U28	P	Digital power input for processor
DVDD_MCUSYS_ SRAM	V19	P	Digital power input for processor SRAM
DVDD_SRAM	T9, U19	P	Digital power input for core SRAM
DVDD_TOP	V8, P9, U9, V10, P11, U11, V11, V12, P13, U13, V13, U14, V14, P15, V15, U17, P18, V18, P19, P21, P22, U16, V16, P17	P	Digital power input for core
DVDD_VQPS(1)	AB22	P	eFuse blowing power control
DVDD18_MSDC0	J30	P	Digital power input for 1.8 V MSDC0/NAND flash IO
DVDD18_MSDC2	AG13	P	Digital power input for 1.8 V MSDC IO
AVDD18_PLLGP	AJ22	P	Analog power input 1.8 V for PLL and oscillator
AVDD33_USB	W28	P	Analog power 3.3 V for USB
DVDD18_IO0	AH30	P	Digital power input for IO
DVDD18_IO1	AB21	P	Digital power input for IO
DVDD18_IO3	AE2	P	Digital power input for IO
DVDD28_MSDC1	L1	P	Digital power input for 1.8/2.8/3.0 V MSDC IO

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Ball Name	Ball Location	Type	Description
DVSS	A1, D1, F1, H1, B2, E2, J2, Y2, AD2, A3, J3, P3, U3, W3, AB3, C4, D4, E4, F4, G4, H4, J4, Y4, A5, C5, D5, E5, F5, G5, H5, J5, K5, T5, Y5, H6, AB6, AD6, AG6, A7, D7, E7, G7, AA7, AC7, AE7, AG7, C8, J8, K8, Y8, AG8, A9, E9, K9, L9, W9, Y9, AA9, AF9, AG9, D10, F10, H10, K10, L10, R10, T10, Y10, AA10, AB10, AE10, AF10, AG10, A11, D11, E11, F11, K11, L11, R11, W11, AA11, AB11, AC11, AD11, AE11, AF11, AG11, D12, L12, R12, T12, W12, Y12, AB12, AC12, AD12, AE12, AG12, A13, C13, D13, E13, F13, G13, J13, K13, L13, R13, W13, AA13, AH13, E14, R14, T14, Y14, AA14, C15, D15, E15, F15, G15, H15, J15, K15, L15, R15, W15, Y15, AA15, AB15, AC15, A16, C16, D16, E16, F16, G16, H16, J16, K16, L16, R16, T16, W16, Y16, AA16, AB16, AC16, AD16, D17, E17, F17, G17, H17, J17, K17, L17, R17, W17, AA17, AB17, AC17, AD17, A18, H18, L18, R18, T18, AE18, C19, D19, E19, F19, G19, H19, J19, K19, L19, R19, A20, F20, K20, L20, R20, AD20, B21, C21, D21, G21, H21, J21, K21, L21, R21, AC21, C22, D22, F22, J22, K22, L22, T22, U22, V22, W22, Y22, AD22, A23, C23, D23, J23, K23, L23, R23, K24, F25, G25, H25, J25, K25, AB25, AC25, AD25, B26, C26, G26, H26, K26, P26, AC26, AD26, AE26, B27, C27, E27, J27, AE27, E28, T28, V28, AA28, C29, J29, A30, F30, H30	G	Ground

1. eFuse programming mode should be supplied with 1.8 V. Connect a 1-µF bypass capacitor to this pin and GND, as close

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as possible to the device.

4.4 Reserved and Unused Pin Handling Recommendations

Table 4-7 provides specific ball handling recommendations for the case when the pins are not used.

Table 4-7 Reserved and Unused Pin Handling Recommendations

Ball Name	Requirement	Ball Location
TESTMODE	Test mode (tie to GND)	W25
DUMMY	Leave unconnected	AJ1, AJ30
AUD_CLK_MOSI, AUD_SYNC_MOSI, AUD_DAT_MOSI0, AUD_DAT_MOSI1, AUXIN1, AUXIN2, AUXIN3, AUXIN4, AUXIN5	These pins should be connected to GND when unused	Y26, AA26, W26, Y27, W18, Y18, AA18, AB18, AC18, AD18

NOTE: All other unused signal balls can be left floating.

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5 Electrical Characteristics

Stresses above the values listed in Table 5-1 may cause permanent damage to the device. The recommended minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies based on characterization results. Exposure to absolute maximum rating conditions may affect device reliability.

The operating conditions in Table 5-2 must not be exceeded in order to ensure correct operation and reliability of the device. All parameters specified in this document refer to these operating conditions, unless noted otherwise.

5.1 Absolute Maximum Ratings

Table 5-1 represents the absolute maximum ratings of the device power pins.

Table 5-1 Absolute Maximum Ratings

Parameter	Conditions	Min	Max	Unit
Digital power input for core	DVDD_TOP	0.76	0.84	V
Digital power input for processor	DVDD_DVFS	0.65 – delta *1	1.025 –delta *1	V
Digital power input for core SRAM	DVDD_SRAM	0.8	0.94	V
Digital power input for processor SRAM	DVDD_MCUSYS_SRAM	0.8	1.025 –delta *1	V
Analog power input	AVDD12_PLLGP, AVDD12_WBG, AVDD12_DSI, AVDD12_CSI0, AVDD12_CSI1, AVDD12_USB	1.14	1.32	V
	AVDD04_DSI	0.495	1.32	V
	AVDD2_EMI	1.06	1.575	V
	AVDDQ_EMI0	0.57	1.575	V
	AVDD18_RDDR	1.7	1.9	V
	AVDD18_PLLGP, AVDD18_AP, AVDD18_DSI, AVDD18_WBG, AVDD18_CSI, AVDD18_USB_P0, AVDD18_USB_P1	1.7	1.98	V
	AVDD33_USB	2.9165	3.2849	V
Digital power input	DVDD_VQPS	0	1.98	V
	DVDD18_IO0, DVDD18_IO1, DVDD18_IO3, DVDD18_MSDC0, DVDD18_MSDC2	-0.3	2.1	V
	DVDD28_MSDC1	-0.3	3.3	V
Storage temperature		-65	150	°C

*1 PTPOD is applied in DVDD_DVFS & DVDD_MCUSYS_SRAM power domains. Real voltage values are derived from PTPOD controller.

5.1.1 Storage Conditions

Table 5-2 defines specifics for the storage conditions.

Table 5-2 Storage Conditions

Parameter		Min	Max	Unit
Shelf life in sealed bag	40 °C / 90% RH		24	months
After bag opened(1)				
Mounted	30 °C / 60% RH		168	h
Stored			20	% RH
Baking(2)				
Low temperature device containers	40 °C +5 °C/-0 °C and < 5% RH	192		h

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Parameter		Min	Max	Unit
High temperature device containers	125 °C +5 °C/-0 °C	24		h

1. For devices subjected to infrared reflow, vapor-phase reflow, or equivalent processing.
2. Devices require baking before mounting, if humidity Indicator card is above 20% when read at 23 °C ± 5 °C or Mounted/Stored conditions are not met.

5.2 Recommended Operating Conditions

Table 5-3 represents the recommended operating conditions of the device power pins.

Table 5-3 Recommended Operating Conditions

Pin Name	Description	Mode	Min	Typ	Max	Unit
AVDD12_PLLGP	Analog power input for PLL	1.2 V	1.14	1.2	1.26	V
AVDD18_PLLGP		1.8 V	1.7	1.8	1.9	V
AVDD18_AP	Analog power input for AUXADC and TSENSE	1.8 V	1.7	1.8	1.9	V
AVDD18_RDDR	Analog power input for DDR	1.8 V	1.7	1.8	1.9	V
AVDD2_EMI	Analog power input for DDR	LPDDR3	1.14	1.2	1.3	V
		LPDDR4	1.06	1.1	1.17	
		LPDDR4X	1.06	1.1	1.17	
		DDR3	1.425	1.5	1.575	
		DDR3L	1.283	1.35	1.45	
		DDR4	1.14	1.2	1.26	
AVDDQ_EMI0	Analog power input for EMI	LPDDR3	1.14	1.2	1.3	V
		LPDDR4	1.06	1.1	1.17	
		LPDDR4X	0.57	0.6	0.65	
		DDR3	1.425	1.5	1.575	
		DDR3L	1.283	1.35	1.45	
		DDR4	1.14	1.2	1.26	
AVDD12_WBG	Analog power for wireless connectivity	1.2 V	1.14	1.2	1.26	V
AVDD18_WBG		1.8 V	1.7	1.8	1.9	V
AVDD04_DSI	Analog power for DSI	0.8V	0.495	0.8	0.88	V
AVDD12_DSI		1.2 V	1.14	1.2	1.26	V
AVDD18_DSI		1.8 V	1.7	1.8	1.9	V
AVDD12_CSI0	Analog power for CSI	1.2 V	1.14	1.2	1.26	V
AVDD12_CSI1		1.2 V	1.14	1.2	1.26	V
AVDD18_CSI		1.8 V	1.7	1.8	1.9	V
AVDD12_USB	Analog power for USB	1.2 V	1.14	1.2	1.26	V
AVDD18_USB_P0		1.8 V	1.7	1.8	1.9	V
AVDD18_USB_P1		1.8 V	1.7	1.8	1.9	V
AVDD33_USB		3.07 V	2.9165	3.07	3.2235	V
DVDD_VQPS	Digital power input for eFuse IO		1.7	1.8	1.9	V
DVDD18_IO0	Digital power input for IO		1.7	1.8	1.9	V
DVDD18_IO1			1.7	1.8	1.9	V
DVDD18_IO3			1.7	1.8	1.9	V
DVDD18_MSDC0	Digital power input for EMMC/NAND flash IO		1.7	1.8	1.9	V
DVDD28_MSDC1	Digital power input for MSDC1 IO	GPIO / SD3.0	1.7	1.8	1.9	V
		SD2.0	2.85	3	3.15	V

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Pin Name	Description	Mode	Min	Typ	Max	Unit
DVDD18_MSDC2	Digital power input for MSDC2 IO		1.7	1.8	1.9	V
DVDD_TOP	Digital power input for core (0.6 V is VAD suspend mode) (0.55 V is suspend mode)		0.76	0.8	0.84	V
			0.665	0.7	0.735	V
			0.618	0.65	0.682	V
			0.57	0.6	0.63	V
			0.523	0.55	0.577	V
DVDD_DVFS	Digital power input for processor		0.65 - Δ(1)	0.8 - Δ(1)	1.025 - Δ(1)	V
DVDD_SRAM	Digital power input for core SRAM	Operation mode	0.8	0.9	0.94	V
		Retention mode	0.56	N/A	N/A	V
DVDD_MCUSYS_SRAM	Digital power input for processor SRAM	Operation mode	0.8	0.9 - Δ(1)	1.05 - Δ(1)	V
		Retention mode	0.6	N/A	N/A	V
Operating junction temperature			-20		105	°C

1. Performance Thermal Power Over Drive (PTPOD) is applied in DVDD_DVFS and DVDD_MCUSYS_SRAM power domains. Real voltage values are derived from PTPOD controller.

5.3 DC Electrical Specifications

This section provides DC electrical characteristics per buffer type.

5.3.1 GPIO18 DC Specifications

Table 5-4 shows GPIO18 DC buffer electrical characteristics.

Table 5-4 GPIO18 DC Specifications

Parameter		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO(1)	V
R_{PU}	Input pull-up resistance	40	75	190	kΩ
R_{PD}	Input pull-down resistance	40	75	190	kΩ
OUTPUT					
$V_{OH(DC)}$	DC output logic high voltage	0.75 × VDDIO(1)			V
$V_{OL(DC)}$	DC output logic low voltage			0.25 × VDDIO(1)	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IO0). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, Power Domain column.

5.3.2 KP2KIO DC Specifications

Table 5-5 shows KP2KIO DC buffer electrical characteristics.

Table 5-5 KP2KIO DC Specifications

Parameter		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO(1)		VDDIO(1) + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO(1)	V
R_{PU}	Input pull-up resistance			2	kΩ

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Parameter		Min	Typ	Max	Unit
R_{PD}	Input pull-down resistance			2	kΩ
OUTPUT					
$V_{OH(DC)}$	DC output logic high voltage	0.75 × VDDIO[1]			V
$V_{OL(DC)}$	DC output logic low voltage			0.25 × VDDIO[1]	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IO1). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, Power Domain column.

5.3.3 KP200KIO DC Specifications

Table 5-6 shows KP200KIO DC buffer electrical characteristics.

Table 5-6 KP200KIO DC Specifications

Parameter		Min	Typ	Max	Unit
Operating Voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO[1]		VDDIO[1] + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO[1]	V
R_{PU}	Input pull-up resistance	200			kΩ
R_{PD}	Input pull-down resistance	200			kΩ
OUTPUT					
$V_{OH(DC)}$	DC output logic high voltage	0.75 × VDDIO[1]			V
$V_{OL(DC)}$	DC output logic low voltage			0.25 × VDDIO[1]	V

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IO1). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, Power Domain column.

5.3.4 I2C18IO DC Specifications

Table 5-7 shows I2C18IO DC buffer specifications.

Table 5-7 I2C18IO DC Specifications

Parameter		Min	Typ	Max	Unit
Operating voltage = 1.8 V					
INPUT					
V_{IH}	Input logic high voltage	0.65 × VDDIO[1]		VDDIO[1] + 0.3	V
V_{IL}	Input logic low voltage	-0.3		0.35 × VDDIO[1]	V
R_{PU}	Input pull-up resistance		N/A		kΩ
R_{PD}	Input pull-down resistance	40	75	190	kΩ
OUTPUT					
$V_{OL(DC)}$	DC output logic low voltage			0.2 × VDDIO[1]	V
EXTERNAL Pull-Up Resistance					
R_{EPU}	External pull-up resistance		1		kΩ

1. VDDIO in this table stands for corresponding power supply (i.e. DVDD18_IO1 or DVDD18_IO3). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, Power Domain column.

5.3.5 MSDC0IO DC Specifications

Table 5-8 shows MSDC0IO DC buffer specifications.

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Table 5-8 MSDC0IO DC Specifications

Parameter			Min	Typ	Max	Unit
Operating voltage = 1.8V						
INPUT						
V_{IH}	Input logic high voltage		1.3		2.0	V
V_{IL}	Input logic low voltage		-0.3		0.58	V
R_{PU}	Input pull-up resistance	R_{PU} = 10 kΩ R[1:0] = 0b01	5	7.5	10	kΩ
		R_{PU} = 50 kΩ R[1:0] = 0b10	10	50	100	kΩ
R_{PD}	Input pull-down resistance	R_{PD} = 10 kΩ R[1:0] = 0b01	5	7.5	10	kΩ
		R_{PD} = 50 kΩ R[1:0] = 0b10	10	50	100	kΩ
OUTPUT						
$V_{OH(DC)}$	DC output logic high voltage		1.4			V
$V_{OL(DC)}$	DC output logic low voltage				0.45	V

5.3.6 MSDC1IO DC Specifications

Table 5-9 shows MSDC1IO DC buffer specifications.

Table 5-9 MSDC1IO DC Specifications

Parameter		Mode	Min	Typ	Max	Unit
INPUT						
V_{IH}	Input logic high voltage	SD Card 2.0 VCC3IO = 3 V	0.625 × VCC3IO(1)		VCC3IO(1) + 0.3	V
		SD Card 3.0 VCC3IO = 1.8 V	0.7 × VCC3IO(1)		VCC3IO(1) + 0.3	V
		GPIO VCC3IO = 1.8V	1.27		VCC3IO(1) + 0.3	V
V_{IL}	Input logic low voltage	SD Card 2.0 VCC3IO = 3 V	-0.3		0.25 × VCC3IO(1)	V
		SD Card 3.0 VCC3IO = 1.8 V	-0.3		0.3 × VCC3IO(1)	V
		GPIO VCC3IO = 1.8V	-0.3		0.58	V
R_{PU}	Input pull-up resistance	R_{PU} = 10 kΩ R[1:0] = 0b01	5	7.5	10	kΩ
		R_{PU} = 50 kΩ R[1:0] = 0b10	10	50	100	kΩ
R_{PD}	Input pull-down resistance	R_{PD} = 10 kΩ R[1:0] = 0b01	5	7.5	10	kΩ
		R_{PD} = 50 kΩ R[1:0] = 0b10	10	50	100	kΩ
OUTPUT						
$V_{OH(DC)}$	DC output logic high voltage	SD Card 2.0 VCC3IO = 3 V	0.75 × VCC3IO(1)		VCC3IO(1) + 0.3	V
		SD Card 3.0 VCC3IO = 1.8 V	1.4		VCC3IO(1) + 0.3	V

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Parameter		Mode	Min	Typ	Max	Unit
		GPIO VCC3IO = 1.8V	1.4		VCC3IO[1] + 0.3	V
$V_{OL(DC)}$	DC output logic low voltage	SD Card 2.0 VCC3IO = 3 V	-0.3		0.125 × VCC3IO[1]	V
		SD Card 3.0 VCC3IO = 1.8 V	-0.3		0.45	V
		GPIO VCC3IO = 1.8V	-0.3		0.45	V

1. VCC3IO in this table stands for corresponding power supply (i.e. DVDD28_MSDC1). For more information on the power supply name on the corresponding ball, see Table 4-5 Pin Characteristics, Power Domain column.

5.3.7 DDRIO DC Specifications

The EMI DDR3/L electrical characteristics are compliant with JEDEC Standard—JESD79-3D.
The EMI DDR4 electrical characteristics are compliant with JEDEC Standard—JESD79-4A.
The EMI LPDDR3 electrical characteristics are compliant with JEDEC Standard—JESD209-3C.
The EMI LPDDR4 electrical characteristics are compliant with JEDEC Standard—JESD209-4B.

5.4 Power Management

5.4.1 Power Sequences

This section describes the power-on/power-off sequences required to ensure proper device operation.
Figure 5-1 shows the power-on/power-off sequences.

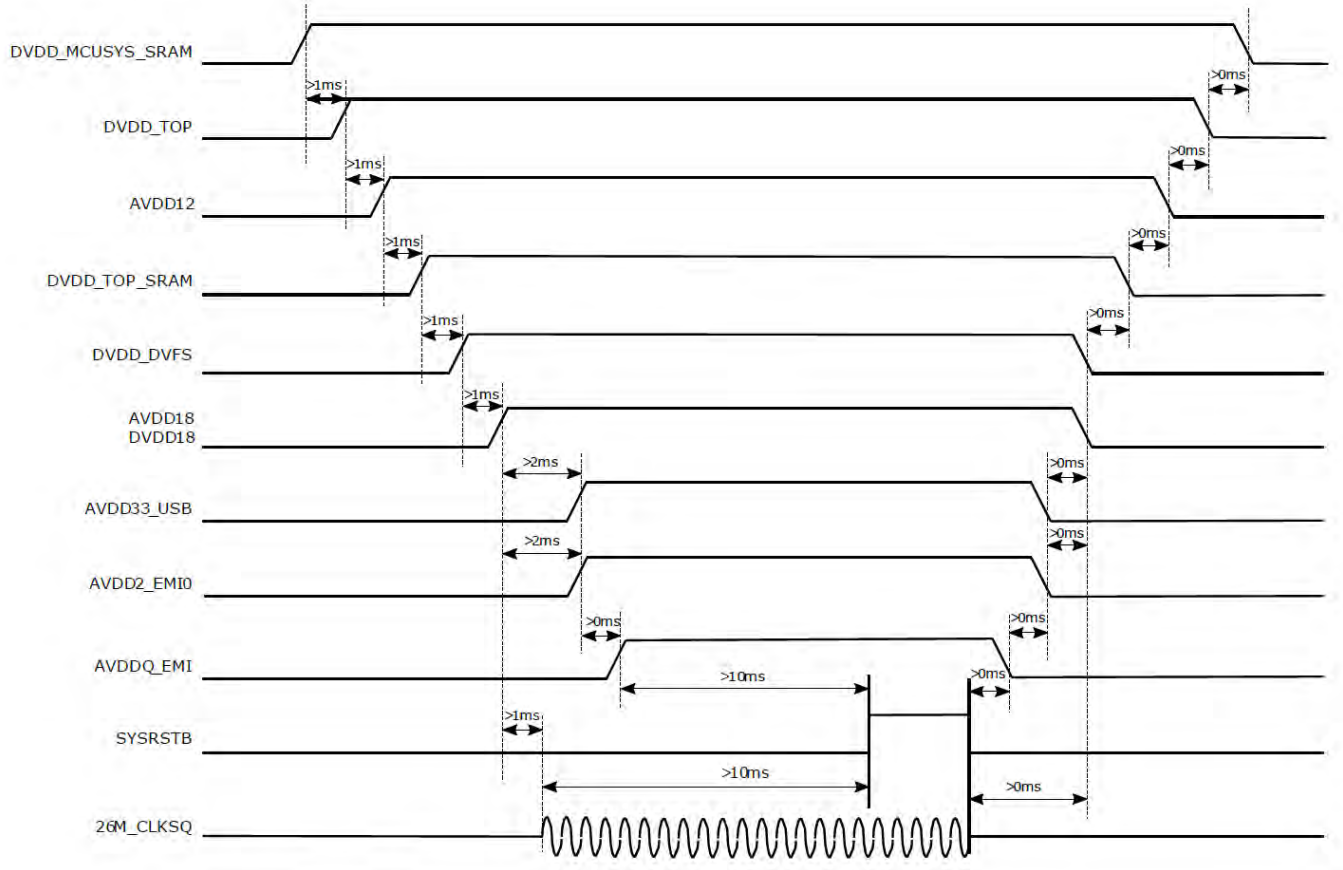

Figure 5-1 Power-on/Power-off Sequence

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5.5 Reset

The TOPRGU generates reset signals and distributes them to each system. A WDT is also included in this module.

The TOPRGU supports the following features:

- Hardware reset signals for the whole chip
- Software controllable reset
- WDT
- Reset output signals for companion chips

Figure 5-2 shows the block diagram of TOPRGU in the MT8365.

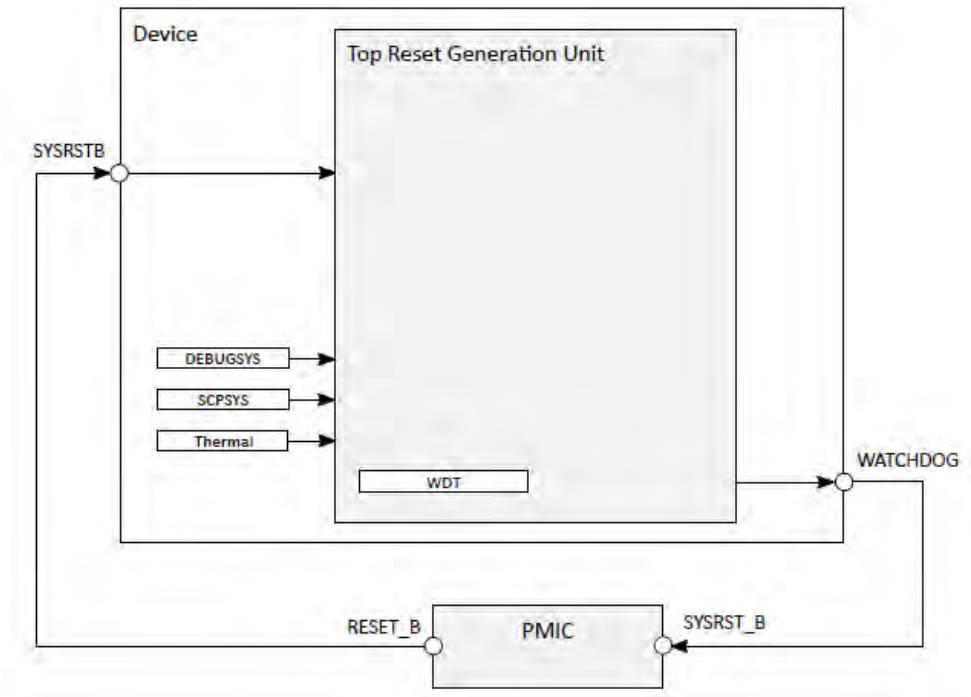

Figure 5-2 Reset Block Diagram

5.5.1 Reset Signal Descriptions

Table 5-10 shows Reset signal description.

Table 5-10 Reset Signal Descriptions

Signal Name	Type	Description	Ball Location
SYSRSTB	DI	System reset input	AC30
WATCHDOG	DO	Watchdog reset output	AB30

5.5.2 Reset Timing Characteristics

Table 5-11 presents timing characteristics for Resets in the device.

Table 5-11 Reset Timing Characteristics

Min	Parameter		Min	Max	Unit
RST01	t_w	Pulse width, RESET	400		µs
RST02	t_h	Hold time, RESET after all supplies valid	40		ms

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6 Clock Characteristics

The device has three external input clocks— low frequency (RTC32K_CK), high frequency (26M_CLKQ), and (XIN_WBG). Figure 6-1 shows the external clock sources and clock outputs.

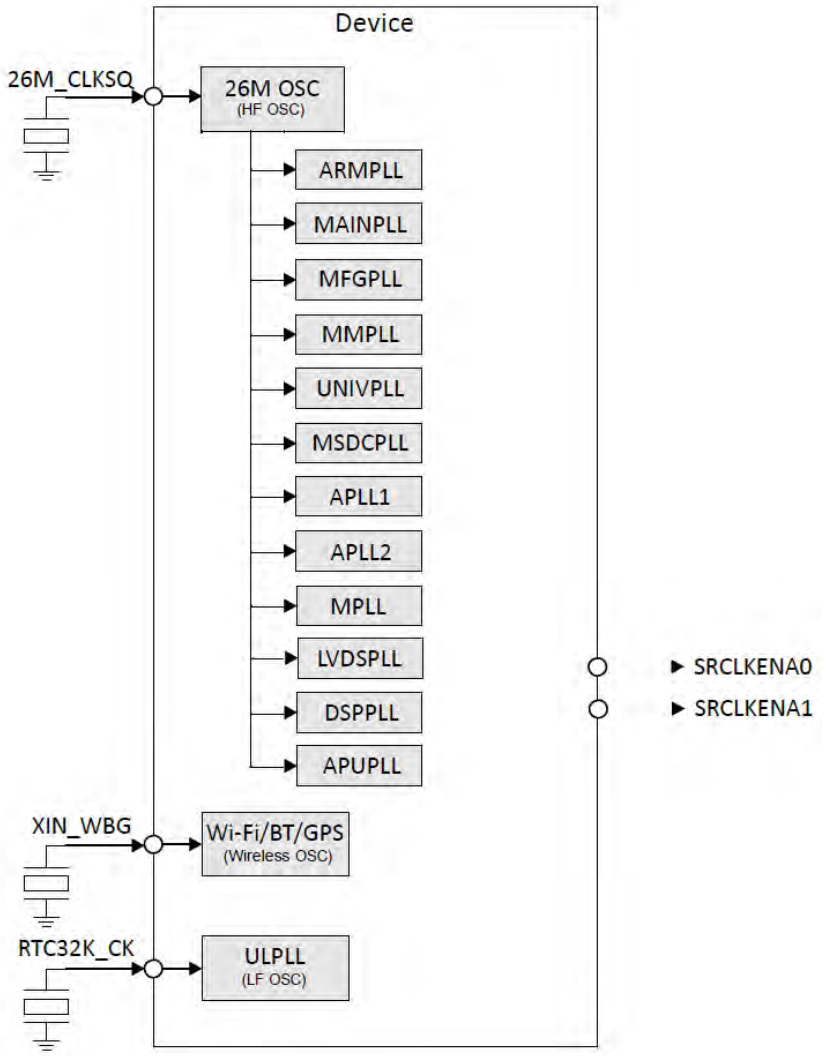

Figure 6-1 Device Clock Diagram

6.1 Maximum Supported Frequency

Table 6-1 shows the maximum core and peripheral speed limitations and correlations.

Table 6-1 Maximum Supported Frequency Limitations

Module		Max	Unit
Quad-core Arm Cortex-A53	CPU	2000	MHz
Graphics Accelerator	GPU	800	MHz
AI Processor Unit	APU	700	MHz
Single-core HiFi 4 Audio Engine	DSP	600	MHz
External Memory Interface	DDR3/L	1600	Mbps
	DDR4	3200	Mbps
	LPDDR3	1600	Mbps
	LPDDR4/X	3200	Mbps

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Module		Max	Unit
Memory Card Controller	SD Card	200	MHz
	eMMC	200	MHz
	SDIO	200	MHz
NAND Flash Interface	NFI	200	MHz
Display Parallel Interface	DPI	75	MHz
Display Serial Interface	DSI	1200	MHz
Low Voltage Differential Signaling	LVDS	75	MHz
Image Signal Processor	ISP	312	MHz
Camera Parallel Interface	CPI	93.45	MHz
Camera Serial Interface	CSI	1500	MHz
Video Encoder	VENC	312	MHz
Video Decoder	VDEC	312	MHz
Inter-IC Sound	I2S master mode (sampling frequency)	192	kHz
	I2S slave mode (sampling frequency)	48	kHz
Time Division Multiplexed Interface	TDM (sampling frequency)	192	kHz
Pulse Density Modulation	PDM	3.25	MHz
Pulse Code Modulation	PCM (sampling frequency)	48	kHz
Sony/Philips Digital Interface Format	S/PDIF	192	kHz
Inter-Integrated Circuit	I2C	1	MHz
Universal Asynchronous Receiver/Transmitter	UART	961,200	bps
Serial Peripheral Interface	SPI	50	MHz
Auxiliary Analog-to-Digital Converter	AUXADC (clock rate)	4	MHz
JTAG interface	JTAG	10	MHz
Pulse Width Modulation	PWM	13	MHz
Ethernet	MII	25	MHz
	RMII	50	MHz
Wireless Communication Module	Wi-Fi	2484	MHz
	BT	2480	MHz
Universal Serial Bus 2.0	USB2.0 High Speed	480	Mbps
	USB2.0 Full Speed	12	Mbps
	USB2.0 Low Speed	1.5	Mbps

6.2 PLL Specifications

Table 6-2 shows 26-MHz clock reference specification for supplying PLLs.

Table 6-2 26-MHz Reference Clock Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency (System, MIPI, MEM)		26		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$F_{OUT-JIT}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V

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Parameter		Min	Typ	Max	Unit
AVDD12	Analog power supply	1.14	1.2	1.26	V
T_c	Operating temperature	-20		80	°C

Table 6-3 shows ARMPLL specifications.

Table 6-3 ARMPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		800		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-4 shows MAINPLL specifications.

Table 6-4 MAINPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		1092		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			30	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-5 shows MFGPLL specifications.

Table 6-5 MFGPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		450		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-6 shows MMPLL specifications.

Table 6-6 MMPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz

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Parameter		Min	Typ	Max	Unit
F_{OUT}	Output clock frequency		320		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-7 shows UNIVPLL specifications.

Table 6-7 UNIVPLL Specifications

Parameter		Mode	Min	Typ	Max	Unit
F_{IN}	Input clock frequency			26		MHz
F_{OUT}	Output clock frequency	PLL		1248		MHz
		USB		192		MHz
t_{SET}	Settling time			20		µs
$F_{OUT(D)}$	Output clock duty cycle		47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)	1248 MHz			30	ps
		192 MHz			60	ps
DVDD	Digital power supply		0.54	0.8	0.88	V
AVDD18	Analog power supply		1.7	1.8	1.9	V
AVDD12	Analog power supply		1.14	1.2	1.26	V

Table 6-8 shows MSDCPLL specifications.

Table 6-8 MSDCPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		400		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-9 shows APLL1 specifications.

Table 6-9 APLL1 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		180.6336		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V

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Parameter		Min	Typ	Max	Unit
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-10 shows APLL2 specifications.

Table 6-10 APLL2 Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		196.608		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-11 shows MPLL specifications.

Table 6-11 MPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		208		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-12 shows LVDSPLL specifications.

Table 6-12 LVDSPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		300		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-13 shows DSPPLL specifications.

Table 6-13 DSPPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		195		MHz

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Parameter		Min	Typ	Max	Unit
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-14 shows APUPLL specifications.

Table 6-14 APUPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		26		MHz
F_{OUT}	Output clock frequency		195		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	47	50	53	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			60	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
AVDD12	Analog power supply	1.14	1.2	1.26	V

Table 6-15 shows ULPLL specifications.

Table 6-15 ULPLL Specifications

Parameter		Min	Typ	Max	Unit
F_{IN}	Input clock frequency		32.746		MHz
F_{OUT}	Output clock frequency		26		MHz
t_{SET}	Settling time		20		µs
$F_{OUT(D)}$	Output clock duty cycle	45	50	55	%
$t_{J(CLK)}$	Output clock jitter (period jitter)			700	ps
DVDD	Digital power supply	0.54	0.8	0.88	V
AVDD18	Analog power supply	1.7	1.8	1.9	V

6.3 Crystal Oscillator

A 26-MHz crystal oscillator (XTAL) with external 26-MHz clock buffer and a 32-kHz clock output is integrated in the device. The mode of operation is detected automatically, which means if an external clock is detected, the device will enter external 26-MHz clock mode, otherwise it will enter 32-kHz clock mode.

Table 6-16 and Figure 6-2 define the XTAL component specification requirements and XTAL reference clock circuit.

Table 6-16 XTAL Component Specification

Parameter	Min	Typ	Max	Unit
Parallel resonance crystal frequency		26		MHz
Frequency tolerance	-20		20	ppm
Clock swing	0.85	1.1	1.3	V
Duty cycle	45	50	55	%

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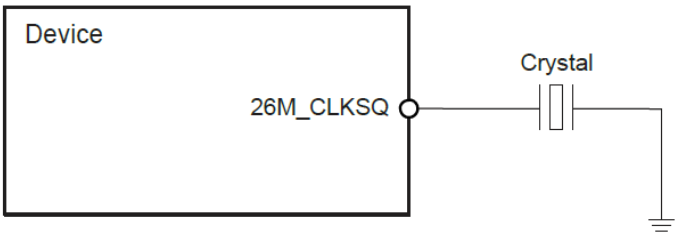

Figure 6-2 XTAL Reference Clock Diagram

6.4 External TCXO Clock Sources

Table 6-17 defines the external reference clock source specification requirements.

Table 6-17 External 26-MHz Reference Clock Source Specification

Parameter	Min	Typ	Max	Unit
Supported frequency		26		MHz
Input capacitance			30	pF
Input resistance	3			kΩ
Swing Vpp	0.85		1.3	V
PN requirement 5 Hz			-83	dBc/Hz
PN requirement 10 Hz			-90	dBc/Hz
PN requirement 100 Hz			-115	dBc/Hz
PN requirement 1 kHz			-137	dBc/Hz
PN requirement 10 kHz			-150	dBc/Hz
PN requirement 100 kHz			-153	dBc/Hz

6.5 Clock Signal Descriptions

Table 6-18 presents clock signal descriptions.

Table 6-18 Clock Signal Descriptions

Signal Name	Type	Description	Ball Location
26M_CLKSQ	AIO	26 MHz clock input	AC20
RTC32K_CK	DI	32 kHz clock input	Y28
SRCLKENA0	DO	Output signal; control of PMIC 26 MHz/Buck/LDO normal mode or sleep mode (high: normal mode; low: sleep mode or low power mode)	AB27
SRCLKENA1	DO	Output signal; control of PMIC 26 MHz/Buck/LDO on or off	AB27, AB28

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7 Package Information

7.1 Thermal Specifications

7.1.1 Thermal Operating Specifications

Table 7-1 presents the thermal resistance characteristics and maximum operating temperatures of the device.

Table 7-1 Thermal Operating Specifications

Parameter		Value	Unit
Tjmax	Maximum operating junction temperature	105	°C
θ_{JA}	Package thermal resistances in nature convection	23.04	°C/Watt
θ_{JC}	Thermal resistance	4.23	°C/Watt
θ_{JT}	Thermal characterization parameter	1.455	°C/Watt

7.2 Top Marking

Figure 7-1 shows the device top marking definition.

Figure 7-1 Device Top Marking

Table 7-2 presents the printed device reference and decoding.

Table 7-2 Printed Device Reference and Decoding

Parameter		Value	Description
NNNNNNN	Part number	MT8365	Wireless connected multimedia system
DDDD	Date code		For internal use only
####	Internal control code		For internal use only
XXXXXXX	Lot number		For internal use only
O	Pin one designator		Pin one location

7.3 Mechanical Drawing

The following figure shows printed device reference diagram (VFBGA 12.2 mm × 11.8 mm, 633-ball, 0.4 mm pitch package).

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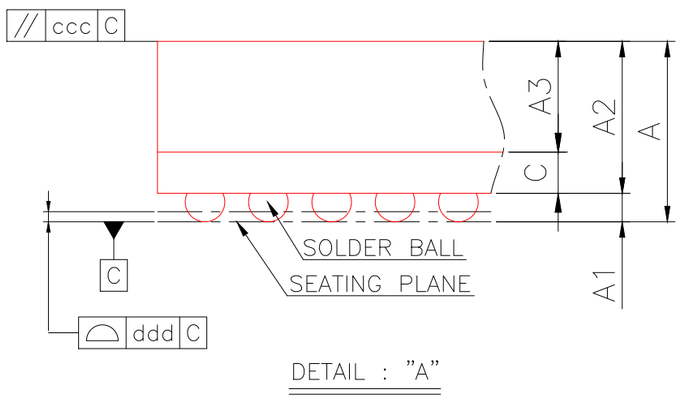

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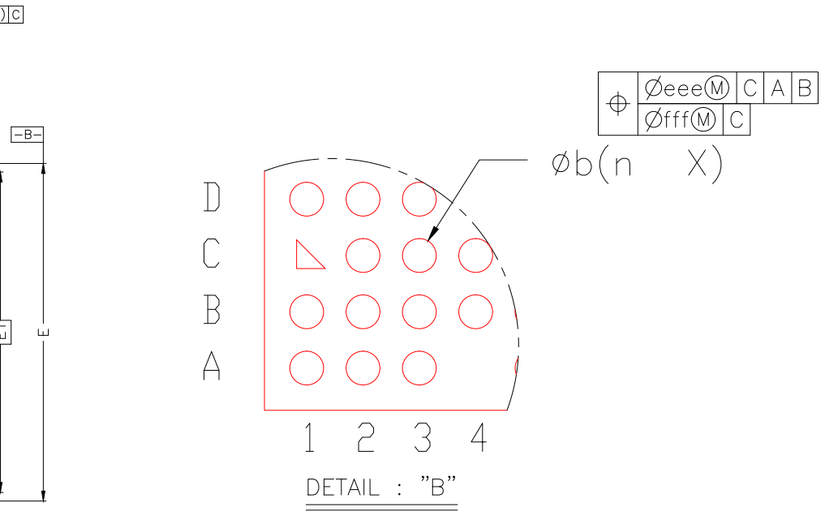

DETAIL : "B"

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	12.15	12.20	12.25
	Y	E	11.75	11.80	11.85
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.45 Ref.		
Substrate Thickness		C	0.141 Ref.		
Substrate+Mold Thickness		A2	0.541	0.591	0.641
Total Thickness		A	–	–	0.90
Ball Diameter			0.25		
Ball Stand Off		A1	0.14	0.18	0.22
Ball Width		b	0.22	0.27	0.32
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	633		
Edge Ball Center to Center	X	D1	11.60		
	Y	E1	11.20		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

TITLE	PACKAGE OUTLINE		
MFC VFBGA 633 L 12.2X 11.8 X 0.9 max		MEDIATEK	
DWG. NO.	REV.	SHEET	UNIT
MT-SP00882	A	1 OF 2	MM

8 Legal and Support Information

8.1 Related Documents and Products

Documents:

- **MMD (MediaTek Module Design)**—Application note for PDN and DRAM design implementation methods
- **MT6357ARV & MT6390 Audio HW Design Notice**—Application note for Audio connectivity including system level block diagram, bias and UL path, schematic and layout recommendations, unused pin handling, and pop noise soluitions.
- **MT8365 HW Design Notice**—Application note including generic and peripheral interfaces such as GPIO, MSDC, NAND flash, USB, Camera, DSI LVDS, DPI LCM, Audio, Ethernet, and power design implementation recommendations.
- **MT8365 System HW Design Difference of MT6357ARV and MT6390ARV PMIC**—Application note including differences between the PMIC's buck and LDO design, power-on/power-off sequences, and reference schematic examples.
- **MT8365 PCB Design Guidelines**—Application note including footprint recommendations, PCB stack-up, placement notes, design guidelines for high-speed digital signals and different implementation methods.

Companion chips:

- **MT6357**—Integrated Power Management IC (PMIC)
- **MT6390**—Integrated Power Management IC (PMIC)
- **MT6631**—Dual-band (2.4 GHz and 5 GHz) 1 x 1 802.11ac Wi-Fi; Bluetooth 5.0, GPS, FM receiver
- **MT7663**—Dual-band (2.4 GHz and 5 GHz) 2 x 2 802.11ac Wi-Fi with MU-MIMO; Bluetooth 5.1

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