



**THE DATASHEET OF  
74HCT3G07GD,125**





# 74HC3G07; 74HCT3G07

Triple buffer with open-drain outputs

Rev. 6 — 13 December 2023

Product data sheet

## 1. General description

The 74HC3G07; 74HCT3G07 is a triple buffer with open-drain outputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
  - For 74HC3G07: CMOS level
  - For 74HCT3G07: TTL level
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74HC3G07DP</a> <a href="#">74HCT3G07DP</a>	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	<a href="#">SOT505-2</a>
<a href="#">74HC3G07DC</a> <a href="#">74HCT3G07DC</a>	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	<a href="#">SOT765-1</a>

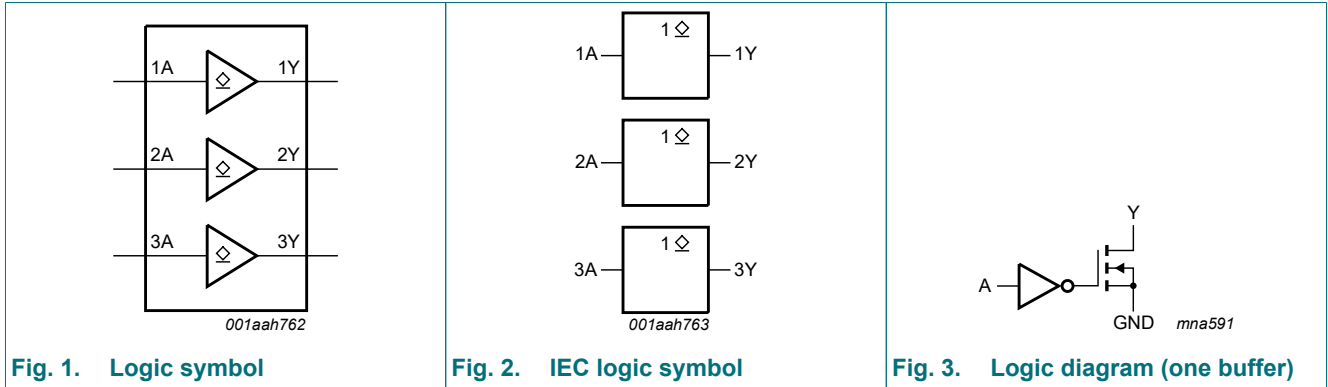
## 4. Marking

Table 2. Marking code

Type number	Marking code [1]
74HC3G07DP	H07
74HCT3G07DP	T07
74HC3G07DC	H07
74HCT3G07DC	T07

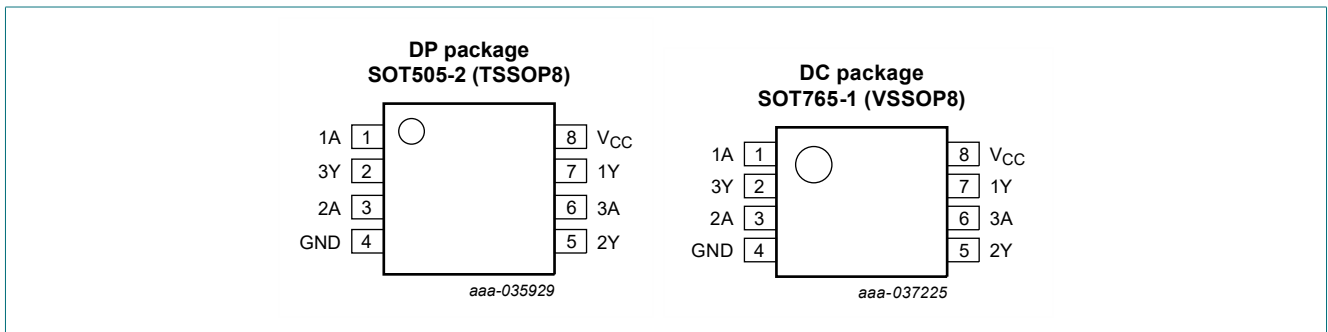
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram



### 6. Pinning information

#### 6.1. Pinning



#### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V <sub>CC</sub>	8	supply voltage

### 7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input nA	Output nY
L	L
H	Z

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ [1]	-20	-	mA
$V_O$	output voltage	active mode [1]	-0.5	$V_{CC} + 0.5$	V
		high-impedance mode [1]	-0.5	7.0	V
$I_O$	output current	$V_O = -0.5\text{ V}$ to $7.0\text{ V}$ [1]	-25	-	mA
$I_{CC}$	supply current	[1]	-	50	mA
$I_{GND}$	ground current	[1]	-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_D$	dynamic power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) package:  $P_{tot}$  derates linearly with 4.6 mW/K above 96 °C.

For SOT765-1 (VSSOP8) package:  $P_{tot}$  derates linearly with 4.9 mW/K above 99 °C.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC3G07			74HCT3G07			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	6.0	0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
<b>74HC3G07</b>								
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1.0	μA
I <sub>LO</sub>	output leakage current	V <sub>I</sub> = V <sub>IH</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±5.0	-	±10	μA
I <sub>CC</sub>	supply current	per input pin; V <sub>CC</sub> = 6.0 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	-	10	-	20	μA
C <sub>I</sub>	input capacitance		-	1.5	-	-	-	pF
<b>74HCT3G07</b>								
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±1.0	-	±1.0	μA
I <sub>LO</sub>	output leakage current	V <sub>I</sub> = V <sub>IH</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	-	-	±5.0	-	±10	μA
I <sub>CC</sub>	supply current	per input pin; V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	-	10	-	20	μA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>CC</sub> = 4.5 V to 5.5 V; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0 A	-	-	375	-	410	μA
C <sub>I</sub>	input capacitance		-	1.5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
<b>74HC3G07</b>								
t <sub>PZL</sub>	OFF-state to LOW propagation delay	nA to nY; see Fig. 4						
		V <sub>CC</sub> = 2.0 V	-	25	95	-	125	ns
		V <sub>CC</sub> = 4.5 V	-	9	19	-	25	ns
		V <sub>CC</sub> = 6.0 V	-	7	16	-	20	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	nA to nY; see Fig. 4						
		V <sub>CC</sub> = 2.0 V	-	25	95	-	125	ns
		V <sub>CC</sub> = 4.5 V	-	11	23	-	30	ns
		V <sub>CC</sub> = 6.0 V	-	10	23	-	26	ns
t <sub>THL</sub>	HIGH to LOW output transition time	nY; see Fig. 4						
		V <sub>CC</sub> = 2.0 V	-	18	95	-	125	ns
		V <sub>CC</sub> = 4.5 V	-	6	19	-	25	ns
		V <sub>CC</sub> = 6.0 V	-	5	16	-	20	ns
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> [2]	-	4	-	-	-	pF
<b>74HCT3G07</b>								
t <sub>PZL</sub>	OFF-state to LOW propagation delay	nA to nY; V <sub>CC</sub> = 4.5 V; see Fig. 4	-	11	27	-	32	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	nA to nY; V <sub>CC</sub> = 4.5 V; see Fig. 4	-	10	26	-	31	ns
t <sub>THL</sub>	HIGH to LOW output transition time	nY; V <sub>CC</sub> = 4.5 V; see Fig. 4	-	6	19	-	22	ns
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V [2]	-	4		-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

[2] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

11.1. Waveforms and test circuit

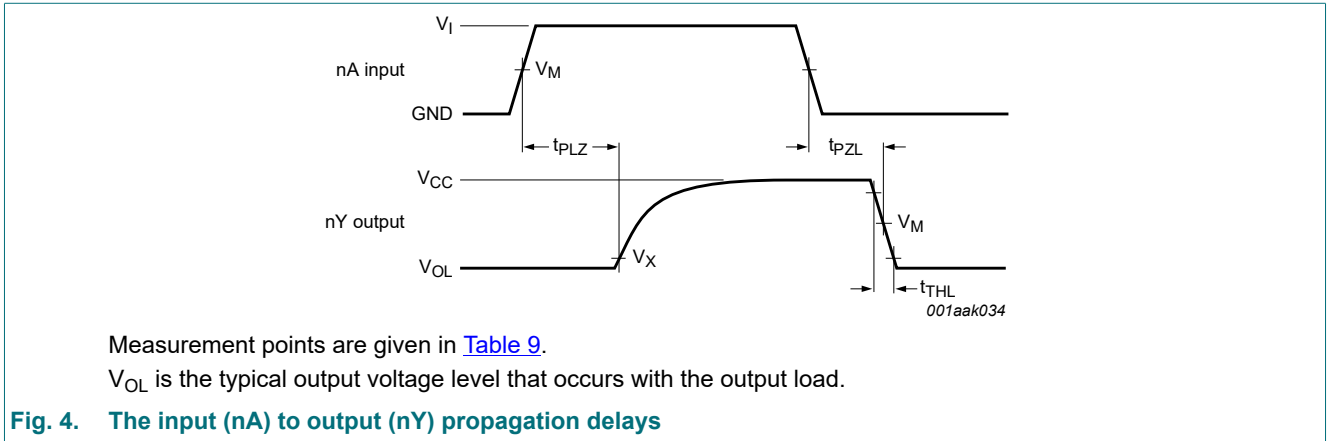


Table 9. Measurement points

Type	Input	Output	
	$V_M$	$V_M$	$V_X$
74HC3G07	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$
74HCT3G07	1.3 V	1.3 V	$0.1 \times V_{CC}$

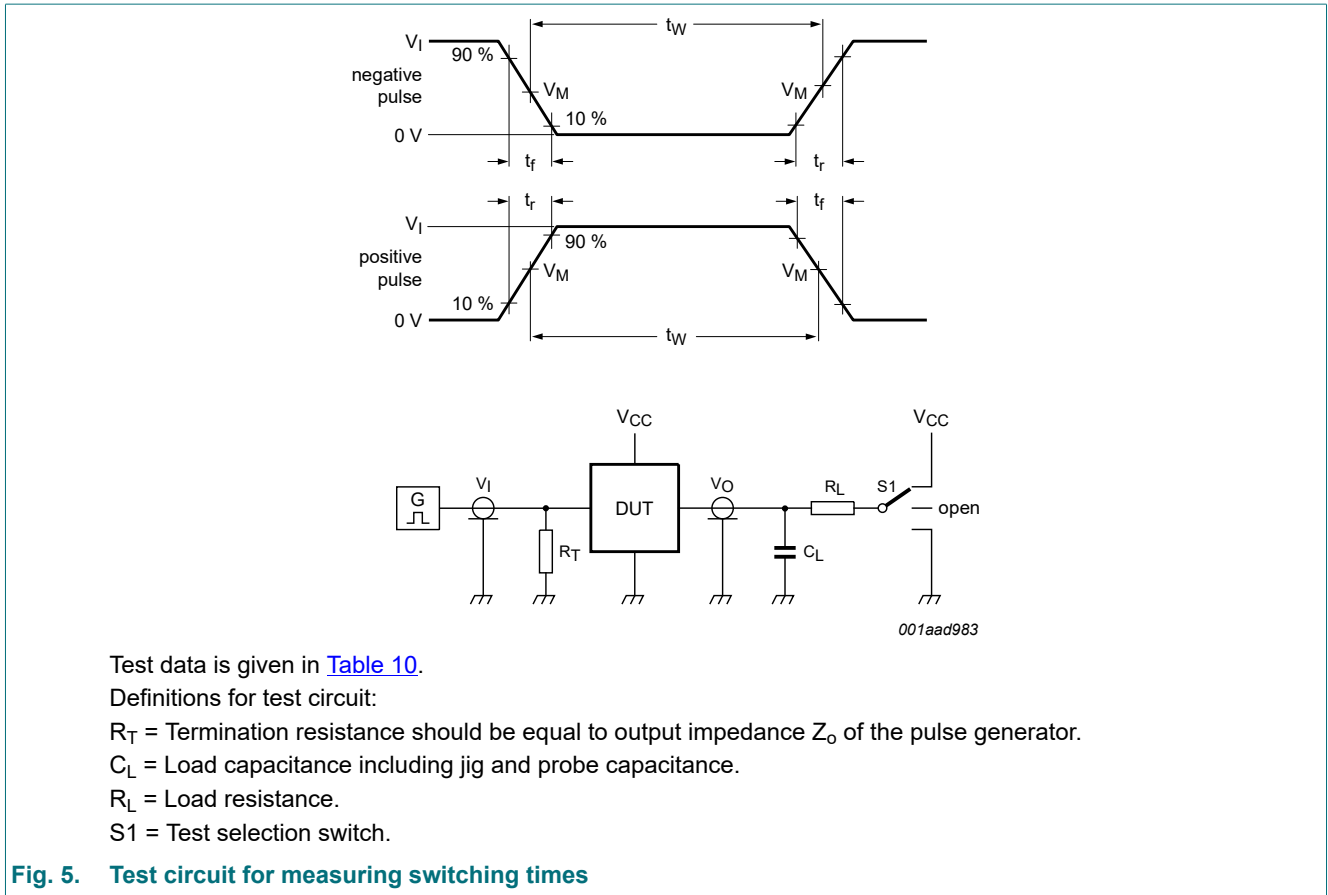


Fig. 5. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{pZL}, t_{pLZ}$
74HC3G07	GND to $V_{CC}$	$\leq 6$ ns	50 pF	1 k $\Omega$	$V_{CC}$
74HCT3G07	GND to 3 V	$\leq 6$ ns	50 pF	1 k $\Omega$	$V_{CC}$

## 12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

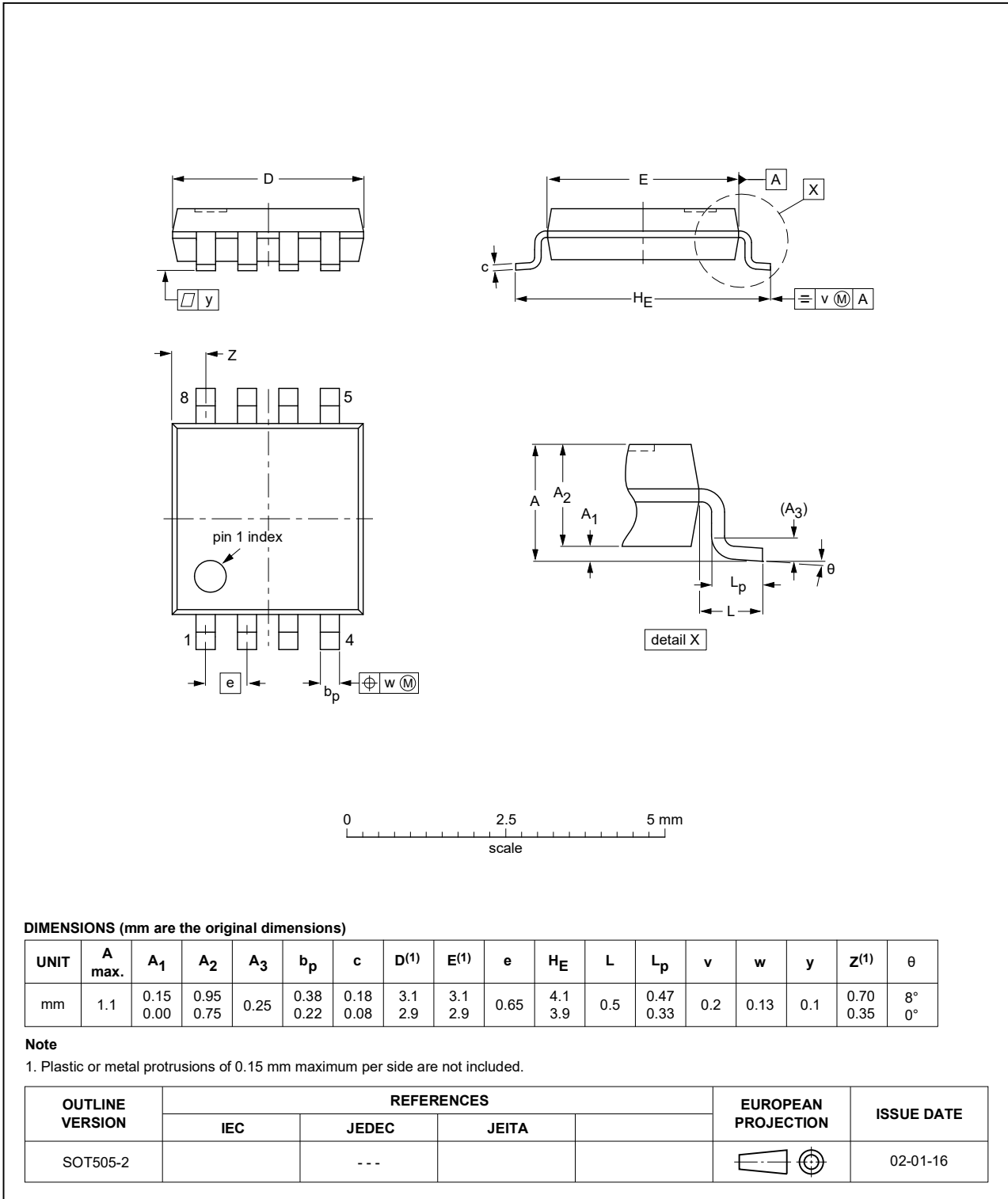


Fig. 6. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Fig. 7. Package outline SOT765-1 (VSSOP8)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT3G07 v.6	20231213	Product data sheet	-	74HC_HCT3G07 v.5
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2</a> updated.</li> <li>• <a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li>• <a href="#">Section 8</a>: <math>P_{tot}</math> and derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74HC_HCT3G07 v.5	20190124	Product data sheet	-	74HC_HCT3G07 v.4
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Type numbers 74HC3G07GD and 74HCT3G07GD (SOT996-2) removed.</li> <li>• Package outline drawing <a href="#">SOT765-1</a> (VSSOP8) updated.</li> </ul>			
74HC_HCT3G07 v.4	20131216	Product data sheet	-	74HC_HCT3G07 v.3
Modifications:	<ul style="list-style-type: none"> <li>• Features and benefits updated (errata).</li> </ul>			
74HC_HCT3G07 v.3	20130814	Product data sheet	-	74HC_HCT3G07 v.2
Modifications:	<ul style="list-style-type: none"> <li>• For type numbers 74HC3G07GD and 74HCT3G07GD XSON8U has changed to XSON8.</li> </ul>			
74HC_HCT3G07 v.2	20090512	Product data sheet	-	74HC_HCT3G07 v.1
74HC_HCT3G07 v.1	20031015	Product specification	-	-

## 15. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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