



**THE DATASHEET OF  
CBT3384DK,118**



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Kind regards,

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# CBT3384

## 10-bit bus switch with 5-bit output enables

Rev. 06 — 2 November 2009

Product data sheet

### 1. General description

The CBT3384 provides ten bits of high-speed TTL-compatible bus switching. The low ON resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3384 device is organized as two 5-bit bus switches with two separate output enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ) inputs. When  $n\overline{OE}$  is LOW, the switch is on and port A is connected to the B port. When  $n\overline{OE}$  is HIGH, each switch is disabled.

The CBT3384 is characterized for operation from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

### 2. Features

- 5  $\Omega$  switch connection between two ports
- TTL-compatible control input levels
- Multiple package options
- See CBTD3384 for CBT3384 with level shifting diodes
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ CDM JESD22-C101C exceeds 1000 V

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
CBT3384D	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
CBT3384DB	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
CBT3384DK	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	SSOP24 <sup>[1]</sup>	plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT556-1
CBT3384PW	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

[1] Also known as QSOP24 package

## 4. Functional diagram

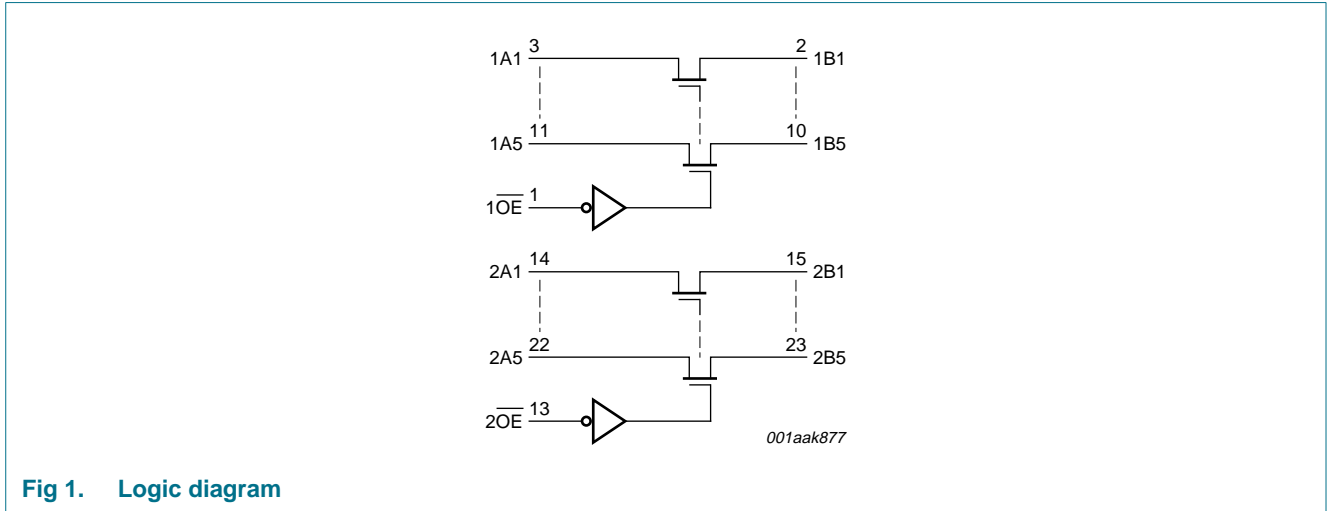


Fig 1. Logic diagram

## 5. Pinning information

### 5.1 Pinning

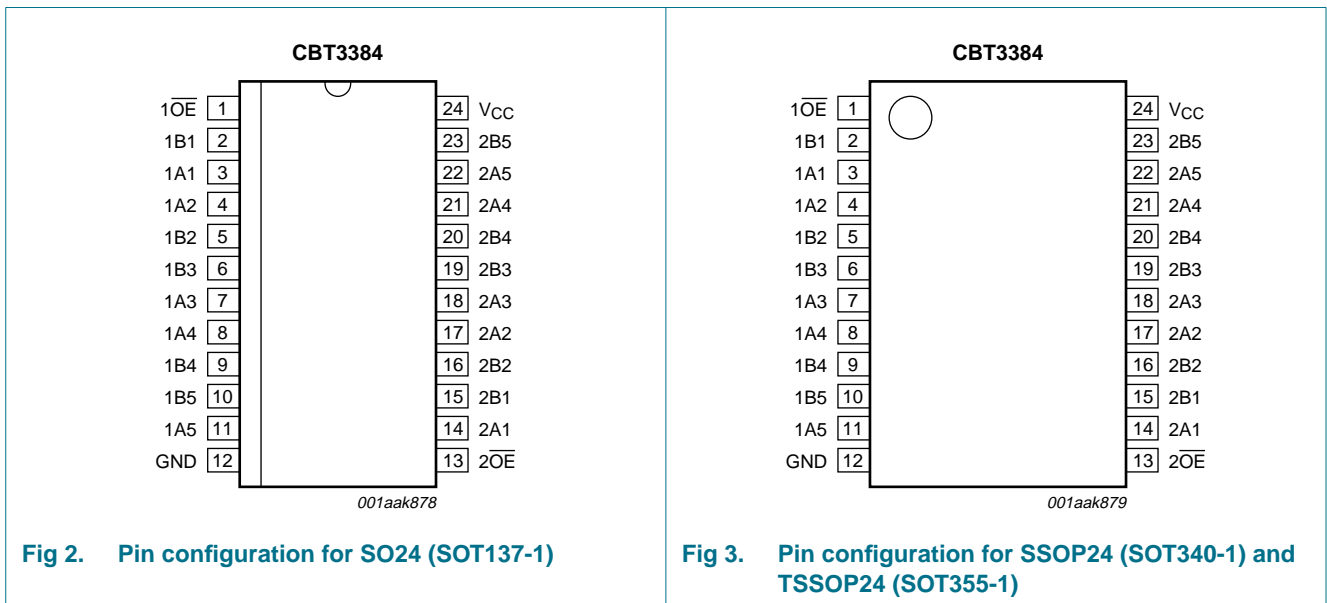


Fig 2. Pin configuration for SO24 (SOT137-1)

Fig 3. Pin configuration for SSOP24 (SOT340-1) and TSSOP24 (SOT355-1)

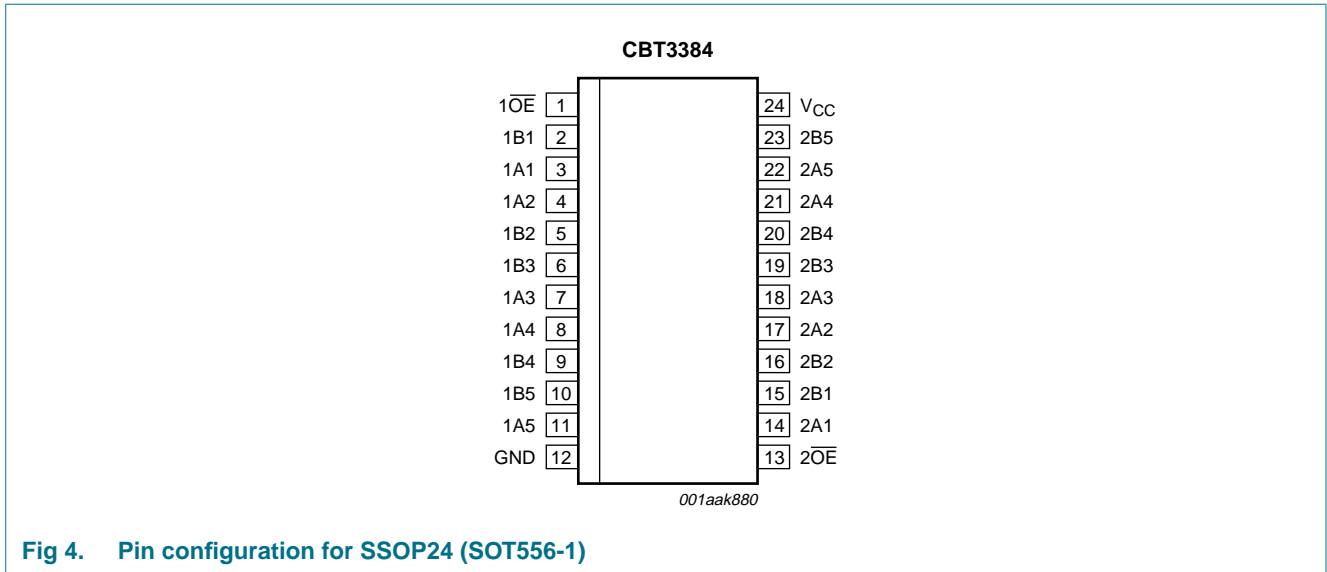


Fig 4. Pin configuration for SSOP24 (SOT556-1)

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 13	output enable input (active LOW)
1A1 to 1A5	3, 4, 7, 8, 11	data input/output (A port)
2A1 to 2A5	14, 17, 18, 21, 22	data input/output (A port)
1B1 to 1B5	2, 5, 6, 9, 10	data input/output (B port)
2B1 to 2B5	15, 16, 19, 20, 23	data input/output (B port)
GND	12	ground (0 V)
VCC	24	positive supply voltage

## 6. Functional description

Table 3. Function selection<sup>[1]</sup>

Input		Input/output	
1OE	2OE	1An, 1Bn	2An, 2Bn
L	L	1An = 1Bn	2An = 2Bn
L	H	1An = 1Bn	Z
H	L	Z	2An = 2Bn
H	H	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).<sup>[1]</sup>

$T_{amb} = -40\text{ °C to }+85\text{ °C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		<sup>[2]</sup> -0.5	+7.0	V
$I_O$	output current	$V_O < 0\text{ V}$	-	±128	mA
$I_{IK}$	input clamping current	$V_{I/O} = 0\text{ V}$	-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Section 8](#). is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_{IH}$	HIGH-state input voltage		2.0	-	-	V
$V_{IL}$	LOW-state input voltage		-	-	0.8	V
$T_{amb}$	ambient temperature	operating in free air	-40	-	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			Unit
			Min	Typ <sup>[1]</sup>	Max	
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5\text{ V}; I_I = -18\text{ mA}$	-	-	-1.2	V
$I_I$	input leakage current	$V_{CC} = 5.5\text{ V}; V_I = \text{GND or } 5.5\text{ V}$	-	-	±1	µA
$I_{CC}$	supply current	$V_{CC} = 5.5\text{ V}; I_O = 0\text{ mA}; V_I = V_{CC}\text{ or GND}$	-	-	3	µA
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 5.5\text{ V}$ ; one input at 3.4 V, other inputs at $V_{CC}$ or GND <sup>[2]</sup>	-	-	2.5	mA
$V_{pass}$	pass voltage	output HIGH; $V_I = V_{CC} = 5.0\text{ V}; I_O = -100\text{ µA}$	3.6	3.9	4.2	V
$C_I$	input capacitance	control pins; $V_I = 3\text{ V or } 0\text{ V}$	-	4.0	-	pF
$C_{io(off)}$	off-state input/output capacitance	port off; $V_I = 3\text{ V or } 0\text{ V}; n\overline{OE} = V_{CC}$	-	10.0	-	pF

**Table 6. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			Unit
			Min	Typ <sup>[1]</sup>	Max	
R <sub>ON</sub>	ON resistance	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 64 mA <a href="#">[3]</a>	-	5	7	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 30 mA <a href="#">[3]</a>	-	5	7	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 2.4 V; I <sub>I</sub> = -15 mA <a href="#">[3]</a>	-	10	15	Ω

- [1] All typical values are at V<sub>CC</sub> = 5 V, T<sub>amb</sub> = 25 °C.
- [2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.
- [3] Measured by the voltage drop between the nAn and the nBn terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nAn or nBn) terminals.

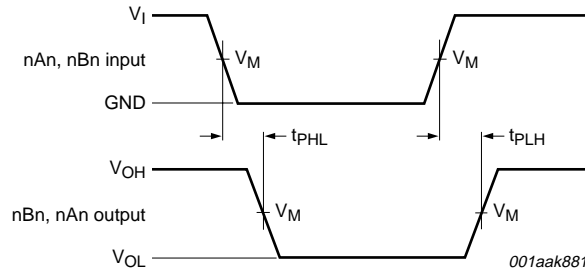
## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
 Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nAn, nBn to nBn, nAn; <a href="#">[1][2]</a> see <a href="#">Figure 5</a>	-	-	0.25	-	0.25	ns
		V <sub>CC</sub> = 5.0 V ± 0.5 V	-	-	0.25	-	0.25	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	n $\overline{O}E$ to nAn or nBn; see <a href="#">Figure 6</a>	1.2	2.3	5.7	1.2	5.6	ns
		V <sub>CC</sub> = 5.0 V ± 0.5 V	1.2	2.3	5.7	1.2	5.6	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	n $\overline{O}E$ to nAn or nBn; see <a href="#">Figure 6</a>	1.2	2.3	5.7	1.2	6.0	ns
		V <sub>CC</sub> = 5.0 V ± 0.5 V	1.2	2.3	5.7	1.2	6.0	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	n $\overline{O}E$ to nAn or nBn; see <a href="#">Figure 6</a>	1.7	3.6	5.2	1.7	5.5	ns
		V <sub>CC</sub> = 5.0 V ± 0.5 V	1.7	3.6	5.2	1.7	5.5	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\overline{O}E$ to nAn or nBn; see <a href="#">Figure 6</a>	1.7	2.7	5.2	1.7	6.6	ns
		V <sub>CC</sub> = 5.0 V ± 0.5 V	1.7	2.7	5.2	1.7	6.6	ns

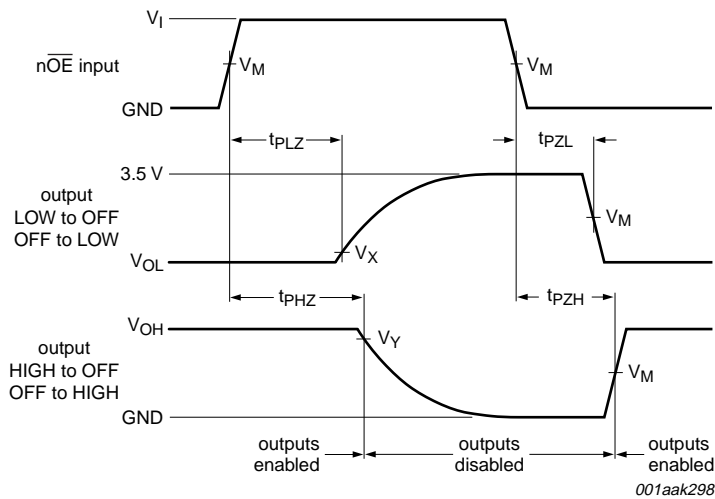
- [1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

11. Waveforms



Measurement points are given in [Table 8](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 5. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times**



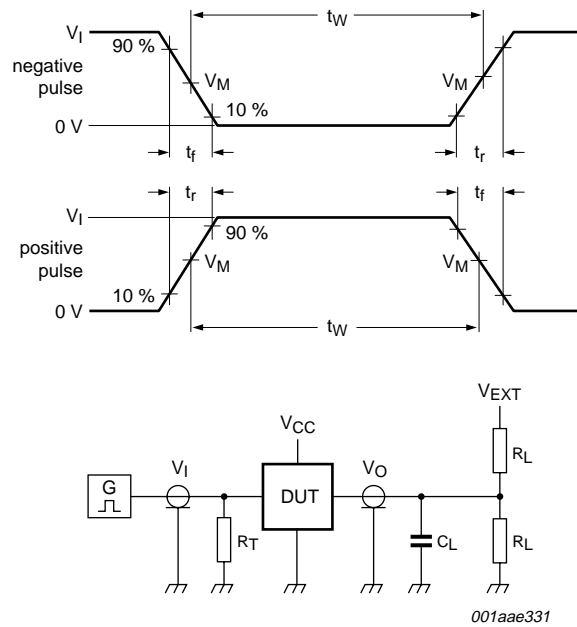
Measurement points are given in [Table 8](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. Enable and disable times**

**Table 8. Measurement points**

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	GND to 3.0 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

12. Test information



Test data is given in [Table 9](#).

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z<sub>o</sub> = 50 Ω.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator.

V<sub>EXT</sub> = External voltage for measuring switching times.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>		
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>
V <sub>CC</sub> = 5.0 V ± 0.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

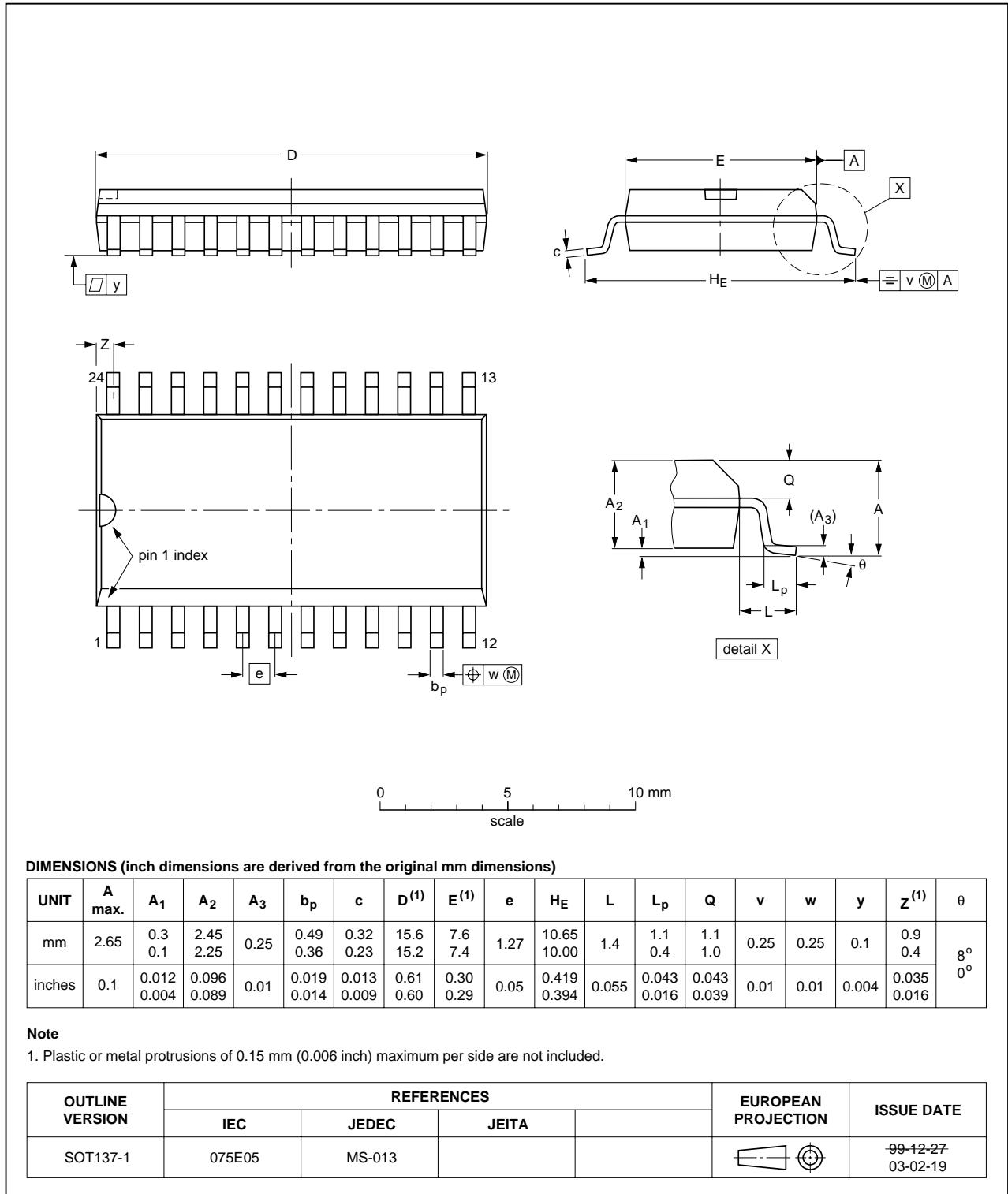


Fig 8. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

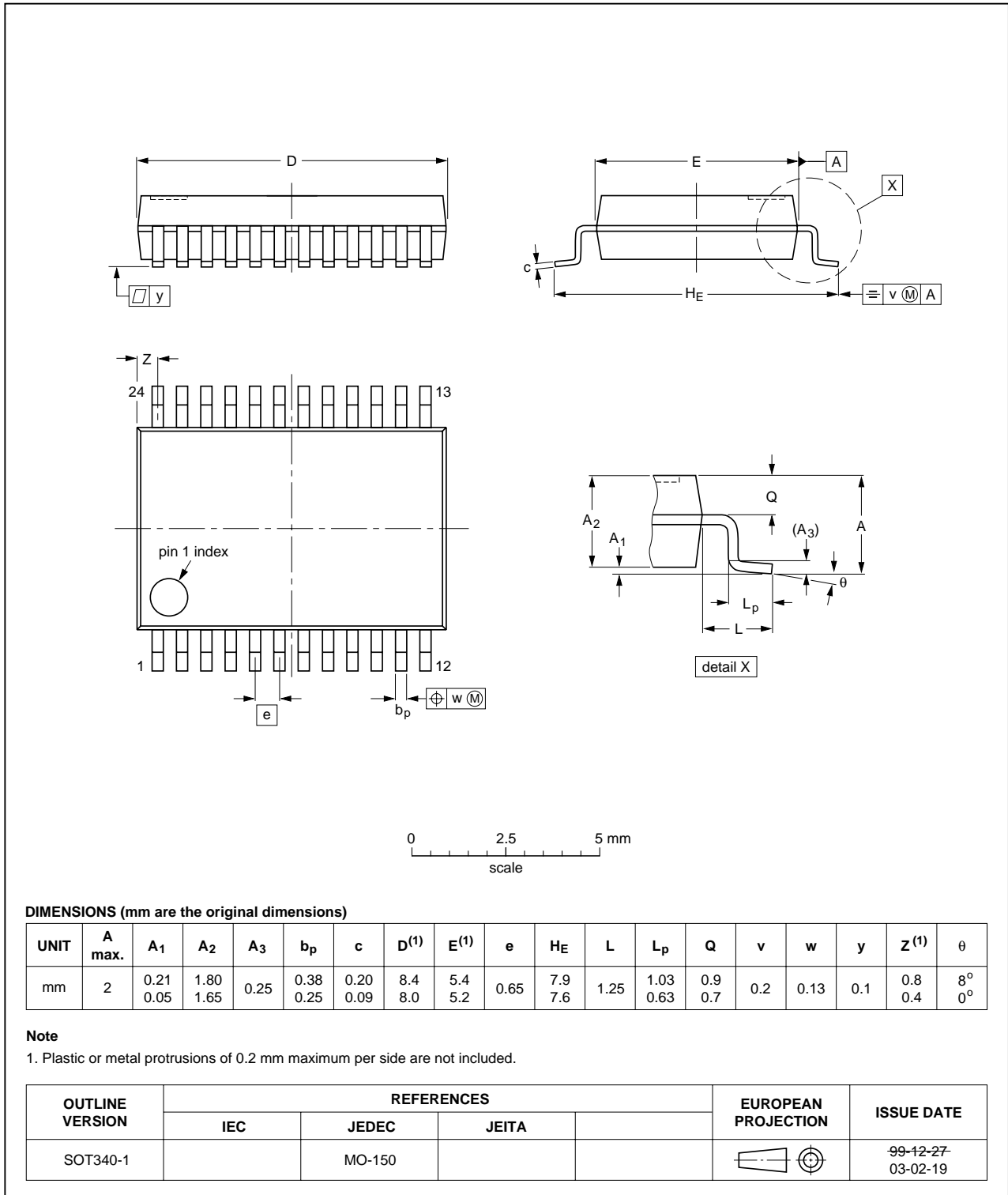


Fig 9. Package outline SOT340-1 (SSOP24)

SSOP24: plastic shrink small outline package; 24 leads; body width 3.9 mm; lead pitch 0.635 mm SOT556-1

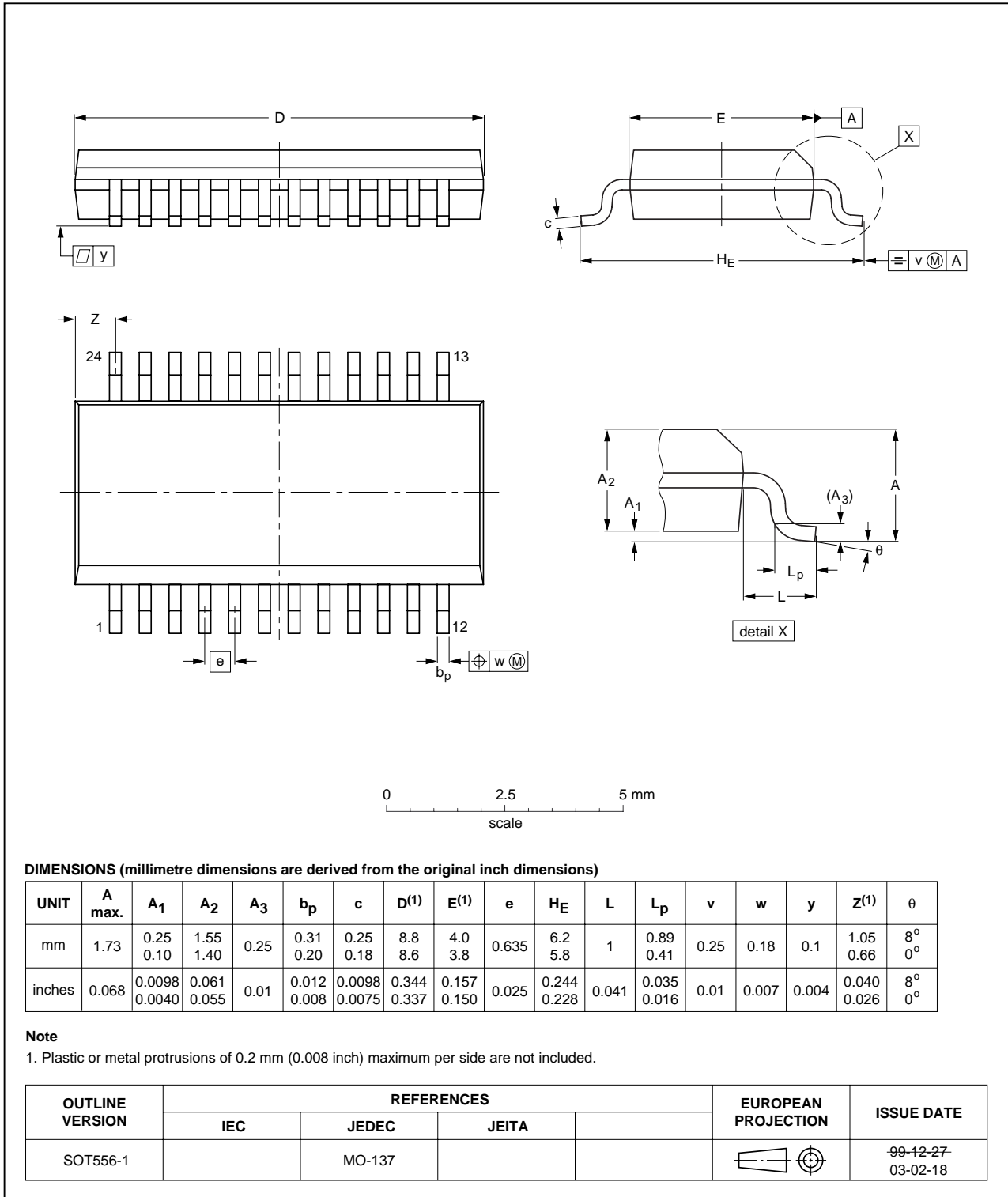


Fig 10. Package outline SOT556-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

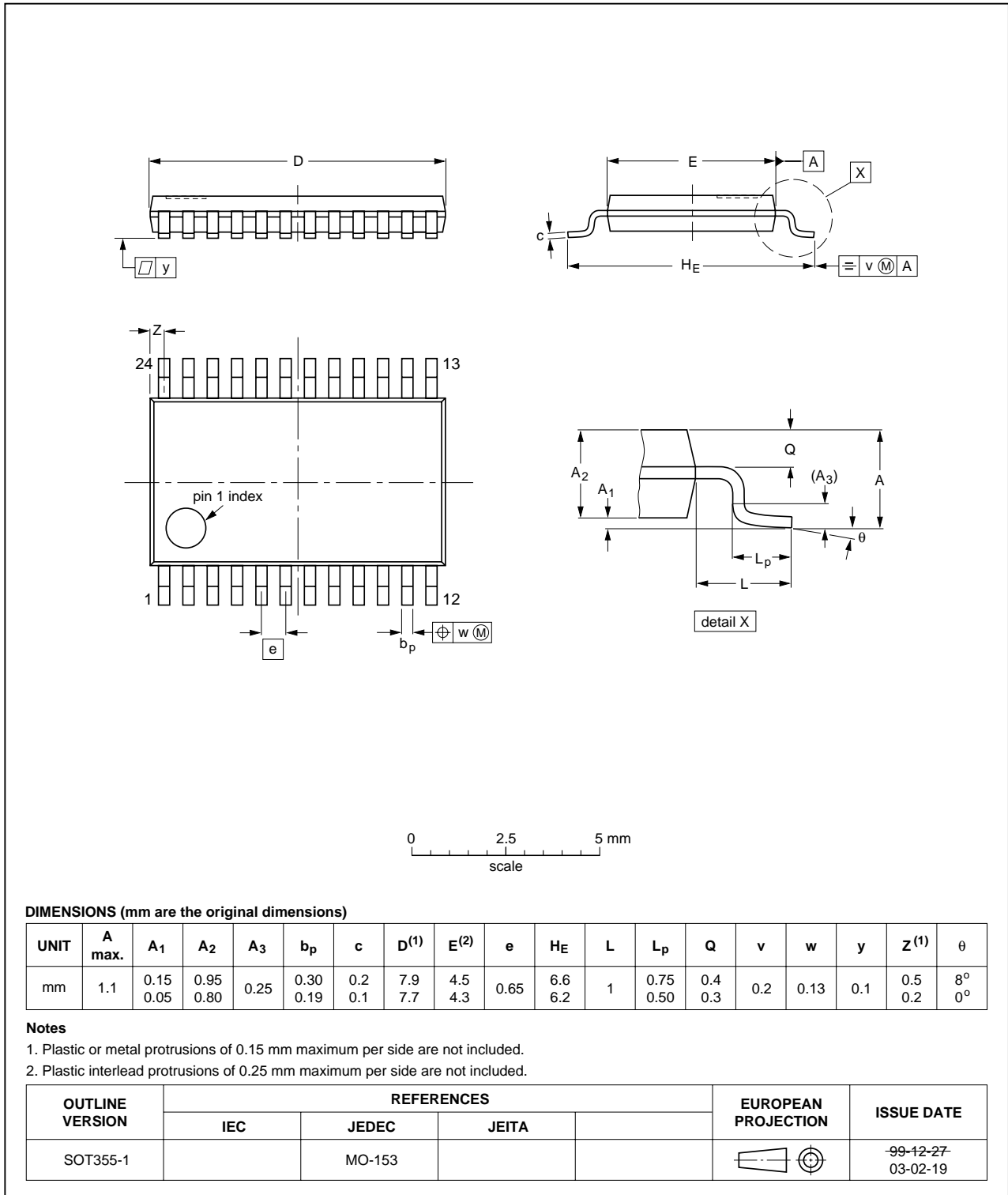


Fig 11. Package outline SOT355-1 (TSSOP24)

## 14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3384_6	20091102	Product data sheet	-	CBT3384_5
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Changed: <a href="#">Table 6 “Static characteristics”</a> <ol style="list-style-type: none"> <li>a. Pass voltage values have changed.</li> <li>b. Undershoot static current protection removed.</li> </ol> </li> <li>• Changed: <a href="#">Table 7 “Dynamic characteristics”</a> <ol style="list-style-type: none"> <li>a. Enable and disable times values have changed.</li> </ol> </li> </ul>			
CBT3384_5	20011220	Product specification	-	CBT3384_4
CBT3384_4	20010319	Product specification	-	CBT3384_3
CBT3384_3	20001113	Product specification	-	CBT3384_2
CBT3384_2	20000128	Product specification	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
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