THE DATASHEET OF

PI4MSD5V9547LEX

8-Channel I2C-Bus Multiplexer with Reset

Description

The PI4MSD5V9547 is an octal bidirectional translating multiplexer controlled by the I2C-bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Only one SCx/SDx channel can be selected at a time, determined by the contents of the programmable control register. The device powers up with Channel 0 connected, allowing immediate communication between the master and downstream devices on that channel.

An active LOW reset input allows the PI4MSD5V9547 to recover from a situation where one of the downstream I2C-buses is stuck in a LOW state. Pulling the RESET pin LOW resets the I2C-bus state machine and causes all the channels to be deselected as does the internal Power-On Reset (POR) function.

The pass gates of the switches are constructed such that the VCC pin can be used to limit the maximum high voltage which is passed by the PI4MSD5V9547. This allows the use of different bus voltages on each pair, so that 1.2V, 1.8V or 2.5V or 3.3V parts can communicate with 5V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5V tolerant.

Features

- 1-of-8 bidirectional translating multiplexer
- I2C-bus interface logic
- Operating power supply voltage from 1.65V to 5.5V
- Allows voltage level translation between 1.2V, 1.8V, 2.5V, 3.3V and 5V buses
- Low standby current
- Low Ron switches
- Active LOW reset input
- Channel selection via I2C bus
- Power-up with one channel on
- Capacitance isolation when channel disabled
- No glitch on power-up
- Supports hot insertion
- 5V tolerant inputs
- 0Hz to 400kHz clock frequency
- ESD protection exceeds 8000V HBM per JESD22-A114, and 1000V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100mA
- Packaging (Pb-free & Green):
  - 24-Pin, TSSOP (L)
  - 24-Pin, TQFN (ZD)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Block Diagram

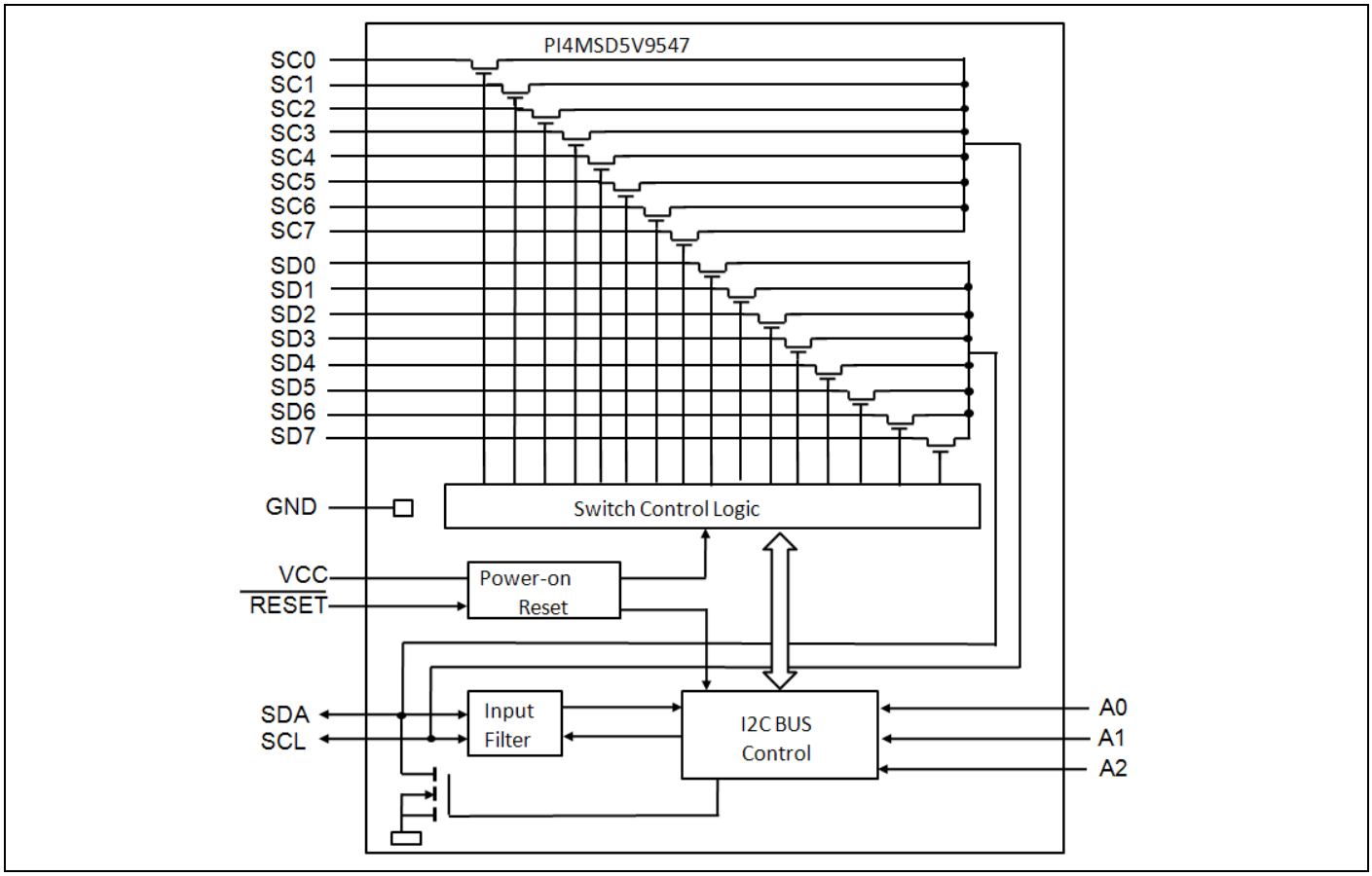
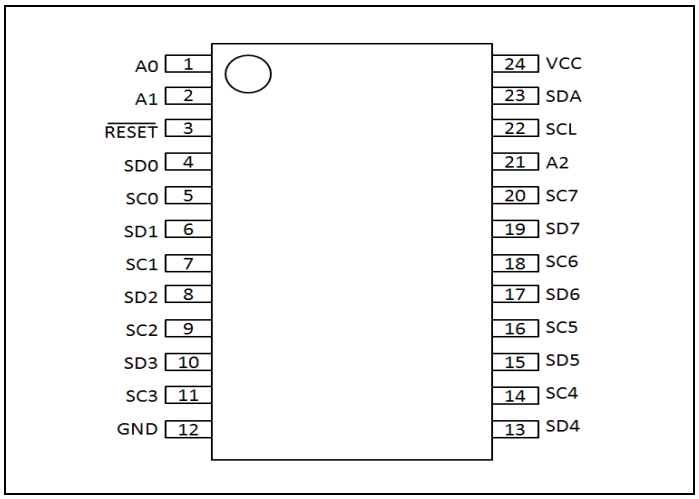
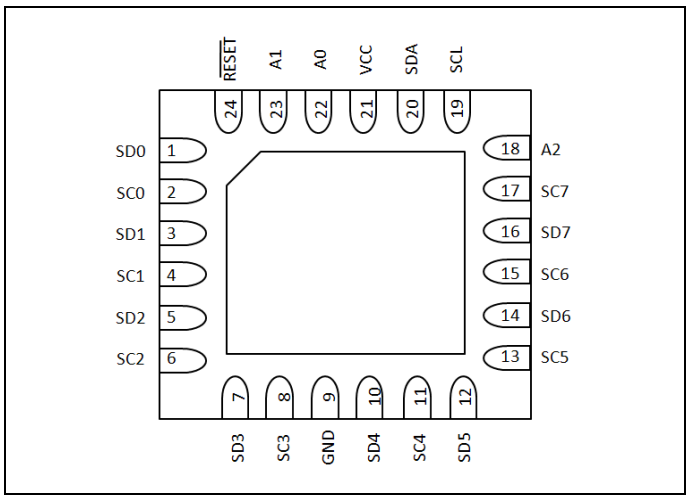


Figure 1. Block Diagram

Pin Configuration



TSSOP/SOIC



TQFN

Pin Description

Pin Number		Pin Name	Type	Description
TSSOP/SOIC	TQFN			
1	22	A0	I	address input 0
2	23	A1	I	address input 1
3	24	$\overline{\text{RESET}}$	I	active LOW reset input
4	1	SD0	I/O	serial data 0
5	2	SC0	I/O	serial clock 0
6	3	SD1	I/O	serial data 1
7	4	SC1	I/O	serial clock 1
8	5	SD2	I/O	serial data 2
9	6	SC2	I/O	serial clock 2
10	7	SD3	I/O	serial data 3
11	8	SC3	I/O	serial clock 3
12	9	GND	Ground	supply ground
13	10	SD4	I/O	serial data 4
14	11	SC4	I/O	serial clock 4
15	12	SD5	I/O	serial data 5
16	13	SC5	I/O	serial clock 5
17	14	SD6	I/O	serial data 6
18	15	SC6	I/O	serial clock 6
19	16	SD7	I/O	serial data 7
20	17	SC7	I/O	serial clock 7
21	18	A2	I	address input 2
22	19	SCL	I/O	serial clock line
23	20	SDA	I/O	serial data line
24	21	VCC	Power	supply voltage

Maximum Ratings

Storage Temperature .....–55°C to +125°C
Supply Voltage port B .....–0.5V to +6.0V
Supply Voltage port A .....–0.5V to +6.0V
DC Input Voltage ..... –0.5V to +6.0V
Control Input Voltage (EN)… ..... –0.5V to +6.0V
Total Power Dissipation (1).....100mW
Input Current (EN, VCC, GND).....50mA
ESD: HBM Mode 8000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	V_{CCA} Positive DC Supply Voltage	1.65		5.5	V
V_{EN}	Enable Control Pin Voltage	GND		5.5	V
V_{IO}	I/O Pin Voltage	GND		5.5	V
Δt /ΔV	Input transition rise or fall time			10	ns/V
T_A	Operating Temperature Range	−40		+85	°C

DC Electrical Characteristics

Unless otherwise specified, -40°C ≤ T_A ≤ 85°C, 1.1V ≤ Vcc ≤ 3.6V

Symbol	Parameter	Conditions	VCC	Min	Typ	Max	Unit
Supply							
VCC	Supply Voltage			1.65		5.5	V
ICC	supply current	operating mode; no load, V_I = VCC or GND, f_{SCL} = 100kHz	3.6V to 5.5V		65	100	uA
			2.3V to 3.6V		20	50	uA
			1.65V to 2.3V		10	30	uA
Istb	standby current	standby mode; VCC = 3.6V, no load; V_I = VCC or GND, f_{SCL} = 0kHz	3.6V to 5.5V		0.3	1	uA
			2.3V to 3.6V		0.1	1	uA
			1.65V to 2.3V		0.1	1	uA
VPOR[1]	power-on reset voltage	no load; V_I = VCC or GND	3.6V to 5.5V		1.3	1.5	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage		1.65V to 5.5V	-0.5		+0.3VCC	V
V_{IH}	HIGH-level input voltage		1.65V to 2V	0.75VCC		6	V
			2V to 5.5V	0.7VCC		6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V	1.65V to 5.5V	3			mA
		V_{OL} = 0.6V	1.65V to 5.5V	6			mA
I_{IL}	LOW-level input current	V_I = GND	1.65V to 5.5V	-1		+1	uA
I_{IH}	HIGH-level input current	V_I = VCC	1.65V to 5.5V	-1		+1	uA
Ci	input capacitance	VI = GND	1.65V to 5.5V		14	19	pF
Select inputs A0, A1, A2, Reset							
V_{IL}	LOW-level input voltage		1.65V to 5.5V	-0.5		+0.3VCC	V
V_{IH}	HIGH-level input voltage		1.65V to 5.5V	0.7VCC		6	V
I_{IL}	LOW-level input current	V_I = GND	1.65V to 5.5V	-1		+1	uA
Ci	input capacitance	V_I = GND	1.65V to 5.5V		3	5	pF
Pass Gate							

Symbol	Parameter	Conditions	VCC	Min	Typ	Max	Unit
Ron	ON-state resistance	V_O = 0.4V, I_O = 15mA	4.5V to 5.5V	4	9	24	Ω
			3V to 3.6V	5	11	31	Ω
		V_O = 0.4V, I_O = 10mA	2.3V to 2.7V	7	16	55	Ω
			1.65V to 2V	9	20	70	Ω
Vpass	switch output voltage	Vin =VCC, Iout = -100uA	5V		3.6		V
			4.5V to 5.5V	2.8		4.5	V
			3.3V		2.2		V
			3V to 3.6V	1.6		2.8	V
			2.5V		1.5		V
			2.3V to 2.7V	1.1		2	V
			1.8V		0.9		V
			1.65V to 2V	0.54		1.3	V
I_L	leakage current	VI = VCC or GND	1.65V to 5.5V	-1		+1	uA
Cio	input/output capacitance	VI = VCC or GND	1.65V to 5.5V		3	5	pF

Note:
1. VCC must be lowered to 0.2 V for at least 5 us in order to reset part.

AC Electrical Characteristics

Tamb = -40°C to +85°C; unless otherwise specified.

Symbol	Parameter	Conditions	VCC	Min	Typ	Max	Unit
t_{PD}[1]	propagation delay	from SDA to SDx, or SCL to SCx	1.65V to 5.5V			0.3	ns
RESET							
tw(rst)L	LOW-level reset time		1.65V to 5.5V	4			ns
trst	reset time	SDA clear	1.65V to 5.5V	500			ns
$t_{REC;STA}$	recovery time to START condition		1.65V to 5.5V	0			ns

Note
1. Pass gate propagation delay is calculated from the 20 Ω typical Ron and the 15pF load capacitance.

I2C Interface Timing Requirements

Symbol	Parameter	STANDARD MODE I^2C BUS		FAST MODE I^2C BUS		Unit
		Min	Max	Min	Max	
fscl	I2C clock frequency	0	100	0	400	kHz
t_{Low}	I2C clock high time	4.7		1.3		µs
t_{High}	I2C clock low time	4		0.6		µs
t_{SP}	I2C spike time		50		50	ns
$t_{SU:DAT}$	I2C serial-data setup time	250		100		ns
$t_{HD:DAT}$	I2C serial-data hold time	0 [1]		0 [1]		µs
tr	I2C input rise time		1000		300	ns
tf	I2C input fall time		300		300	ns
t_{BUF}	I2C bus free time between stop and start	4.7		1.3		µs
$t_{SU:STA}$	I2C start or repeated start condition setup	4.7		0.6		µs
$t_{HD:STA}$	I2C start or repeated start condition hold	4		0.6		µs
$t_{SU:STO}$	I2C stop condition setup	4		0.6		µs
$t_{VD:DAT}$	Valid-data time (high to low) [2] SCL low to SDA output low valid		1		1	µs

Symbol	Parameter	STANDARD MODE I²C BUS		FAST MODE I²C BUS		Unit
		Min	Max	Min	Max	
	Valid-data time (low to high) [2] SCL low to SDA output high valid		0.6		0.6	µs
$t_{VD:ACK}$	Valid-data time of ACK condition ACK signal from SCL low to SDA output low		1		1	µs
Cb	I2C bus capacitive load		400		400	pF

Notes:
1. A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the VIH min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
2. Data taken using a 1-kΩ pull up resistor and 50-pF load Notes

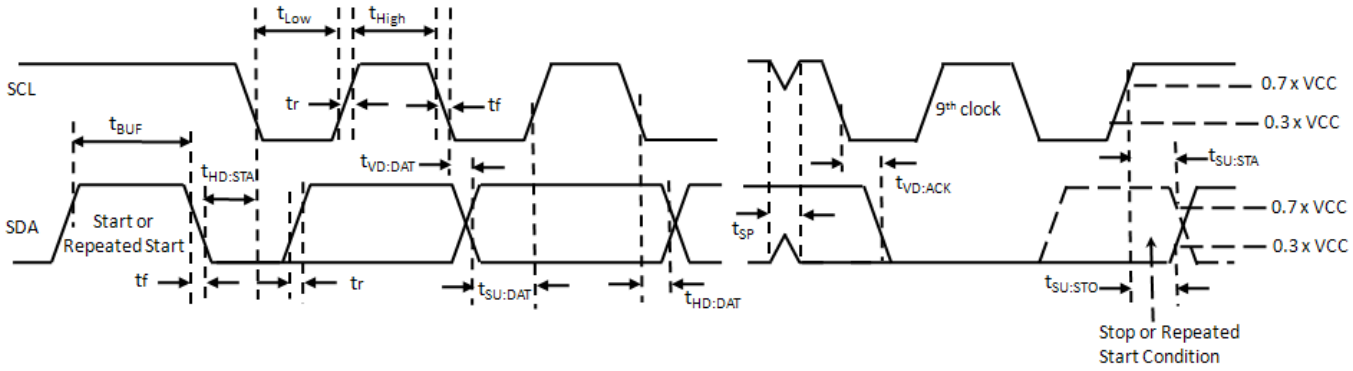


Figure 2. Definition of Timing on the I2C-bus

Application Information

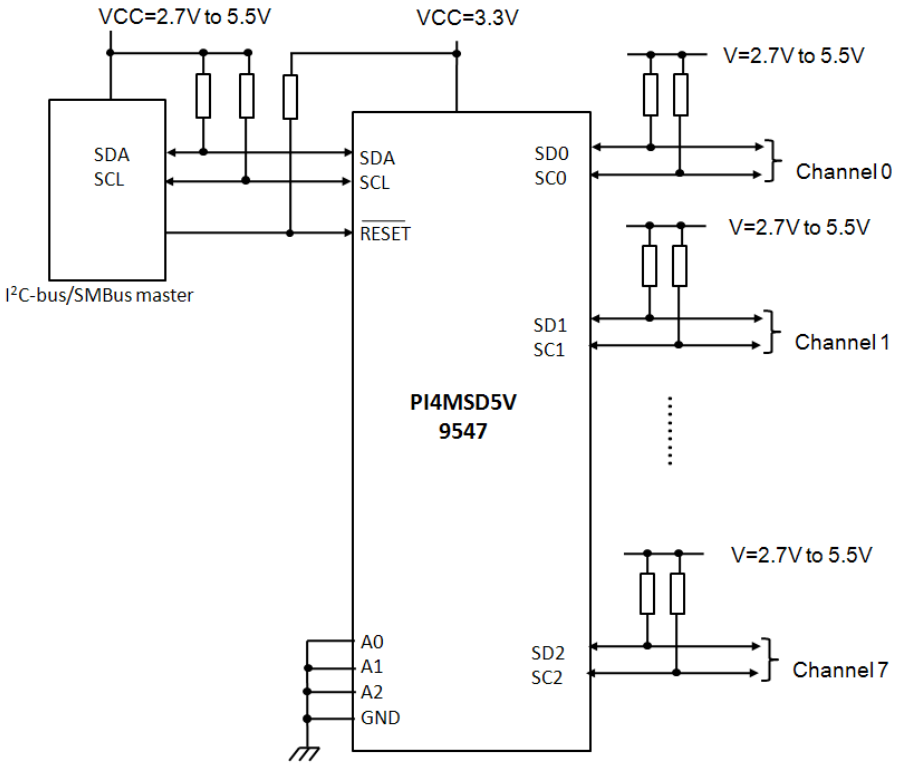


Figure 3. Typical Application

Recommended Application Voltage Condition

VCC	VPU1	VPU2
1.8V	1.5V-5.5V	1.2V-5.5V
2.5V	1.8V-5.5V	1.8V-5.5V
3.3V	2.7V-5.5V	2.7V-5.5V
5V	4.5V-5.5V	4.5V-5.5V

Device Addressing

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PI4MSD5V9547 is shown in Figure 4.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

Figure 4. Device Address

Control Register

Following the successful acknowledgement of the slave address, the bus master sends a byte to the PI4MSD5V9547 which is stored in the Control register. If multiple bytes are received by the PI4MSD5V9547, it saves the last byte received. This register can be written and read via the I2C-bus.

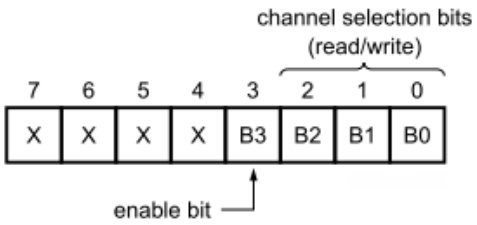


Figure 5. Control Register

Control Register Definition

A SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PI4MSD5V9547 has been addressed. The 4 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I2C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Table 1. Control Register

D7	D6	D5	D4	B3	B2	B1	B0	Command
X	X	X	X	0	X	X	X	no channel selected
X	X	X	X	1	0	0	0	channel 0 enabled
X	X	X	X	1	0	0	1	channel 1 enabled
X	X	X	X	1	0	1	0	channel 2 enabled
X	X	X	X	1	0	1	1	channel 3 enabled
X	X	X	X	1	1	0	0	channel 4 enabled
X	X	X	X	1	1	0	1	channel 5 enabled
X	X	X	X	1	1	1	0	channel 6 enabled
X	X	X	X	1	1	1	1	channel 7 enabled
0	0	0	0	1	0	0	0	channel 0 enabled; power-up/reset default state

Control register: Write — channel selection; Read — channel status

Power-On Reset

When power is applied to VCC, an internal Power-On Reset (POR) holds the PI4MSD5V9547 in a reset condition until VCC has reached VPOR. At this point, the reset condition is released and the PI4MSD5V9547 registers and I2C-bus state machine are initialized to their default states (all zeroes), causing all the channels to be deselected. Thereafter, VCC must be lowered below 0.2 V for at least 5 us in order to reset the device.

The Reset Input

The RESET input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of tw(rst)L, the PI4MSD5V9547 will reset its register and I2C-bus state machine and will deselect all channels. The RESET input must be connected to VCC through a pull-up resistor.

Voltage Translation

The pass gate transistors of the PI4MSD5V9547 are constructed such that the VCC voltage can be used to limit the maximum voltage that is passed from one I2C-bus to another.

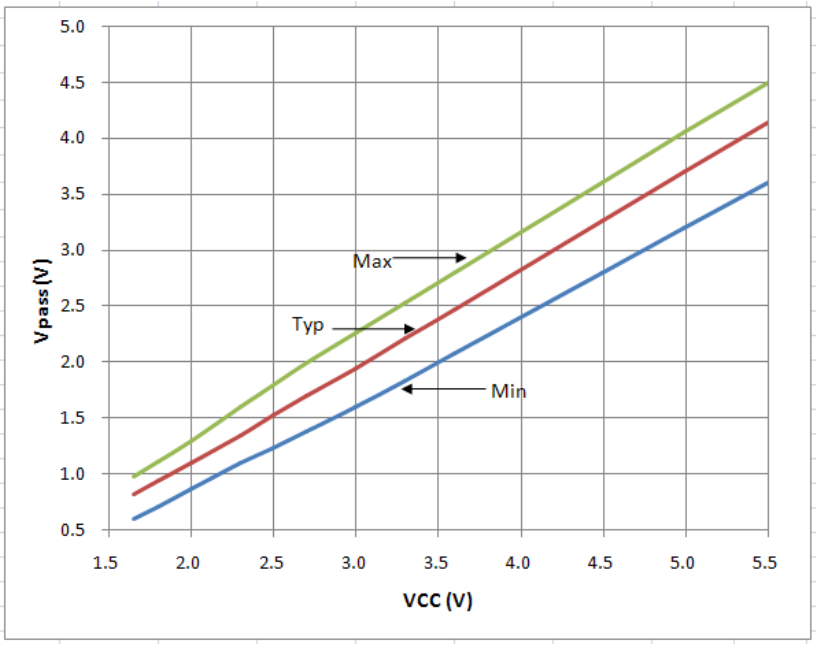


Figure 6. Vpass Voltage VS Vcc

Figure 6 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in Section "DC Electrical characteristics" of this data sheet).

In order for the PI4MSD5V9547 to act as a voltage translator, the Vpass voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5V, and the downstream buses were 3.3V and 2.7V, then Vpass should be equal to or below 2.7V to clamp the downstream bus voltages effectively.

Looking at Figure 6, we see that Vpass (max) is at 2.7V when the PI4MSD5V9547 supply voltage is 3.5V or lower so the PI4MSD5V9547 supply voltage could be set to 3.3V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels

I2C BUS

The I2C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals

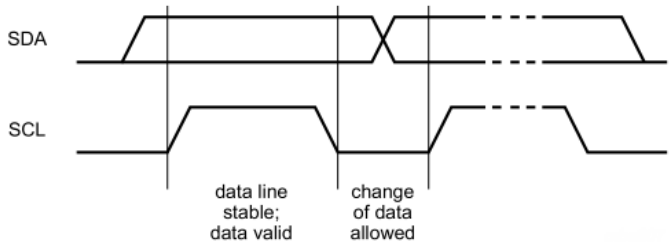


Figure 7. Bit Transfer

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P)

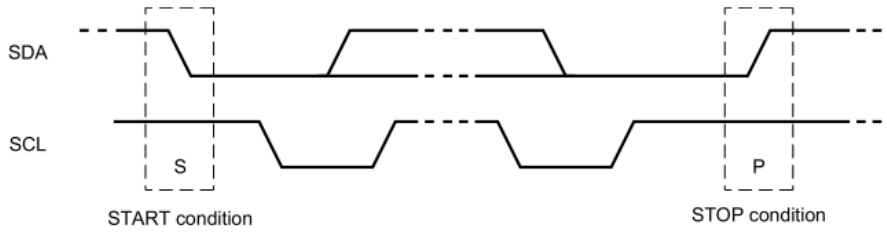


Figure 8. Definition of Start and Stop Conditions

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'

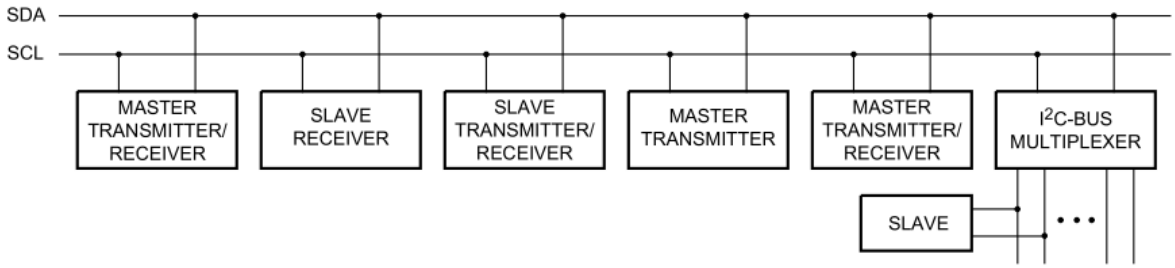


Figure 9. System Configuration

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of 8 bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

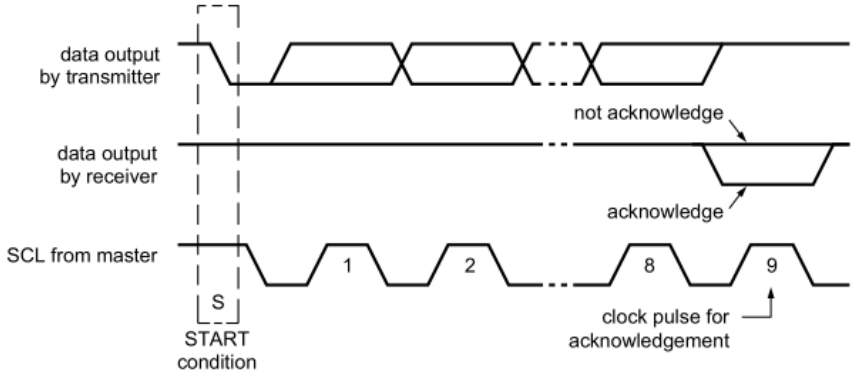


Figure 10. Acknowledgment on I2C Bus

Data is transmitted to the PI4MSD5V9547 control register using the write mode shown in bellow

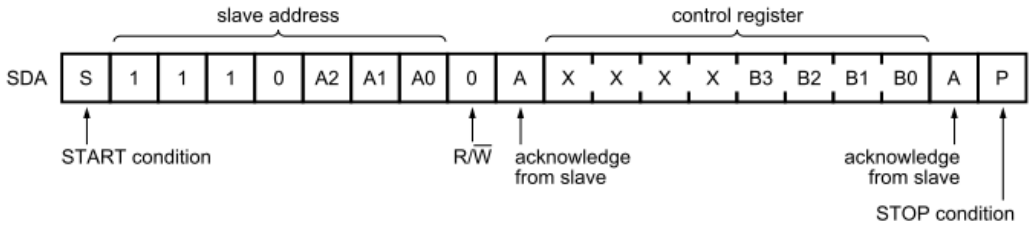


Figure 11. Write Control Register

Data is transmitted to the PI4MSD5V9547 control register using the write mode shown in bellow

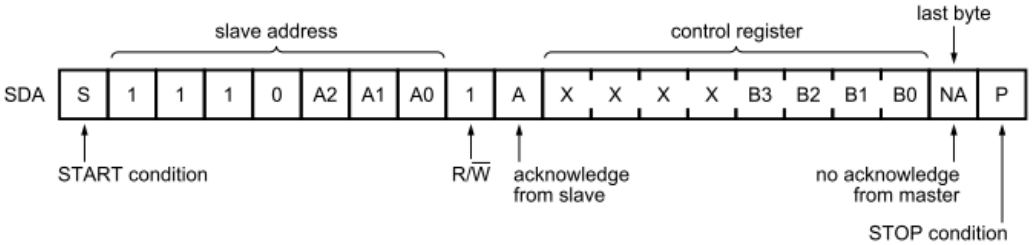


Figure 12. Read Control Register

Part Marking

L Package

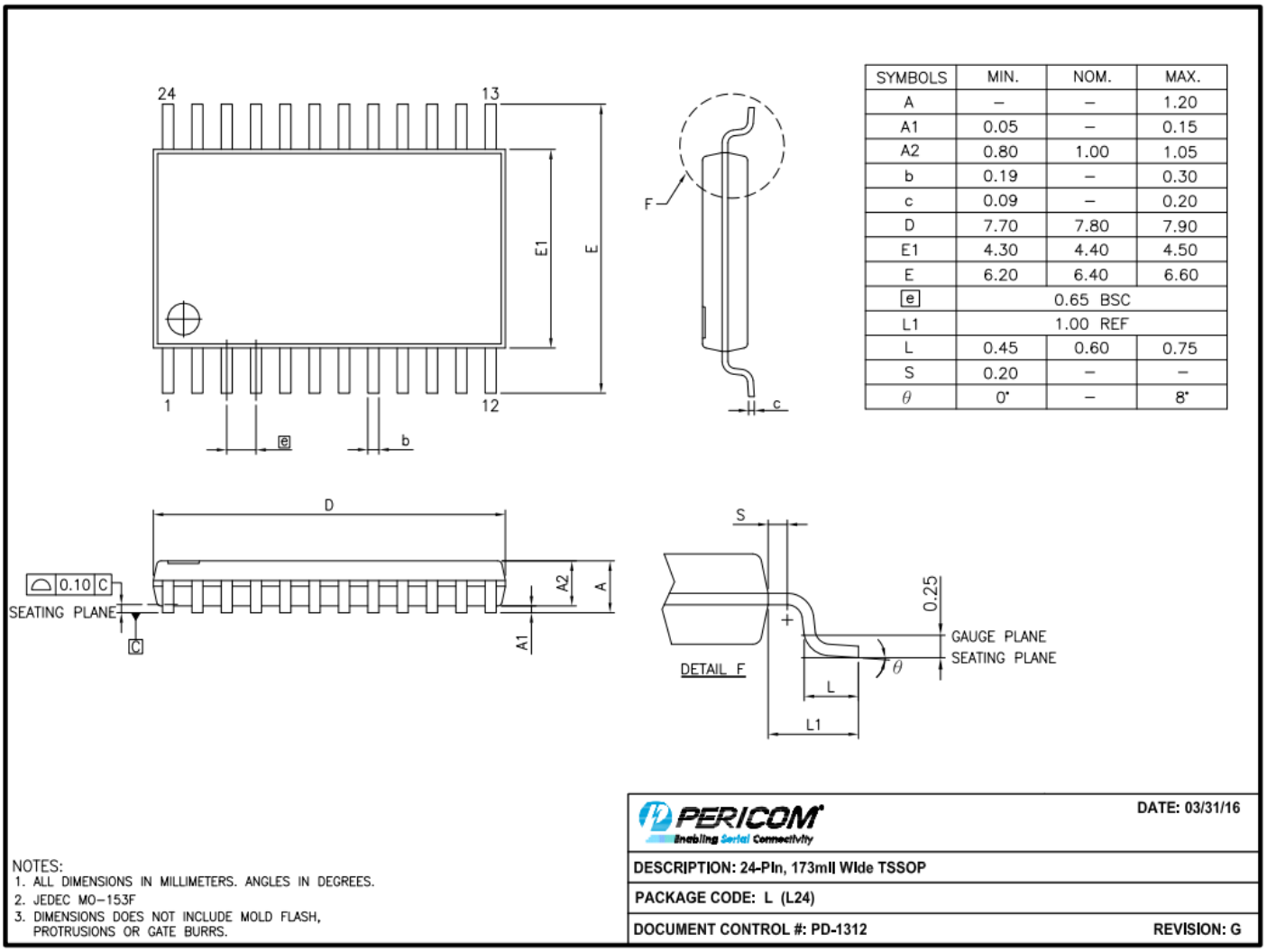
Z: Die Rev
YYWW: Date Code (Year & Workweek)
1st G: Assembly Site Code
2nd G: Wafer Fab Site Code
The Bar above 2nd "G" means Cu wire

ZD Package

Z: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd G: Wafer Fab Site Code
Bar above fab code means Cu wire

Packaging Mechanical

24-TSSOP (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

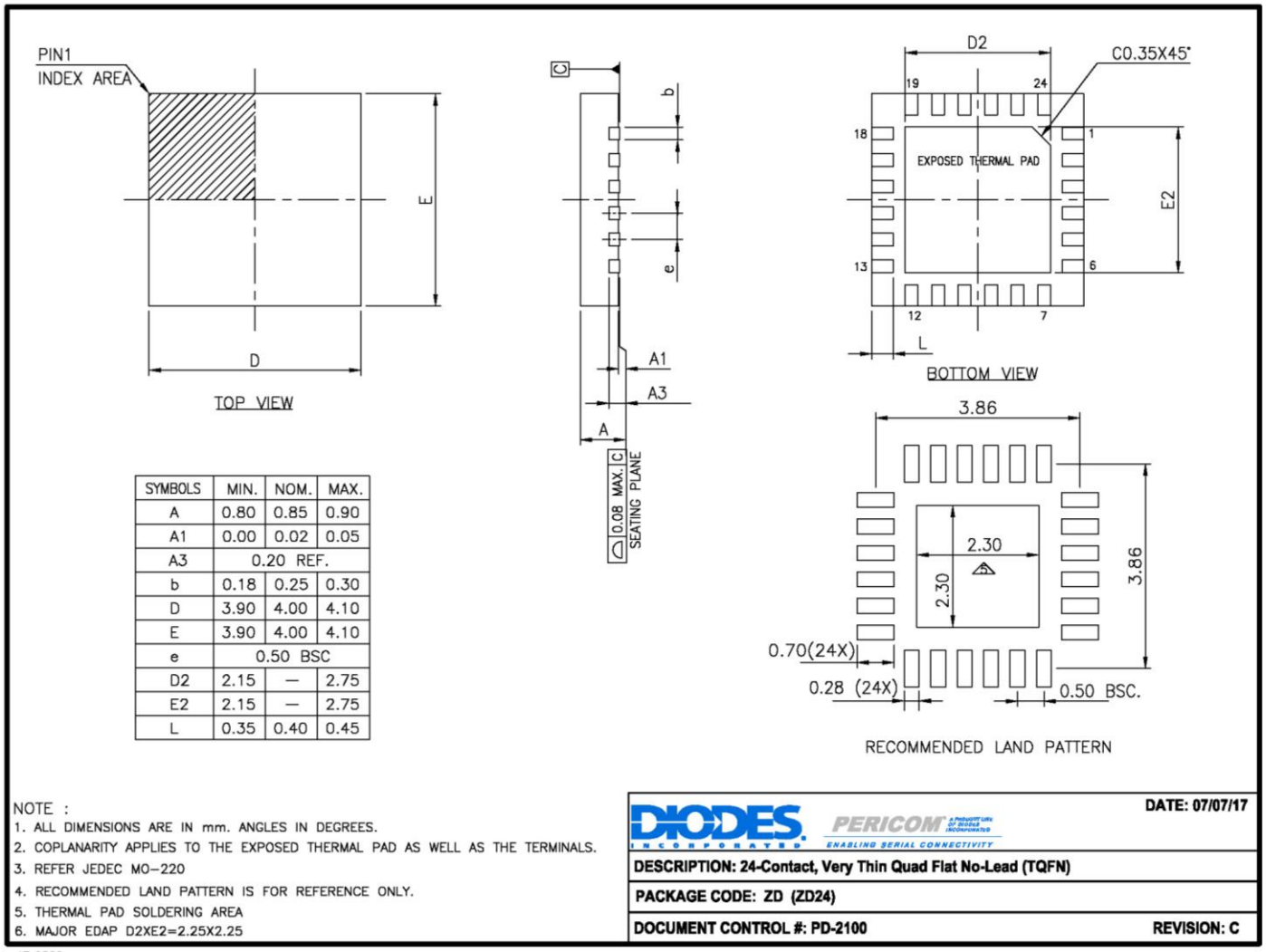
DATE: 03/31/16

DESCRIPTION: 24-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L24)

DOCUMENT CONTROL #: PD-1312 REVISION: G

24-TQFN (ZD)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e		0.50 BSC	
D2	2.15	—	2.75
E2	2.15	—	2.75
L	0.35	0.40	0.45

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA
6. MAJOR EDAP D2XE2=2.25X2.25

DATE: 07/07/17

DESCRIPTION: 24-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD (ZD24)

DOCUMENT CONTROL #: PD-2100 REVISION: C

17-0533

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Orderable Part Number	Package Code	Package Description	Status
PI4MSD5V9547LE	L	24-Pin,173 mil Wide (TSSOP)	NRND
PI4MSD5V9547LEX	L	24-Pin,173 mil Wide (TSSOP)	Active
PI4MSD5V9547ZDEX	ZD	24-Pin,Very Thin Quad Flat No-Lead (TQFN)	EOL

Notes:

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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