



Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

General Description

The MAX6439–MAX6442 are a family of ultra-low-power battery monitors with integrated microprocessor (μ P) supervisors. The battery monitors are offered with single or dual low-battery output options that can be used to signal when the battery is OK (enabling full system operation), when the battery is low (for low-power system operation), and when the battery is dead (to disable system operation). These devices also have an independent μ P supervisor that monitors V_{CC} and provides an active-low reset output. A manual reset function is available to reset the μ P with a push-button. No external components are required.

The MAX6439–MAX6442 are offered with several factory-trimmed low-battery threshold combinations ideal for single-cell lithium-ion (Li+) or multicell alkaline/NiCd/NiMH applications. When the battery voltage drops below each specified low threshold, the low-battery outputs are asserted to alert the system. When the voltage rises above the specified high thresholds, the outputs are deasserted after a 150ms minimum timeout period, ensuring the voltages have stabilized before power circuitry is activated or providing microprocessor reset timing. The low and high thresholds provide hysteresis in battery-operated systems to eliminate output chattering.

The MAX6439/MAX6440 offer factory-trimmed battery monitors with a single output. The MAX6441/MAX6442 offer factory-trimmed battery monitors with dual outputs. All battery monitors have open-drain low-battery outputs.

The MAX6439–MAX6442 monitor system voltages (V_{CC}) from 1.8V to 3.3V with seven fixed reset threshold options. Each device is offered with two minimum reset timeout periods of 150ms or 1200ms. The MAX6439/MAX6441 are offered with an open-drain \overline{RESET} output and the MAX6440/MAX6442 are offered with a push-pull \overline{RESET} output.

The MAX6439–MAX6442 are offered in a SOT23 package and are fully specified over a -40°C to $+85^{\circ}\text{C}$ temperature range.

Applications

Battery-Powered Systems (Single-Cell Li+ or Two-/Three-Cell NiMH, NiCd, Alkaline)

Cell Phones/Cordless Phones

Portable Medical Devices

Electronic Toys

Pagers

PDA's

MP3 Players

Features

- ◆ Factory-Trimmed V_{BATT} Threshold Options for Monitoring Single-Cell Li+ or Multicell Alkaline/NiCd/NiMH Applications
- ◆ Immune to Short Battery Voltage Transients
- ◆ Low Current (2.5 μ A typ at 3.6V)
- ◆ Single and Dual Low-Battery Output Options
- ◆ 150ms Minimum \overline{LBO} Timeout Period
- ◆ Independent μ P Reset with Manual Reset
- ◆ Factory-Set Reset Thresholds for Monitoring V_{CC} from 1.8V to 3.3V
- ◆ Available with 150ms (min) and 1.2s (min) V_{CC} Reset Timeout Period Options
- ◆ -40°C to $+85^{\circ}\text{C}$ Operating Temperature Range
- ◆ Small 6- and 8-Pin SOT23 Packages
- ◆ No External Components

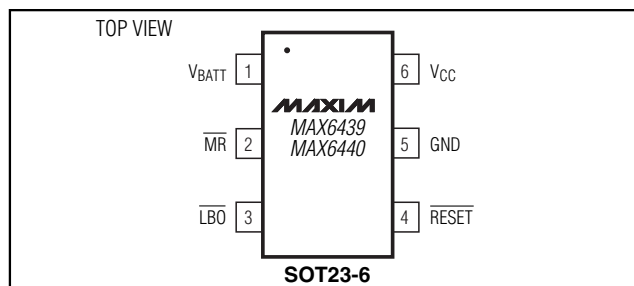
Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-----------------|--|-------------|
| MAX6439UT__D_-T | -40°C to $+85^{\circ}\text{C}$ | 6 SOT23-6 |
| MAX6440UT__D_-T | -40°C to $+85^{\circ}\text{C}$ | 6 SOT23-6 |
| MAX6441KA__D_-T | -40°C to $+85^{\circ}\text{C}$ | 8 SOT23-8 |
| MAX6442KA__D_-T | -40°C to $+85^{\circ}\text{C}$ | 8 SOT23-8 |

Note: The first two “_” are placeholders for the battery monitor voltage levels. Desired threshold levels are set by the part number suffix found in Tables 1 and 2. The third “_” is the V_{CC} reset threshold level suffix found in Table 3. The “_” after the D is a placeholder for the reset timeout period suffix found in Table 4. All devices are available in tape-and-reel only. There is a 2500-piece minimum order increment for standard versions. Sample stock is typically held on standard versions only. Nonstandard versions require a minimum order increment of 10,000 pieces. Contact factory for availability.

Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing “-T” with “+T” when ordering.

Pin Configurations



Pin Configurations continued at end of data sheet.



Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

ABSOLUTE MAXIMUM RATINGS

| | |
|---|------------------------------|
| V_{BATT} , V_{CC} to GND..... | -0.3V to +6V* |
| Open-Drain \overline{LBO} , \overline{LBOH} , \overline{LBOL} , \overline{LBOLH} to GND ... | -0.3V to +6V* |
| Open-Drain \overline{RESET} to GND | -0.3V to +6V* |
| Push-Pull \overline{RESET} to GND..... | -0.3V to ($V_{CC} + 0.3$ V) |
| \overline{MR} to GND | -0.3V to ($V_{CC} + 0.3$ V) |
| Input/Output Current, All Pins | 20mA |
| Continuous Power Dissipation ($T_A = +70^\circ\text{C}$) | |
| 6-Pin SOT23 (derate 8.7mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$)..... | 695mW |
| 8-Pin SOT23 (derate 8.9mW/ $^\circ\text{C}$ above +70 $^\circ\text{C}$)..... | 714mW |

| | |
|--|---|
| Operating Temperature Range | -40 $^\circ\text{C}$ to +85 $^\circ\text{C}$ |
| Junction Temperature..... | +150 $^\circ\text{C}$ |
| Storage Temperature Range | -65 $^\circ\text{C}$ to +150 $^\circ\text{C}$ |
| Lead Temperature (soldering, 10s)..... | +300 $^\circ\text{C}$ |

*Applying 7V for a duration of 1ms does not damage the device.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{BATT} = 1.2\text{V}$ to 5.5V, $V_{CC} = 1.2\text{V}$ to 5.5V, $T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$, unless otherwise specified. Typical values are at $T_A = +25^\circ\text{C}$.) (Note1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------------|--|-------|------|-------|---------------|
| V_{BATT} Operating Voltage Range | V_{BATT} | $T_A = 0^\circ\text{C}$ to +85 $^\circ\text{C}$ | 1.0 | | 5.5 | V |
| | | $T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$ | 1.2 | | 5.5 | |
| V_{CC} Operating Voltage Range | V_{CC} | $T_A = 0^\circ\text{C}$ to +85 $^\circ\text{C}$ | 1.0 | | 5.5 | V |
| | | $T_A = -40^\circ\text{C}$ to +85 $^\circ\text{C}$ | 1.2 | | 5.5 | |
| $V_{CC} + V_{BATT}$ Supply Current | $I_{CC} + I_{BATT}$ | $V_{BATT} = 3.6\text{V}$, $V_{CC} = 3.3\text{V}$, no load (Note 2) | | 2.5 | 7 | μA |
| V_{BATT} THRESHOLDS | | | | | | |
| HTH Threshold | HTH | MAX6439UT_J, MAX6440UT_J | 3.510 | 3.60 | 3.690 | V |
| | | MAX6439UT_I, MAX6440UT_I | 3.413 | 3.50 | 3.588 | |
| | | MAX6439UT_H, MAX6440UT_H | 3.315 | 3.40 | 3.485 | |
| | | MAX6439UT_G, MAX6440UT_G | 3.218 | 3.30 | 3.383 | |
| | | MAX6439UT_T, MAX6440UT_T | 2.535 | 2.60 | 2.665 | |
| | | MAX6439UT_S, MAX6440UT_S | 2.438 | 2.50 | 2.563 | |
| | | MAX6439UT_R, MAX6440UT_R | 2.340 | 2.40 | 2.460 | |
| | | MAX6439UT_Q, MAX6440UT_Q | 2.243 | 2.30 | 2.358 | |
| LTH Threshold | LTH | MAX6439UTF, MAX6440UTF | 3.023 | 3.10 | 3.178 | V |
| | | MAX6439UTE, MAX6440UTE | 2.925 | 3.00 | 3.075 | |
| | | MAX6439UTD, MAX6440UTD | 2.828 | 2.90 | 2.973 | |
| | | MAX6439UTC, MAX6440UTC | 2.730 | 2.80 | 2.870 | |
| | | MAX6439UTB, MAX6440UTB | 2.633 | 2.70 | 2.768 | |
| | | MAX6439UTA, MAX6440UTA | 2.535 | 2.60 | 2.665 | |
| | | MAX6439UTP, MAX6440UTP | 2.048 | 2.10 | 2.153 | |
| | | MAX6439UTO, MAX6440UTO | 1.950 | 2.00 | 2.050 | |
| | | MAX6439UTN, MAX6440UTN | 1.853 | 1.90 | 1.948 | |
| | | MAX6439UTM, MAX6440UTM | 1.755 | 1.80 | 1.845 | |
| | | MAX6439UTL, MAX6440UTL | 1.658 | 1.70 | 1.743 | |
| | | MAX6439UTK, MAX6440UTK | 1.560 | 1.60 | 1.640 | |

Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

MAX6439-MAX6442

ELECTRICAL CHARACTERISTICS (continued)

($V_{BATT} = 1.2V$ to $5.5V$, $V_{CC} = 1.2V$ to $5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise specified. Typical values are at $T_A = +25^{\circ}C$.) (Note1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|--------|--------------------------|-------|-------|-------|-------|
| HTH- Threshold | HTH- | MAX6441UT_J, MAX6442UT_J | 3.510 | 3.600 | 3.690 | V |
| | | MAX6441UT_I, MAX6442UT_I | 3.413 | 3.500 | 3.588 | |
| | | MAX6441UT_H, MAX6442UT_H | 3.315 | 3.400 | 3.485 | |
| | | MAX6441UT_G, MAX6442UT_G | 3.218 | 3.300 | 3.383 | |
| | | MAX6441UT_T, MAX6442UT_T | 2.535 | 2.600 | 2.665 | |
| | | MAX6441UT_S, MAX6442UT_S | 2.438 | 2.500 | 2.563 | |
| | | MAX6441UT_R, MAX6442UT_R | 2.340 | 2.400 | 2.460 | |
| HTH+ Threshold | HTH+ | MAX6441UT_J, MAX6442UT_J | 3.686 | 3.780 | 3.875 | V |
| | | MAX6441UT_I, MAX6442UT_I | 3.583 | 3.675 | 3.767 | |
| | | MAX6441UT_H, MAX6442UT_H | 3.481 | 3.570 | 3.659 | |
| | | MAX6441UT_G, MAX6442UT_G | 3.378 | 3.465 | 3.552 | |
| | | MAX6441UT_T, MAX6442UT_T | 2.662 | 2.730 | 2.798 | |
| | | MAX6441UT_S, MAX6442UT_S | 2.559 | 2.625 | 2.691 | |
| | | MAX6441UT_R, MAX6442UT_R | 2.457 | 2.520 | 2.583 | |
| LTH- Threshold | LTH- | MAX6441UTF, MAX6442UTF | 3.023 | 3.100 | 3.178 | V |
| | | MAX6441UTE, MAX6442UTE | 2.925 | 3.000 | 3.075 | |
| | | MAX6441UTD, MAX6442UTD | 2.828 | 2.900 | 2.973 | |
| | | MAX6441UTC, MAX6442UTC | 2.730 | 2.800 | 2.870 | |
| | | MAX6441UTB, MAX6442UTB | 2.633 | 2.700 | 2.768 | |
| | | MAX6441UTA, MAX6442UTA | 2.535 | 2.600 | 2.665 | |
| | | MAX6441UTP, MAX6442UTP | 2.048 | 2.100 | 2.153 | |
| | | MAX6441UTO, MAX6442UTO | 1.950 | 2.000 | 2.050 | |
| | | MAX6441UTN, MAX6442UTN | 1.853 | 1.900 | 1.948 | |
| | | MAX6441UTM, MAX6442UTM | 1.755 | 1.800 | 1.845 | |
| | | MAX6441UTL, MAX6442UTL | 1.658 | 1.700 | 1.743 | |
| LTH+ Threshold | LTH+ | MAX6441UTF, MAX6442UTF | 3.174 | 3.255 | 3.337 | V |
| | | MAX6441UTE, MAX6442UTE | 3.071 | 3.150 | 3.229 | |
| | | MAX6441UTD, MAX6442UTD | 2.969 | 3.045 | 3.121 | |
| | | MAX6441UTC, MAX6442UTC | 2.867 | 2.940 | 3.014 | |
| | | MAX6441UTB, MAX6442UTB | 2.764 | 2.835 | 2.906 | |
| | | MAX6441UTA, MAX6442UTA | 2.662 | 2.730 | 2.798 | |
| | | MAX6441UTP, MAX6442UTP | 2.150 | 2.205 | 2.260 | |
| | | MAX6441UTO, MAX6442UTO | 2.048 | 2.100 | 2.153 | |
| | | MAX6441UTN, MAX6442UTN | 1.945 | 1.995 | 2.045 | |
| | | MAX6441UTM, MAX6442UTM | 1.843 | 1.890 | 1.937 | |
| | | MAX6441UTL, MAX6442UTL | 1.740 | 1.785 | 1.830 | |
| MAX6441UTK, MAX6442UTK | 1.638 | 1.680 | 1.722 | | | |

Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

ELECTRICAL CHARACTERISTICS (continued)

($V_{BATT} = 1.2V$ to $5.5V$, $V_{CC} = 1.2V$ to $5.5V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise specified. Typical values are at $T_A = +25^\circ C$.) (Note1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|--|-------|-------|---------------------|----------|
| \overline{LBO} , \overline{LBOL} , \overline{LBOH} , \overline{LBOLH} Timeout Period | t_{LBOP} | V_{BATT} rising above threshold | 150 | 225 | 300 | ms |
| \overline{LBO} , \overline{LBOL} , \overline{LBOH} , \overline{LBOLH} Delay Time | t_{LBOD} | V_{BATT} falling below threshold | | 100 | | μs |
| \overline{LBO} , \overline{LBOL} , \overline{LBOH} , \overline{LBOLH} Output Low (Open Drain) | V_{OL} | (V_{BATT} or V_{CC}) $\geq 1.2V$, $I_{SINK} = 50\mu A$, asserted low | | | 0.3 | V |
| | | (V_{BATT} or V_{CC}) $\geq 1.6V$, $I_{SINK} = 100\mu A$, asserted low | | | 0.3 | |
| | | (V_{BATT} or V_{CC}) $\geq 2.7V$, $I_{SINK} = 1.2mA$, asserted low | | | 0.3 | |
| | | (V_{BATT} or V_{CC}) $\geq 4.5V$, $I_{SINK} = 3.2mA$, asserted low | | | 0.3 | |
| \overline{LBO} , \overline{LBOL} , \overline{LBOH} , \overline{LBOLH} Output Open-Drain Leakage Current | I_{LKG} | Output deasserted | | | 500 | nA |
| VCC Reset Threshold | V_{TH} | MAX64_----- T | 3.000 | 3.075 | 3.150 | V |
| | | MAX64_----- S | 2.850 | 2.925 | 3.000 | |
| | | MAX64_----- R | 2.550 | 2.625 | 2.700 | |
| | | MAX64_----- Z | 2.250 | 2.313 | 2.375 | |
| | | MAX64_----- Y | 2.125 | 2.188 | 2.250 | |
| | | MAX64_----- W | 1.620 | 1.665 | 1.710 | |
| | | MAX64_----- V | 1.530 | 1.575 | 1.620 | |
| VCC Reset Hysteresis | | | 0.3 | | | % |
| VCC to \overline{RESET} Delay | | VCC falling at $10mV/\mu s$ from ($V_{TH} + 100mV$) to ($V_{TH} - 100mV$) | | 50 | | μs |
| VCC to \overline{RESET} Timeout Period | t_{RP} | MAX64_----- D3 | 150 | 225 | 300 | ms |
| | | MAX64_----- D7 | 1200 | 1800 | 2400 | |
| \overline{MR} Input Voltage | V_{IL} | | | | $0.3 \times V_{CC}$ | V |
| | V_{IH} | | | | $0.7 \times V_{CC}$ | |
| \overline{MR} Minimum Pulse Width | t_{MPW} | | 1 | | | μs |
| \overline{MR} Glitch Rejection | | | | 100 | | ns |
| \overline{MR} to \overline{RESET} Delay | | | | 200 | | ns |
| \overline{MR} Reset Timeout Period | t_{MRP} | | 150 | 225 | 300 | ms |
| \overline{MR} Pullup Resistance | | \overline{MR} to VCC | 750 | 1500 | 2250 | Ω |
| \overline{MR} Rising Debounce Period | t_{DEB} | (Note 3) | 150 | 225 | 300 | ms |

Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

ELECTRICAL CHARACTERISTICS (continued)

($V_{BATT} = 1.2V$ to $5.5V$, $V_{CC} = 1.2V$ to $5.5V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise specified. Typical values are at $T_A = +25^\circ C$.) (Note1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------|---|---------------------|-----|-----|-------|
| \overline{RESET} Output High (Push-Pull) | V_{OH} | $V_{CC} \geq 1.53V$, $I_{SOURCE} = 100\mu A$, \overline{RESET} deasserted | $0.8 \times V_{CC}$ | | | V |
| | | $V_{CC} \geq 2.55V$, $I_{SOURCE} = 500\mu A$, \overline{RESET} deasserted | $0.8 \times V_{CC}$ | | | |
| \overline{RESET} Output Low | V_{OL} | $V_{CC} \geq 1.0V$, $I_{SINK} = 50\mu A$, \overline{RESET} asserted | 0.3 | | | V |
| | | $V_{CC} \geq 1.2V$, $I_{SINK} = 100\mu A$, \overline{RESET} asserted | 0.3 | | | |
| | | $V_{CC} \geq 2.12V$, $I_{SINK} = 1.2mA$, \overline{RESET} asserted | 0.3 | | | |
| \overline{RESET} Output Leakage Current (Open Drain) | | \overline{RESET} deasserted | 500 | | | nA |

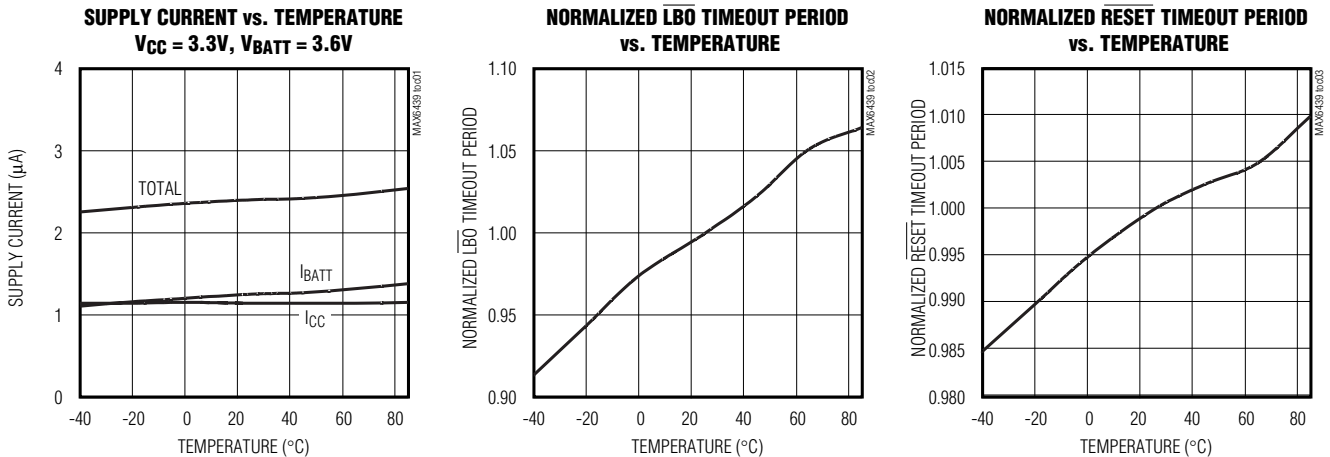
Note 1: Production testing done at $T_A = +25^\circ C$; limits over temperature guaranteed by design only.

Note 2: The device is powered up by the highest voltage between V_{BATT} and V_{CC} .

Note 3: \overline{MR} input ignores falling input pulses, which occur within the \overline{MR} debounce period (t_{DEB}) after a valid \overline{MR} reset assertion. This prevents invalid reset assertion due to switch bounce.

Typical Operating Characteristics

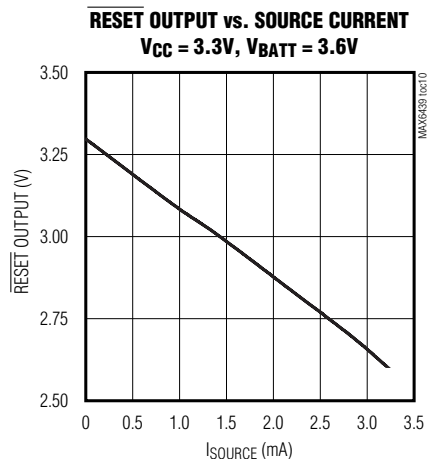
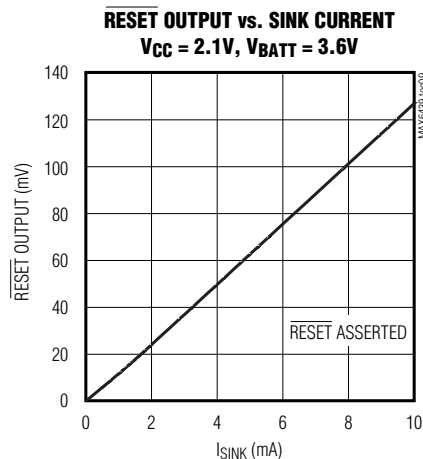
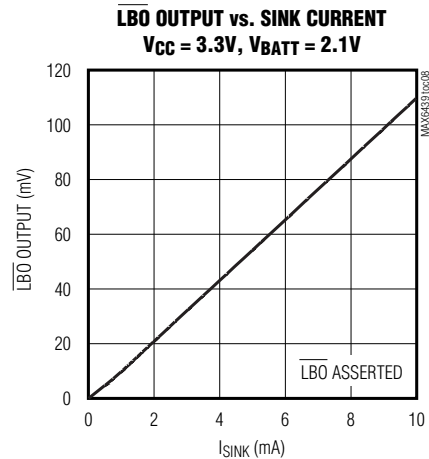
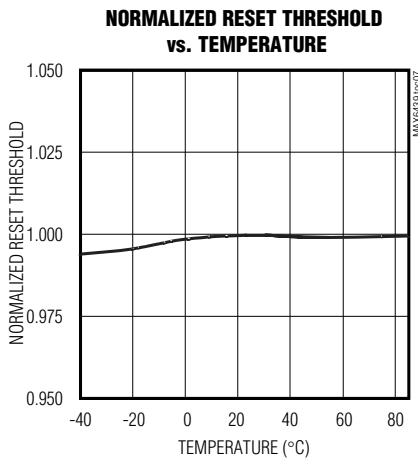
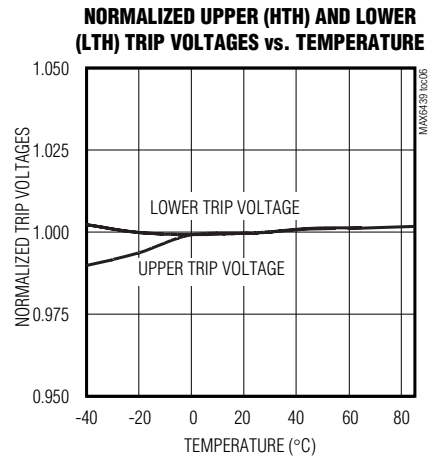
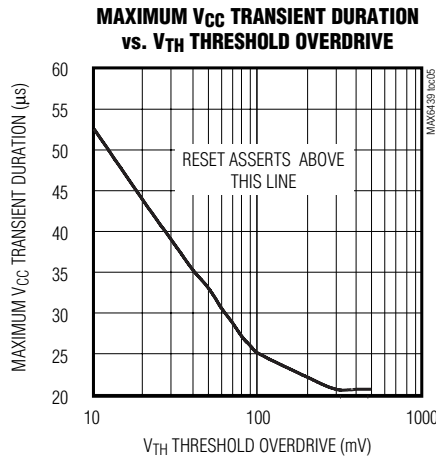
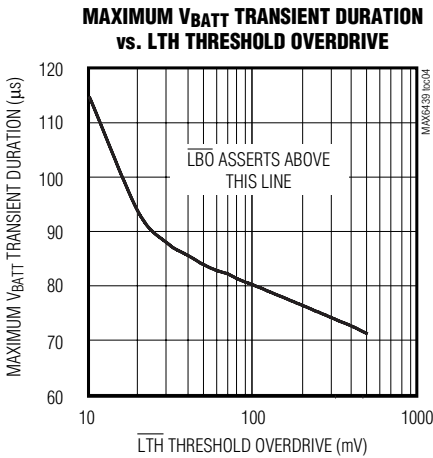
($V_{BATT} = 1.2V$ to $5.5V$, $V_{CC} = 1.2V$ to $5.5V$, unless otherwise specified. Typical values are at $T_A = +25^\circ C$.)



Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

Typical Operating Characteristics (continued)

($V_{BATT} = 1.2V$ to $5.5V$, $V_{CC} = 1.2V$ to $5.5V$, unless otherwise specified. Typical values are at $T_A = +25^\circ C$.)



Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

Pin Description

MAX6439-MAX6442

| PIN | | NAME | FUNCTION |
|---------------------|---------------------|---------------------------|---|
| MAX6439/ MAX6440 | MAX6441/ MAX6442 | | |
| 1 | 1 | V _{BATT} | Battery Voltage Input. Input for battery voltage threshold monitors and device power supply if V _{BATT} is greater than V _{CC} . |
| 2 | 3 | $\overline{\text{MR}}$ | Manual Reset Input, Active-Low, Internal 1.5k Ω Pullup to V _{CC} . Pull low to assert a one-shot edge-triggered $\overline{\text{RESET}}$ output for the $\overline{\text{MR}}$ reset timeout period. Leave unconnected or connect to V _{CC} if unused. The $\overline{\text{MR}}$ input is debounced for $\overline{\text{MR}}$ rising edges to prevent false reset events. |
| 3 | — | $\overline{\text{LBO}}$ | Low-Battery Output, Active Low, Open Drain. $\overline{\text{LBO}}$ is asserted when V _{BATT} drops below the LTH specification and remains asserted until V _{BATT} rises above the HTH specification for at least 150ms. |
| 4 | 5 | $\overline{\text{RESET}}$ | Reset Output, Active Low, Push-Pull or Open Drain. $\overline{\text{RESET}}$ changes from high to low when the V _{CC} input drops below the selected reset threshold and remains low for the V _{CC} reset timeout period after V _{CC} exceeds the reset threshold. $\overline{\text{RESET}}$ is one-shot edge-trigger pulsed low for the $\overline{\text{MR}}$ reset timeout period when the $\overline{\text{MR}}$ input is pulled low. $\overline{\text{RESET}}$ is an open-drain output for the MAX6439/MAX6441, and a push-pull output for the MAX6440/MAX6442. The push-pull outputs are referenced to V _{CC} . $\overline{\text{RESET}}$ is guaranteed to be in the correct logic state for V _{BATT} or V _{CC} > 1.0V. |
| 5 | 2 | GND | Ground |
| 6 | 8 | V _{CC} | V _{CC} Voltage Input. Input for V _{CC} reset threshold monitor and device power supply if V _{CC} is greater than V _{BATT} . |
| — | 6 | $\overline{\text{LBOH}}$ | Low-Battery Output High, Active Low, Open Drain. $\overline{\text{LBOH}}$ is asserted when V _{BATT} drops below the HTH- specification. $\overline{\text{LBOH}}$ is deasserted when V _{BATT} rises above the HTH+ specification for at least 150ms. |
| — | 7 | $\overline{\text{LBOL}}$ | Low-Battery Output Low, Active Low, Open Drain. $\overline{\text{LBOL}}$ is asserted when V _{BATT} drops below the LTH- specification. $\overline{\text{LBOL}}$ is deasserted when V _{BATT} rises above the LTH+ specification for at least 150ms. |
| — | 4 | $\overline{\text{LBOLH}}$ | Low-Battery Output Low/High, Active Low, Open Drain. $\overline{\text{LBOLH}}$ is asserted when V _{BATT} drops below the LTH- specification. $\overline{\text{LBOLH}}$ is deasserted when V _{BATT} rises above the HTH+ specification for at least 150ms. |

Detailed Description

The MAX6439-MAX6442 family is available with several monitoring options. The factory-trimmed thresholds eliminate the requirement for external components. The MAX6439/MAX6440 have single low-battery outputs and the MAX6441/MAX6442 have dual low-battery outputs (see Figure 1a and Figure 1b).

The MAX6439-MAX6442 combine a 1.23V reference with two comparators, logic, and timing circuitry to provide the user with information about the charge state of the power-supply batteries. The MAX6441/MAX6442

monitor separate high-voltage and low-voltage thresholds to determine battery status. The output(s) can be used to signal when the battery is charged, when the battery is low, and when the battery is empty. Factory-trimmed thresholds are ideal for monitoring single-cell Li+ or multicell alkaline/NiCd/NiMH power supplies.

When the power-supply voltage drops below the specified low threshold, the low-battery output asserts. When the voltage rises above the specified high threshold following a 150ms (min) timeout period, the low-battery output is deasserted. This ensures the supply voltage

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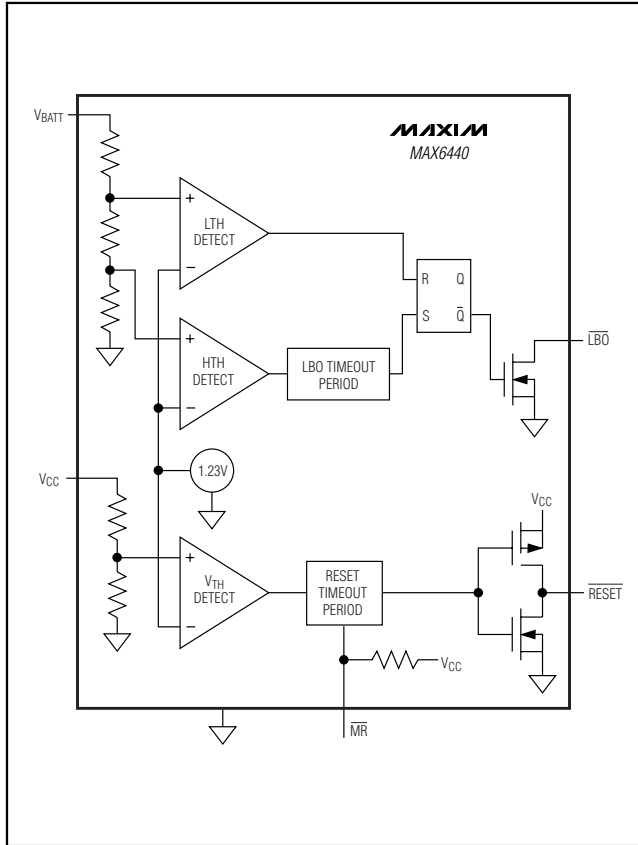


Figure 1a. Functional Diagram

has stabilized before power-converter or microprocessor activity is enabled.

These devices also have an independent μ P supervisor that monitors V_{CC} and provides an active-low reset output. A manual reset function is available to allow the user to reset the μ P with a push-button.

Low-Battery Output

The low-battery outputs are available in active-low (\overline{LBO} , \overline{LBOL} , \overline{LBOH} , \overline{LBOLH}), open-drain configurations. The low-battery outputs can be pulled to a voltage independent of V_{CC} or V_{BATT} , up to 5.5V. This allows the device to monitor and operate from direct battery voltage while interfacing to higher voltage microprocessors.

The MAX6439/MAX6440 single-output voltage monitors provide a single low-battery output, \overline{LBO} . These fixed-threshold devices assert \overline{LBO} when V_{BATT} drops below V_{LTH-} and remain asserted for at least 150ms after V_{BATT} rises above V_{LTH+} (see Figure 2). The MAX6441/MAX6442 triple-output voltage monitors provide three

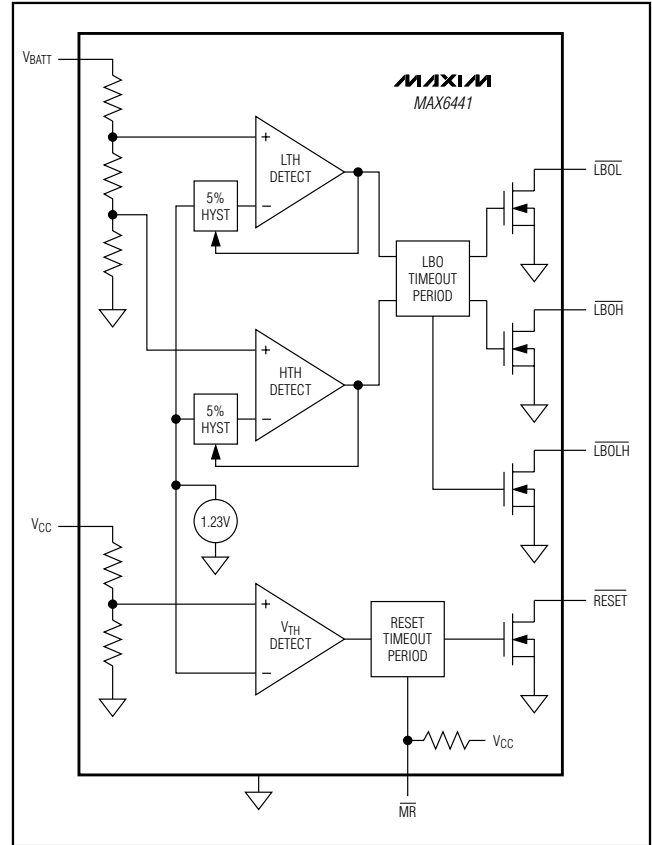


Figure 1b. Functional Diagram

low-battery outputs: \overline{LBOH} , \overline{LBOL} , and \overline{LBOLH} . \overline{LBOH} asserts when V_{BATT} drops below V_{HTH-} and remains asserted for at least 150ms after V_{BATT} rises above V_{HTH+} . \overline{LBOL} asserts when V_{BATT} drops below V_{LTH-} and remains asserted for at least 150ms after V_{BATT} rises above V_{LTH+} . \overline{LBOLH} asserts when V_{BATT} drops below V_{LTH-} and remains asserted for at least 150ms after V_{BATT} rises above V_{LTH+} (see Figure 3). For fast-rising V_{BATT} input, the \overline{LBOL} timeout period must complete before the $\overline{LBOH}/\overline{LBOLH}$ timeout period begins.

Reset Output

The MAX6439-MAX6442 provide an active-low reset output (\overline{RESET}). \overline{RESET} is asserted when the voltage at V_{CC} falls below the reset threshold level. Reset remains asserted for the reset timeout period after V_{CC} exceeds the threshold. If V_{CC} goes below the reset threshold before the reset timeout period is completed, the internal timer restarts. The MAX6439/MAX6441 have open-drain reset outputs, while the MAX6440/MAX6442 have push-pull reset outputs (see Figure 4).

Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

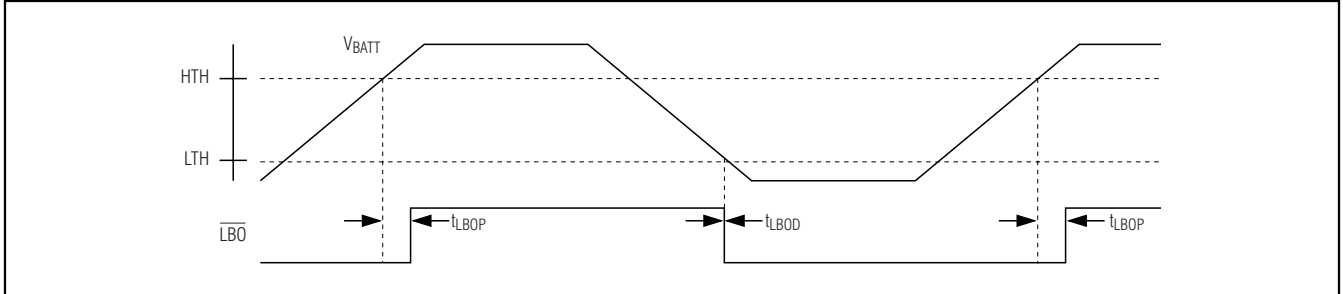


Figure 2. Single Low-Battery Output Timing

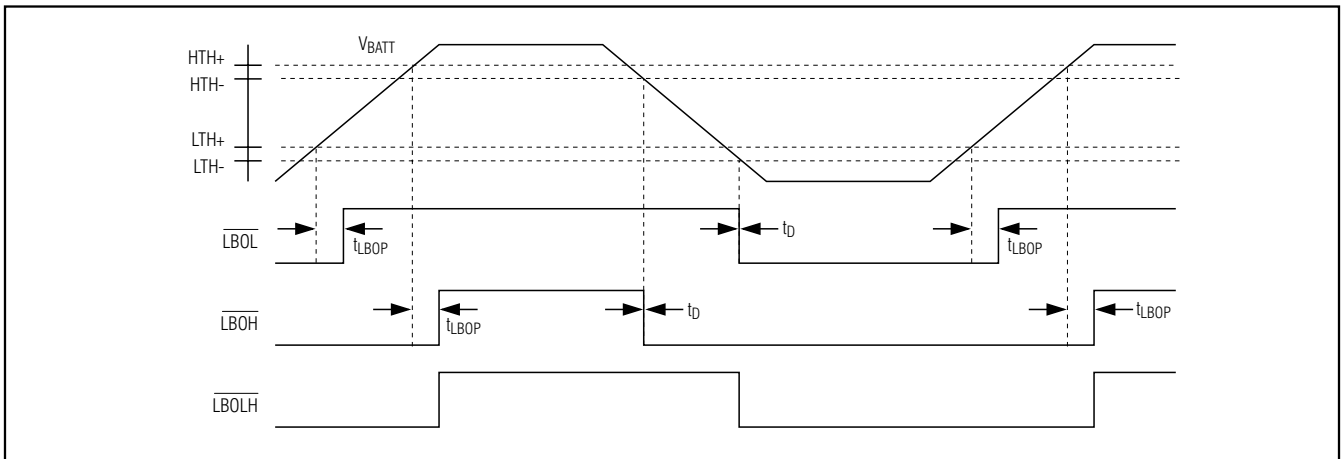


Figure 3. Dual Low-Battery Output Timing

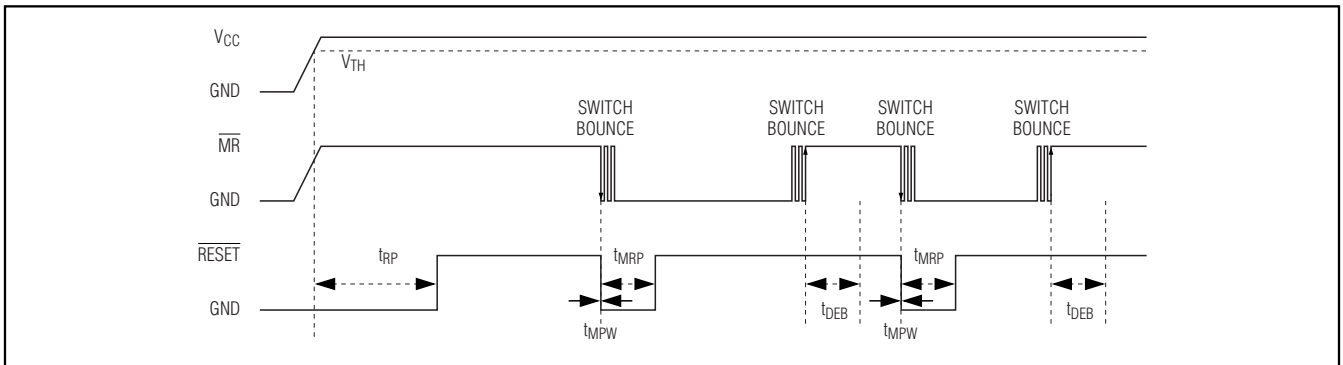


Figure 4. $\overline{\text{RESET}}$ Timing Diagram

Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μP Reset

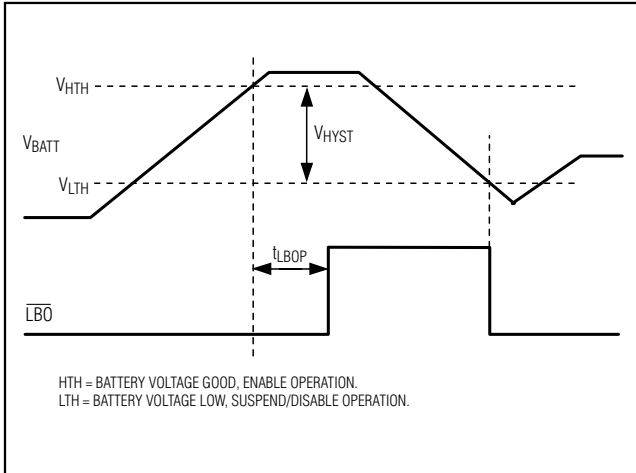


Figure 5. Hysteresis

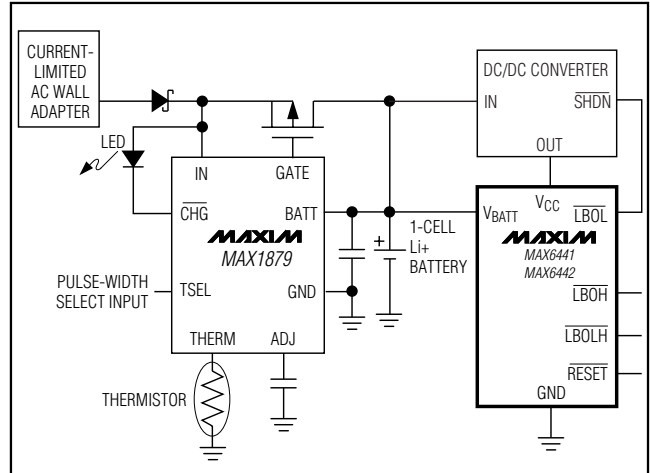


Figure 6. Li+ Charger Application (Using MAX1879)

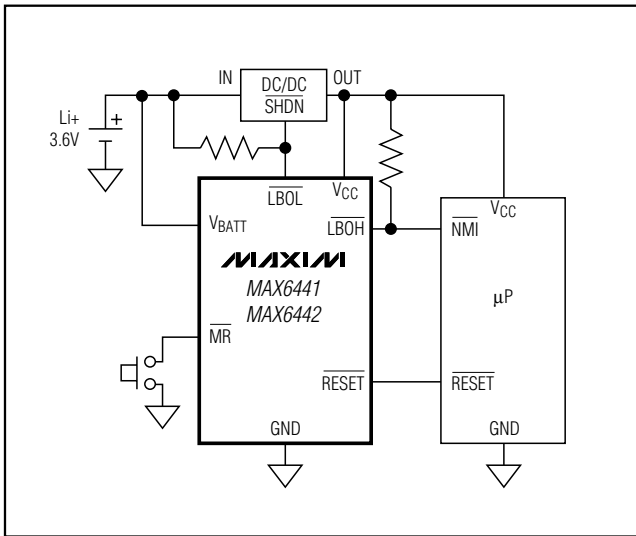


Figure 7. DC-to-DC Converter Application

Manual Reset

Many microprocessor-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset while the monitored supplies remain above their reset thresholds. These devices have a dedicated active-low \overline{MR} pin. When \overline{MR} is pulled low, \overline{RESET} asserts a one-shot low pulse for the \overline{MR} reset timeout period. The \overline{MR} input has an internal 1.5k Ω pullup resistor to VCC and can be left unconnected if not used. \overline{MR} can be driven with CMOS-

logic levels, open-drain/open-collector outputs, or a momentary push-button switch to GND (the MR function is internally debounced for the t_{DEB} timeout period) to create a manual reset function. If MR is driven from long cables, or if the device is used in a noisy environment, connect a 0.1 μF capacitor from \overline{MR} to GND to provide additional noise immunity (see Figure 4).

Hysteresis

Hysteresis increases the comparator's noise margin by increasing the upper threshold or decreasing the lower threshold. The hysteresis prevents the output from oscillating (chattering) when V_{BATT} is near the low-battery threshold. This is especially important for applications where the load on the battery creates significant fluctuations in battery voltages (see Figure 5).

Applications Information

Li+ Battery Charger Application

The MAX6441/MAX6442 dual-output battery monitors can be used in conjunction with a battery charger to provide a system with additional information about the battery charge state. Many battery chargers, such as the MAX1879, provide the user with a CHG output, which tells the system when the battery is charged. The MAX6441/MAX6442 dual-output battery monitors provide three outputs, which can be used to relay the battery condition to the system. This information is useful in determining which system resources can be powered by the battery at the current charge state (see Figure 6).

Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

Table 1. Factory-Trimmed Lower and Upper Threshold Combinations for Single-Cell Li+ or Three-Cell Alkaline/NiCd/NiMH Applications

| LOWER THRESHOLD (LTH) | VOLTAGES | UPPER THRESHOLD (HTH) | | | |
|-----------------------|----------|-----------------------|------|------|------|
| | | 3.3V | 3.4V | 3.5V | 3.6V |
| | 2.6V | AG | AH | AI | AJ |
| | 2.7V | BG | BH | BI | BJ |
| | 2.8V | CG | CH | CI | CJ |
| | 2.9V | DG | DH | DI | DJ |
| | 3.0V | EG | EH | EI | EJ |
| | 3.1V | FG | FH | FI | FJ |

Table 2. Factory-Trimmed Lower and Upper Threshold Combinations for Two-Cell Alkaline/NiCd/NiMH Applications

| LOWER THRESHOLD (LTH) | VOLTAGES | UPPER THRESHOLD (HTH) | | | |
|-----------------------|----------|-----------------------|------|------|------|
| | | 2.3V | 2.4V | 2.5V | 2.6V |
| | 1.6V | KQ | KR | KS | KT |
| | 1.7V | LQ | LR | LS | LT |
| | 1.8V | MQ | MR | MS | MT |
| | 1.9V | NQ | NR | NS | NT |
| | 2.0V | OQ | OR | OS | OT |
| | 2.1V | PQ | PR | PS | PT |

Table 3. Factory-Trimmed VCC Reset Threshold Levels

| PART NO. SUFFIX (_) | VCC NOMINAL RESET THRESHOLD (V) |
|-----------------------|---------------------------------|
| T | 3.075 |
| S | 2.925 |
| R | 2.625 |
| Z | 2.313 |
| Y | 2.188 |
| W | 1.665 |
| V | 1.575 |

DC-to-DC Converter Application

The MAX6441/MAX6442 triple-output battery monitors can be used in conjunction with a DC-to-DC converter to power microprocessor systems using a single Li+ cell or two to three alkaline/NiCd/NiMH cells. The $\overline{\text{LBOH}}$ output indicates that the battery voltage is weak, and is used to warn the microprocessor of potential problems. Armed with this information, the microprocessor can

Table 4. VCC Reset Timeout Period Suffix Guide

| TIMEOUT PERIOD SUFFIX | ACTIVE TIMEOUT PERIOD (ms) | |
|-----------------------|----------------------------|------|
| | MIN | MAX |
| D3 | 150 | 300 |
| D7 | 1200 | 2400 |

reduce system power consumption. The $\overline{\text{LBOL}}$ output indicates the battery is empty, and system power should be disabled. By connecting $\overline{\text{LBOL}}$ to the SHDN pin of the DC-to-DC converter, power to the microprocessor is removed. Microprocessor power does not return until the battery has recharged to a voltage greater than $V_{\text{LTH+}}$ (see Figure 7).

Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

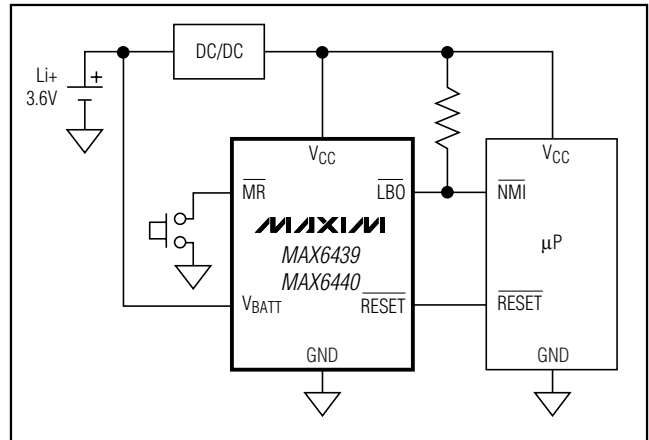
Selector Guide

| PART | OPEN-DRAIN RESET | PUSH-PULL RESET | SINGLE LOW-BATTERY OUTPUT | DUAL LOW-BATTERY OUTPUT |
|---------|------------------|-----------------|---------------------------|-------------------------|
| MAX6439 | X | — | X | — |
| MAX6440 | — | X | X | — |
| MAX6441 | X | — | — | X |
| MAX6442 | — | X | — | X |

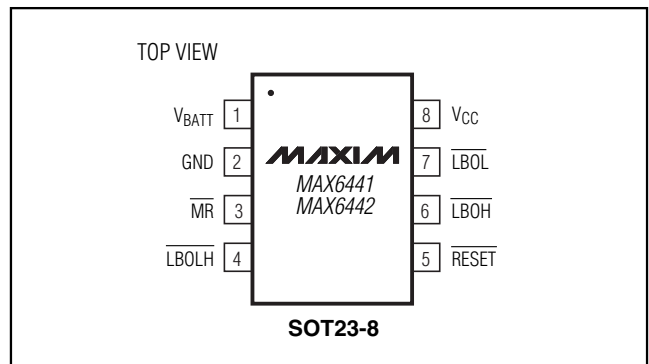
Standard Versions Table

| PART | TOP MARK |
|----------------|----------|
| MAX6439UTDHRD3 | ABMN |
| MAX6439UTDHSD3 | ABMO |
| MAX6439UTEHRD3 | ABMP |
| MAX6439UTEHSD3 | ABMQ |
| MAX6439UTEIRD3 | ABMR |
| MAX6439UTEISD3 | ABMS |
| MAX6440UTDHRD3 | ABMT |
| MAX6440UTDHSD3 | ABMU |
| MAX6440UTEHRD3 | ABMV |
| MAX6440UTEHSD3 | ABMW |
| MAX6440UTEIRD3 | ABMX |
| MAX6440UTEISD3 | ABMY |
| MAX6441KADHRD3 | AEEI |
| MAX6441KADHSD3 | AEEJ |
| MAX6441KAEHRD3 | AEEK |
| MAX6441KAEHSD3 | AEEL |
| MAX6441KAEIRD3 | AEEM |
| MAX6441KAEISD3 | AEEN |
| MAX6442KADHRD3 | AEEO |
| MAX6442KADHSD3 | AEEP |
| MAX6442KAEHRD3 | AEEQ |
| MAX6442KAEHSD3 | AEER |
| MAX6442KAEIRD3 | AEES |
| MAX6442KAEISD3 | AEET |

Typical Application Circuit



Pin Configurations (continued)



Chip Information

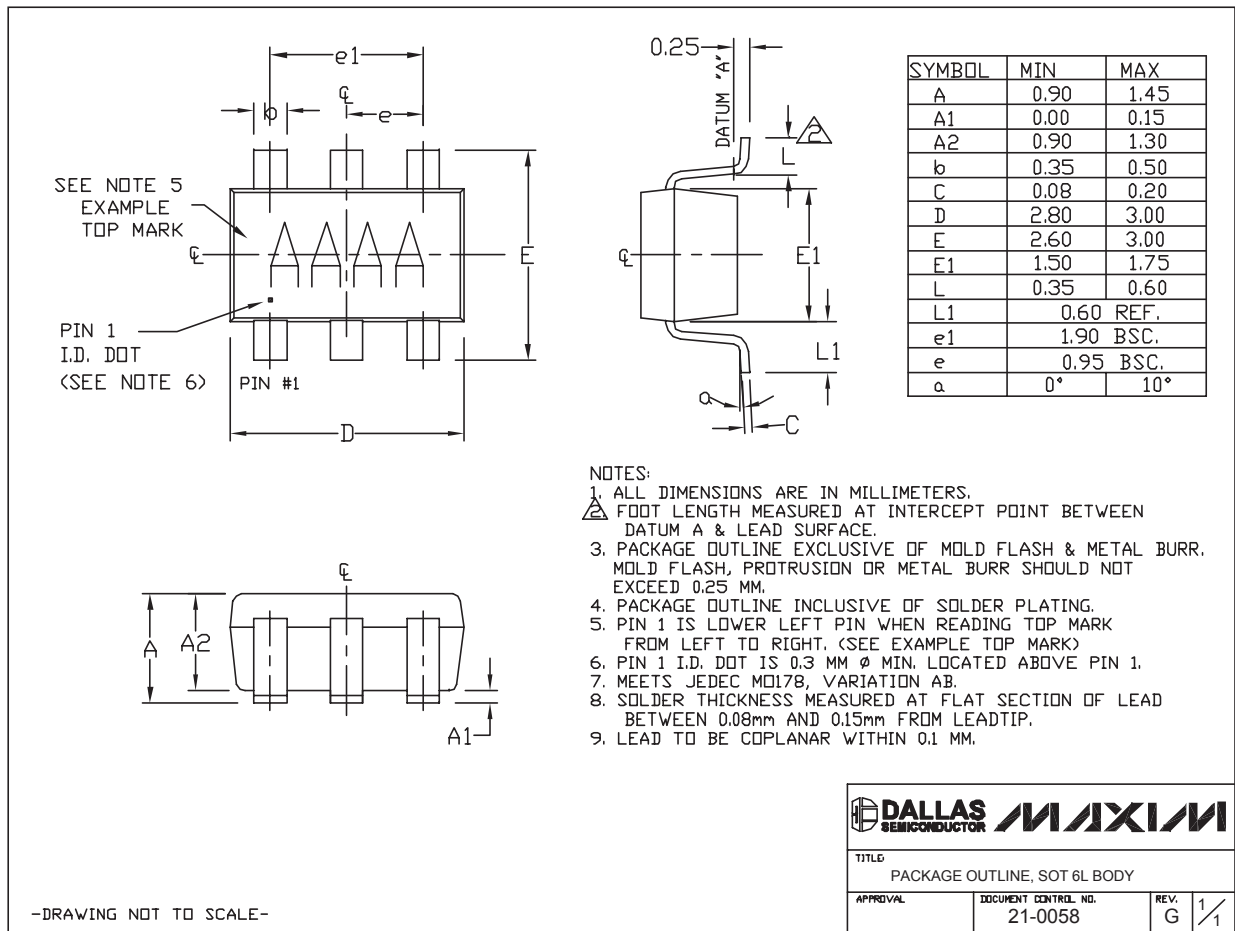
TRANSISTOR COUNT: 1478
 PROCESS: BiCMOS

Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX6439-MAX6442



SOT6L

Low-Power, Single-/Dual-Level Battery Monitors with Hysteresis and Integrated μ P Reset

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

| SYMBOL | MIN | MAX |
|----------|------------|------------|
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.28 | 0.45 |
| C | 0.09 | 0.20 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| L | 0.30 | 0.60 |
| L2 | 0.25 BSC. | |
| e | 0.65 BSC. | |
| e1 | 1.95 REF. | |
| θ | 0 $^\circ$ | 8 $^\circ$ |

NOTE:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- Δ FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
- PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
- PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
- COPLANARITY 4 MILS. MAX.
- PIN 1 I.D. DOT IS 0.3 MM \bar{y} MIN. LOCATED ABOVE PIN 1.
- SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
- MEETS JEDEC MO178.

DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, SOT-23, 8L BODY

| | | | |
|----------|---------------------------------|-----------|-----|
| APPROVAL | DOCUMENT CONTROL NO. 21-0078 | REV. D | 1/1 |
|----------|---------------------------------|-----------|-----|

SOT23-8L EFS

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