



**THE DATASHEET OF
SN74LVTH373PW**



SN54LVTH373, SN74LVTH373 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS689H – MAY 1997 – REVISED OCTOBER 2003

- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Unregulated Battery Operation Down to 2.7 V
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

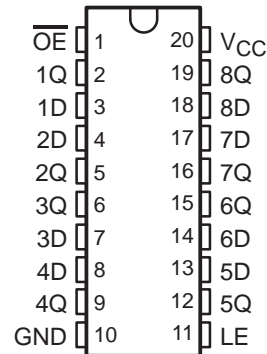
description/ordering information

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

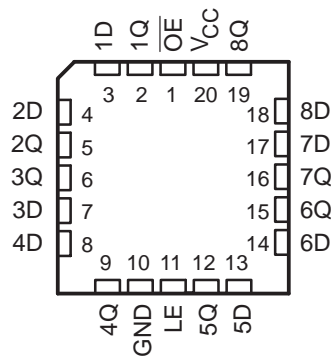
While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

SN54LVTH373 . . . J OR W PACKAGE
SN74LVTH373 . . . DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVTH373 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 85°C | SOIC – DW | Tube | SN74LVTH373DW | LVTH373 |
| | | Tape and reel | SN74LVTH373DWR | |
| | SOP – NS | Tape and reel | SN74LVTH373NSR | LVTH373 |
| | SSOP – DB | Tape and reel | SN74LVTH373DBR | LXH373 |
| -55°C to 125°C | TSSOP – PW | Tube | SN74LVTH373PW | LXH373 |
| | | Tape and reel | SN74LVTH373PWR | |
| | CDIP – J | Tube | SNJ54LVTH373J | SNJ54LVTH373J |
| | CFP – W | Tube | SNJ54LVTH373W | SNJ54LVTH373W |
| | LCCC – FK | Tube | SNJ54LVTH373FK | SNJ54LVTH373FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

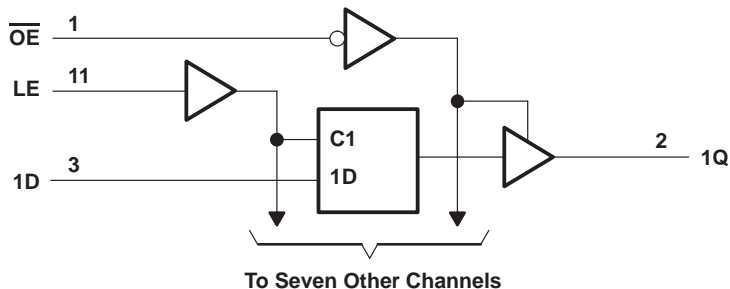
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE
(each latch)

| INPUTS | | | OUTPUT |
|-----------------|----|---|--------|
| \overline{OE} | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

logic diagram (positive logic)



SN54LVTH373, SN74LVTH373 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_{OL} : SN54LVTH373 | 96 mA |
| SN74LVTH373 | 128 mA |
| Current into any output in the high state, I_O (see Note 2): SN54LVTH373 | 48 mA |
| SN74LVTH373 | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DB package | 70°C/W |
| DW package | 58°C/W |
| NS package | 60°C/W |
| PW package | 83°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

| | | SN54LVTH373 | | SN74LVTH373 | | UNIT |
|--------------------------|------------------------------------|-----------------|-----|-------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 2.7 | 3.6 | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | | 5.5 | | 5.5 | V |
| I_{OH} | High-level output current | | –24 | | –32 | mA |
| I_{OL} | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | 200 | | μs/V |
| T_A | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54LVTH373 | | | SN74LVTH373 | | | UNIT | |
|--------------------|---|--|-----------------------------|---------|-----|--------------|---------|-----|---------------|---------------|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | | |
| V_{IK} | $V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$ | | -1.2 | | | -1.2 | | | V | |
| V_{OH} | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$ | | $V_{CC}-0.2$ | | | $V_{CC}-0.2$ | | | V | |
| | $V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$ | | 2.4 | | | 2.4 | | | | |
| | $V_{CC} = 3\text{ V}$ | $I_{OH} = -24\text{ mA}$ $I_{OH} = -32\text{ mA}$ | 2 | | | 2 | | | | |
| V_{OL} | $V_{CC} = 2.7\text{ V}$ | $I_{OL} = 100\text{ }\mu\text{A}$ | 0.2 | | | 0.2 | | | V | |
| | | $I_{OL} = 24\text{ mA}$ | 0.5 | | | 0.5 | | | | |
| | $V_{CC} = 3\text{ V}$ | $I_{OL} = 16\text{ mA}$ | 0.4 | | | 0.4 | | | | |
| | | $I_{OL} = 32\text{ mA}$ | 0.5 | | | 0.5 | | | | |
| | | $I_{OL} = 48\text{ mA}$ | 0.55 | | | 0.55 | | | | |
| | | $I_{OL} = 64\text{ mA}$ | | | | 0.55 | | | | |
| I_I | $V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$ | | 10 | | | 10 | | | μA | |
| | Control inputs | $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$ | ± 1 | | | ± 1 | | | | |
| | Data inputs | $V_{CC} = 3.6\text{ V}$ | $V_I = V_{CC}$ $V_I = 0$ | 1 -5 | | | 1 -5 | | | |
| I_{off} | $V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$ | | | | | ± 100 | | | μA | |
| $I_I(\text{hold})$ | Data inputs | $V_{CC} = 3\text{ V}$ | $V_I = 0.8\text{ V}$ | 75 | | | 75 | | | μA |
| | | | $V_I = 2\text{ V}$ | -75 | | | -75 | | | |
| | | $V_{CC} = 3.6\text{ V}\ddagger$, $V_I = 0\text{ to }3.6\text{ V}$ | | | | 500 -750 | | | | |
| I_{OZH} | $V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$ | | 5 | | | 5 | | | μA | |
| I_{OZL} | $V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$ | | -5 | | | -5 | | | μA | |
| I_{OZPU} | $V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = \text{don't care}$ | | $\pm 100^*$ | | | ± 100 | | | μA | |
| I_{OZPD} | $V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $\overline{OE} = \text{don't care}$ | | $\pm 100^*$ | | | ± 100 | | | μA | |
| I_{CC} | $V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$ | Outputs high | 0.19 | | | 0.19 | | | mA | |
| | | Outputs low | 5 | | | 5 | | | | |
| | | Outputs disabled | 0.19 | | | 0.19 | | | | |
| $\Delta I_{CC}\S$ | $V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND | | 0.2 | | | 0.2 | | | mA | |
| C_i | $V_I = 3\text{ V or }0$ | | 3 | | | 3 | | | pF | |
| C_o | $V_O = 3\text{ V or }0$ | | 7 | | | 7 | | | pF | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | SN54LVTH373 | | | | SN74LVTH373 | | | | UNIT |
|-----------------|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|-------------------------|-----|------|
| | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | |
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, LE high | | | | 3 | 3 | 3 | 3 | ns |
| t _{su} | Setup time, data before LE↓ | | | | 1.1 | 0.4 | 1.1 | 0.4 | ns |
| t _h | Hold time, data after LE↓ | | | | 1.7 | 2 | 1.4 | 1.4 | ns |

switching characteristics over recommended free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH373 | | | | SN74LVTH373 | | | | UNIT | |
|------------------|------------------------|----------------|------------------------------------|-----|-------------------------|-----|------------------------------------|------|-------------------------|-----|------|-----|
| | | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP† | MAX | MIN | | MAX |
| t _{PLH} | D | Q | 1.4 | 4.1 | 4.7 | | 1.5 | 2.6 | 3.9 | 4.5 | | ns |
| t _{PHL} | | | 1.4 | 4.1 | 4.7 | | 1.5 | 2.6 | 3.9 | 4.5 | | |
| t _{PLH} | LE | Q | 1.6 | 4.4 | 5.1 | | 1.7 | 2.7 | 4.2 | 4.9 | | ns |
| t _{PHL} | | | 1.6 | 4.4 | 5.1 | | 1.7 | 2.7 | 4.2 | 4.9 | | |
| t _{PZH} | $\overline{\text{OE}}$ | Q | 1.2 | 5 | 6.1 | | 1.3 | 3 | 4.8 | 5.9 | | ns |
| t _{PZL} | | | 1.2 | 5 | 5.7 | | 1.3 | 3 | 4.8 | 5.5 | | |
| t _{PHZ} | $\overline{\text{OE}}$ | Q | 1.6 | 5.5 | 5.7 | | 1.9 | 3 | 4.6 | 4.9 | | ns |
| t _{PLZ} | | | 0.8 | 4.8 | 4.9 | | 1.9 | 3 | 4.5 | 4.6 | | |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

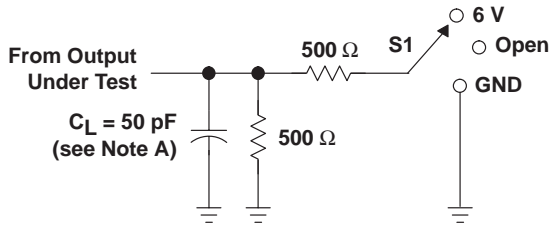
SN54LVTH373, SN74LVTH373

3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

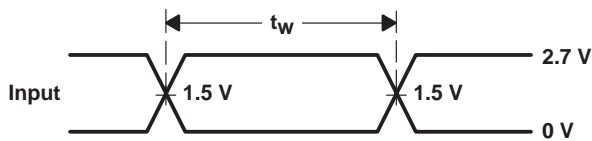
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PARAMETER MEASUREMENT INFORMATION

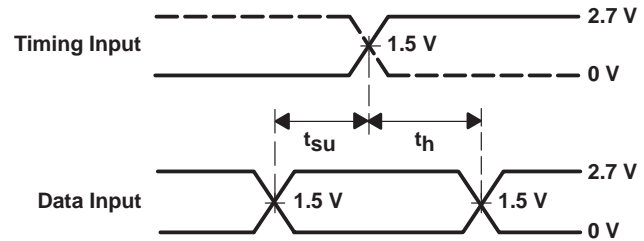


LOAD CIRCUIT

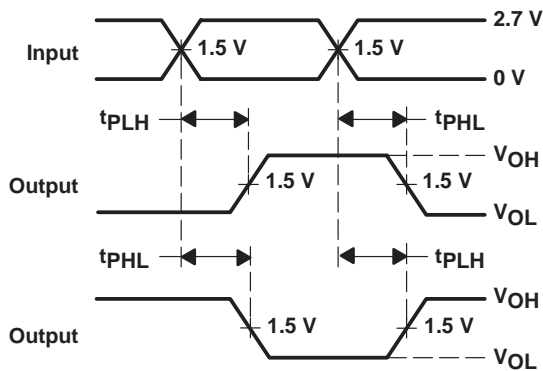
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



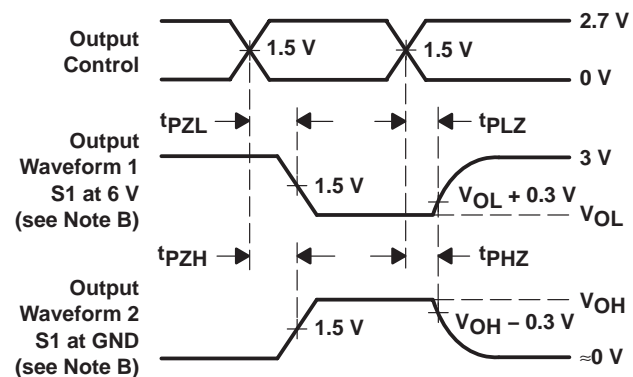
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| 5962-9950901Q2A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9950901Q2A SNJ54LVTH 373FK |
| 5962-9950901QRA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9950901QR A SNJ54LVTH373J |
| 5962-9950901QSA | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9950901QS A SNJ54LVTH373W |
| SN74LVTH373DBR | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH373 |
| SN74LVTH373DBR.B | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH373 |
| SN74LVTH373DW | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH373 |
| SN74LVTH373DW.B | Active | Production | SOIC (DW) 20 | 25 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH373 |
| SN74LVTH373DWR | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH373 |
| SN74LVTH373DWR.B | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH373 |
| SN74LVTH373NSR | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH373 |
| SN74LVTH373NSR.B | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH373 |
| SN74LVTH373PW | Active | Production | TSSOP (PW) 20 | 70 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH373 |
| SN74LVTH373PW.B | Active | Production | TSSOP (PW) 20 | 70 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH373 |
| SN74LVTH373PWR | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH373 |
| SN74LVTH373PWR.B | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH373 |
| SN74LVTH373PWRE4 | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH373 |
| SN74LVTH373PWRG4 | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH373 |
| SNJ54LVTH373FK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 9950901Q2A SNJ54LVTH 373FK |
| SNJ54LVTH373J | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9950901QR A SNJ54LVTH373J |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--------------------------------------|
| SNJ54LVTH373W | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9950901QS A SNJ54LVTH373W |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54LVTH373, SN74LVTH373 :

- Catalog : [SN74LVTH373](#)

- Enhanced Product : [SN74LVTH373-EP](#), [SN74LVTH373-EP](#)

- Military : [SN54LVTH373](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH373DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVTH373DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVTH373NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LVTH373PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH373DBR | SSOP | DB | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVTH373DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74LVTH373NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74LVTH373PWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |

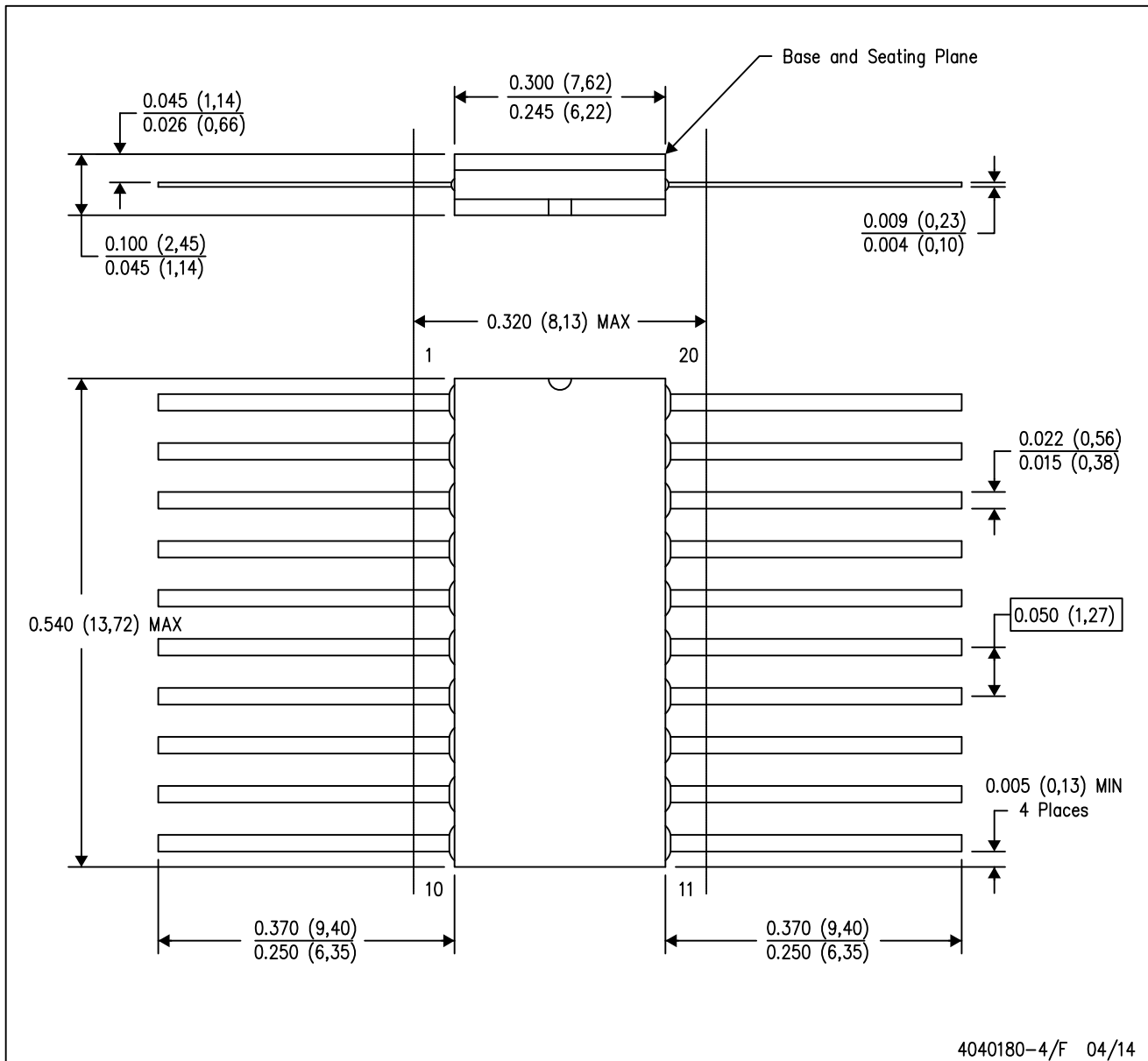
TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9950901Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SN74LVTH373DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LVTH373DW.B | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LVTH373PW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVTH373PW.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SNJ54LVTH373FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

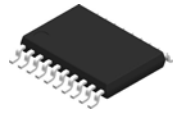
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

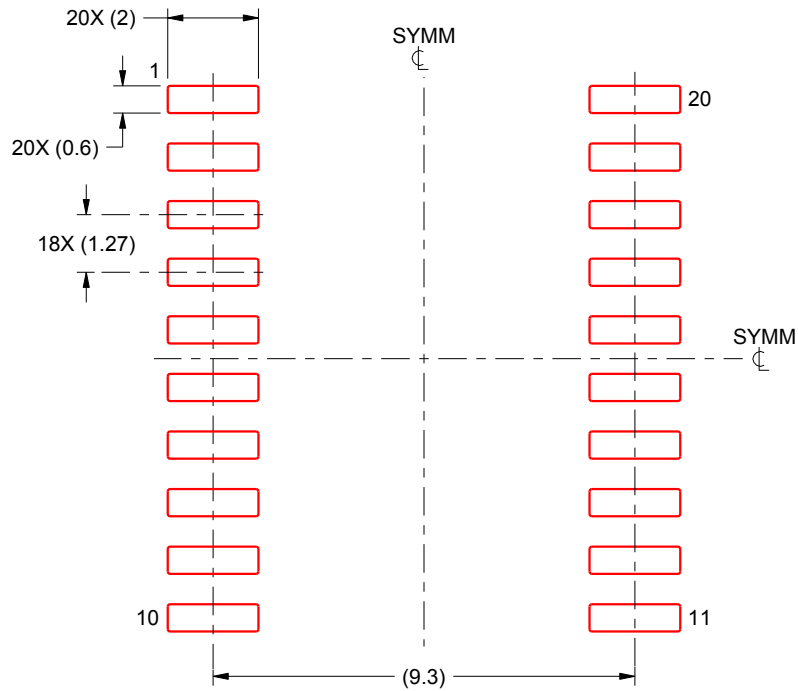
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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