THE DATASHEET OF

ADM7155ACPZ-02-R7

600 mA, Ultralow Noise, High PSRR, RF Linear Regulator

Data Sheet

ADM7155

FEATURES

- Input voltage range: 2.3 V to 5.5 V
- Output voltage range: 1.2 V to 3.4 V
- Maximum load current: 600 mA
- Low noise
  - 0.9 µV rms total integrated noise from 100 Hz to 100 kHz
  - 1.6 µV rms total integrated noise from 10 Hz to 100 kHz
- Noise spectral density: 1.5 nV/√Hz from 10 kHz to 1 MHz
- PSRR: >90 dB from 200 Hz to 200 kHz; 57 dB at 1 MHz
- Dropout voltage: 120 mV typical at V_{OUT} = 3.3 V, I_{OUT} = 600 mA
- Initial accuracy: ±0.5%
- Accuracy over line, load, and temperature: −2.0% (minimum), +1.5% (maximum)
- Quiescent current, I_{GND} = 4 mA at no load
- Low shutdown current: 0.2 µA
- Stable with a 10 µF ceramic output capacitor
- 8-lead LFCSP and 8-lead SOIC packages
- Precision enable
- Supported by ADIsimPower tool

APPLICATIONS

- Regulation to noise sensitive applications: PLLs, VCOs, and PLLs with integrated VCOs
- Communications and infrastructure
- Backhaul and microwave links

TYPICAL APPLICATION CIRCUIT

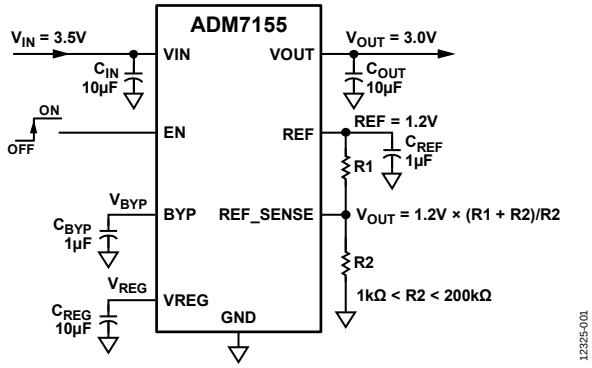

Figure 1. Regulated 3.0 V Output from 3.5 V Input

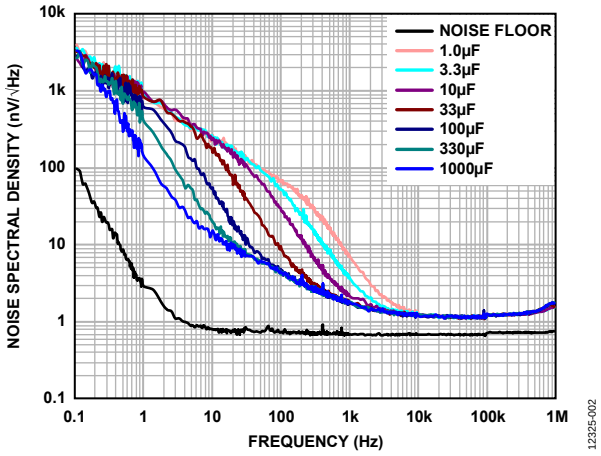

Figure 2. Noise Spectral Density for Different Values of C_{BYP}

GENERAL DESCRIPTION

The ADM7155 is an adjustable linear regulator that operates from 2.3 V to 5.5 V and provides up to 600 mA of load current. Output voltages from 1.2 V to 3.4 V are possible depending on the model. Using an advanced proprietary architecture, it provides high power supply rejection and ultralow noise, achieving excellent line and load transient response with only a 10 µF ceramic output capacitor.

The ADM7155 is available in four models that optimize power dissipation and PSRR performance as a function of input and output voltage. See Table 9 and Table 10 for selection guides.

The ADM7155 regulator typical output noise is 0.9 µV rms from 100 Hz to 100 kHz for fixed output voltage options and 1.5 nV/√Hz for noise spectral density from 10 kHz to 1 MHz.

The ADM7155 is available in 8-lead, 3 mm × 3 mm LFCSP and 8-lead SOIC packages, making it not only a very compact solution but also providing excellent thermal performance for applications requiring up to 600 mA of load current in a small, low profile footprint.

Table 1. Related Devices

Model	Input Voltage	Output Current	Fixed/Adj[1]	Package
ADM7150ACP	4.5 V to 16 V	800 mA	Fixed	8-Lead LFCSP
ADM7150ARD	4.5 V to 16 V	800 mA	Fixed	8-Lead SOIC
ADM7151ACP	4.5 V to 16 V	800 mA	Adj	8-Lead LFCSP
ADM7151ARD	4.5 V to 16 V	800 mA	Adj	8-Lead SOIC
ADM7154ACP	2.3 V to 5.5 V	600 mA	Fixed	8-Lead LFCSP
ADM7154ARD	2.3 V to 5.5 V	600 mA	Fixed	8-Lead SOIC

[1] Adj means adjustable.

Rev. C
Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

8/2016—Rev. B to Rev. C

Changes to Programmable Precision Enable Section and Figure 53 ... 17

9/2015—Rev. A to Rev. B

Changed 3.0 V to 2.4 V ... 14

12/2014—Rev. 0 to Rev. A

Changes to Figure 35 to Figure 40 ... 12
Changes to Figure 45 ... 15

10/2014—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = V_{OUT_MAX} + 0.5 V, EN = V_{IN}; I_{LOAD} = 10 mA; C_{IN} = C_{OUT} = C_{REG} = 10 µF; C_{REF} = C_{BYP} = 1 µF; T_A = 25°C for typical specifications; T_J = −40°C to +125°C for minimum/maximum specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		2.3		5.5	V
LOAD CURRENT	I_{LOAD}				600	mA
OPERATING SUPPLY CURRENT	I_{GND}	I_{LOAD} = 0 µA		4.0	7.0	mA
		I_{LOAD} = 600 mA		6.5	10	mA
SHUTDOWN CURRENT	I_{IN_SD}	EN = GND		0.2	2	µA
NOISE						
Output Noise	OUT_{NOISE}	10 Hz to 100 kHz, V_{OUT} = 1.2 V to 3.4 V		1.6		µV rms
		100 Hz to 100 kHz, V_{OUT} = 1.2 V to 3.4 V		0.9		µV rms
Noise Spectral Density	OUT_{NSD}	10 kHz to 1 MHz, V_{OUT} = 1.2 V to 3.4 V		1.5		nV/√Hz
POWER SUPPLY REJECTION RATIO	PSRR	I_{OUT} = 400 mA				
ADM7155-01		1 kHz to 100 kHz, V_{IN} = 2.3 V		92		dB
		1 MHz, V_{IN} = 2.3 V		65		dB
ADM7155-02		1 kHz to 100 kHz, V_{IN} = 2.9 V		94		dB
		1 MHz, V_{IN} = 2.9 V		61		dB
ADM7155-03		1 kHz to 100 kHz, V_{IN} = 3.4 V		94		dB
		1 MHz, V_{IN} = 3.4 V		57		dB
ADM7155-04		1 kHz to 100 kHz, V_{IN} = 3.9 V		94		dB
		1 MHz, V_{IN} = 3.9 V		57		dB
OUTPUT VOLTAGE ACCURACY		V_{OUT} = V_{REF}				
Initial Accuracy	V_{OUT}	I_{LOAD} = 10 mA, T_J = +25°C	−0.5		+0.5	%
		1 mA < I_{LOAD} < 600 mA, T_J = −40°C to +85°C	−2.0		+1.5	%
		1 mA < I_{LOAD} < 600 mA	−2.0		+2.0	%
REGULATION						
Line	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = V_{OUT_MAX} + 0.5 V to 5.5 V	−0.02		+0.02	%/V
Load[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 1 mA to 600 mA		0.3	1.6	%/A
CURRENT-LIMIT THRESHOLD[2]	I_{LIMIT}					
V_{REF}				22		mA
V_{OUT}			700	960	1200	mA
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = 400 mA, V_{OUT} = 3.3 V		80	130	mV
		I_{OUT} = 600 mA, V_{OUT} = 3.3 V		120	210	mV
PULL-DOWN RESISTANCE						
VOUT	V_{OUT_PULL}	EN = 0 V, V_{OUT} = 1 V, V_{IN} = 5.5 V		550		Ω
REG	V_{REG_PULL}	EN = 0 V, V_{REG} = 1 V, V_{IN} = 5.5 V		33		kΩ
REF	V_{REF_PULL}	EN = 0 V, V_{REF} = 1 V, V_{IN} = 5.5 V		620		Ω
BYP	V_{BYP_PULL}	EN = 0 V, V_{BYP} = 1 V, V_{IN} = 5.5 V		400		Ω
START-UP TIME[4]						
V_{OUT}	$t_{STARTUP}$	V_{OUT} = 3.3 V		1.2		ms
V_{REG}	$t_{REG\_STARTUP}$	V_{OUT} = 3.3 V		0.55		ms
V_{REF}	$t_{REF\_STARTUP}$	V_{OUT} = 3.3 V		0.44		ms
THERMAL SHUTDOWN						
Threshold	TS_{SD}	T_J rising		150		°C
Hysteresis	TS_{SD_HYS}			15		°C
UNDERVOLTAGE THRESHOLDS						
Input Voltage						
Rising	$UVLO_{RISE}$				2.29	V
Falling	$UVLO_{FALL}$		1.95			V
Hysteresis	$UVLO_{HYS}$			200		mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
V_{REG} THRESHOLDS[5]						
Rising	$V_{REG\_UVLORISE}$				1.94	V
Falling	$V_{REG\_UVLOFALL}$		1.60			V
Hysteresis	$V_{REG\_UVLOHYS}$			185		mV
PRECISION EN INPUT		2.3 V ≤ V_{IN} ≤ 5.5 V				
Logic High	EN_{HIGH}		1.13	1.22	1.31	V
Logic Low	EN_{LOW}		1.05	1.13	1.22	V
Logic Hysteresis	EN_{HYS}			90		mV
Leakage Current	I_{EN-LKG}	EN = V_{IN} or GND		0.01	1	µA

[1] Based on an endpoint calculation using 1 mA and 600 mA loads.
[2] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. Dropout applies only for output voltages above 2.3 V.
[4] Start-up time is defined as the time between the rising edge of V_{EN} to V_{OUT}, V_{REG}, or V_{REF} being at 90% of the nominal value.
[5] The output voltage is disabled until the V_{REG} UVLO rise threshold is crossed. The V_{REG} output is disabled until the input voltage UVLO rising threshold is crossed.

Table 3. Input and Output Capacitors, Recommended Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
MINIMUM CAPACITANCE						
Input[1]	C_{IN}	T_A = −40°C to +125°C	7.0			µF
Regulator[1]	C_{REG}	T_A = −40°C to +125°C	7.0			µF
Output[1]	C_{OUT}	T_A = −40°C to +125°C	7.0			µF
Bypass	C_{BYP}	T_A = −40°C to +125°C	0.1			µF
Reference	C_{REF}	T_A = −40°C to +125°C	0.7			µF
CAPACITOR ESR						
C_{REG}, C_{OUT}, C_{IN}, C_{REF}	R_{ESR}	T_A = −40°C to +125°C	0.001		0.2	Ω
C_{BYP}	R_{ESR}	T_A = −40°C to +125°C	0.001		2.0	Ω

[1] The minimum input, regulator, and output capacitances must be greater than 7.0 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VIN to GND	−0.3 V to +7 V
VREG to GND	−0.3 V to VIN, or +4 V (whichever is less)
VOUT to GND	−0.3 V to VREG, or +4 V (whichever is less)
BYP to VOUT	±0.3 V
EN to GND	−0.3 V to +7 V
BYP to GND	−0.3 V to VREG, or +4 V (whichever is less)
REF to GND	−0.3 V to VREG, or +4 V (whichever is less)
REF_SENSE to GND	−0.3 V to +4 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Operating Ambient Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADM7155 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit provided that the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θJA) of the package is based on modeling and calculation using a 4-layer PCB. The junction-to-ambient thermal resistance is highly dependent on the application and PCB layout. In applications where high maximum power dissipation exists, close attention to thermal PCB design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit board. See JESD51-7 and JESD51-9 for detailed information on the board construction.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer PCB. JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the PCB temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA}, θ_{JC}, and Ψ_{JB} are specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
8-Lead LFCSP	36.7	23.5	13.3	°C/W
8-Lead SOIC	36.9	27.1	18.6	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

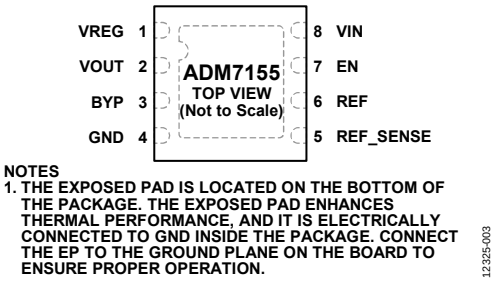

Figure 3. 8-Lead LFCSP Pin Configuration

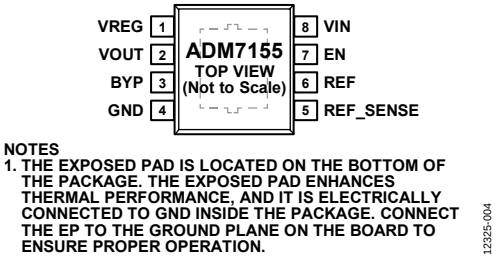

Figure 4. 8-Lead SOIC Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VREG	Regulated Input Supply Voltage to LDO Amplifier. Bypass VREG to GND with a 10 µF or greater capacitor.
2	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 10 µF or greater capacitor.
3	BYP	Low Noise Bypass Capacitor. Connect a 1 µF capacitor from the BYP pin to GND to reduce noise. Do not connect a load to ground.
4	GND	Ground Connection.
5	REF_SENSE	Reference Sense. Connect Pin 5 to the REF pin. Do not connect Pin 5 to VOUT or GND.
6	REF	Low Noise Reference Voltage Output. Bypass REF to GND with a 1 µF capacitor. Short REF_SENSE to REF for fixed output voltages. Do not connect a load to ground.
7	EN	Enable. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
8	VIN	Regulator Input Supply Voltage. Bypass VIN to GND with a 10 µF or greater capacitor.
	EP	Exposed Pad. The exposed pad is located on the bottom of the package. The exposed pad enhances thermal performance, and it is electrically connected to GND inside the package. Connect the EP to the ground plane on the board to ensure proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{OUT} + 0.5 V, or V_{IN} = 2.3 V, whichever is greater; V_{EN} = V_{IN}; I_{OUT} = 10 mA; C_{IN} = C_{OUT} = C_{REG} = 10 µF; C_{REF} = C_{BYP} = 1 µF; T_A = 25°C, unless otherwise noted.

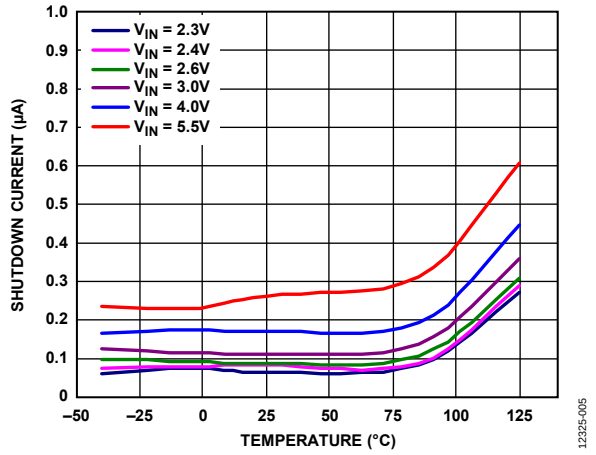

Figure 5. Shutdown Current vs. Temperature at Various Input Voltages, V_{OUT} = 1.8 V

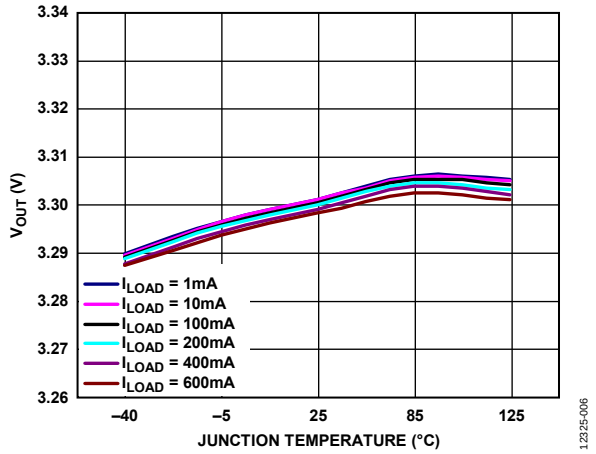

Figure 6. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J) at Various Loads, V_{OUT} = 3.3 V

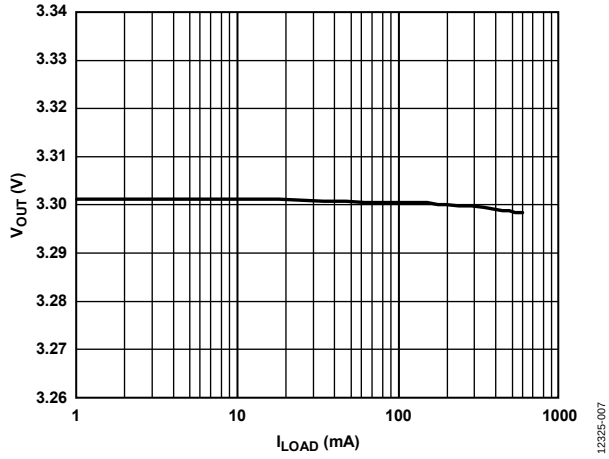

Figure 7. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 3.3 V

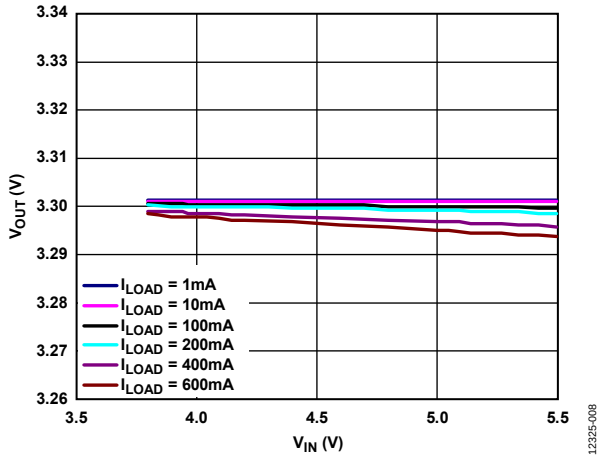

Figure 8. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) at Various Loads, V_{OUT} = 3.3 V

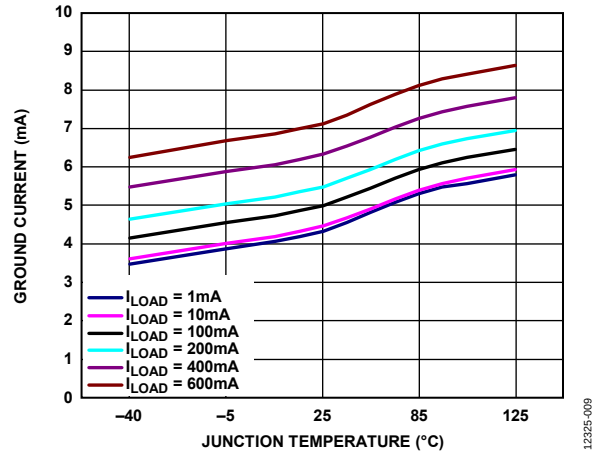

Figure 9. Ground Current vs. Junction Temperature (T_J) at Various Loads, V_{OUT} = 3.3 V

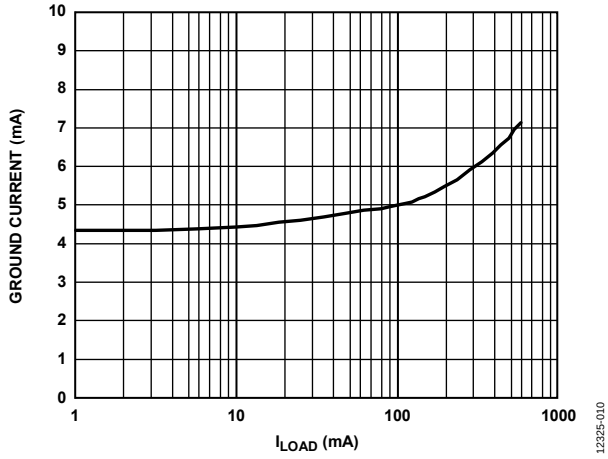

Figure 10. Ground Current vs. Load Current (I_{LOAD}), V_{OUT} = 3.3 V

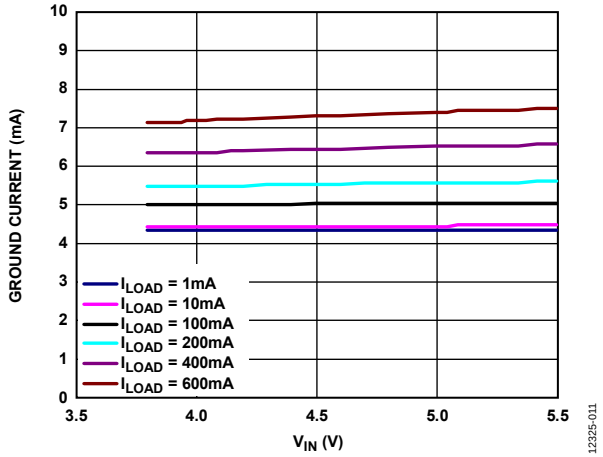

Figure 11. Ground Current vs. Input Voltage (V_{IN}) at Various Loads, V_{OUT} = 3.3 V

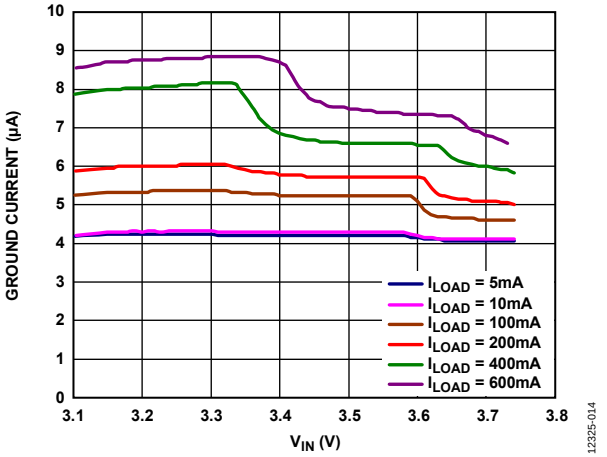

Figure 14. Ground Current vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 3.3 V

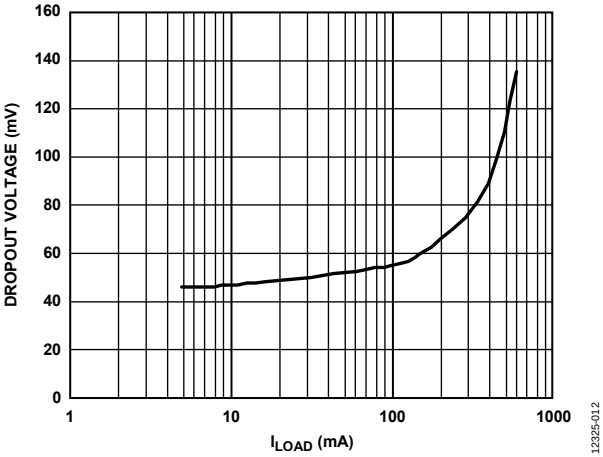

Figure 12. Dropout Voltage vs. Load Current (I_{LOAD}), V_{OUT} = 3.3 V

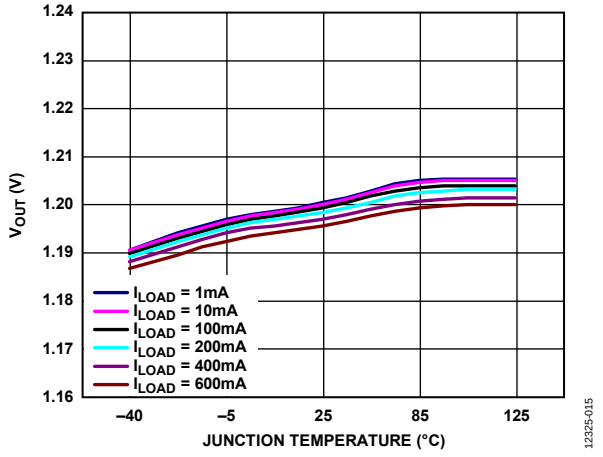

Figure 15. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J) at Various Loads, V_{OUT} = 1.2 V

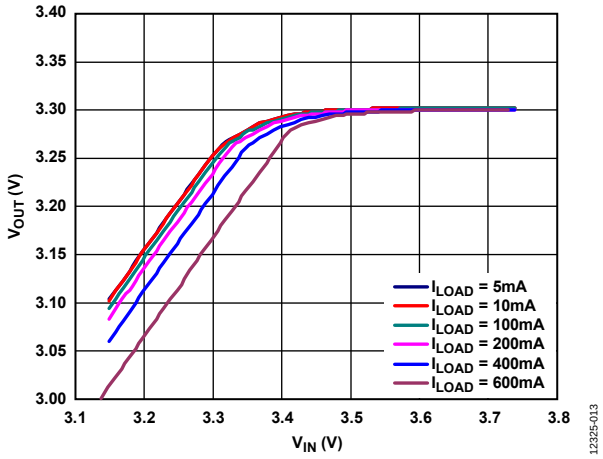

Figure 13. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 3.3 V

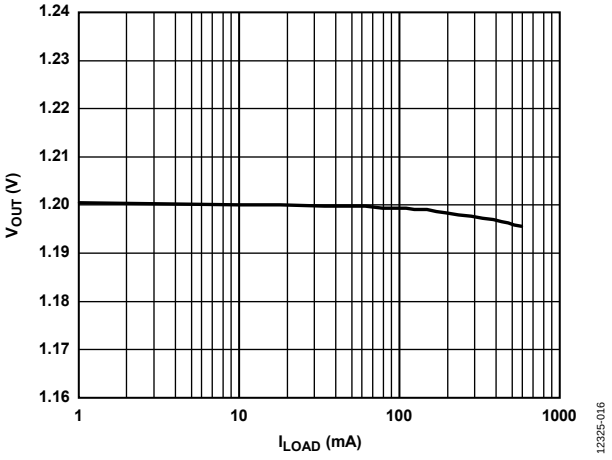

Figure 16. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 1.2 V

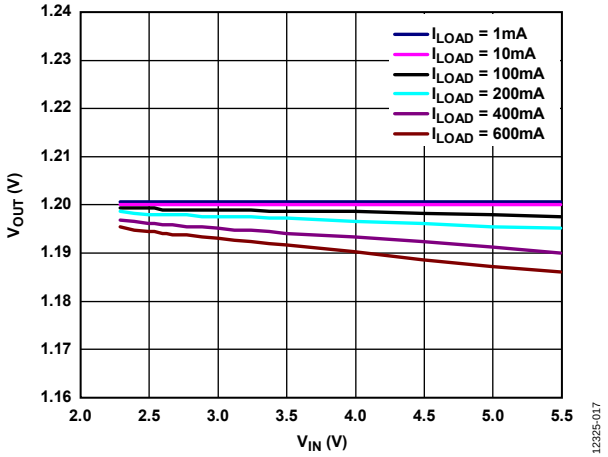

Figure 17. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) at Various Loads, V_{OUT} = 1.2 V

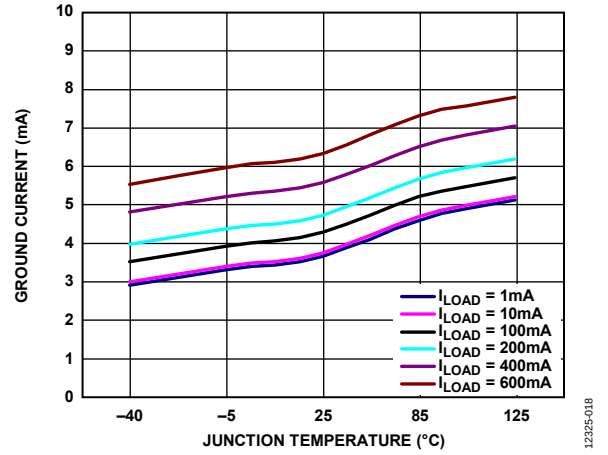

Figure 18. Ground Current vs. Junction Temperature (T_J) at Various Loads, V_{OUT} = 1.2 V

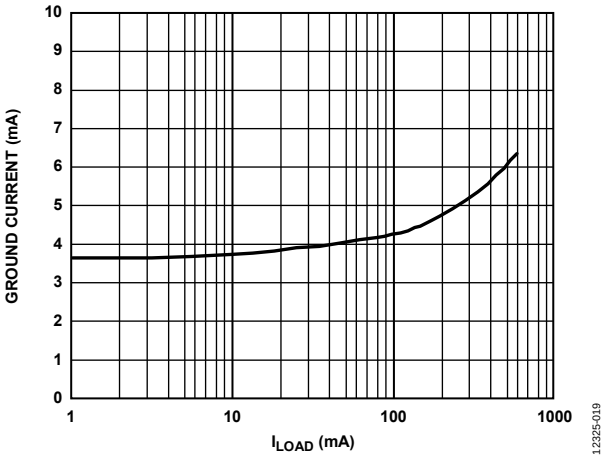

Figure 19. Ground Current vs. Load Current (I_{LOAD}), V_{OUT} = 1.2 V

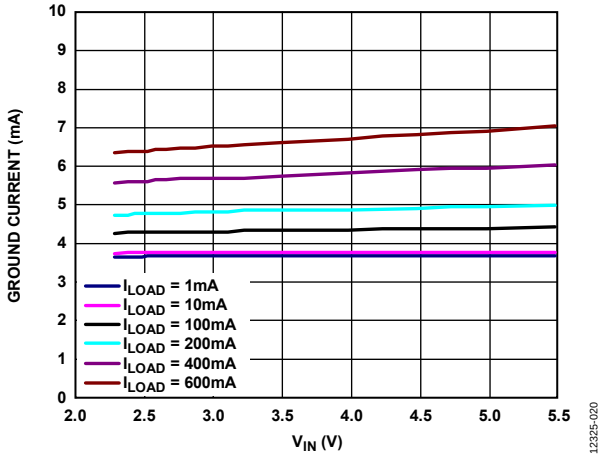

Figure 20. Ground Current vs. Input Voltage (V_{IN}) at Different Loads, V_{OUT} = 1.2 V

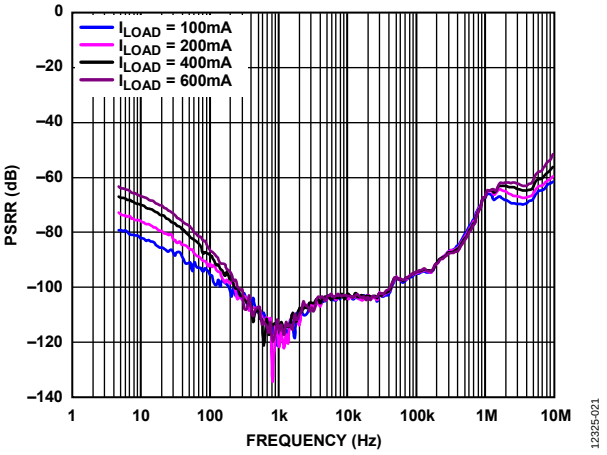

Figure 21. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Loads, V_{OUT} = 3.3 V, V_{IN} = 4.1 V

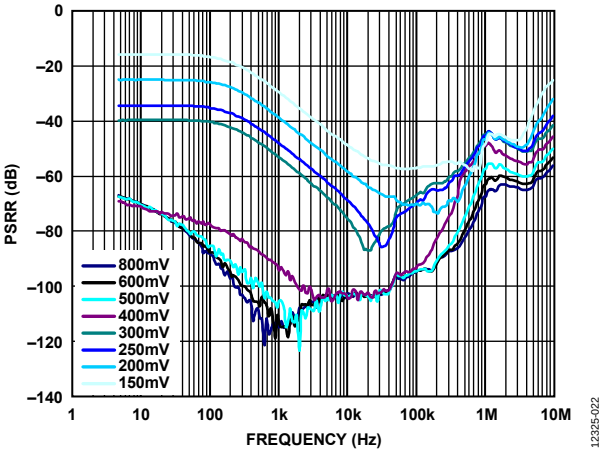

Figure 22. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Headroom Voltages, V_{OUT} = 3.3 V, 400 mA Load

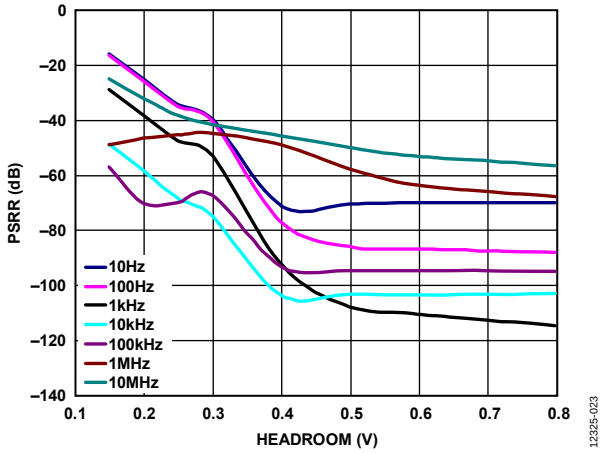

Figure 23. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage at Different Frequencies, V_{OUT} = 3.3 V, 400 mA Load

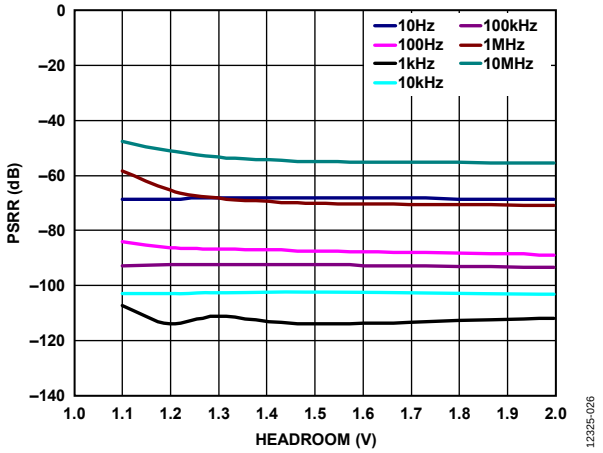

Figure 26. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, Different Frequencies, V_{OUT} = 1.2 V, 400 mA Load

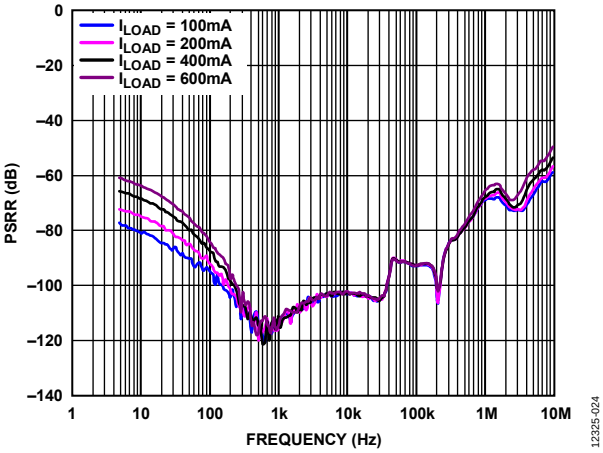

Figure 24. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Loads, V_{OUT} = 1.2 V, V_{IN} = 2.4 V

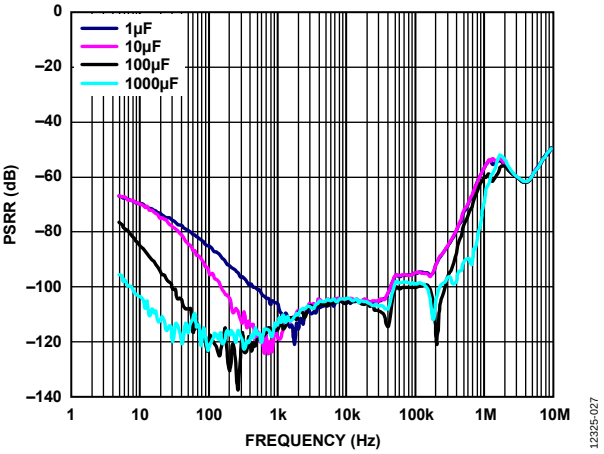

Figure 27. Power Supply Rejection Ratio (PSRR) vs. Frequency, Different C_{BYP}, V_{OUT} = 3.3 V, 400 mA Load, 500 mV Headroom

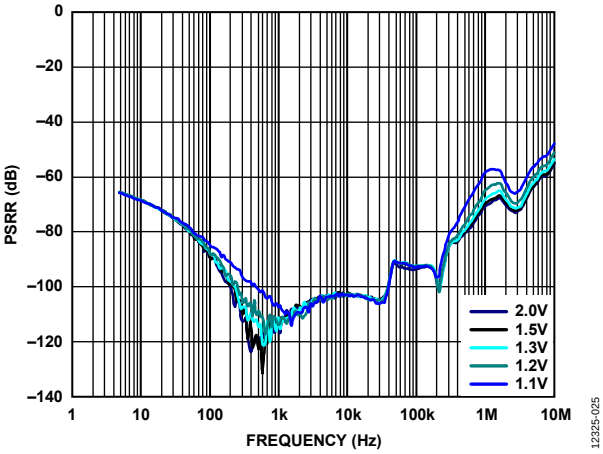

Figure 25. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Headroom Voltages, V_{OUT} = 1.2 V, 400 mA Load

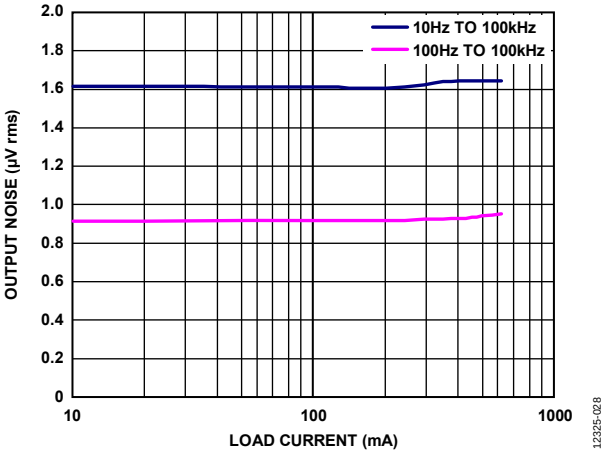

Figure 28. RMS Output Noise vs. Load Current (I_{LOAD})

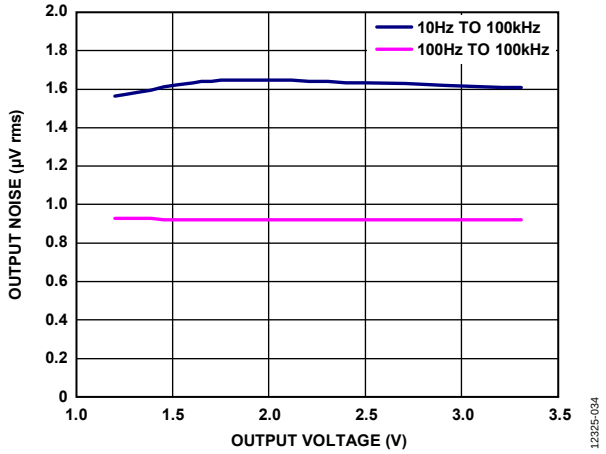

Figure 29. RMS Output Noise vs. Output Voltage

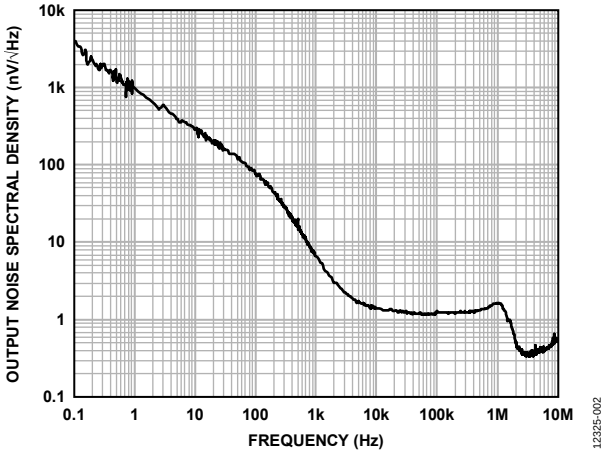

Figure 32. Output Noise Spectral Density, 0.1 Hz to 10 MHz, I_{LOAD} = 100 mA

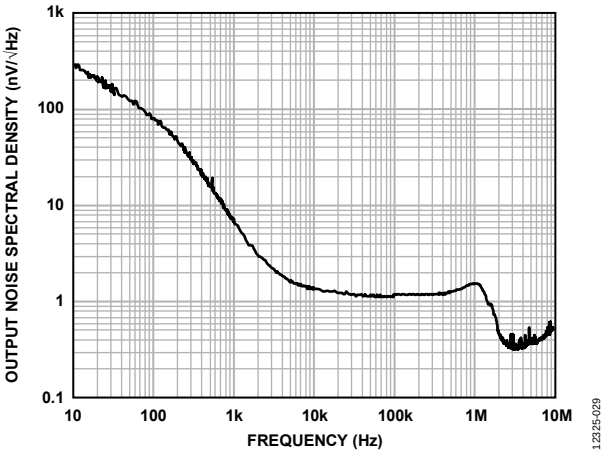

Figure 30. Output Noise Spectral Density, 10 Hz to 10 MHz, I_{LOAD} = 100 mA

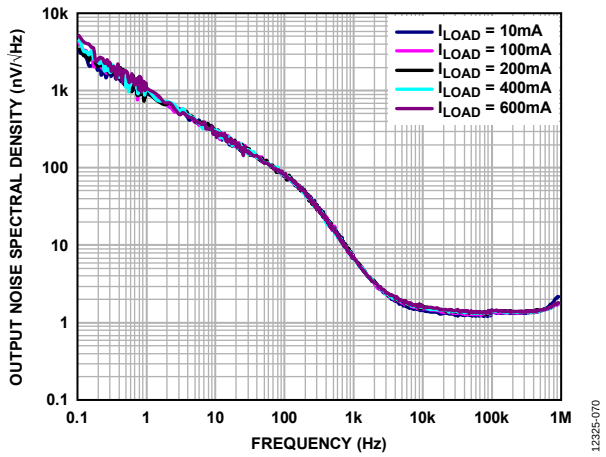

Figure 33. Output Noise Spectral Density at Various Loads, 0.1 Hz to 1 MHz

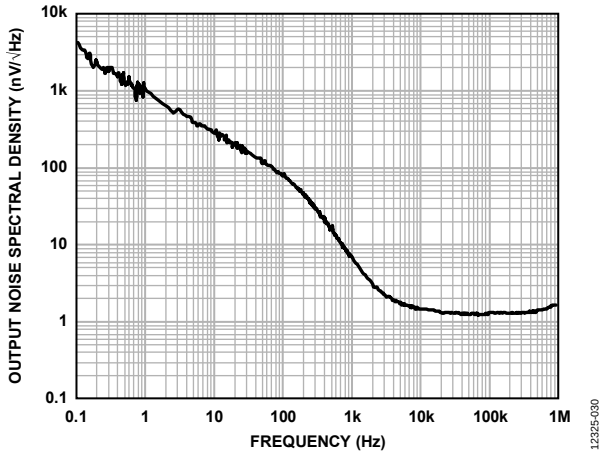

Figure 31. Output Noise Spectral Density, 0.1 Hz to 1 MHz, I_{LOAD} = 10 mA

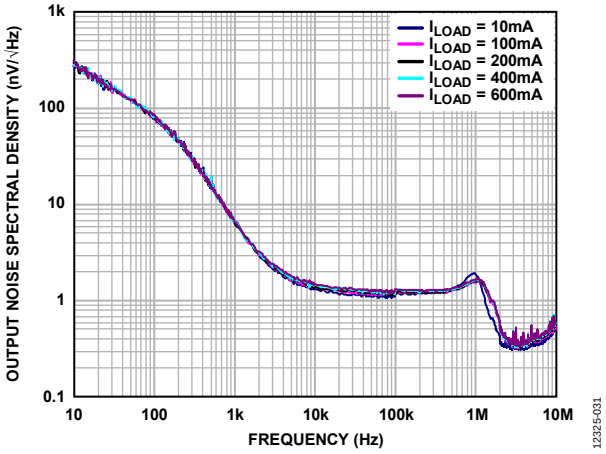

Figure 34. Output Noise Spectral Density at Various Loads, 10 Hz to 10 MHz

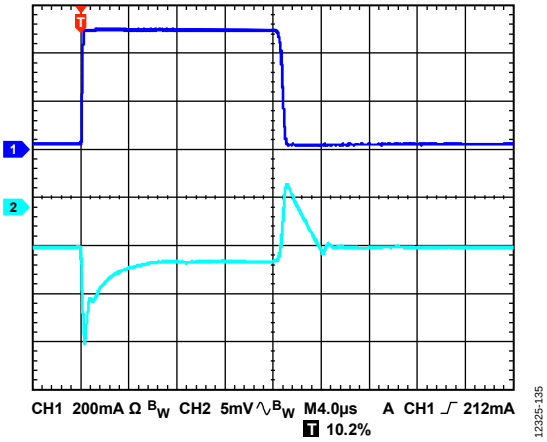

Figure 35. Load Transient Response, I_{LOAD} = 10 mA to 510 mA, V_{OUT} = 3.3 V, V_{IN} = 3.8 V, CH1 = I_{OUT}, CH2 = V_{OUT}

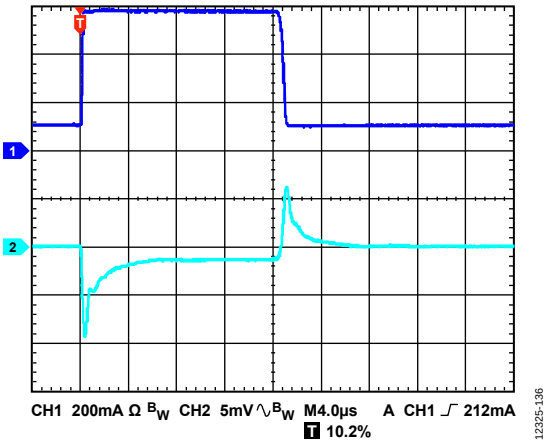

Figure 36. Load Transient Response, I_{LOAD} = 100 mA to 600 mA, V_{OUT} = 3.3 V, V_{IN} = 3.8 V, CH1 = I_{OUT}, CH2 = V_{OUT}

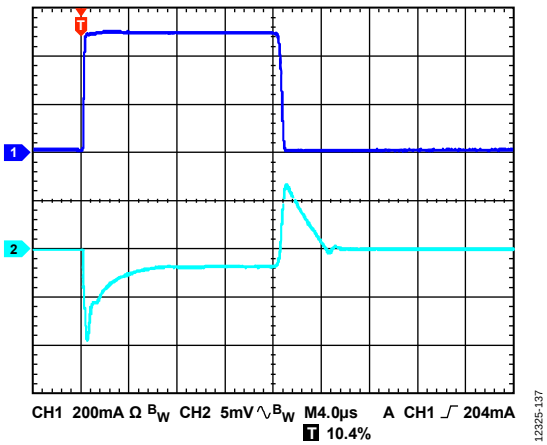

Figure 37. Load Transient Response, I_{LOAD} = 10 mA to 510 mA, V_{OUT} = 1.8 V, V_{IN} = 2.3 V, CH1 = I_{OUT}, CH2 = V_{OUT}

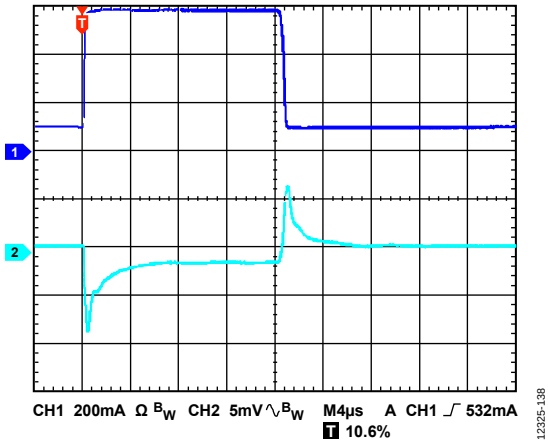

Figure 38. Load Transient Response, I_{LOAD} = 100 mA to 600 mA, V_{OUT} = 1.8 V, V_{IN} = 2.3 V, CH1 = I_{OUT}, CH2 = V_{OUT}

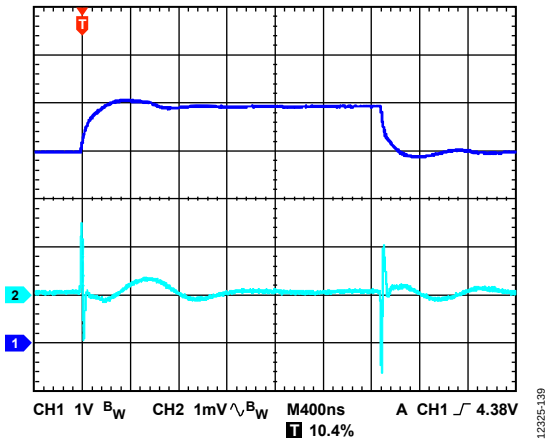

Figure 39. Line Transient Response, 1 V Input Step, I_{LOAD} = 600 mA, V_{OUT} = 3.3 V, V_{IN} = 3.9 V, CH1 = V_{IN}, CH2 = V_{OUT}

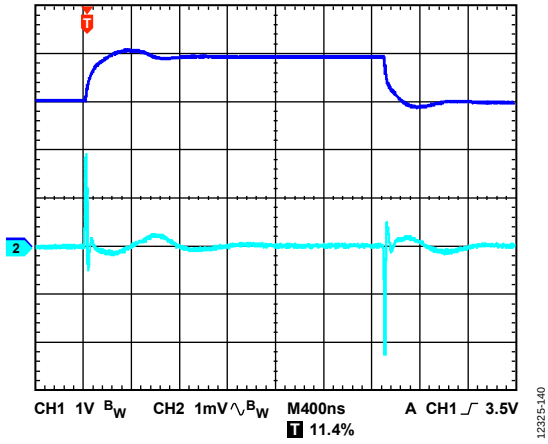

Figure 40. Line Transient Response, 1 V Input Step, I_{LOAD} = 600 mA, V_{OUT} = 1.8 V, V_{IN} = 2.4 V, CH1 = V_{IN}, CH2 = V_{OUT}

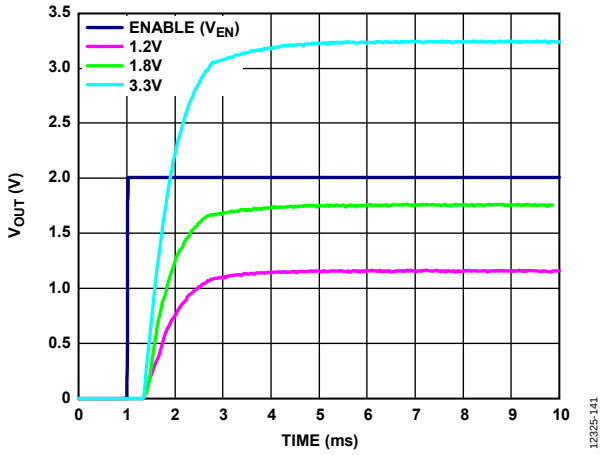

Figure 41. V_{OUT} Start-Up Time After V_{EN} Rising, Different Output Voltages, V_{IN} = 5 V

THEORY OF OPERATION

The ADM7155 is an ultralow noise, high power supply rejection ratio (PSRR) linear regulator targeting radio frequency (RF) applications. The input voltage range is 2.3 V to 5.5 V, and it can deliver up to 600 mA of load current. Typical shutdown current consumption is 0.2 µA at room temperature.

Optimized for use with 10 µF ceramic capacitors, the ADM7155 provides excellent transient performance.

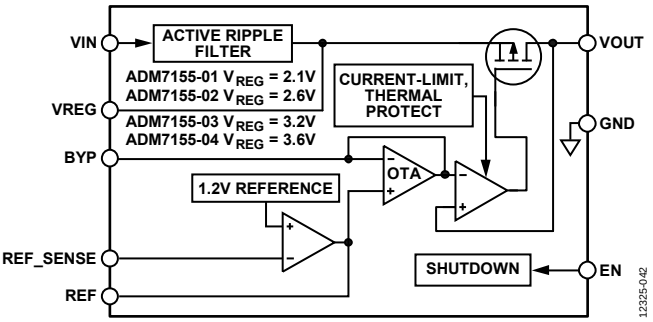

Figure 42. Simplified Internal Block Diagram

Internally, the ADM7155 consists of a reference, an error amplifier, and a P-channel MOSFET pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

By heavily filtering the reference voltage, the ADM7155 is able to achieve 1.5 nV/√Hz output typical from 10 kHz to 1 MHz. Because the error amplifier is always in unity gain, the output noise is independent of the output voltage.

To maintain very high PSRR over a wide frequency range, the ADM7155 architecture uses an internal active ripple filter. This stage isolates the low output noise LDO from noise on the VIN pin. The result is that the PSRR of the ADM7155 is significantly higher over a wider frequency range than any single stage LDO.

The ADM7155 output voltage can be adjusted between 1.2 V and 3.4 V and is available in four models that optimize the input voltage and output voltage ranges to keep power dissipation as low as possible without compromising PSRR performance. The output voltage is determined by an external voltage divider according to the following equation:

$$V_{OUT} = 1.2\ V \times (1 + R1/R2)$$

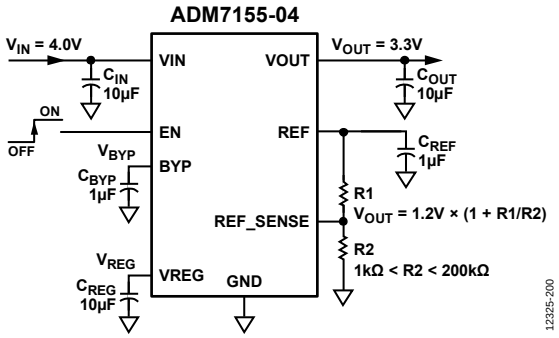

Figure 43. Typical Adjustable Output Voltage Application Schematic

The R2 value must be greater than 1 kΩ to prevent excessive loading of the reference voltage appearing on the REF pin. To minimize errors in the output voltage caused by the REF_SENSE pin input current, the R2 value must be less than 200 kΩ. For example, when R1 and R2 each equal 200 kΩ, the output voltage is 2.4 V. The output voltage error introduced by the REF_SENSE pin input current is 10 mV or 0.33%, assuming a maximum REF_SENSE pin input current of 100 nA at T_J = 125°C.

The ADM7155 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on, and when EN is low, VOUT turns off. For automatic startup, tie EN to VIN.

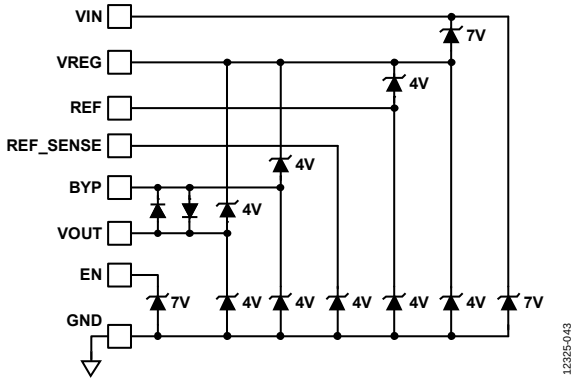

Figure 44. Simplified ESD Protection Block Diagram

The ESD protection devices are shown in the block diagram as Zener diodes (see Figure 44).

APPLICATIONS INFORMATION

ADIsimPOWER DESIGN TOOL

The ADM7155 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance within minutes. ADIsimPower can optimize designs for cost, area, efficiency, and device count, taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about, and to obtain ADIsimPower design tools, visit www.analog.com/ADIsimPower.

CAPACITOR SELECTION

Multilayer ceramic capacitors (MLCCs) combine small size, low ESR, low ESL, and wide operating temperature range, making them an ideal choice for bypass capacitors. They are not without faults, however. Depending on the dielectric material, the capacitance can vary dramatically with temperature, dc bias, and ac signal level. Therefore, selecting the proper capacitor results in the best circuit performance.

Output Capacitor

The ADM7155 is designed for operation with ceramic capacitors but functions with most commonly used capacitors when care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 10 µF capacitance with an ESR of 0.2 Ω or less is recommended to ensure the stability of the ADM7155. Output capacitance also affects transient response to changes in load current. Using a larger value of output capacitance improves the transient response of the ADM7155 to large changes in load current. Figure 45 shows the transient responses for an output capacitance value of 10 µF.

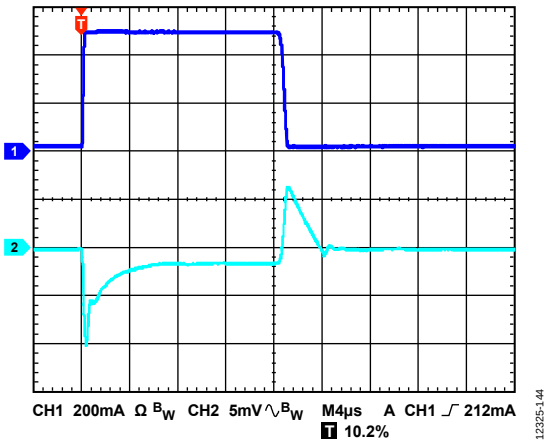

Figure 45. Output Transient Response, V_{OUT} = 3.3 V, C_{OUT} = 10 µF, CH1 = Load Current, CH2 = V_{OUT}

Input and VREG Capacitor

Connecting a 10 µF capacitor from VIN to GND reduces the circuit sensitivity to PCB layout, especially when long input traces or high source impedance are encountered.

To maintain the best possible stability and PSRR performance, connect a 10 µF capacitor from VREG to GND. When more than 10 µF of output capacitance is required, increase the input and the VREG capacitors, C_{REG}, to match it.

REF Capacitor

The REF capacitor, C_{REF}, is necessary to stabilize the reference amplifier. Connect at least a 1 µF capacitor between REF and GND.

BYP Capacitor

The BYP capacitor, C_{BYP}, is necessary to filter the reference buffer. A 1 µF capacitor is typically connected between BYP and GND. Capacitors as small as 0.1 µF can be used; however, the output noise voltage of the LDO increases as a result.

In addition, the BYP capacitor value can be increased to reduce the noise below 1 kHz at the expense of increasing the start-up time of the LDO. Very large values of C_{BYP} significantly reduce the noise below 10 Hz. Tantalum capacitors are recommended for capacitors larger than approximately 33 µF because solid tantalum capacitors are less prone to microphonic noise issues. A 1 µF ceramic capacitor in parallel with the larger tantalum capacitor is recommended to ensure good noise performance at higher frequencies.

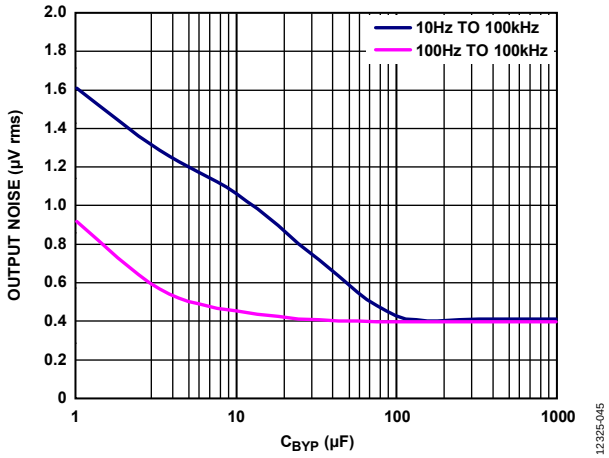

Figure 46. RMS Noise vs. C_{BYP}

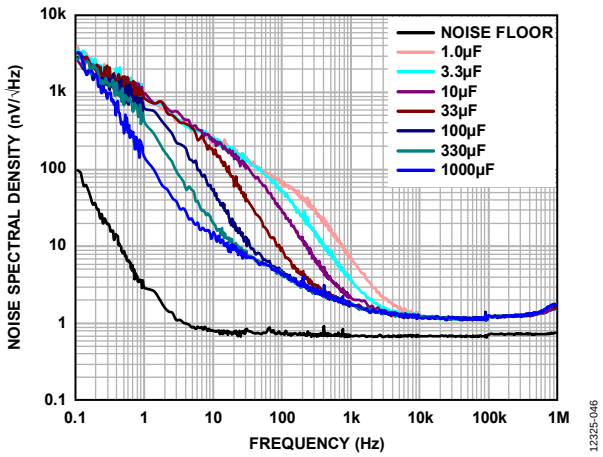

Figure 47. Noise Spectral Density vs. Frequency for Different Capacitances (C_{BYP})

Capacitor Properties

Any good quality ceramic capacitors can be used with the ADM7155 if they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V to 50 V are recommended. However, Y5V and Z5U dielectrics are not recommended because of their poor temperature and dc bias characteristics.

Figure 48 depicts the capacitance vs. dc bias voltage of a 1206, 10 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is ~±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

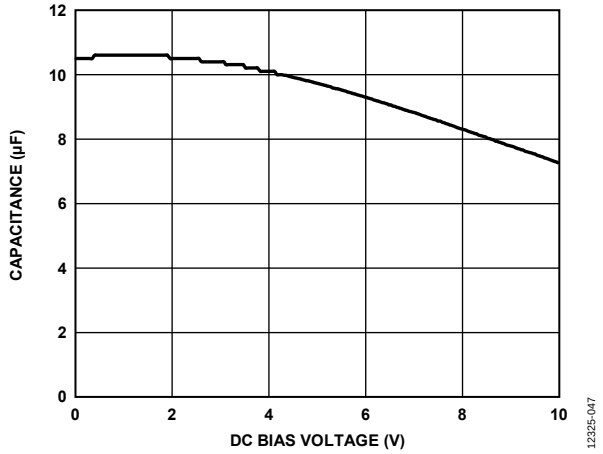

Figure 48. Capacitance vs. DC Bias Voltage

Use Equation 1 to determine the worst case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst case capacitor temperature coefficient.
TOL is the worst case component tolerance.

In this example, the worst case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 9.72 µF at 5 V, as shown in Figure 48.

Substituting these values in Equation 1 yields

$$C_{EFF} = 9.72\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 7.44\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADM7155, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

UNDERVOLTAGE LOCKOUT (UVLO)

The ADM7155 also incorporates an internal UVLO circuit to disable the output voltage when the input voltage is less than the minimum input voltage rating of the regulator. The upper and lower thresholds are internally fixed with about 200 mV of hysteresis.

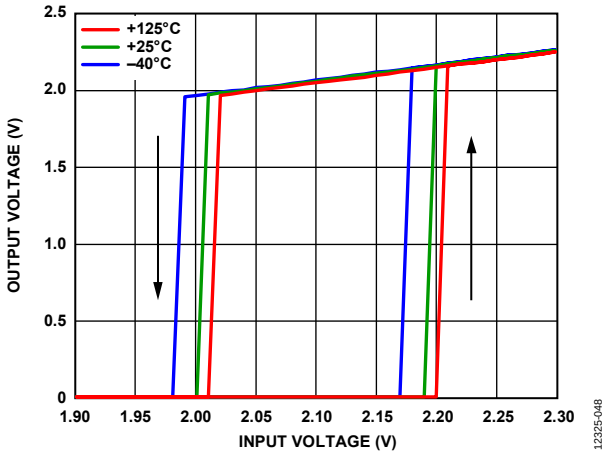

Figure 49. Typical UVLO Behavior at Different Temperatures, V_{OUT} = 3.3 V

Figure 49 shows the typical hysteresis of the UVLO function. This hysteresis prevents on/off oscillations that can occur when caused by noise on the input voltage as it passes through the threshold points.

PROGRAMMABLE PRECISION ENABLE

The ADM7155 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 50, when a rising voltage on EN crosses the upper threshold, nominally 1.22 V, V_{OUT} turns on. When a falling voltage on EN crosses the lower threshold, nominally 1.13 V, V_{OUT} turns off. The hysteresis of the EN threshold is approximately 90 mV.

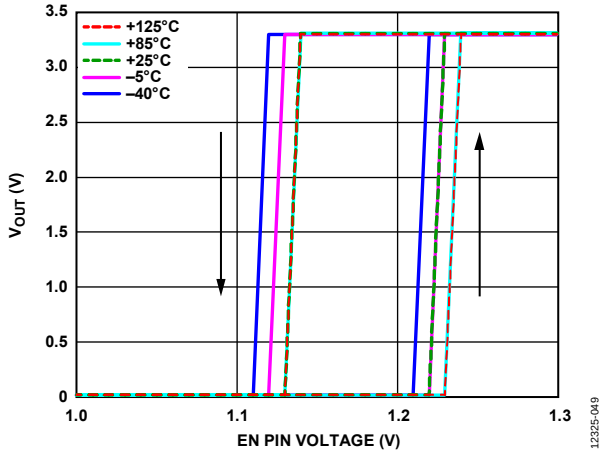

Figure 50. Typical V_{OUT} Response to EN Pin Operation

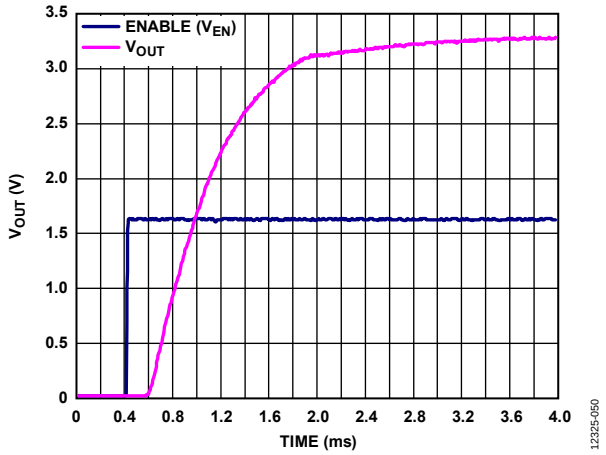

Figure 51. Typical V_{OUT} Response to EN Pin Operation (V_{EN}), V_{OUT} = 3.3 V, V_{IN} = 5 V, C_{BYP} = 1 µF

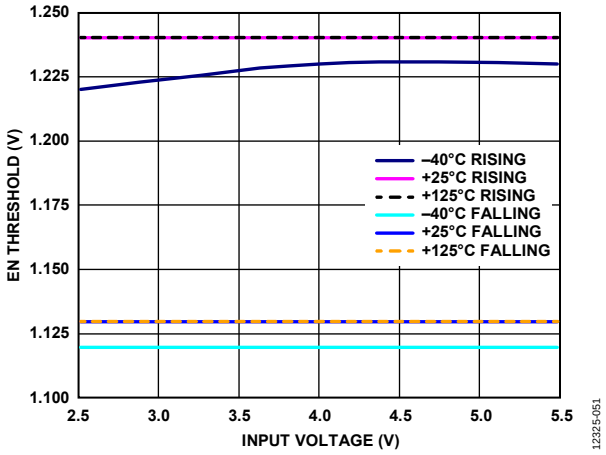

Figure 52. Typical EN Threshold vs. Input Voltages (V_{IN}) for Different Temperatures

The upper and lower thresholds are user programmable and can be set higher than the nominal 1.22 V threshold by using two resistors. The resistance values, R_{EN1} and R_{EN2}, can be determined from

$$R_{EN1} = R_{EN2} \times (V_{IN} - 1.22\ V)/1.22\ V$$

where:

R_{EN2} typically ranges from 10 kΩ to 100 kΩ.

V_{IN} is the desired turn-on voltage.

The hysteresis voltage increases by the factor

$$(R_{EN1} + R_{EN2})/R_{EN2}$$

For the example shown in Figure 53, the EN threshold is 2.44 V with a hysteresis of 200 mV.

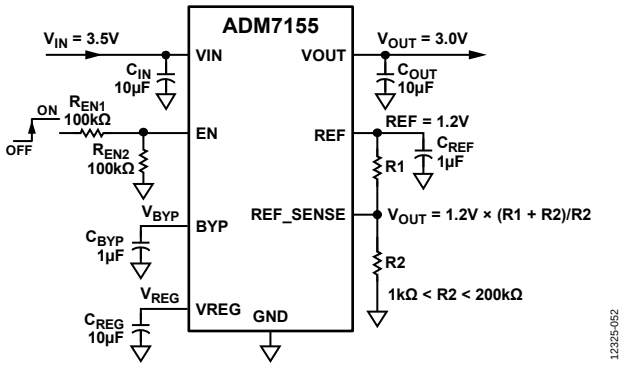

Figure 53. Typical EN Pin Voltage Divider

Figure 53 shows the typical hysteresis of the EN pin. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

START-UP TIME

The ADM7155 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for a 3.3 V output is approximately 1.2 ms from the time the EN active threshold is crossed to when the output reaches 90% of the final value.

The rise time in seconds of the output voltage (10% to 90%) is approximately

$$0.0012 \times C_{BYP}$$

where C_{BYP} is in microfarads.

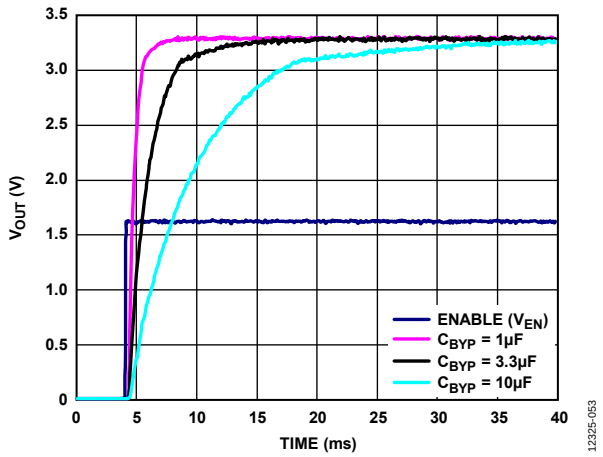

Figure 54. Typical Start-Up Behavior with C_{BYP} = 1 µF to 10 µF

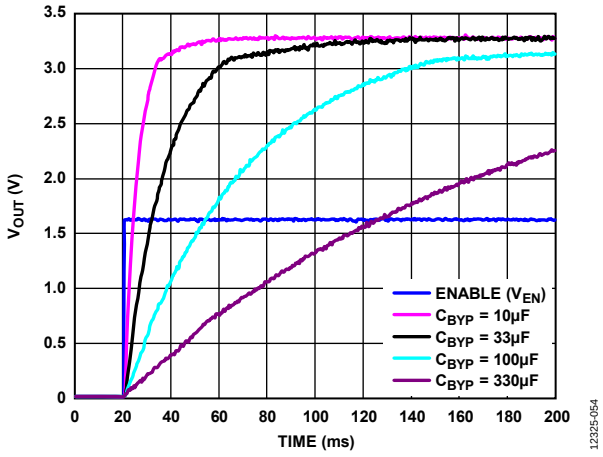

Figure 55. Typical Start-Up Behavior with C_{BYP} = 10 µF to 330 µF

REF, BYP, AND VREG PINS

REF, BYP, and VREG generate voltages internally (V_{REF}, V_{BYP}, and V_{REG}) that require external bypass capacitors for proper operation. Do not, under any circumstances, connect any loads to these pins, because doing so compromises the noise and PSRR performance of the ADM7155. Using larger values of C_{BYP}, C_{REF}, and C_{REG} is acceptable but can increase the start-up time, as described in the Start-Up Time section.

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADM7155 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADM7155 is designed to current limit when the output load reaches 960 mA (typical). When the output load exceeds 960 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C. Under extreme conditions (that is, high ambient temperature and/or high power dissipation), when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again, and the output current is restored to the operating value.

Consider the case where a hard short from VOUT to GND occurs. At first, the ADM7155 current limits, so that only 960 mA is conducted into the short. If self heating of the junction is great enough to cause the temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 900 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 900 mA and 0 mA that continues for as long as the short remains at the output.

Current-limit and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that the junction temperature does not exceed 150°C.

THERMAL CONSIDERATIONS

In applications with a low input to output voltage differential, the ADM7155 does not dissipate much heat. However, in applications with high ambient temperature and/or high input voltage, the heat dissipated in the package may become large enough that it causes the junction temperature of the die to exceed the maximum junction temperature of 150°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers only after the junction temperature decreases below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADM7155 must not exceed 150°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pin and exposed pad to the PCB.

Table 7 shows typical θ_{JA} values of the 8-lead SOIC and 8-lead LFCSP packages for various PCB copper sizes.

Table 8 shows the typical Ψ_{JB} values of the 8-lead SOIC and 8-lead LFCSP.

Table 7. Typical θ_{JA} Values

	θ_{JA} (°C/W)	
Copper Size (mm²)	**8-Lead LFCSP**	**8-Lead SOIC**
25[1]	165.1	165
100	125.8	126.4
500	68.1	69.8
1000	56.4	57.8
6400	42.1	43.6

[1] Device soldered to minimum size pin traces.

Table 8. Typical Ψ_{JB} Values

Package	**Ψ_{JB} (°C/W)**
8-Lead LFCSP	15.1
8-Lead SOIC	17.9

The junction temperature of the ADM7155 is calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = ((V_{IN} - V_{OUT}) \times I_{LOAD}) + (V_{IN} \times I_{GND}) \quad (3)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation caused by ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + (((V_{IN} - V_{OUT}) \times I_{LOAD}) \times \theta_{JA}) \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input to output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 150°C.

The heat dissipation from the package can be improved by increasing the amount of copper attached to the pins and exposed pad of the ADM7155. Adding thermal planes underneath the package also improves thermal performance. However, as shown in Table 7, a point of diminishing returns is eventually reached, beyond which an increase in the copper area does not yield significant reduction in the junction to ambient thermal resistance.

Figure 56 to Figure 61 show junction temperature calculations for different ambient temperatures, power dissipation, and areas of PCB copper.

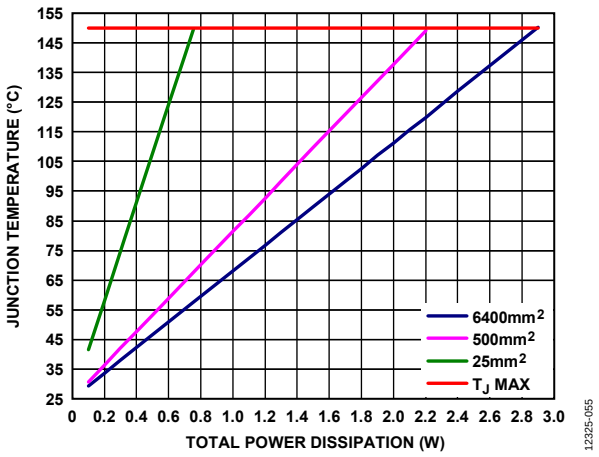

Figure 56. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP, T_A = 25°C

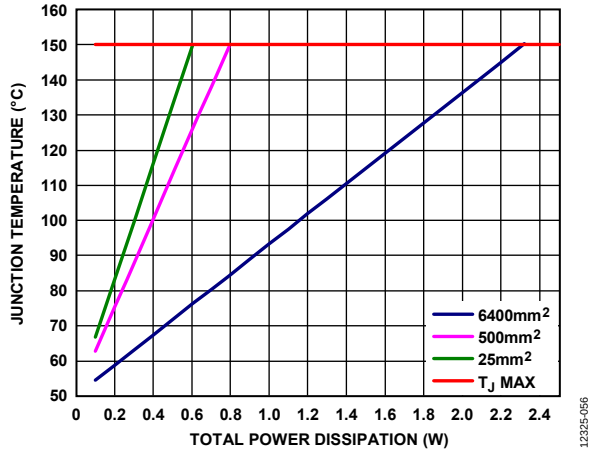

Figure 57. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP, T_A = 50°C

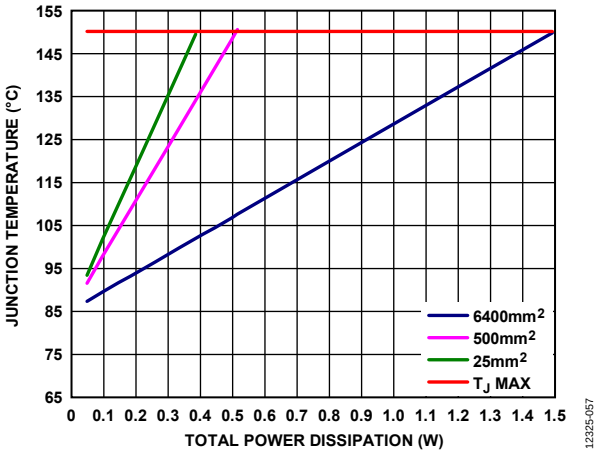

Figure 58. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP, T_A = 85°C

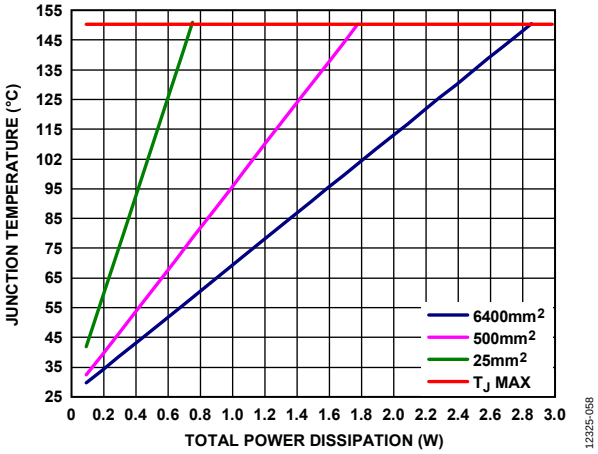

Figure 59. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC, T_A = 25°C

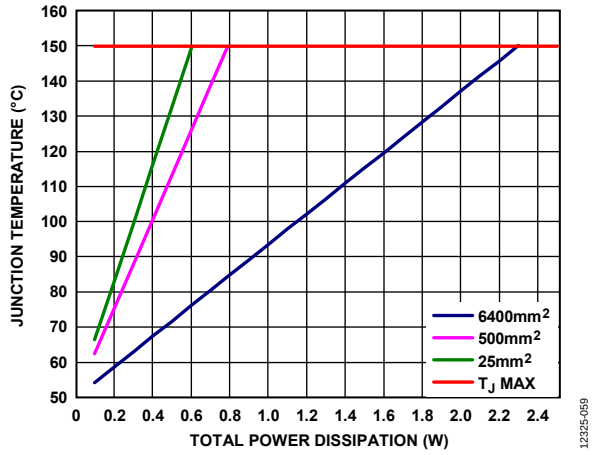

Figure 60. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC, T_A = 50°C

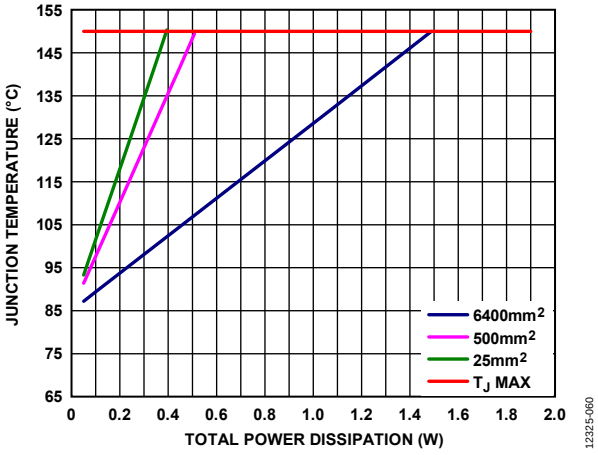

Figure 61. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC, T_A = 85°C

Thermal Characterization Parameter (Ψ_{JB})

When board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise (see Figure 62 and Figure 63). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical value of Ψ_{JB} is 15.1°C/W for the 8-lead LFCSP package and 17.9°C/W for the 8-lead SOIC package.

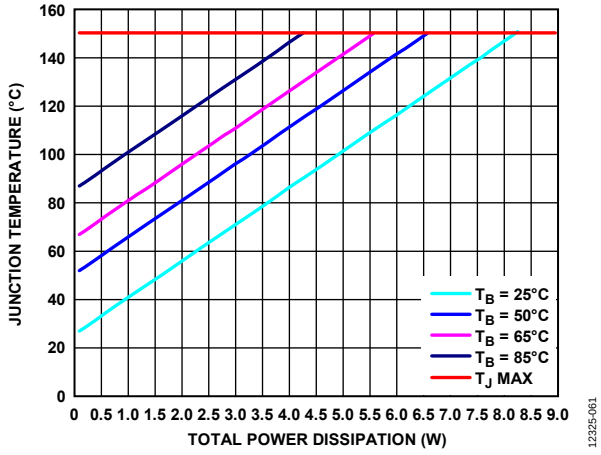

Figure 62. Junction Temperature vs. Total Power Dissipation for the 8-Lead LFCSP

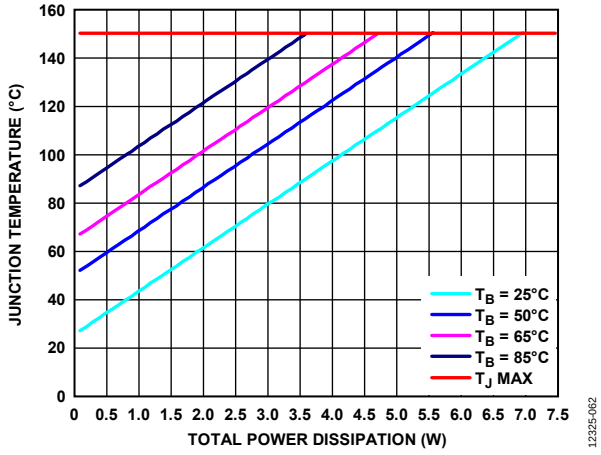

Figure 63. Junction Temperature vs. Total Power Dissipation for the 8-Lead SOIC

PSRR PERFORMANCE

The ADM7155 is available in four models that optimize power dissipation and PSRR performance as a function of input and output voltage. See Table 9 and Table 10 for selection guides.

Table 9. Model Selection Guide for PSRR

Model	V_{OUT_MAX} (V)	PSRR (dB) at 600 mA; $V_{IN} = V_{OUT\_MAX} + 0.5$ V			PSRR (dB) at 400 mA; $V_{IN} = V_{OUT\_MAX} + 0.5$ V		
		10 kHz	100 kHz	1 MHz	10 kHz	100 kHz	1 MHz
ADM7155-01	1.8	101	92	60	102	92	65
ADM7155-02	2.3	101	94	57	101	93	61
ADM7155-03	2.9	103	94	51	102	94	57
ADM7155-04	3.4	103	94	51	102	94	57

Table 10. Model Selection Guide for Input Voltage

Model	V_{OUT} Range (V)	Minimum V_{IN} at 600 mA Load
ADM7155-01	1.2 to 1.8	2.3 V
ADM7155-02	1.2 to 2.3	2.9 V
ADM7155-03	1.2 to 2.9	3.4 V
ADM7155-04	1.2 to 3.4	3.9 V

PCB LAYOUT CONSIDERATIONS

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Place the bypass capacitors (C_{REG}, C_{REF}, and C_{BYP}) for V_{REG}, V_{REF}, and V_{BYP} close to the respective pins (VREG, REF, and BYP) and GND. Use of an 0805, 0603, or 0402 size capacitor achieves the smallest possible footprint solution on boards where area is limited.

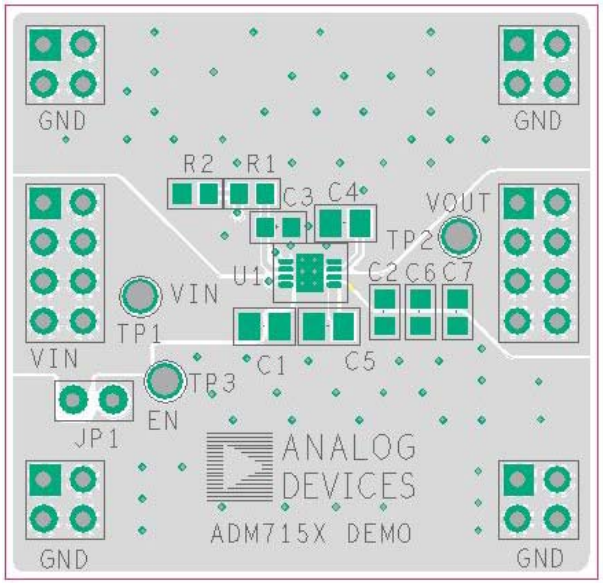

Figure 64. Example 8-Lead LFCSP PCB Layout

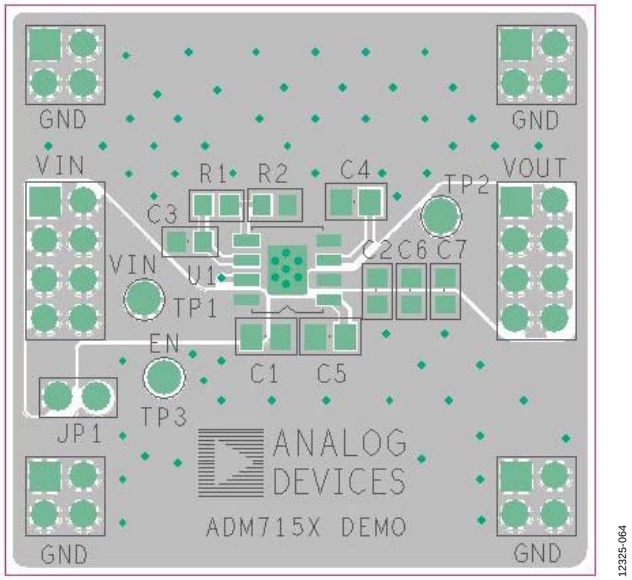

Figure 65. Example 8-Lead SOIC PCB Layout

OUTLINE DIMENSIONS

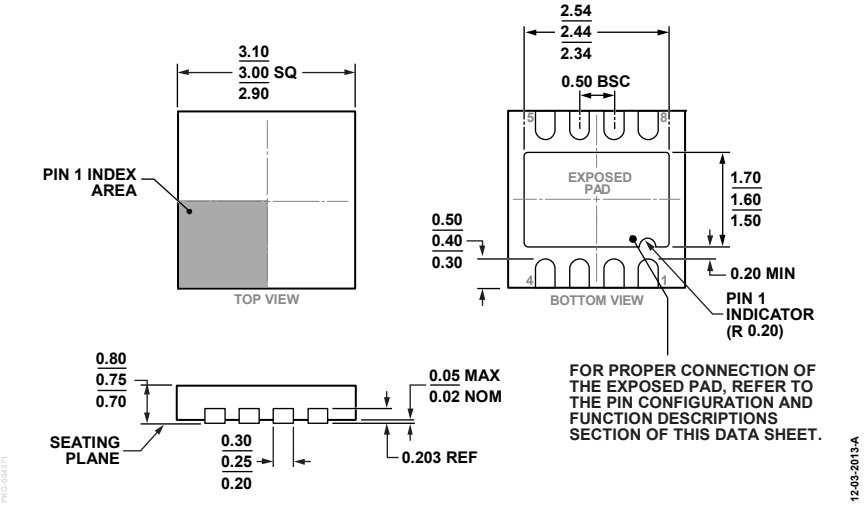

Figure 66. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-21)
Dimensions shown in millimeters

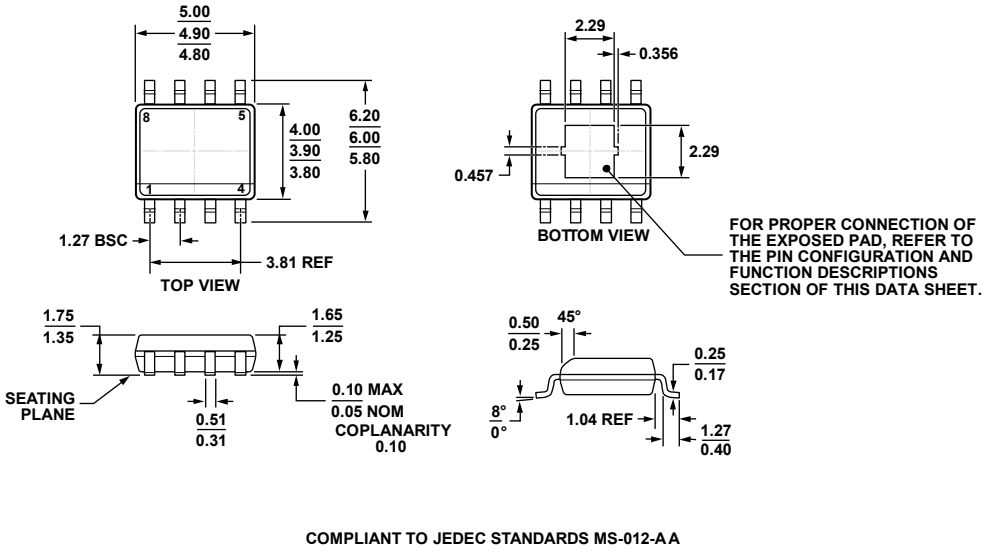

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Figure 67. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage Range (V)	Package Description	Package Option	Branding
ADM7155ACPZ-01-R7	−40°C to +125°C	1.2 to 1.8	8-Lead LFCSP_WD	CP-8-21	LQ8
ADM7155ACPZ-02-R7	−40°C to +125°C	1.2 to 2.4	8-Lead LFCSP_WD	CP-8-21	LQ9
ADM7155ACPZ-03-R7	−40°C to +125°C	1.2 to 2.9	8-Lead LFCSP_WD	CP-8-21	LQA
ADM7155ACPZ-04-R7	−40°C to +125°C	1.2 to 3.4	8-Lead LFCSP_WD	CP-8-21	LQV
ADM7155ARDZ-01-R7	−40°C to +125°C	1.2 to 1.8	8-Lead SOIC_N_EP	RD-8-1	
ADM7155ARDZ-02-R7	−40°C to +125°C	1.2 to 2.4	8-Lead SOIC_N_EP	RD-8-1	
ADM7155ARDZ-03-R7	−40°C to +125°C	1.2 to 2.9	8-Lead SOIC_N_EP	RD-8-1	
ADM7155ARDZ-04-R7	−40°C to +125°C	1.2 to 3.4	8-Lead SOIC_N_EP	RD-8-1	
ADM7155CP-02-EVALZ			Evaluation Board		

[1] Z = RoHS Compliant Part.

D12325-0-8/16(C)

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