THE DATASHEET OF

NHD-1.5-128128G

NEWHAVEN DISPLAY INTERNATIONAL

Product Specification

NHD-1.5-128128G

Graphic Color OLED Display

NHD-	Newhaven Display
1.5-	1.5" Diagonal Size
128128-	128 x 128 Pixels
G-	OLED Glass

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REACH Compliant

RoHS Compliant

NEWHAVEN DISPLAY INTERNATIONAL

Table of Contents

Additional Resources

- **Support Forum:** https://support.newhavendisplay.com/hc/en-us/community/topics
- **GitHub:** https://github.com/newhavendisplay
- **Example Code:** https://support.newhavendisplay.com/hc/en-us/categories/4409527834135-Example-Code/
- **Knowledge Center:** https://www.newhavendisplay.com/knowledge_center.html
- **Quality Center:** https://www.newhavendisplay.com/quality_center.html
- **Precautions for using LCDs/LCMs:** https://www.newhavendisplay.com/specs/precautions.pdf
- **Warranty / Terms & Conditions:** https://www.newhavendisplay.com/terms.html

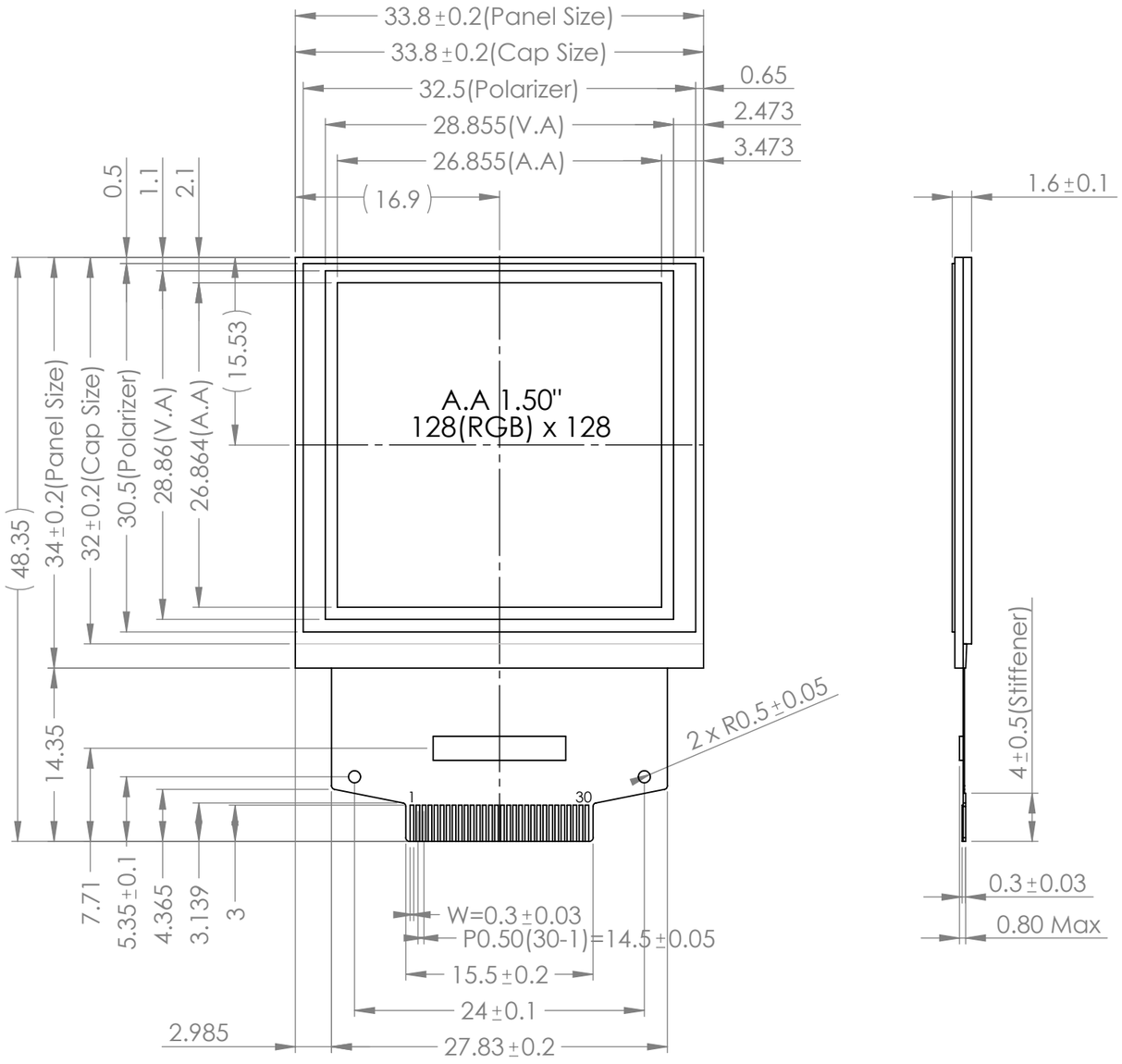
Document Revision History

Revision	Date	Description	Changed By
-	01/15/2019	Initial Release	PB
1	05/08/2020	Added clarification to Vdd (Pin 26) In the Pinout Description	AS
2	08/09/2021	Updated Supply Current Descriptor	ZP
3	04/16/2024	Added Chromaticity Values to Optical Characteristics	KL

Mechanical Drawing

Newhaven Display
NHD-1.5-128128G
Date Code

Part Label (type/format may vary)



Pin	Symbol
1	N.C. (GND)
2	VCC
3	VCOMH
4	VDDIO
5	VSL
6	N.C.
7	D7
8	D6
9	D5
10	D4
11	D3
12	D2
13	D1
14	D0
15	E/RD#
16	R/W#
17	BS0
18	BS1
19	CS#
20	D/C#
21	RES#
22	IREF
23	GPIO1
24	GPIO0
25	N.C.
26	VDD
27	VCI
28	VSS
29	N.C.
30	N.C. (GND)

Product Description: 1.5” 128x128 Color OLED

1. Driver IC: SSD1351
2. Interface: 8-bit 6800/8080 Parallel, 3/4-wire SPI
3. Power Requirement: 2.8V OLED
4. Optical Features: Full Color, Anti-Glare, Full View
5. Recommended FFC Connector: 30pin 0.5mm pitch; Ex. Molex 54104-3033

Standard Tolerance:
(Unless otherwise specified)
Linear: ±0.3mm

NEWHAVEN DISPLAY INTERNATIONAL

Drawing/Part Number: NHD-1.5-128128G
Revision: -

Unless otherwise specified:
• Dimensions are in Millimeters
• Third Angle Projection

Drawn By: K. Lewis
Approved By: K. Lewis
Drawn Date: 04/16/2024
Approved Date: 04/16/2024

Pin Description

Pin No.	Symbol	External Connection	Function Description
1	NC (GND)	-	No connect (can be tied to Ground)
2	V_{CC}	Power Supply	Supply voltage for OLED panel
3	V_{COMH}	Power Supply	Output voltage for COM signal
4	V_{DDIO}	Power Supply	Supply voltage for I/O pins
5	V_{SL}	Power Supply	Output voltage for SEG signal
6	NC	-	No connect
7	D7	MPU	**Parallel interface**: 8-bit bi-directional data bus **Serial interface**: D0 = Serial Clock signal (SCLK) D1 = Serial Data Input signal (SDIN)
8	D6	MPU	
9	D5	MPU	
10	D4	MPU	
11	D3	MPU	
12	D2	MPU	
13	D1	MPU	
14	D0	MPU	
15	E /RD	MPU	**6800 mode**: Enable signal. Falling edge triggered **8080 mode**: Active LOW Read signal
16	R/W /WR	MPU	**6800 mode**: Read/Write signal. LOW: Write. HIGH: Read **8080 mode**: Active LOW Write signal
17	BS0	MPU	MPU interface select signal
18	BS1	MPU	MPU interface select signal
19	/CS	MPU	Active LOW Chip Select signal
20	D/C	MPU	Register Select signal. LOW: Command. HIGH: Data
21	/RES	MPU	Active LOW Reset signal
22	I_{REF}	Power Supply	Output current reference for brightness adjustment
23	GPIO1	MPU	See command 0xB5 (can be treated as a no connect)
24	GPIO0	MPU	See command 0xB5 (can be treated as a no connect)
25	NC	-	No connect
26	V_{DD}	Power Supply	Supply voltage for Logic (generated internally from V_{CI}.) Connect 1µF cap to GND.
27	V_{CI}	Power Supply	Supply voltage for Operation
28	V_{SS}	Power Supply	Ground
29	NC	-	No connect
30	NC (GND)	-	No connect (can be tied to Ground)

Recommended display connector: 30pin 0.5mm pitch top contact FFC connector (Molex 54104-3033 or equivalent)

Interface Selection

MPU Interface Pin Assignment Summary

Bus Interface	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	BS0	BS1	/CS	D/C	/RES	GPIO1	GPIO0
8-bit 6800	D[7:0]								E	R/W	1	1	/CS	D/C	/RES	NC	NC
8-bit 8080	D[7:0]								/RD	/WR	0	1	/CS	D/C	/RES	NC	NC
4-wire SPI	0					NC	SDIN	SCLK	0	0	0	0	/CS	D/C	/RES	NC	NC
3-wire SPI	0					NC	SDIN	SCLK	0	0	1	0	/CS	0	/RES	NC	NC

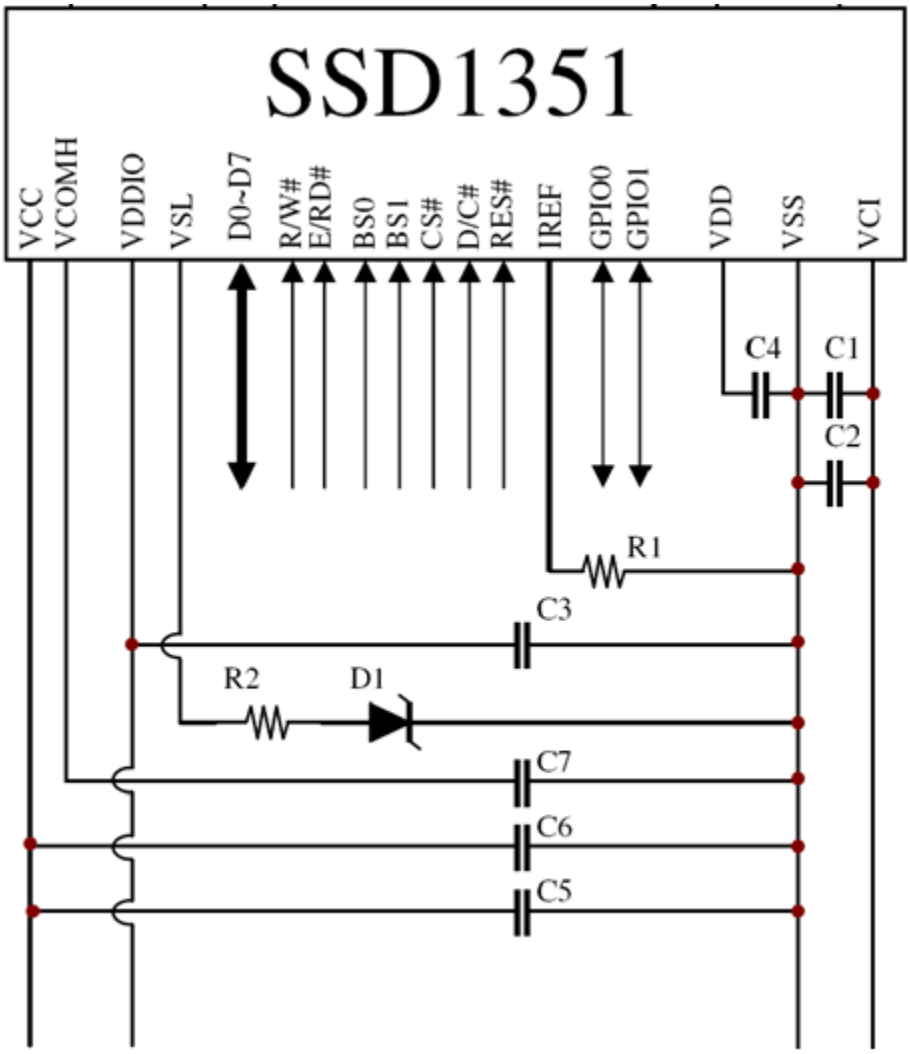
Note:

"NC" : No Connect

"1" : VDD

"0" : VSS

Wiring Diagram



MCU Interface Selection:	BS0 and BS1
Pins connected to MCU interface:	D7~D0, E/RD#, R/W#, CS#, D/C#, and RES#

C1, C5 : 0.1 µF
C2 : 4.7 µF
C6 : 10 µF
C3, C4: 1 µF
C7 : 4.7uF / 25V Tantalum Capacitor
R1 : 560k Ω, R1 = (Voltage at IREF – VSS) / IREF
R2 : 50 Ω, 1/4W
D1 : ≈1.4V, 0.5W

Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T_{OP}	Absolute Max	-40	-	+70	°C
Storage Temperature Range	T_{ST}	Absolute Max	-40	-	+85	°C
Supply Voltage for Logic	V_{DD}	-	2.4	2.5	2.6	V
Supply Voltage for I/O pins	V_{DDIO}	-	1.65	1.8	V_{CI}	V
Supply Voltage for Operation	V_{CI}	-	2.4	2.8	3.5	V
Supply Voltage for Display	V_{CC}	-	12.5	13	13.5	V
Supply Current (Display)	I_{CC}	V_{CC}=13V, 50% ON	-	23.2	29.0	mA
		V_{CC}=13V, 100% ON	-	33.4	42.0	mA
Supply Current (Operation)	I_{CI}	-	-	240	300	µA
Supply Current (Sleep)	$I_{CI, SLEEP}$	V_{CI} = 2.8V	-	4	20	µA
"H" Level input	V_{IH}	-	0.8 * V_{DDIO}	-	V_{DDIO}	V
"L" Level input	V_{IL}	-	V_{SS}	-	0.2 * V_{DDIO}	V
"H" Level output	V_{OH}	-	0.9 * V_{DDIO}	-	V_{DDIO}	V
"L" Level output	V_{OL}	-	V_{SS}	-	0.1 * V_{DDIO}	V

Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Optimal Viewing Angles	Top	ϕY+	-	80	-	-	º
	Bottom	ϕY-		80	-	-	º
	Left	θX-		80	-	-	º
	Right	θX+		80	-	-	º
Contrast Ratio		CR	-	-	>10,000:1	-	-
Response Time	Rise	T_R	T_{OP} =25°C	-	10	-	µs
	Fall	T_F		-	10	-	µs
Brightness		L_V	50% Checkerboard	70	90	-	cd/m²
Lifetime		-	90 cd/m², T_{OP} =25°C, 50% Checkerboard	10,000	-	-	Hrs.
			70 cd/m², T_{OP}=25°C 50% Checkerboard	13,500	-	-	Hrs.
Chromaticity	Red	X_R	-	0.60	0.64	0.68	-
		Y_R	-	0.30	0.34	0.38	-
	Green	X_G	-	0.27	0.31	0.35	-
		Y_G	-	0.58	0.62	0.66	-
	Blue	X_B	-	0.10	0.14	0.18	-
		Y_B	-	0.12	0.16	0.20	-
	White	X_W	-	0.26	0.30	0.34	-
		Y_W	-	0.29	0.33	0.37	-

Note: Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until **Half-Brightness**. The Display OFF command can be used to extend the lifetime of the display.
Luminance of active pixels will degrade faster than inactive pixels. Residual (burn-in) images may occur. To avoid this, every pixel should be illuminated uniformly.

Controller information

Built-in SSD1351 Controller: https://support.newhavendisplay.com/hc/en-us/articles/4414478016663-SSD1351

Table of Commands

(D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated
Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	15	0	0	0	1	0	1	0	1	Set Column Address	A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
1	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	75	0	1	1	1	0	1	0	1	Set Row Address	A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
1	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0	A0	1	0	1	0	0	0	0	0	Set Re-map / Color Depth (Display RAM to Panel)	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Column address 0 is mapped to SEG0 [reset] A[1]=1b, Column address 127 is mapped to SEG0 A[2]=0b, Color sequence: A → B → C [reset] A[2]=1b, Color sequence is swapped: C → B → A A[3]=0b, Reserved A[3]=1b, Reserved A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0. Where N is the Multiplex ratio. A[5]=0b, Disable COM Split Odd Even A[5]=1b, Enable COM Split Odd Even [reset] A[7:6] Set Color Depth, 00b / 01b: 65k color [reset] 10b: 262k color 11b 262k color, 16-bit format 2 Refer to Table 8-8 for details
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 1	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set vertical scroll by RAM from 0~127. [reset=00h]
0 1	A2 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by Row from 0-127. [reset=60h] **Note** (1) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.
0	A4~A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4h: All OFF A5h: All ON (All pixels have GS63) A6h : Reset to normal display [reset] A7h: Inverse Display (GS0 -> GS63, GS1 -> GS62, ...)
0 1	AB A[7:0]	1 A_7	0 A_6	1 0	0 0	1 0	0 0	1 0	1 A_0	Function Selection	A[0]=0b, Select external V_{DD} A[0]=1b, Enable internal V_{DD} regulator [reset] A[7:6]=00b, Select 8-bit parallel interface [reset] A[7:6]=01b, Select 16-bit parallel interface A[7:6]=11b, Select 18-bit parallel interface
0	AD	1	0	1	0	1	1	0	1	NOP	Command for no operation.
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode ON/OFF	AEh = Sleep mode On (Display OFF) AFh = Sleep mode OFF (Display ON)
0	B0	1	0	1	1	0	0	0	0	NOP	Command for no operation.
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Reset (Phase 1) / Pre-charge (Phase 2) period	A[3:0] Phase 1 period of 5~31 DCLK(s) clocks [reset=0010b] A[3:0]: 0-1 invalid 2 = 5 DCLKs 3 = 7 DCLKs : 15 = 31DCLKs A[7:4] Phase 2 period of 3~15 DCLK(s) clocks [reset=1000b] A[7:4]: 0-2 invalid 3 = 3 DCLKs 4 = 4 DCLKs : 15 =15DCLKs Note (1) 0 DCLK is invalid in phase 1 & phase 2 (2)This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	B2	1	0	1	1	0	0	1	0	Display Enhancement	A[7:0] = 00h, B[7:0] = 00h, C[7:0] = 00h normal [reset] A[7:0] = A4h, B[7:0] = 00h, C[7:0] = 00h enhance display performance
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	0	0	0	0	0	0	0	0		
1	C[7:0]	0	0	0	0	0	0	0	0		
0	B3	1	0	1	1	0	0	1	1	Front Clock Divider (DivSet)/ Oscillator Frequency	A[3:0] [reset=0001], divide by DIVSET where A[7:4] Oscillator frequency, frequency increases as level increases [reset=1101b] **Note** (1) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B4	1	0	1	1	0	1	0	0	Set Segment Low Voltage (VSL)	A[1:0]=00 External VSL [reset] A[1:0]=01,10,11 are invalid **Note** (1) When external VSL is enabled, in order to avoid distortion in display pattern, an external circuit is needed to connect between VSL and V_{SS} as shown in Figure 14-1
1	A[7:0]	1	0	1	0	0	0	A_1	A_0		
1	B[7:0]	1	0	1	1	0	1	0	1		
1	C[7:0]	0	1	0	1	0	1	0	1		
0	B5	1	0	1	1	0	1	0	1	Set GPIO	A[1:0] GPIO0: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH A[3:2] GPIO1: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH
1	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	B6	1	0	1	1	0	1	0	0	Set Second Pre-charge Period	A[3:0] Set Second Pre-charge Period 0000b invalid 0001b 1 DCLKS 0010b 2 DCLKS .... 1000 8 DCLKS [reset] .... 1111 15 DCLKS
1	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		

A[3:0]	DIVSET
0000	divide by 1
0001	divide by 2
0010	divide by 4
0011	divide by 8
0100	divide by 16
0101	divide by 32
0110	divide by 64
0111	divide by 128
1000	divide by 256
1001	divide by 512
1010	divide by 1024
>=1011	invalid

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	B8	1	0	1	1	1	0	0	0	Look Up Table for Gray Scale Pulse width	The next 63 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : A62[7:0]: Gamma Setting for GS62, A63[7:0]: Gamma Setting for GS63 **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS62 < Setting of GS63 (2) GS0 has only pre-charge but no current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0.
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A62[7:0]	$A62_7$	$A62_6$	$A62_5$	$A62_4$	$A62_3$	$A62_2$	$A62_1$	$A62_0$		
1	A63[7:0]	$A63_7$	$A63_6$	$A63_5$	$A63_4$	$A63_3$	$A63_2$	$A63_1$	$A63_0$		
0	B9	1	0	1	1	1	0	0	1	Use Built-in Linear LUT [reset= linear]	Reset to default Look Up Table: GS1 = 0 DCLK GS2 = 2 DCLK GS3 = 4 DCLK GS4 = 6 DCLK ... GS62 = 122 DCLK GS63 = 124 DCLK
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 17h]
1	A[4:0]	0	0	0	A_4	A_3	A_2	A_1	A_0		

A[4:0]	Hex code	pre-charge voltage
00000	00h	0.20 x V_{CC}
:	:	:
11111	1Fh	0.60 x V_{CC}

Note
(1) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.

0	BE	1	0	1	1	1	1	1	0	Set V_{COMH} Voltage	Set COM deselect voltage level [reset = 05h]
1	A[2:0]	0	0	0	0	0	A_2	A_1	A_0		

A[2:0]	Hex code	V_{COMH}
000	00h	0.72 x V_{CC}
:	:	:
101	05h	0.82 x V_{CC} [reset]
:	:	:
111	07h	0.86 x V_{CC}

Note
(1) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	C1	1	1	0	0	0	0	0	1	Set Contrast Current for Color A,B,C	A[7:0] Contrast Value Color A [reset=10001010b] B[7:0] Contrast Value Color B [reset=01010001b] C[7:0] Contrast Value Color C [reset=10001010b]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	C7	1	1	0	0	0	1	1	1	Master Contrast Current Control	A[3:0] : 0000b reduce output currents for all colors to 1/16 0001b reduce output currents for all colors to 2/16 .... 1110b reduce output currents for all colors to 15/16 1111b no change [reset]
1	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	CA	1	1	0	0	1	0	1	0	Set MUX Ratio	A[6:0] MUX ratio 16MUX ~ 128MUX, [reset=127], (Range from 15 to 127)
1	A[6:0]	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	D1	1	0	1	0	1	1	0	1	NOP	Command for No Operation
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[7:0]: MCU protection status [reset = 12h] A[7:0] = 12b, Unlock OLED driver IC MCU interface from entering command [reset] A[7:0] = 16b, Lock OLED driver IC MCU interface from entering command A[7:0] = B0b, Command A2,B1,B3,BB,BE,C1 inaccessible in both lock and unlock state [reset] A[7:0] = B1b, Command A2,B1,B3,BB,BE,C1 accessible if in unlock state **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Set (GAC) (D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated
Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

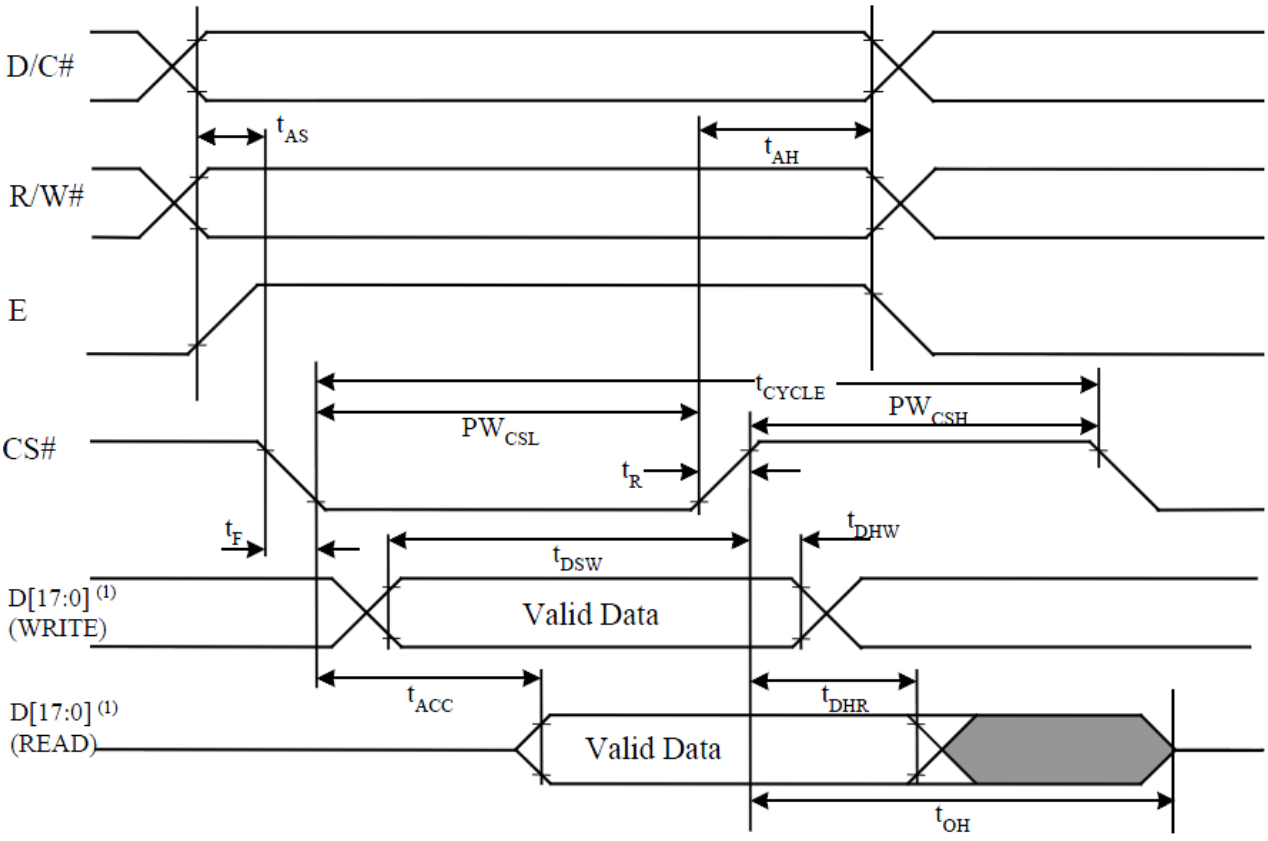
Graphic acceleration command											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0	96	1	0	0	1	0	1	1	0	Horizontal Scroll	A[7:0] = 00000000b No scrolling A[7:0] = 00000001b to 00111111b Scroll towards SEG127 with 1 column offset A[7:0] = 01000000b to 11111111b Scroll towards SEG0 with 1 column offset B[6:0] : start row address C[7:0] : number of rows to be H-scrolled B+C <= 128 D[6:0] : Reserved (reset=00h) E[1:0] : scrolling time interval 00b test mode 01b normal 10b slow 11b slowest **Note** (1) Operates during display ON.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[6:0]	0	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[6:0]	0	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[1:0]	0	0	0	0	0	0	E_1	E_0		
0	9E	1	0	0	1	1	1	1	0	Stop Moving	Stop horizontal scroll **Note** (1) After sending 9Eh command to stop the scrolling action, the ram data needs to be rewritten
0	9F	1	0	0	1	1	1	1	1	Start Moving	Start horizontal scroll

Note
(1) After executed the graphic command, waiting time is required for update GDDRAM content.
V_{CI} =2.4~3.5V, waiting time = 500ns/pixel.

Timing Characteristics

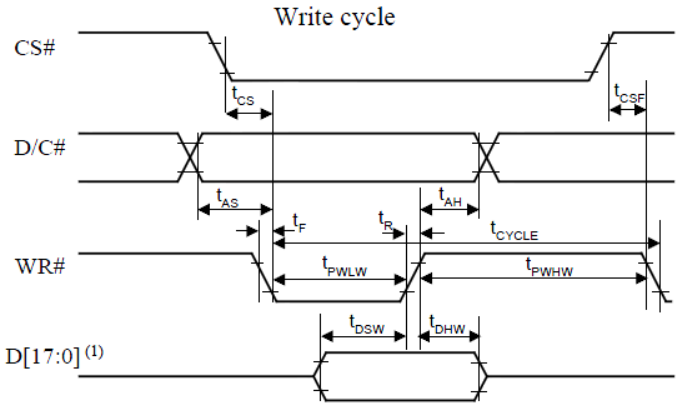
6800-Series MCU Parallel Interface:

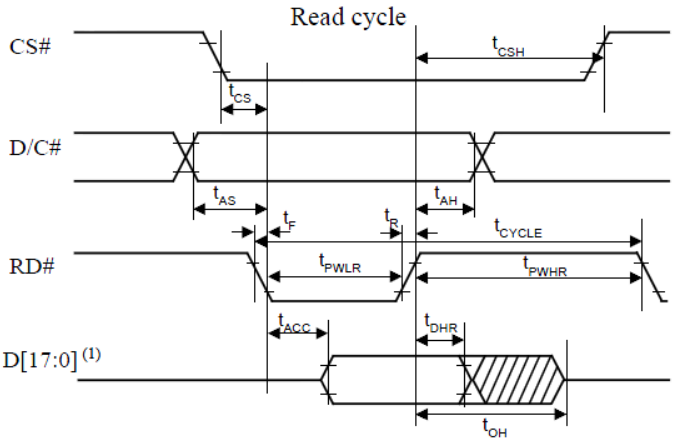
Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (read) Clock Cycle Time (write)	320 300	-	-	ns
t_{AS}	Address Setup Time	24	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8080-Series MCU Parallel Interface:

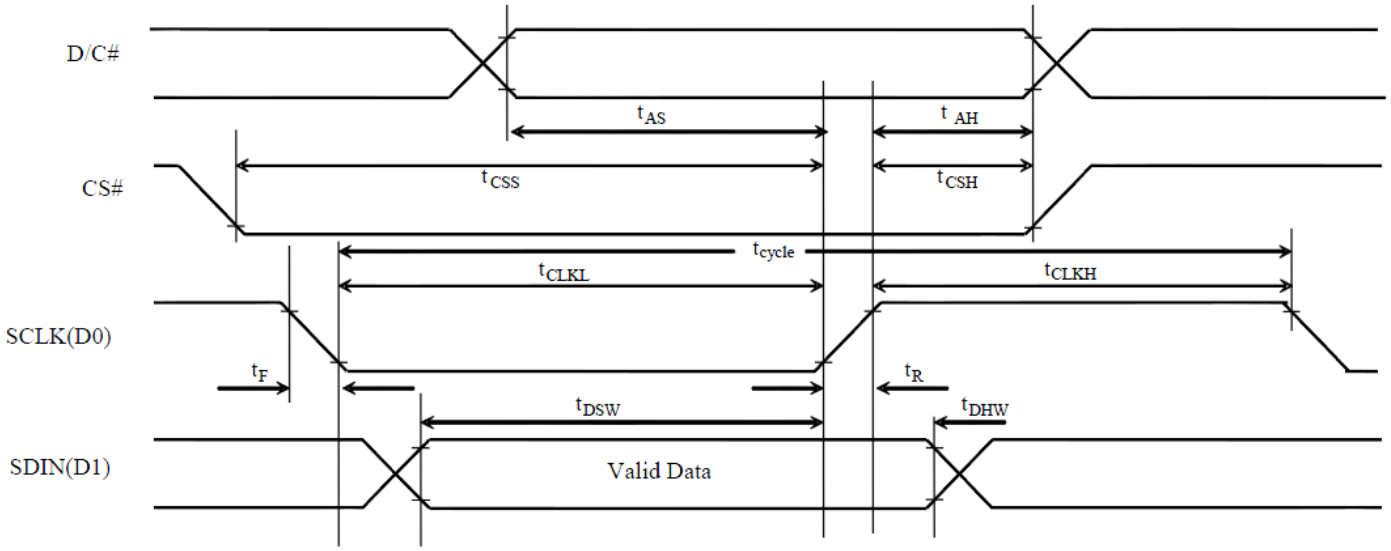
Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	46	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

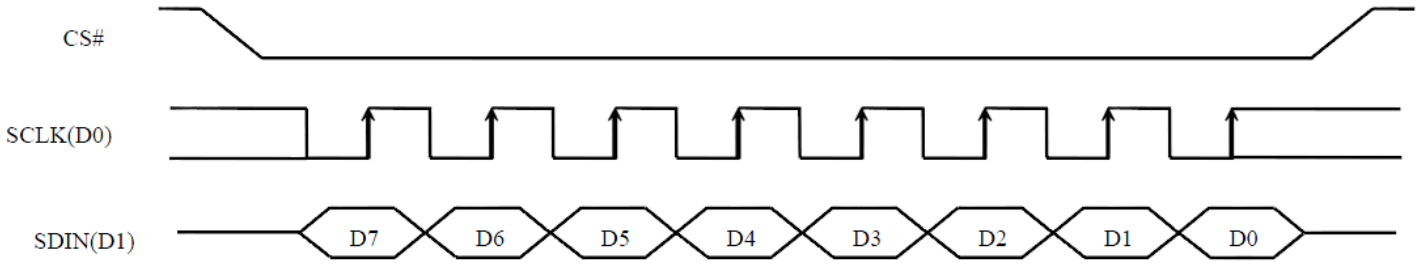




4-wire SPI:

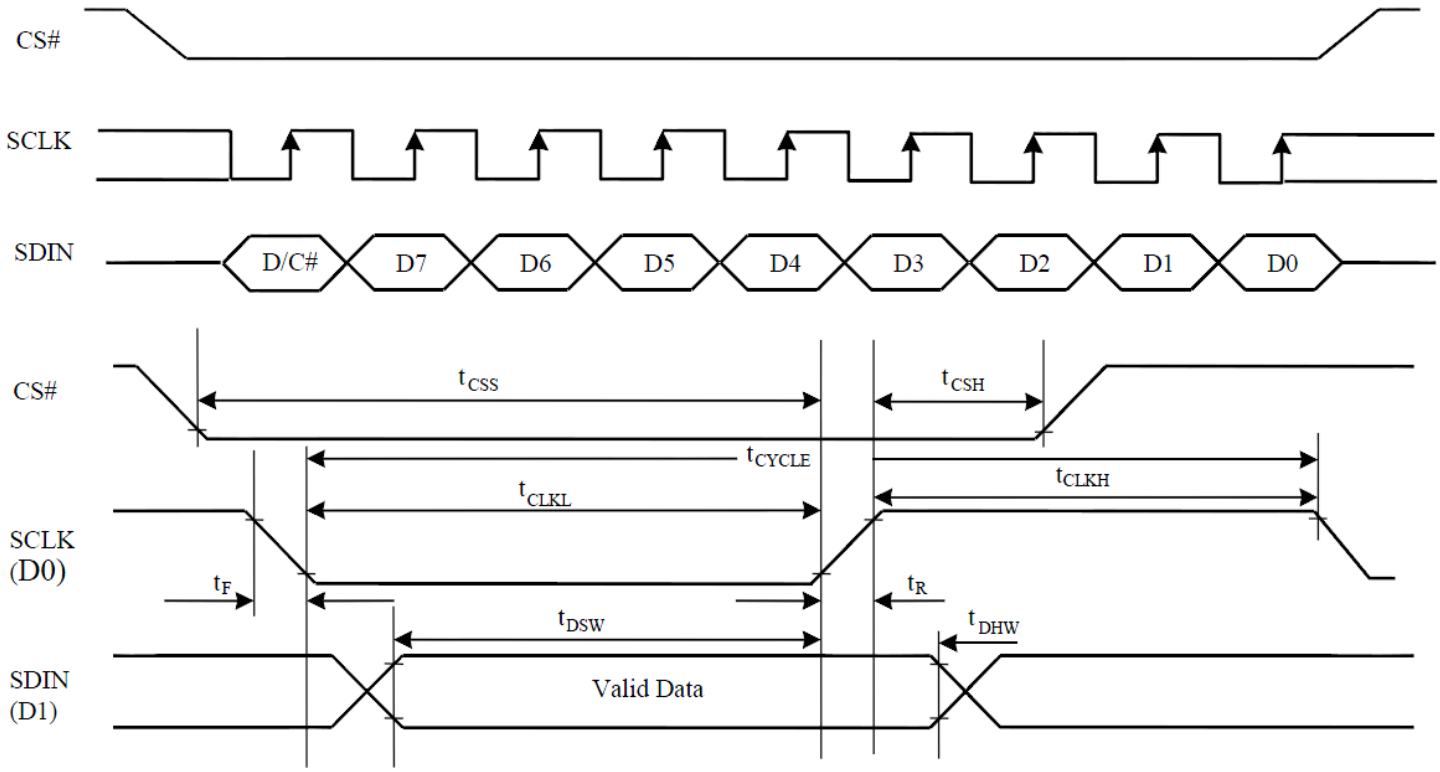
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	220	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	42	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns





3-wire SPI:

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	220	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	44	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



Example Initialization Sequence:

```
void OLED_Init_128128RGB(void)
{
GPIO_ResetBits(RES_pin);
delay_ms(300);
GPIO_SetBits(RES_pin);
delay_ms(10);

oled_Command_128128RGB(0xFD);          //Command lock setting
oled_Data_128128RGB(0x12);             //unlock
oled_Command_128128RGB(0xFD);          //Command lock setting
oled_Data_128128RGB(0xB1);             //unlock

oled_Command_128128RGB(0xAE);          //Set Display OFF

oled_Command_128128RGB(0xB3);          //Set Display Clock Divide Ratio
oled_Data_128128RGB(0xF1);

oled_Command_128128RGB(0xCA);          //Set MUX ratio
oled_Data_128128RGB(0x7F);

oled_Command_128128RGB(0xA2);  //Set Display offset
oled_Data_128128RGB(0x00);

oled_Command_128128RGB(0xA1);          //Set display start line
oled_Data_128128RGB(0x00);

oled_Command_128128RGB(0xA0);          //Set Re-map, color depth
oled_Data_128128RGB(0xB4);

oled_Command_128128RGB(0xB5);          //set GPIO
oled_Data_128128RGB(0x00);

oled_Command_128128RGB(0xAB);          //Function Set
oled_Data_128128RGB(0x01);

oled_Command_128128RGB(0xB4);          //Set Segment Low Voltage
oled_Data_128128RGB(0xA0);
oled_Data_128128RGB(0xB5);
oled_Data_128128RGB(0x55);

oled_Command_128128RGB(0xC1);          //Set Contrast Current
oled_Data_128128RGB(0xC8);
oled_Data_128128RGB(0x80);
oled_Data_128128RGB(0xC8);

oled_Command_128128RGB(0xC7);          //Master Contrast Current Control
oled_Data_128128RGB(0x0F);

oled_Command_128128RGB(0xB9);          //use linear grayscale LUT

oled_Command_128128RGB(0xB1);          //Set Phase Length
oled_Data_128128RGB(0x32);

oled_Command_128128RGB(0xBB);          //Set Pre-charge Voltage
```

```
oled_Data_128128RGB(0x17);

oled_Command_128128RGB(0xB2);          //Display enhancement
oled_Data_128128RGB(0xa4);
oled_Data_128128RGB(0x00);
oled_Data_128128RGB(0x00);

oled_Command_128128RGB(0xB6);          //Set Second Pre-charge Period
oled_Data_128128RGB(0x01);

oled_Command_128128RGB(0xBE);          //Set VCOMH
oled_Data_128128RGB(0x05);

oled_Command_128128RGB(0xA6);          //Normal display

oled_Clear_Screen();                   //Clear Display (write all 0x00's to display RAM)

oled_Command_128128RGB(0xAF);          //Set Display ON

delay_ms(200);

oled_Command_128128RGB(0x5C);          //Enable Write to RAM command
}
```

Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Test the endurance of the display at high storage temperature.	+85°C, 96hrs	2
Low Temperature storage	Test the endurance of the display at low storage temperature.	-40°C, 96hrs	1,2
High Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature.	+70°C, 96hrs	2
Low Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at low temperature.	-40°C, 96hrs	1,2
High Temperature / Humidity Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature with high humidity.	+60°C, 90% RH, 96hrs	1,2
Thermal Shock resistance	Test the endurance of the display by applying electric stress (voltage & current) during a cycle of low and high temperatures.	-30°C,30min -> 25°C,5min -> 70°C,30min = 1 cycle 100 cycles	
Vibration test	Test the endurance of the display by applying vibration to simulate transportation and use.	10-22Hz , 15mm amplitude. 22-500Hz, 1.5G 30min in each of 3 directions X,Y,Z	3
Atmospheric Pressure test	Test the endurance of the display by applying atmospheric pressure to simulate transportation by air.	115mbar, 40hrs	3
Static electricity test	Test the endurance of the display by applying electric static discharge.	VS=800V, RS=1.5kΩ, CS=100pF One time	

Note 1: No condensation to be observed.
Note 2: Conducted after 2 hours of storage at 25°C, 0%RH.
Note 3: Test performed on product itself, not inside a container.
Evaluation Criteria:
1: Display is fully functional during operational tests and after all tests, at room temperature.
2: No observable defects.
3: Luminance >50% of initial value.
4: Current consumption within 50% of initial value

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