



**THE DATASHEET OF  
74LVT646PW,112**



# DATA SHEET

## **74LVT646**

**3.3V Octal bus transceiver/register  
(3-State)**

Product specification  
Supersedes data of 1994 May 20  
IC23 Data Handbook

1998 Feb 19

## 3.3V Octal bus transceiver/register (3-State)

74LVT646

## FEATURES

- Combines 74LVT245 and 74LVT574 type functions in one device
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Output capability: +64mA/−32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- Power-up 3-State
- Power-up reset
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

## DESCRIPTION

The LVT646 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3V.

This device consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers.

Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High.

Output Enable ( $\overline{OE}$ ) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real-time. The DIR determines which bus will receive data when the  $\overline{OE}$  is active (Low).

In the isolation mode ( $\overline{OE} = \text{High}$ ), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the 74LVT646.

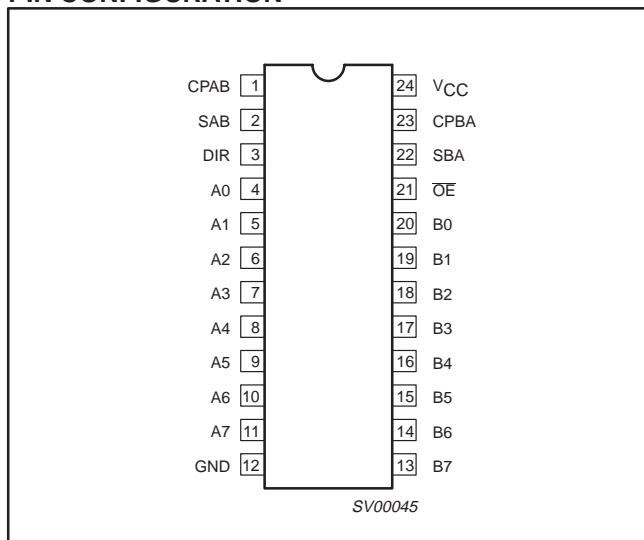
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF}; V_{CC} = 3.3\text{V}$	2.8 2.7	ns
$C_{IN}$	Input capacitance CP, S, $\overline{OE}$ , DIR	$V_{I/O} = 0\text{V}$ or 3.0V	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O} = 0\text{V}$ or 3.0V	10	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 3.6\text{V}$	0.13	mA

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic SOL	−40°C to +85°C	74LVT646 D	74LVT646 D	SOT163-1
24-Pin Plastic SSOP Type II	−40°C to +85°C	74LVT646 DB	74LVT646 DB	SOT399-1
24-Pin Plastic TSSOP Type I	−40°C to +85°C	74LVT646 PW	74LVT646PW DH	SOT360-1

## PIN CONFIGURATION



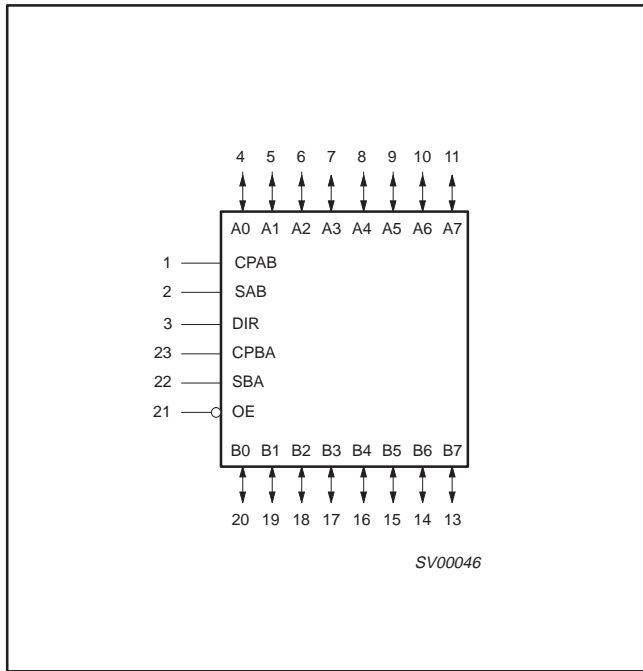
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input (active-low)
12	GND	Ground (0V)
24	$V_{CC}$	Positive supply voltage

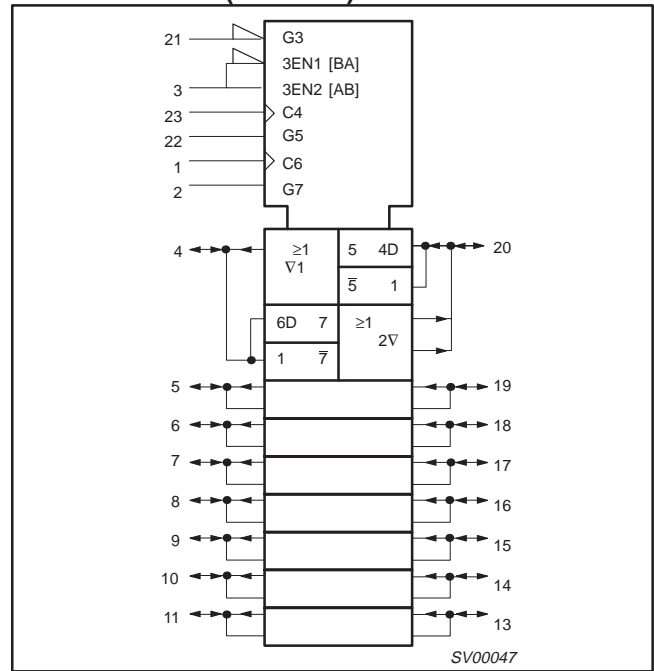
# 3.3V Octal bus transceiver/register (3-State)

# 74LVT646

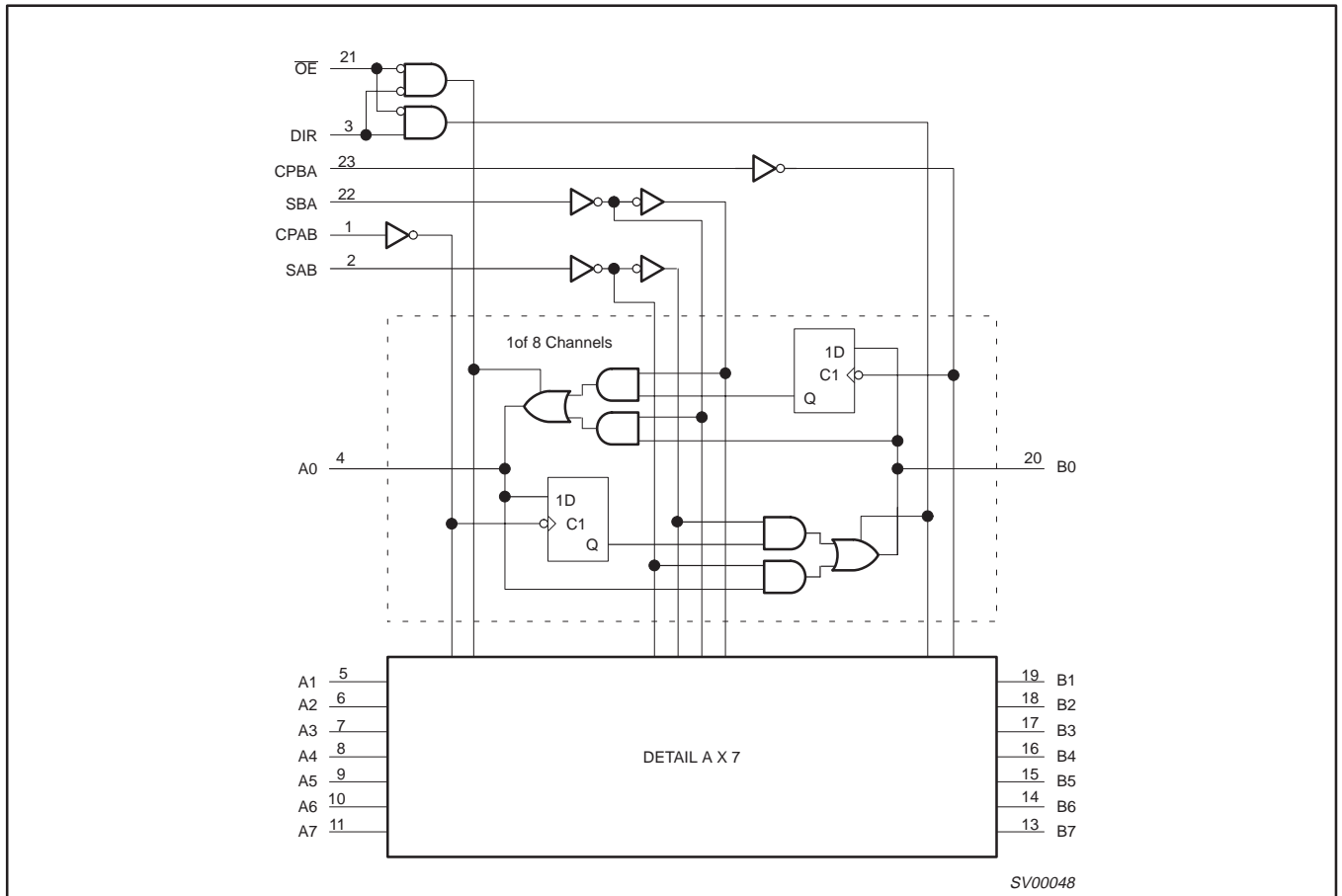
## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)

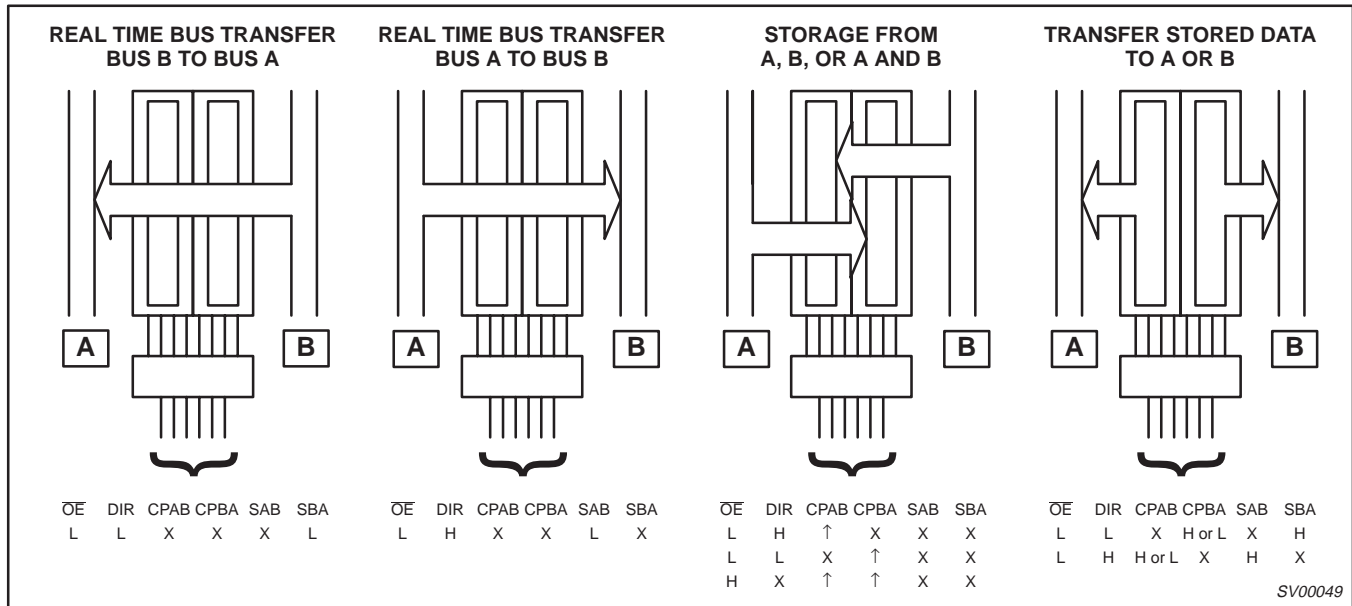


## LOGIC DIAGRAM



### 3.3V Octal bus transceiver/register (3-State)

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#### FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	
X	X	$\uparrow$	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	$\uparrow$	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	$\uparrow$ H or L	$\uparrow$ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level

L = Low voltage level

X = Don't care

$\uparrow$  = Low-to-High clock transition

\* The data output function may be enabled or disabled by various signals at the  $\overline{OE}$  input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

## 3.3V Octal bus transceiver/register (3-State)

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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +7.0	V
I <sub>OUT</sub>	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T <sub>stg</sub>	Storage temperature range		-65 to 150	°C

**NOTES:**

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V <sub>CC</sub>	DC supply voltage	2.7	3.6	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0		V
V <sub>IL</sub>	Input voltage		0.8	V
I <sub>OH</sub>	High-level output current		-32	mA
I <sub>OL</sub>	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP NO TAG	MAX	
$V_{IK}$	Input clamp voltage	$V_{CC} = 2.7V$ ; $I_{IK} = -18mA$		-0.9	-1.2	V
$V_{OH}$	High-level output voltage	$V_{CC} = 2.7$ to $3.6V$ ; $I_{OH} = -100\mu A$	$V_{CC}-0.2$	$V_{CC}-0.1$		V
		$V_{CC} = 2.7V$ ; $I_{OH} = -8mA$	2.4	2.5		
		$V_{CC} = 3.0V$ ; $I_{OH} = -32mA$	2.0	2.2		
$V_{OL}$	Low-level output voltage	$V_{CC} = 2.7V$ ; $I_{OL} = 100\mu A$		0.1	0.2	V
		$V_{CC} = 2.7V$ ; $I_{OL} = 24mA$		0.3	0.5	
		$V_{CC} = 3.0V$ ; $I_{OL} = 16mA$		0.25	0.4	
		$V_{CC} = 3.0V$ ; $I_{OL} = 32mA$		0.3	0.5	
		$V_{CC} = 3.0V$ ; $I_{OL} = 64mA$		0.4	0.55	
$V_{RST}$	Power-up output low voltage <sup>5</sup>	$V_{CC} = 3.6V$ ; $I_O = 1mA$ ; $V_I = GND$ or $V_{CC}$		0.13	0.55	V
$I_I$	Input leakage current	$V_{CC} = 3.6V$ ; $V_I = V_{CC}$ or GND	Control pins	$\pm 0.1$	$\pm 1$	$\mu A$
		$V_{CC} = 0$ or $3.6V$ ; $V_I = 5.5V$		1	10	
		$V_{CC} = 3.6V$ ; $V_I = 5.5V$	I/O Data pins <sup>4</sup>	1	20	
		$V_{CC} = 3.6V$ ; $V_I = V_{CC}$		0.1	1	
		$V_{CC} = 3.6V$ ; $V_I = 0$		-1	-5	
$I_{OFF}$	Output off current	$V_{CC} = 0V$ ; $V_I$ or $V_O = 0$ to $4.5V$		1	$\pm 100$	$\mu A$
$I_{HOLD}$	Bus Hold current A inputs <sup>6</sup>	$V_{CC} = 3V$ ; $V_I = 0.8V$	75	150		$\mu A$
		$V_{CC} = 3V$ ; $V_I = 2.0V$	-75	-150		
		$V_{CC} = 0V$ to $3.6V$ ; $V_{CC} = 3.6V$	$\pm 500$			
$I_{EX}$	Current into an output in the High state when $V_O > V_{CC}$	$V_O = 5.5V$ ; $V_{CC} = 3.0V$		60	125	$\mu A$
$I_{PU/PD}$	Power up/down 3-State output current <sup>3</sup>	$V_{CC} \leq 1.2V$ ; $V_O = 0.5V$ to $V_{CC}$ ; $V_I = GND$ or $V_{CC}$ ; OE/OE = Don't care		15	$\pm 100$	$\mu A$
$I_{CCH}$	Quiescent supply current	$V_{CC} = 3.6V$ ; Outputs High, $V_I = GND$ or $V_{CC}$ , $I_O = 0$		0.13	0.19	mA
$I_{CCL}$		$V_{CC} = 3.6V$ ; Outputs Low, $V_I = GND$ or $V_{CC}$ , $I_O = 0$		3	12	
$I_{CCZ}$		$V_{CC} = 3.6V$ ; Outputs Disabled; $V_I = GND$ or $V_{CC}$ , $I_O = 0$		0.13	0.19	
$\Delta I_{CC}$	Additional supply current per input pin <sup>2</sup>	$V_{CC} = 3V$ to $3.6V$ ; One input at $V_{CC}-0.6V$ , Other inputs at $V_{CC}$ or GND		0.1	0.2	mA

## NOTES:

- All typical values are at and  $T_{amb} = 25^\circ C$ .
- This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND
- This parameter is valid for any  $V_{CC}$  between 0V and 1.2V with a transition time of up to 10msec. From  $V_{CC} = 1.2V$  to  $V_{CC} = 3.3V \pm 0.3V$  a transition time of 100 $\mu$ sec is permitted. This parameter is valid for  $T_{amb} = 25^\circ C$  only.
- Unused pins at  $V_{CC}$  or GND.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

## 3.3V Octal bus transceiver/register (3-State)

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**AC CHARACTERISTICS**GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP <sup>1</sup>	MAX	MAX	
$f_{\text{MAX}}$	Maximum clock frequency	1	150	180			MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay CPAB to Bn or CPBA to An	1	1.8 2.1	3.8 3.8	5.7 5.7	6.7 6.4	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay An to Bn or Bn to An	2	1.3 1.0	2.8 2.7	4.7 4.6	5.4 5.3	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay SAB to Bn or SBA to An	2 3	1.4 1.4	3.7 3.8	6.2 6.2	7.2 6.8	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time OE to An or Bn	5 6	1.0 1.0	4.0 4.1	5.8 6.0	7.2 7.3	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time OE to An or Bn	5 6	2.3 2.2	4.3 3.8	6.5 5.8	6.9 5.9	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time DIR to An or Bn	5 6	1.0 1.2	3.4 3.4	6.5 6.3	7.5 7.1	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time DIR to An or Bn	5 6	1.7 1.5	4.1 3.5	7.2 5.8	8.1 6.3	ns

**NOTE:**1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .**AC SETUP REQUIREMENTS**GND = 0V,  $t_R = 2.5\text{ns}$ ,  $t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
			Min	Typ	Min		
$t_s(\text{H})$ $t_s(\text{L})$	Setup time <sup>1</sup> An to CPAB, Bn to CPBA	4	1.5 2.0	1.0 1.0	1.6 2.4		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time <sup>1</sup> An to CPAB, Bn to CPBA	4	0.0 0.0	-1.0 -1.0	0.0 0.0		ns
$t_w(\text{H})$ $t_w(\text{L})$	Pulse width, High or Low CPAB or CPBA	1	3.3 3.3	1.0 2.0	3.3 3.3		ns

**NOTE:**

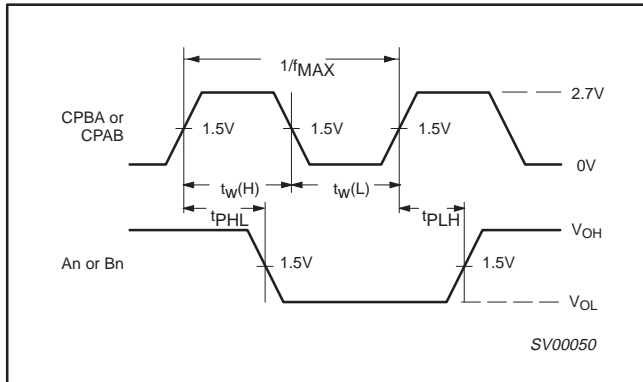
1. This data sheet limit may vary among suppliers.

# 3.3V Octal bus transceiver/register (3-State)

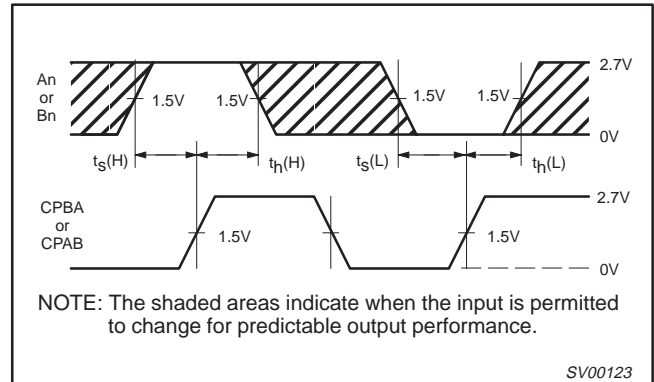
# 74LVT646

## AC WAVEFORMS

$V_M = 1.5V$ ,  $V_{IN} = GND$  to  $2.7V$

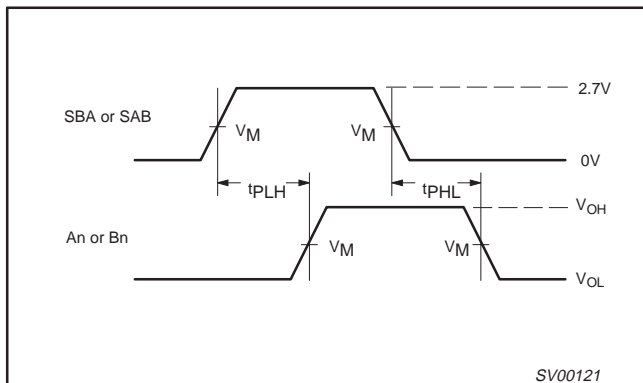


**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**

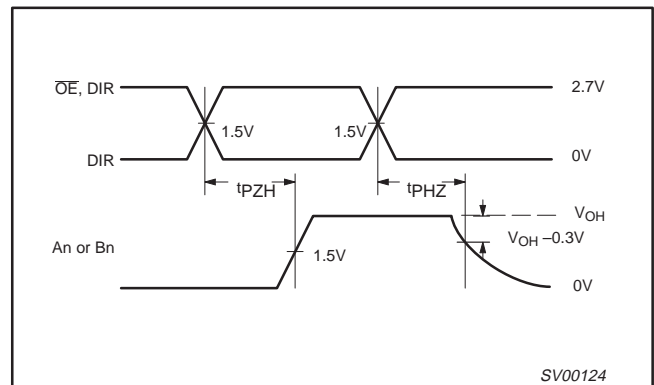


NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

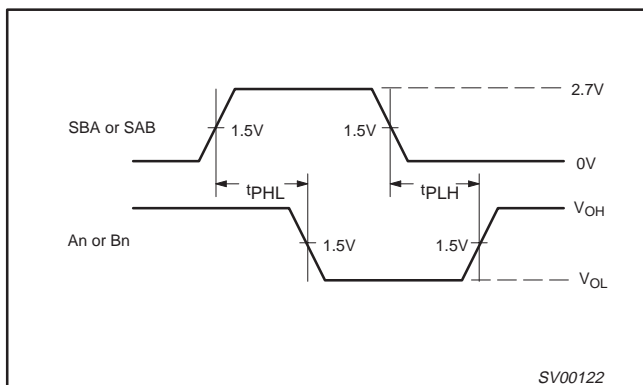
**Waveform 4. Data Setup and Hold Times**



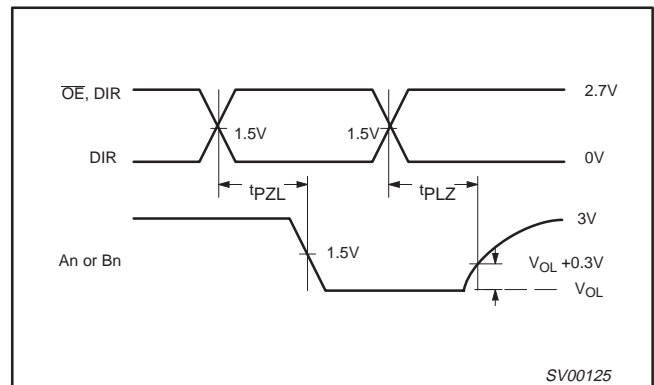
**Waveform 2. Propagation Delay, SAB to Bn or SBA to An, An to Bn or Bn to An**



**Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level**



**Waveform 3. Propagation Delay, SBA to An or SAB to Bn**

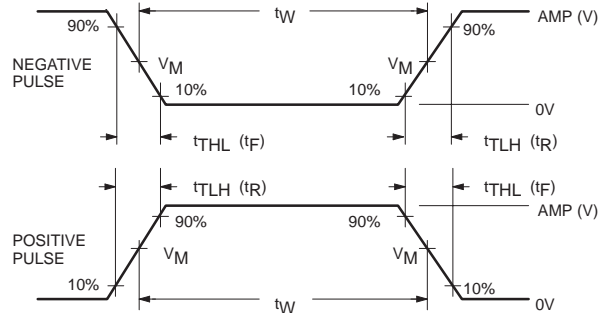
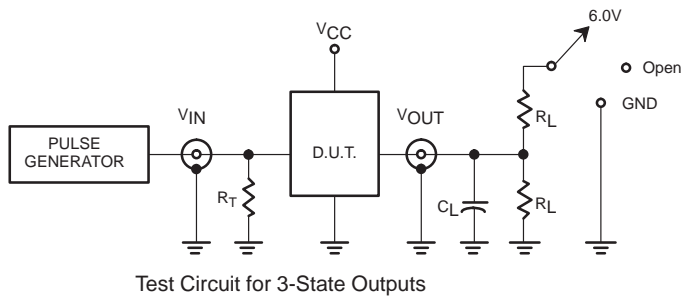


**Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

# 3.3V Octal bus transceiver/register (3-State)

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## TEST CIRCUIT AND WAVEFORM



$V_M = 1.5V$   
Input Pulse Definition

### SWITCH POSITION

TEST	SWITCH
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6V
$t_{PHZ}/t_{PZH}$	GND

### DEFINITIONS

- $R_L$  = Load resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74LVT	2.7V	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$

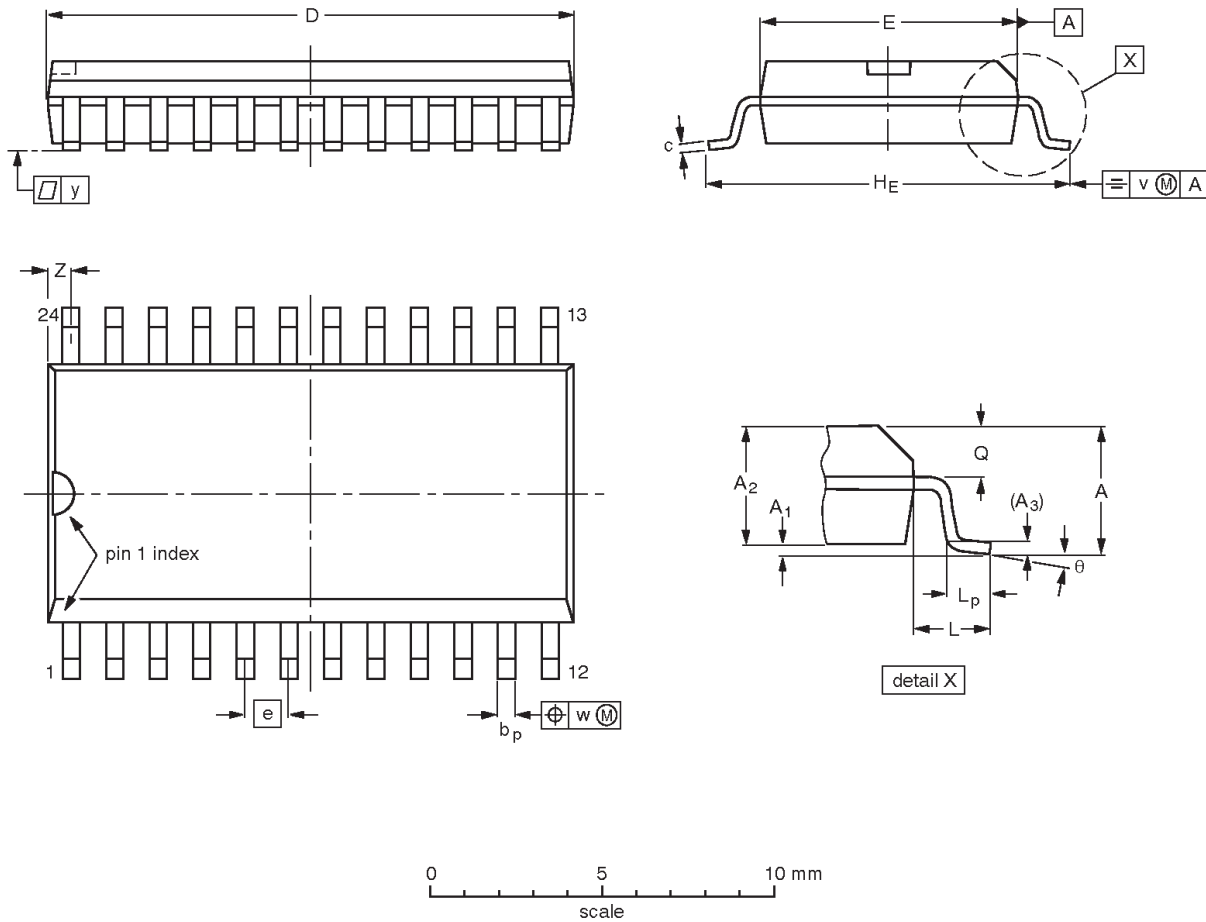
SV00092

# 3.3V Octal bus transceiver/register (3-State)

# 74LVT646

**SO24:** plastic small outline package; 24 leads; body width 7.5 mm

**SOT137-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

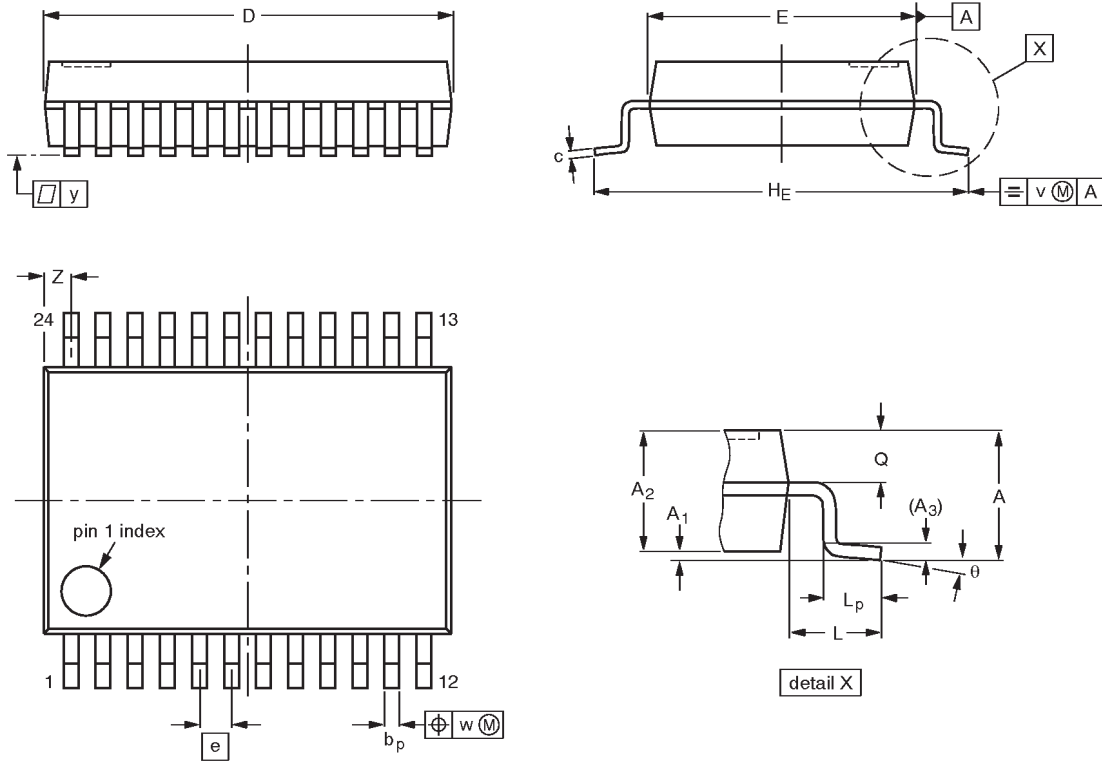
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

# 3.3V Octal bus transceiver/register (3-State)

# 74LVT646

**SSOP24:** plastic shrink small outline package; 24 leads; body width 5.3 mm

**SOT340-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

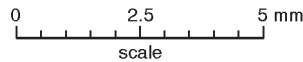
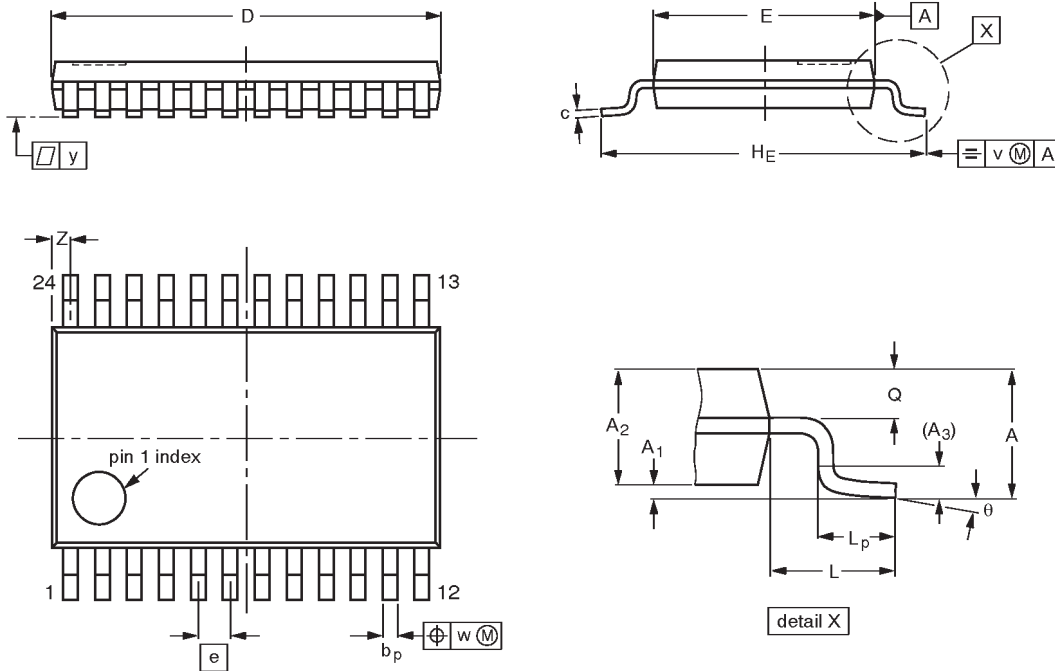
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

### 3.3V Octal bus transceiver/register (3-State)

74LVT646

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				93-06-16 95-02-04

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3.3V Octal bus transceiver/register (3-State)

74LVT646

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**NOTES**

## 3.3V Octal bus transceiver/register (3-State)

74LVT646

## Data sheet status

Data sheet status	Product status	Definition [1]
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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