

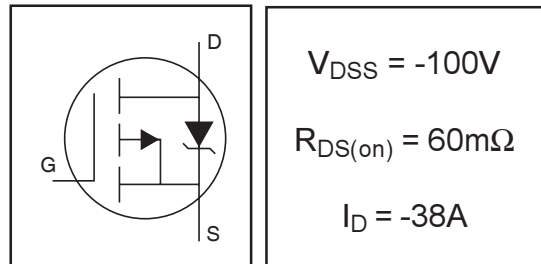


**THE DATASHEET OF  
IRF5210LPBF**

**IRF5210SPbF**  
**IRF5210LPbF**

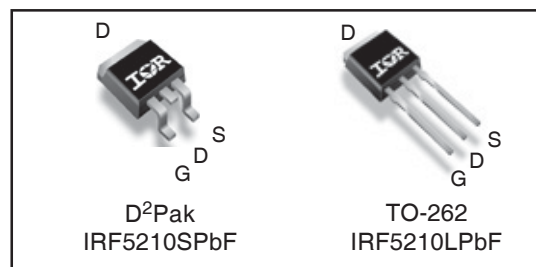
HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- 150°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to  $T_{jmax}$
- Some Parameters are Different from IRF5210S/L
- P-Channel
- Lead-Free



**Description**

Features of this design are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of other applications.



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-38	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-24	
$I_{DM}$	Pulsed Drain Current ①	-140	
$P_D @ T_A = 25^\circ C$	Maximum Power Dissipation	3.1	W
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	170	
	Linear Derating Factor	1.3	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	120	mJ
$I_{AR}$	Avalanche Current ①	-23	A
$E_{AR}$	Repetitive Avalanche Energy ①	17	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-7.4	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑤	—	40	

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	60	m $\Omega$	$V_{GS} = 10V, I_D = -38A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
gfs	Forward Transconductance	9.5	—	—	S	$V_{DS} = -50V, I_D = -23A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	-50	$\mu A$	$V_{DS} = -100V, V_{GS} = 0V$ $V_{DS} = -80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	150	230	nC	$I_D = -23A$
$Q_{gs}$	Gate-to-Source Charge	—	22	33	nC	$V_{DS} = -80V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	81	120	nC	$V_{GS} = -10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = -50V$
$t_r$	Rise Time	—	63	—	ns	$I_D = -23A$
$t_{d(off)}$	Turn-Off Delay Time	—	72	—	ns	$R_G = 2.4\Omega$
$t_f$	Fall Time	—	55	—	ns	$V_{GS} = -10V$ ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—	nH	
$C_{iss}$	Input Capacitance	—	2780	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	800	—	pF	$V_{DS} = -25V$
$C_{rss}$	Reverse Transfer Capacitance	—	430	—	pF	$f = 1.0\text{MHz}$ , See Fig. 5

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	-38	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	-140	A	
$V_{SD}$	Diode Forward Voltage	—	—	-1.6	V	$T_J = 25^\circ\text{C}, I_S = -23A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	170	260	ns	$T_J = 25^\circ\text{C}, I_F = -23A, V_{DD} = -25V$
$Q_{rr}$	Reverse Recovery Charge	—	1180	1770	nC	$di/dt = -100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11)
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.46\text{mH}$   
 $R_G = 25\Omega, I_{AS} = -23A$ . (See Figure 12)
- ③  $I_{SD} \leq -23A, di/dt \leq -650A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$ .

- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

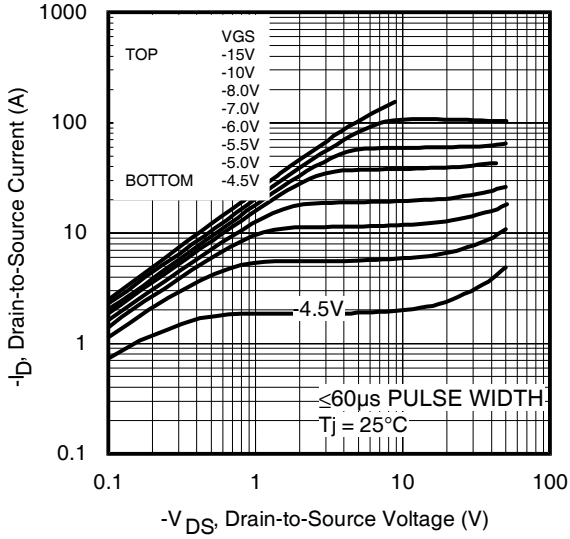


Fig 1. Typical Output Characteristics

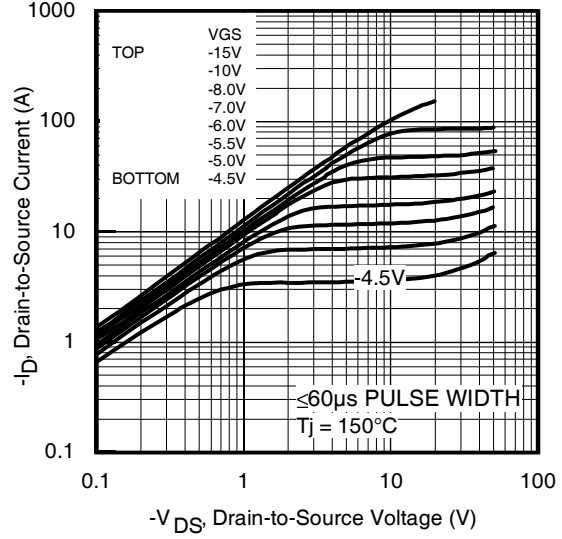


Fig 2. Typical Output Characteristics

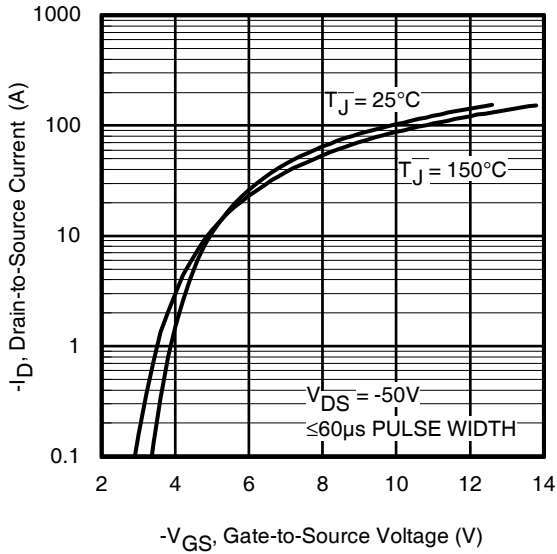


Fig 3. Typical Transfer Characteristics

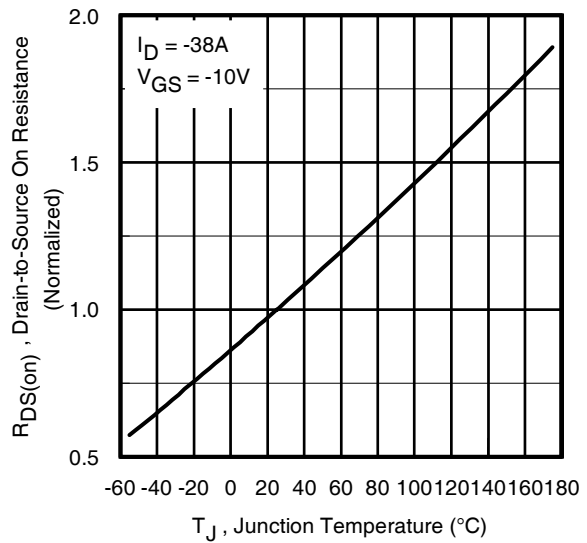
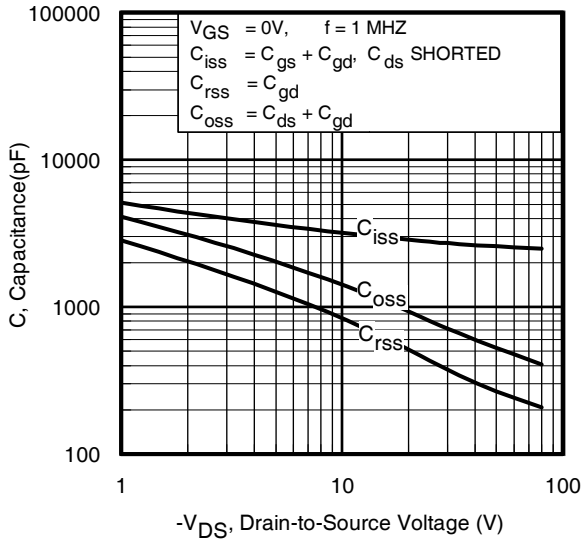
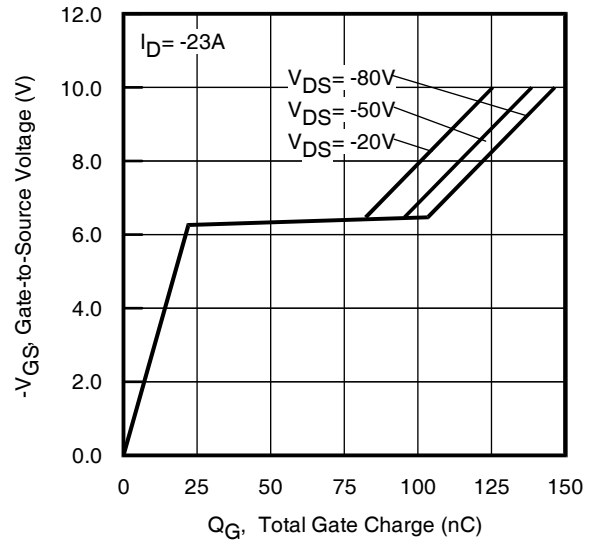


Fig 4. Normalized On-Resistance vs. Temperature

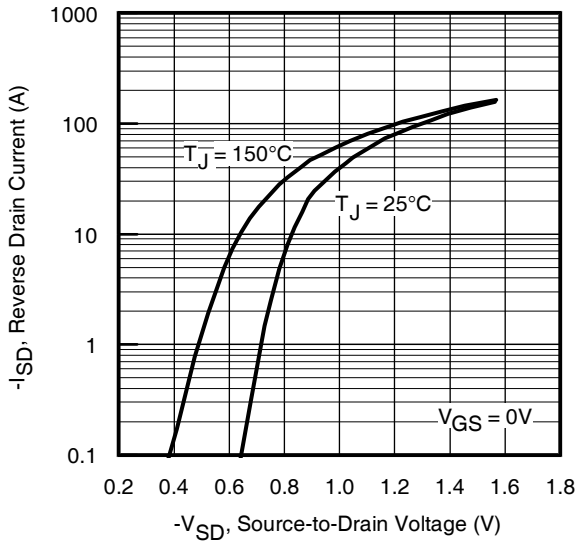
# IRF5210S/LPbF



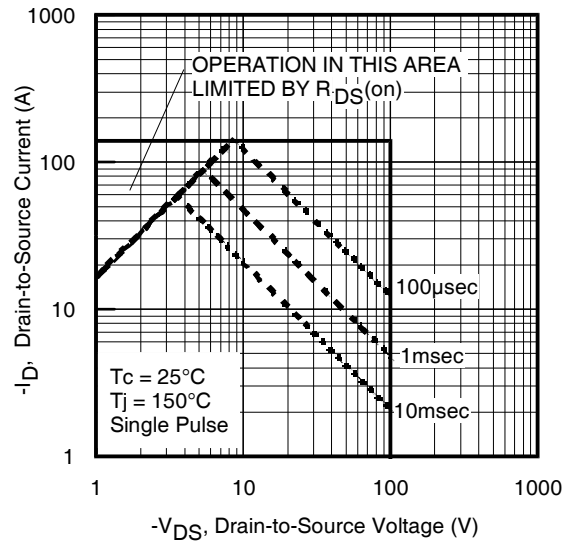
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



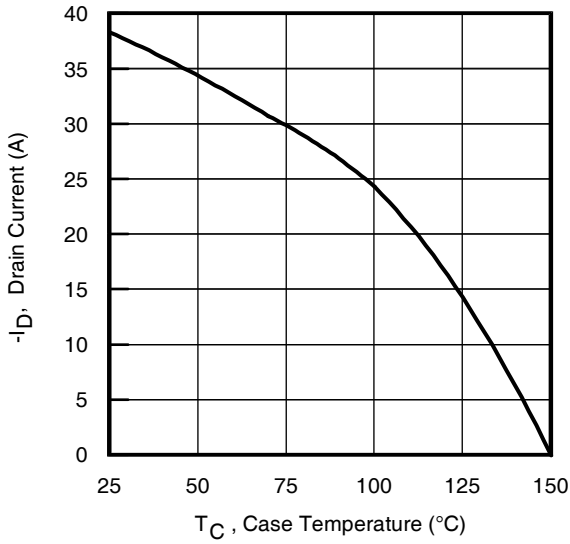
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



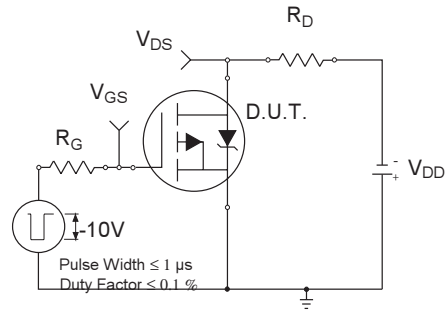
**Fig 7.** Typical Source-Drain Diode Forward Voltage



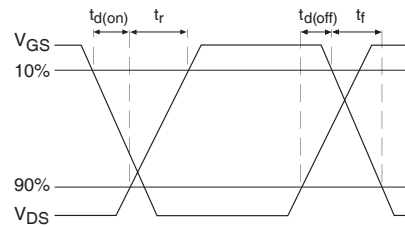
**Fig 8.** Maximum Safe Operating Area



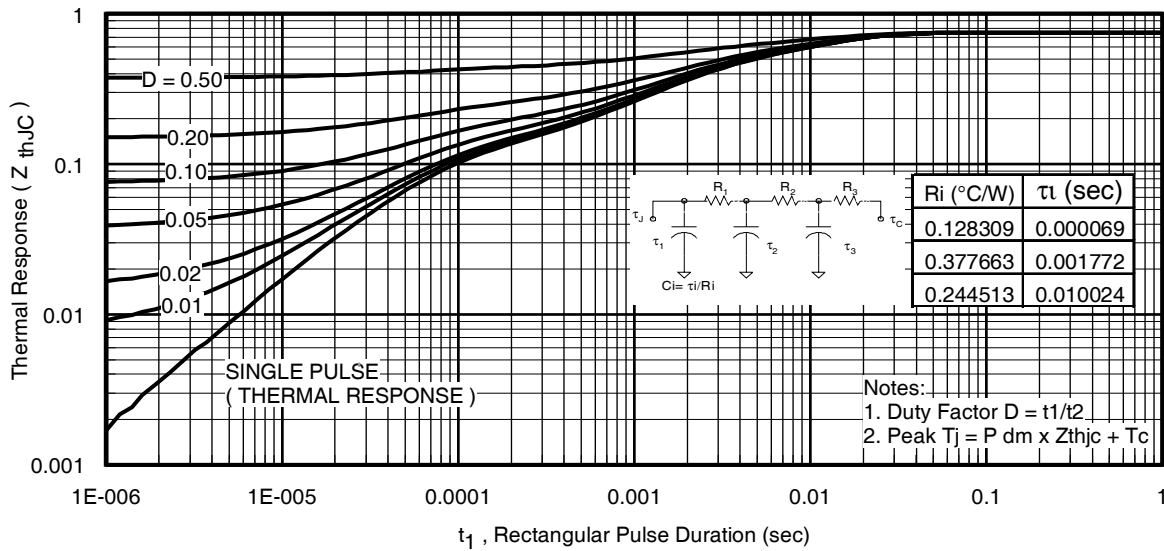
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

# IRF5210S/LPbF

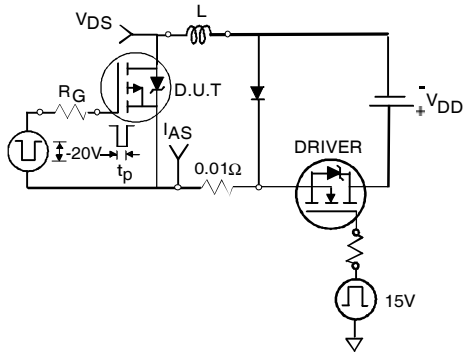


Fig 12a. Unclamped Inductive Test Circuit

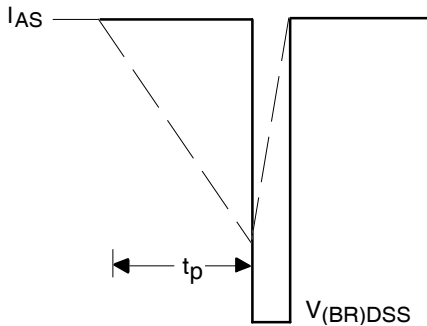


Fig 12b. Unclamped Inductive Waveforms

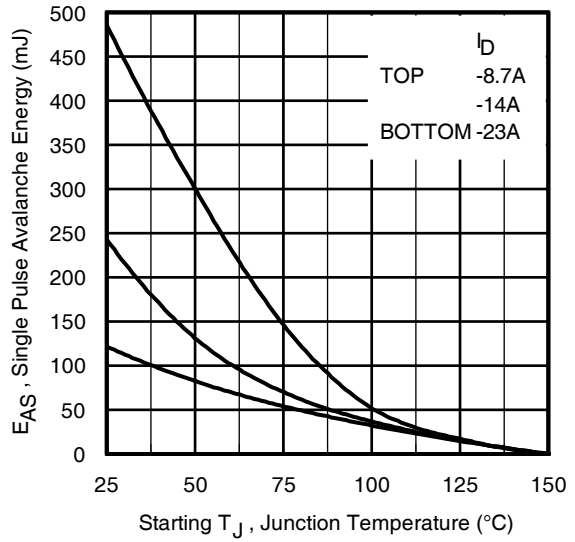


Fig 13. Maximum Avalanche Energy vs. Drain Current

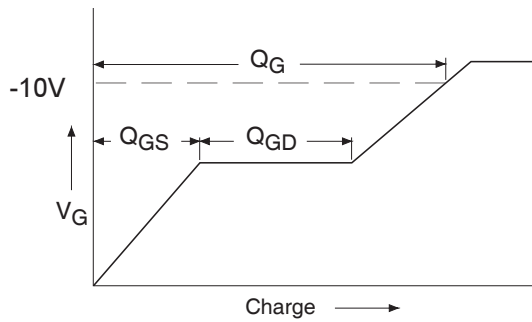


Fig 14a. Basic Gate Charge Waveform

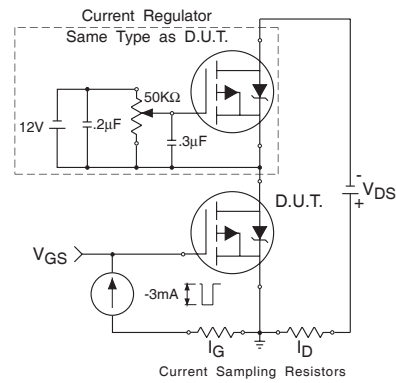
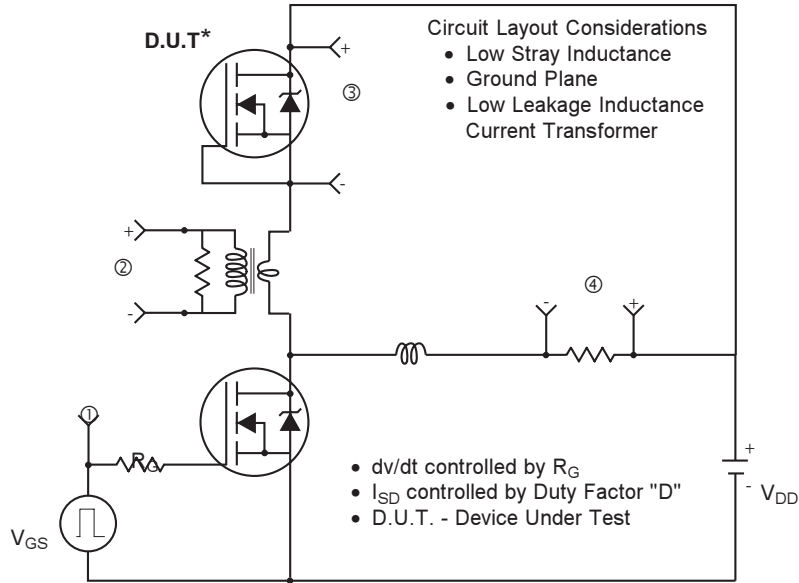
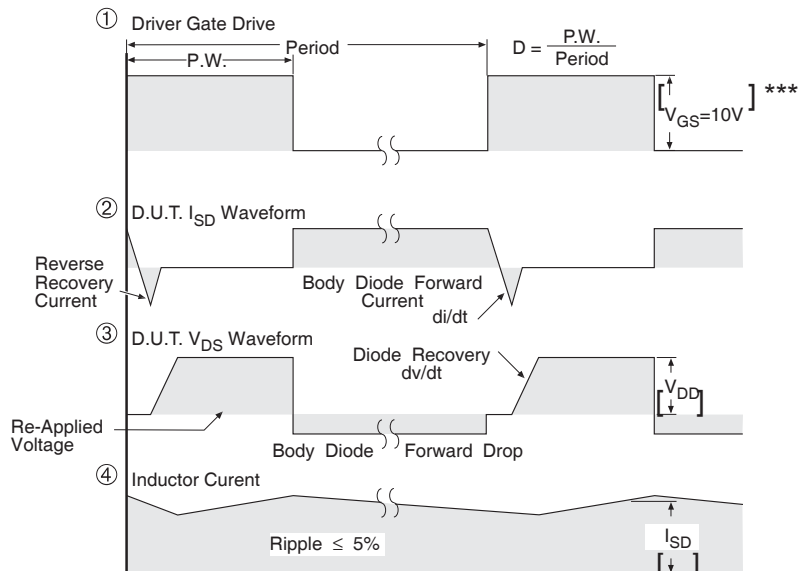


Fig 14b. Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



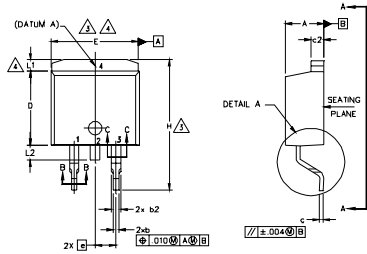
\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

**Fig 15.** For P-Channel HEXFETS

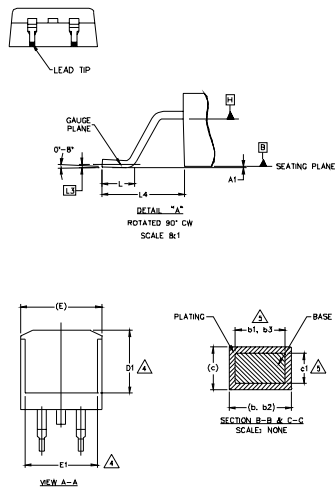
# IRF5210S/LPbF

## D<sup>2</sup>Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
  4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  7. CONTROLLING DIMENSION: INCH.
  8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	0.35	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	6
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	0.23	5
c2	1.14	1.65	.045	.065	
D	8.36	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
H	14.61	15.08	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.65	-	.066	4
L2	1.27	1.78	-	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

- HEXFET  
 1.- GATE  
 2, 4.- DRAIN  
 3.- SOURCE

- IGBTs, COPACK  
 1.- GATE  
 2, 4.- COLLECTOR  
 3.- EMITTER

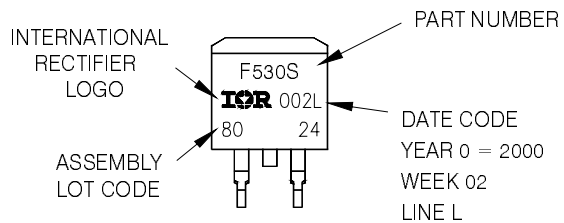
- DIODES  
 1.- ANODE \*  
 2, 4.- CATHODE  
 3.- ANODE

\* PART DEPENDENT.

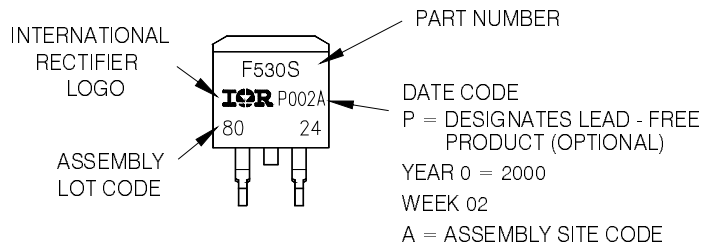
## D<sup>2</sup>Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
 LOT CODE 8024  
 ASSEMBLED ON WW 02, 2000  
 IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead - Free"



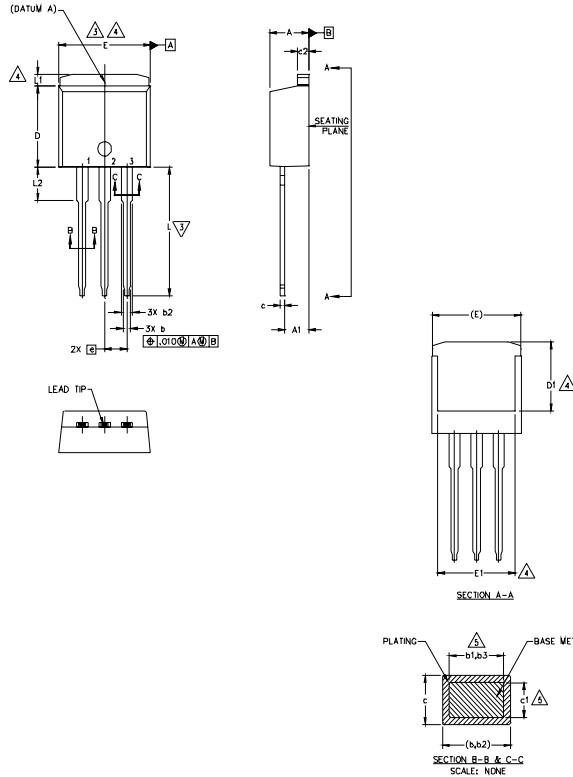
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  6. CONTROLLING DIMENSION: INCH.
  7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.), AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

**LEAD ASSIGNMENTS**

- HEXFET**
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
  - 4.- DRAIN

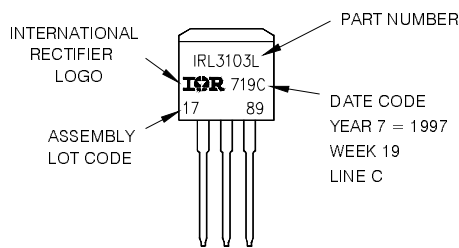
**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

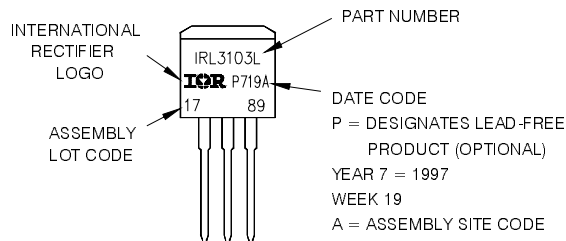
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE 'C'

Note: "P" in assembly line position indicates "Lead - Free"



OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



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