



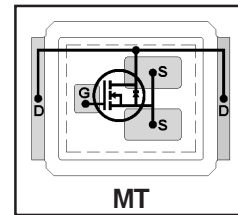
**THE DATASHEET OF  
IRF6618TRPBF**



**IRF6618PbF**  
**IRF6618TRPbF**  
DirectFET™ Power MOSFET ②

- RoHs Compliant ①
- Lead-Free (Qualified up to 260°C Reflow)
- Application Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①

$V_{DSS}$	$V_{GS}$	$R_{DS(on)}$	$R_{DS(on)}$		
30V max	±20V max	2.2mΩ@ 10V	3.4mΩ@ 4.5V		
$Q_{g\ tot}$	$Q_{gd}$	$Q_{gs2}$	$Q_{rr}$	$Q_{oss}$	$V_{gs(th)}$
43nC	15nC	4.0nC	46nC	28nC	1.64V



Applicable DirectFET Package/Layout Pad (see p.7, 8 for details)

SQ	SX	ST		MQ	MX	<b>MT</b>				
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**Description**

The IRF6618PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques. Application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6618PbF balances industry leading on-state resistance while minimizing gate charge along with ultra low package inductance to reduce both conduction and switching losses. The reduced losses make this product ideal for high frequency/high efficiency DC-DC converters that power high current loads such as the latest generation of microprocessors. The IRF6618PbF has been optimized for parameters that are critical in synchronous buck converter's SyncFET sockets.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	30	V
$V_{GS}$	Gate-to-Source Voltage	±20	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	170	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	30	
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ④	24	
$I_{DM}$	Pulsed Drain Current ⑤	240	
$E_{AS}$	Single Pulse Avalanche Energy ⑥	210	mJ
$I_{AR}$	Avalanche Current ⑥	24	A

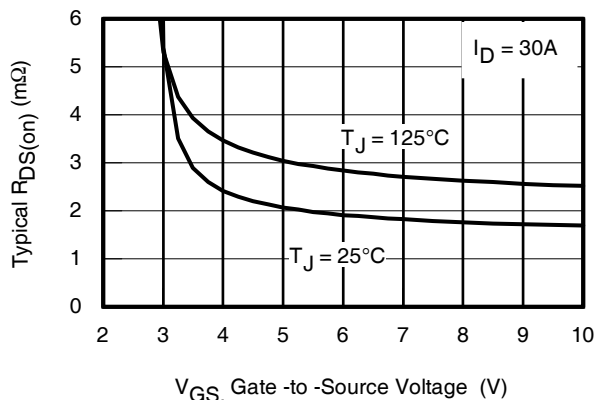


Fig 1. Typical On-Resistance vs. Gate-to-Source Voltage

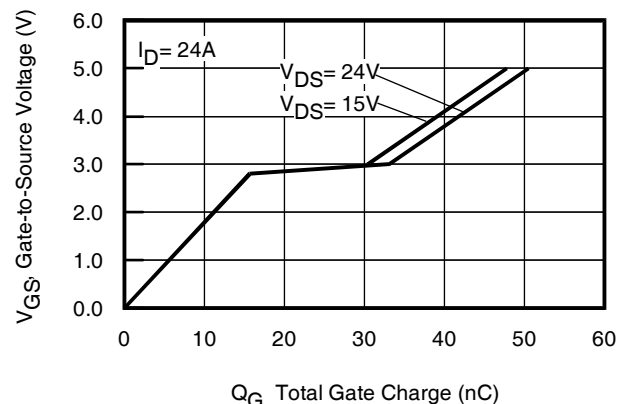


Fig 2. Total Gate Charge vs. Gate-to-Source Voltage

Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④  $T_C$  measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting  $T_J = 25^\circ C$ ,  $L = 0.75mH$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 24A$ .

## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	23	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.7	2.2	m $\Omega$	$V_{GS} = 10V, I_D = 30A$ ⑦
		—	—	3.4		$V_{GS} = 4.5V, I_D = 24A$ ⑦
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.64	2.35	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-5.7	—	mV/°C	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	5.0	$\mu A$	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	1.0		$V_{DS} = 24V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 24V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$g_{fs}$	Forward Transconductance	100	—	—	S	$V_{DS} = 15V, I_D = 24A$
$Q_g$	Total Gate Charge	—	43	65	nC	$V_{DS} = 15V$ $V_{GS} = 4.5V$ $I_D = 24A$ See Fig. 14
$Q_{gs1}$	Pre-Vth Gate-to-Source Charge	—	12	—		
$Q_{gs2}$	Post-Vth Gate-to-Source Charge	—	4.0	—		
$Q_{gd}$	Gate-to-Drain Charge	—	15	23		
$Q_{godr}$	Gate Charge Overdrive	—	12	—		
$Q_{sw}$	Switch Charge ( $Q_{gs2} + Q_{gd}$ )	—	19	—	nC	$V_{DS} = 15V, V_{GS} = 0V$
$Q_{oss}$	Output Charge	—	28	—		
$R_G$	Gate Resistance	—	1.0	2.2	$\Omega$	
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	$V_{DD} = 15V, V_{GS} = 4.5V$ ⑦ $I_D = 24A$ Clamped Inductive Load See Fig. 15 & 16
$t_r$	Rise Time	—	71	—		
$t_{d(off)}$	Turn-Off Delay Time	—	27	—		
$t_f$	Fall Time	—	8.1	—		
$C_{iss}$	Input Capacitance	—	5640	—	pF	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	1260	—		
$C_{riss}$	Reverse Transfer Capacitance	—	570	—		

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	89	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ⑤	—	—	240		
$V_{SD}$	Diode Forward Voltage	—	0.78	1.2	V	$T_J = 25^\circ\text{C}, I_S = 24A, V_{GS} = 0V$ ⑦
$t_{rr}$	Reverse Recovery Time	—	43	65	ns	$T_J = 25^\circ\text{C}, I_F = 24A$
$Q_{rr}$	Reverse Recovery Charge	—	46	69	nC	$di/dt = 100A/\mu s$ ⑦ See Fig. 17

### Notes:

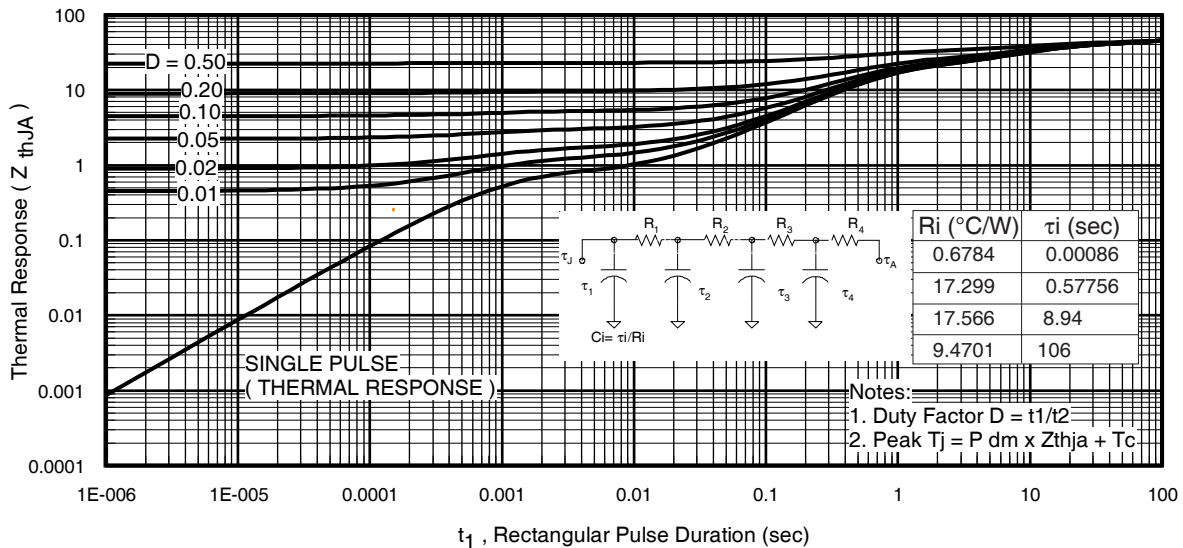
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑦ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③	2.8	W
$P_D @ T_A = 70^\circ\text{C}$	Power Dissipation ③	1.8	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	89	
$T_P$	Peak Soldering Temperature	270	°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-40 to +150	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③ ①	—	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ③ ②	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ② ③	20	—	
$R_{\theta JC}$	Junction-to-Case ③ ①	—	1.4	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③		0.022	W/°C



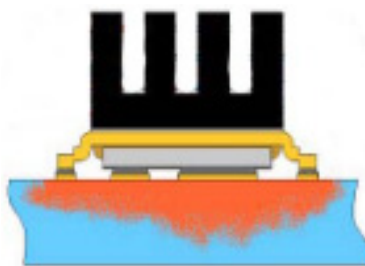
**Fig 3.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

**Notes:**

- ③ Used double sided cooling , mounting pad.
- ② Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ①  $R_{\theta}$  is measured at  $T_J$  of approximately 90°C.



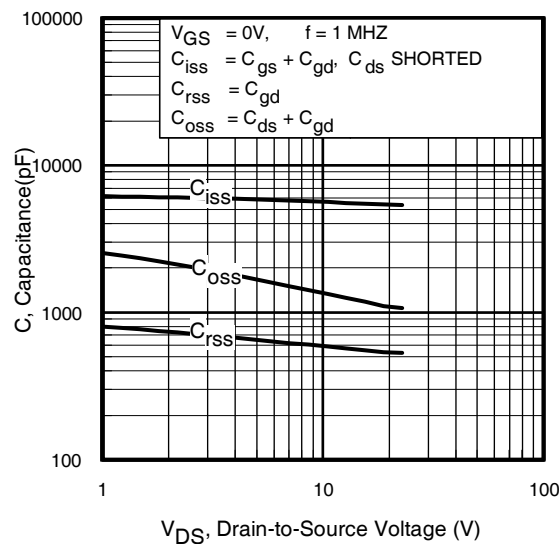
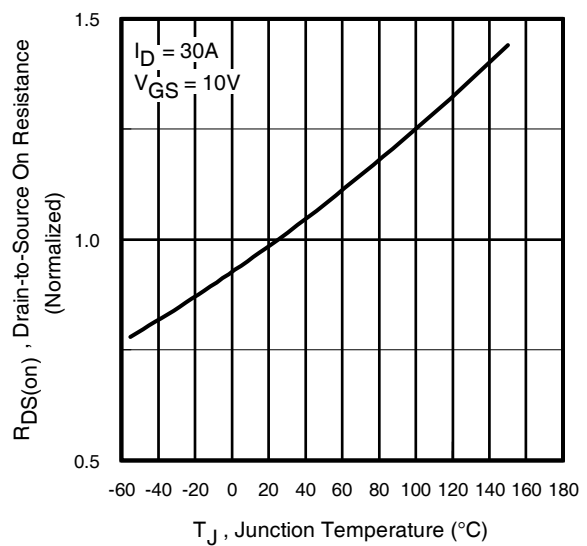
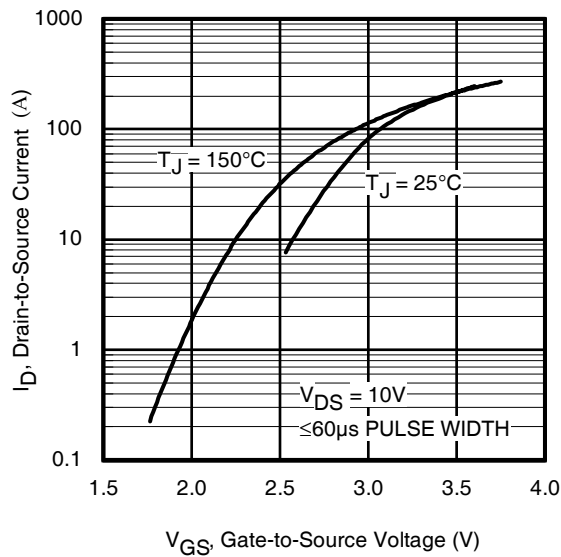
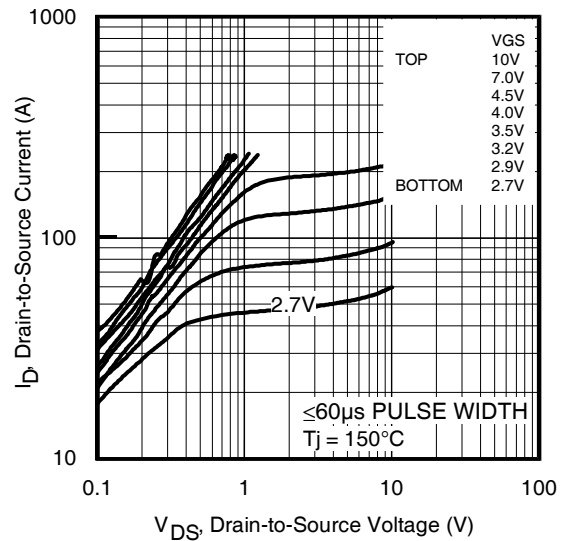
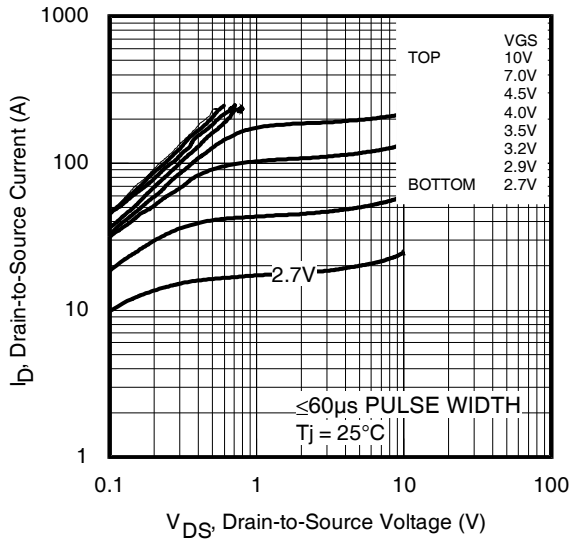
③ Surface mounted on 1 in. square Cu (still air).



② Mounted to a PCB with small clip heatsink (still air)



① Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)



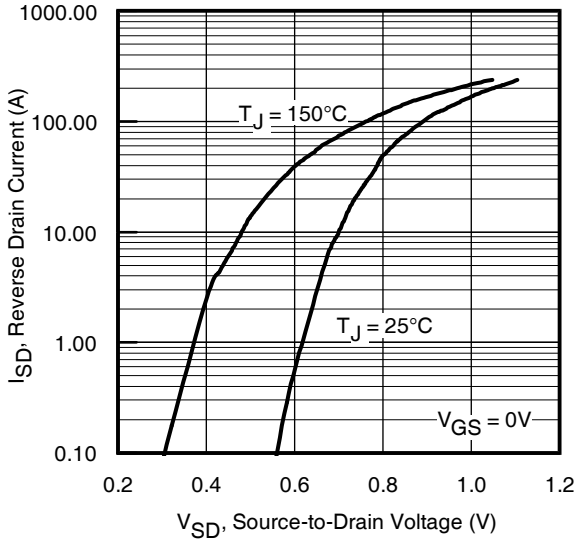


Fig 9. Typical Source-Drain Diode Forward Voltage

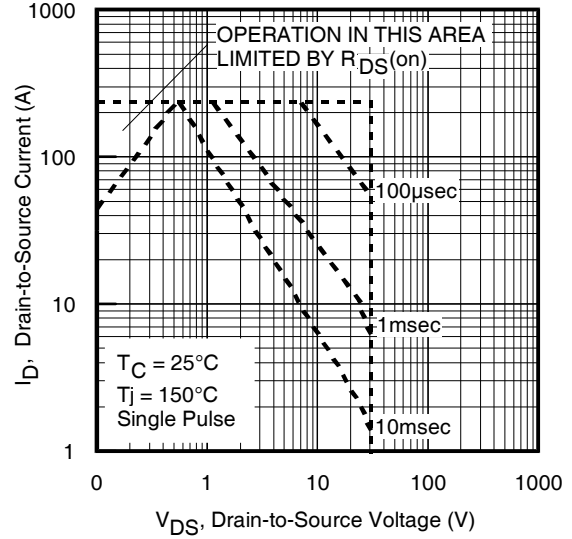


Fig 10. Maximum Safe Operating Area

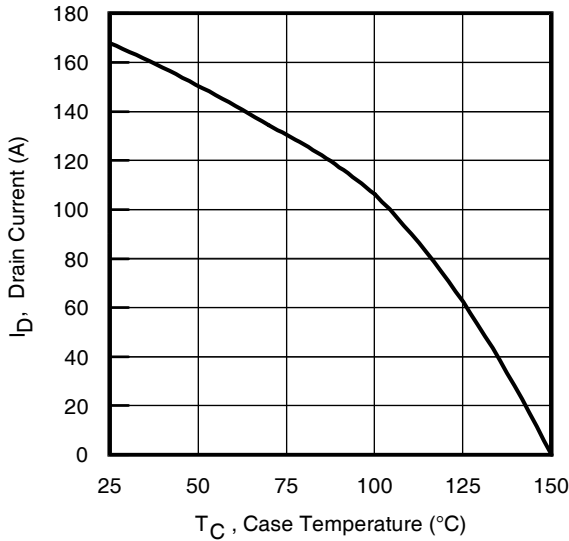


Fig 11. Maximum Drain Current vs. Case Temperature

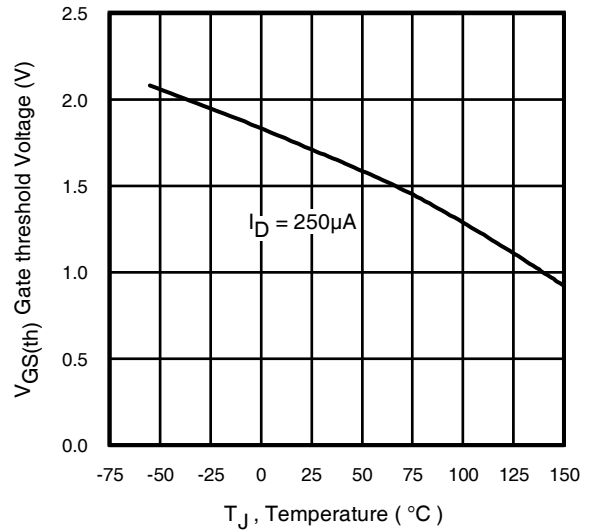


Fig 12. Threshold Voltage vs. Temperature

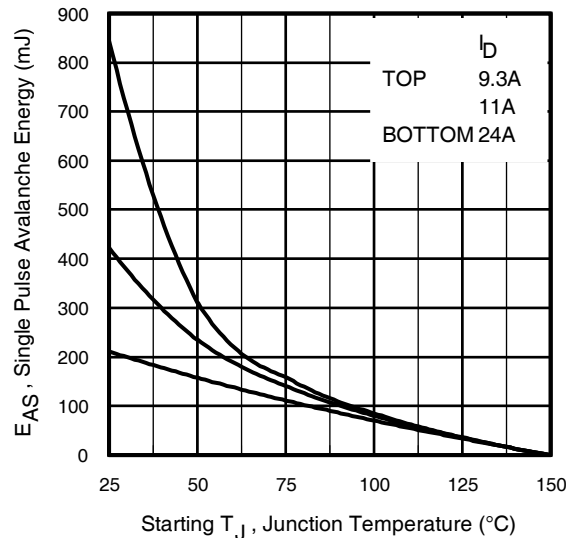
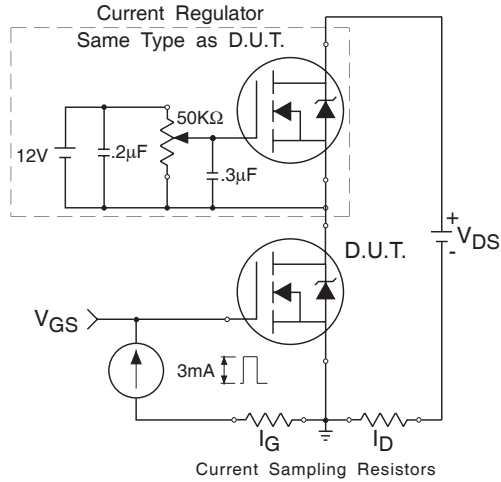
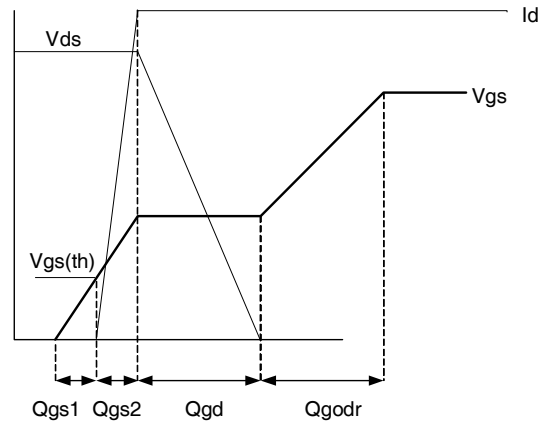


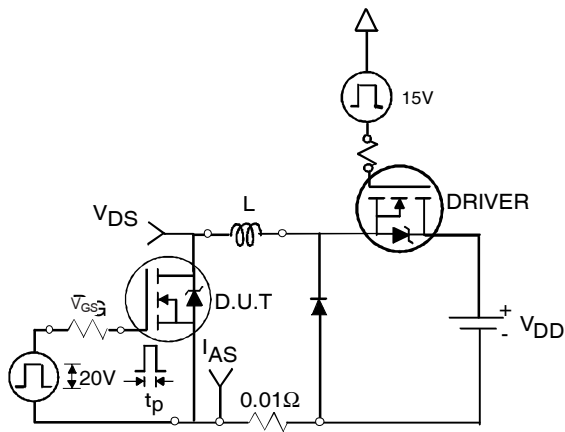
Fig 13. Maximum Avalanche Energy vs. Drain Current



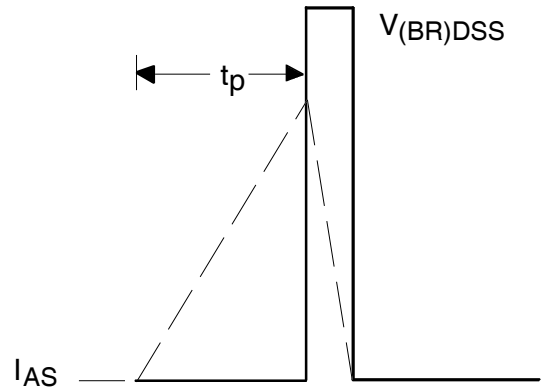
**Fig 14a.** Gate Charge Test Circuit



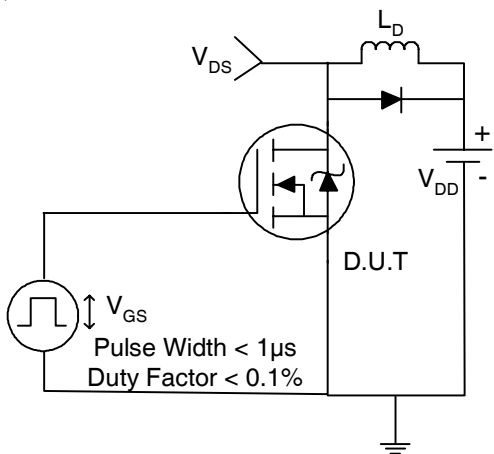
**Fig 14b.** Gate Charge Waveform



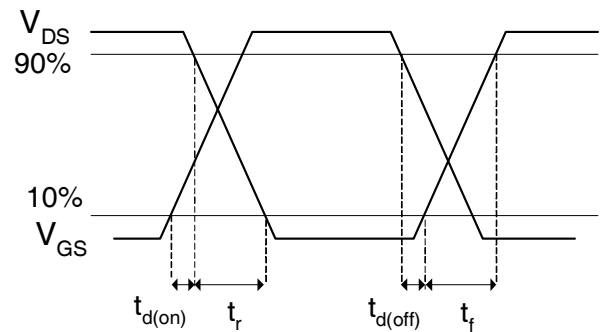
**Fig 15a.** Unclamped Inductive Test Circuit



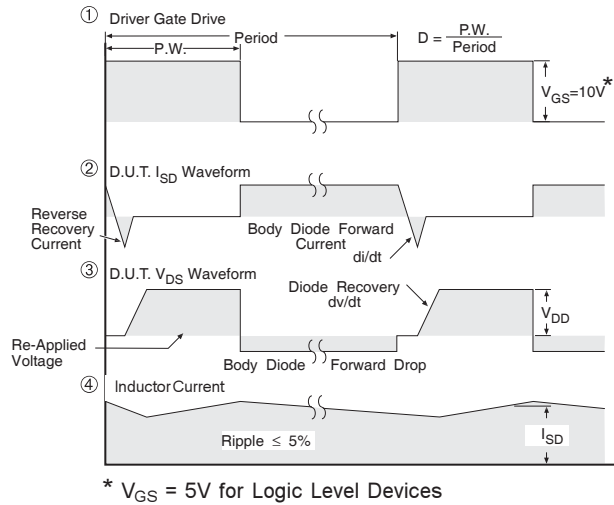
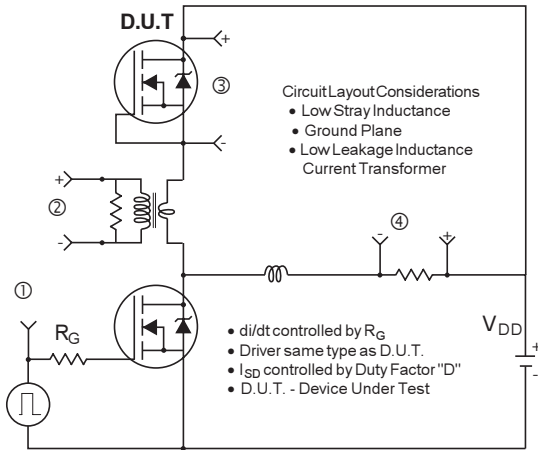
**Fig 15b.** Unclamped Inductive Waveforms



**Fig 16a.** Switching Time Test Circuit



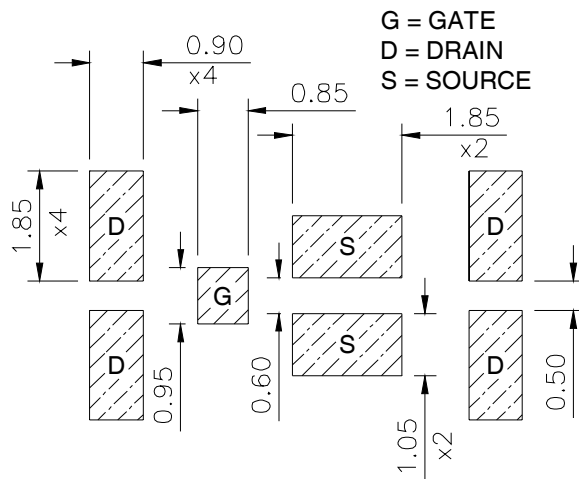
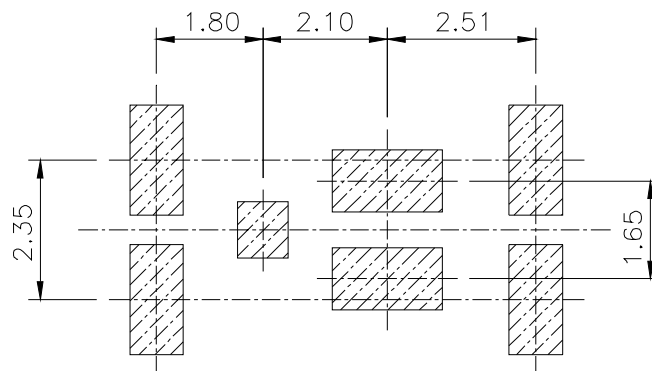
**Fig 16b.** Switching Time Waveforms



**Fig 17. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs**

**DirectFET™ Substrate and PCB Layout, MT Outline ③ (Medium Size Can, T-Designation).**

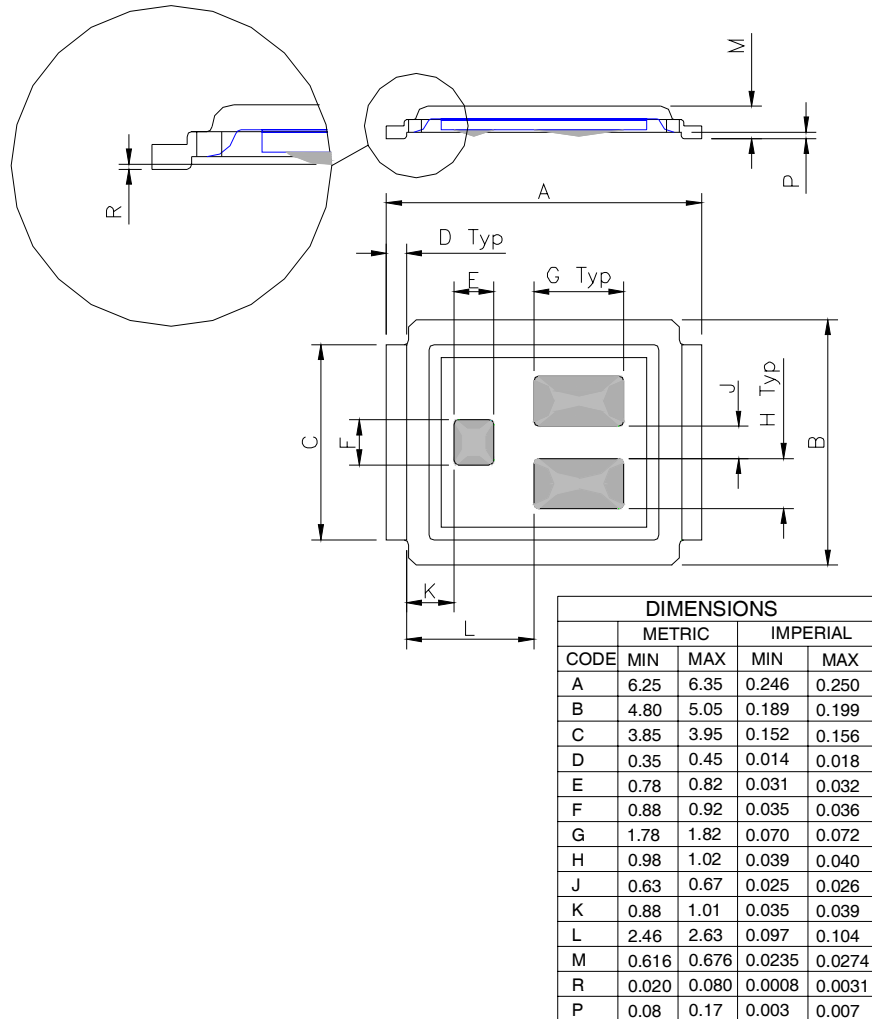
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



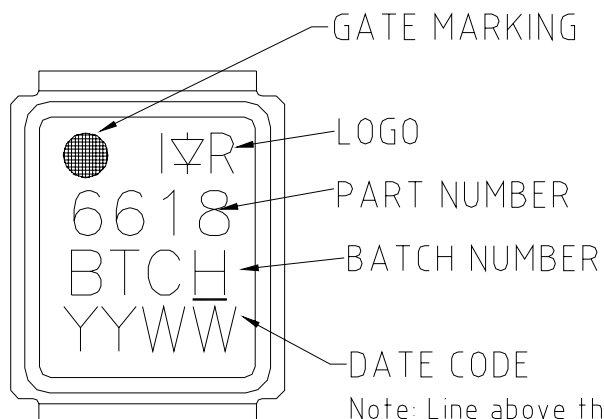
# IRF6618PbF

## DirectFET™ Outline Dimension, MT Outline (Medium Size Can, T-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



## DirectFET™ Part Marking



Note: Line above the last character of the date-code indicates "Lead-Free".



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