



**THE DATASHEET OF  
74VHCT125BQ,115**



# 74VHC125; 74VHCT125

Quad buffer/line driver; 3-state

Rev. 4 — 30 April 2024

Product data sheet

## 1. General description

The 74VHC125; 74VHCT125 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard JESD7-A.

The 74VHC125; 74VHCT125 provides four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs ( $nY$ ) are controlled by the output enable input ( $n\overline{OE}$ ). A HIGH at  $n\overline{OE}$  causes the outputs to assume a high-impedance OFF-state.

The 74VHC125; 74VHCT125 are identical to the 74VHC126; 74VHCT126 but have active LOW enable inputs.

## 2. Features and benefits

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than  $V_{CC}$
- Input levels:
  - The 74VHC125 operates with CMOS logic levels
  - The 74VHCT125 operates with TTL logic levels
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74VHC125D</a> <a href="#">74VHCT125D</a>	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<a href="#">SOT108-1</a>
<a href="#">74VHC125PW</a> <a href="#">74VHCT125PW</a>	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<a href="#">SOT402-1</a>
<a href="#">74VHC125BQ</a> <a href="#">74VHCT125BQ</a>	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	<a href="#">SOT762-1</a>

### 4. Functional diagram

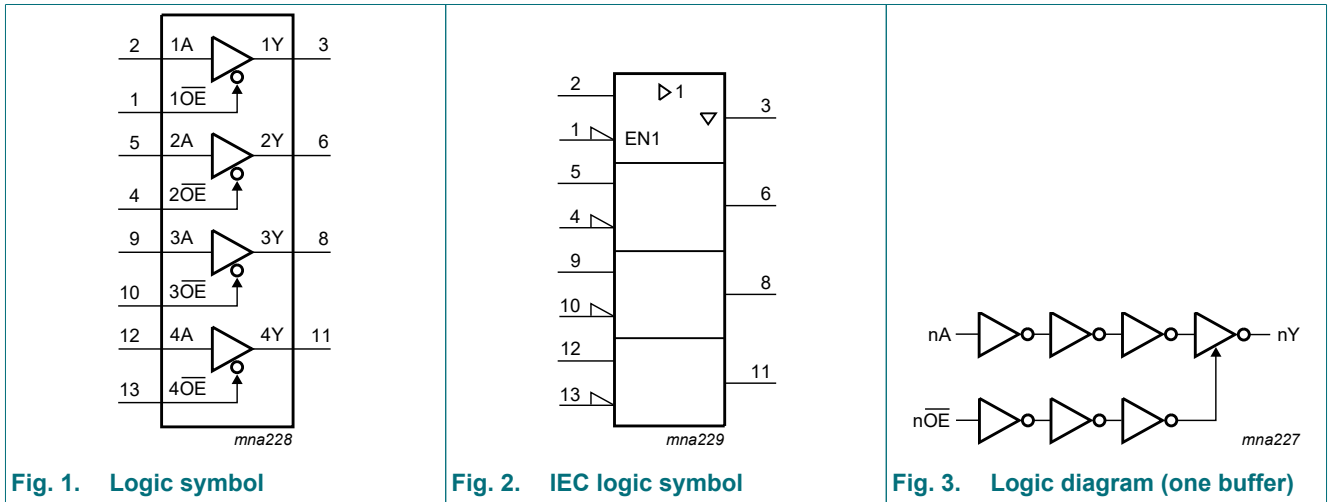


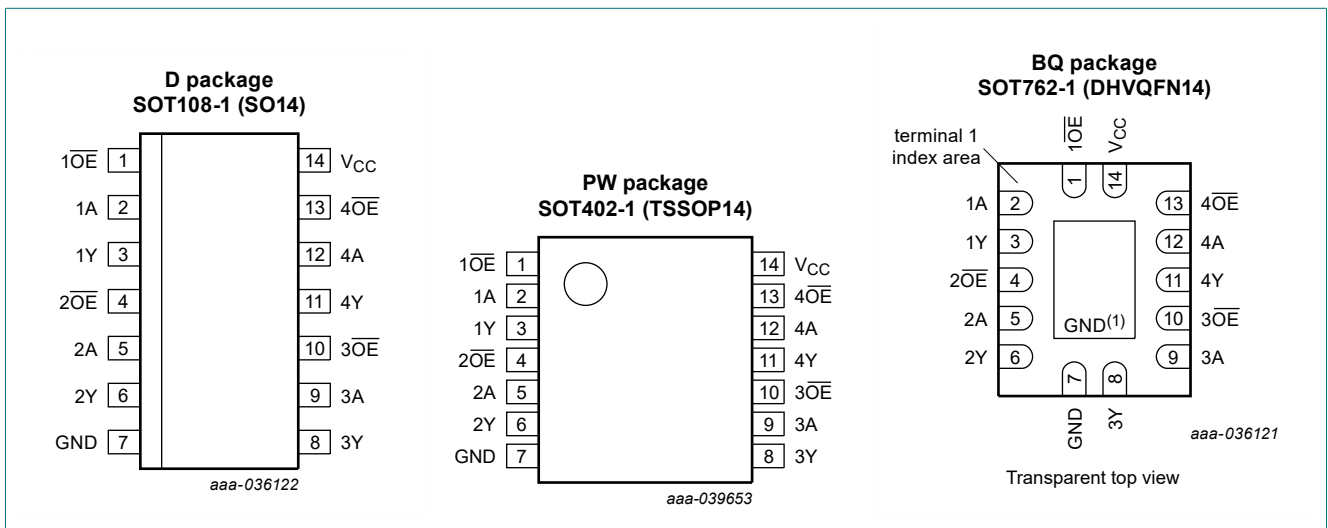
Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Logic diagram (one buffer)

### 5. Pinning information

#### 5.1. Pinning



#### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 4, 10, 13	output enable input (active LOW)
1A, 2A, 3A, 4A	2, 5, 9, 12	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
VCC	14	supply voltage

## 6. Functional description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nA	nY
L	L	L
	H	H
H	X	Z

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V [1]	-20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	$\pm 20$	mA
$I_O$	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5)$ V	-	$\pm 25$	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.  
 For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.  
 For SOT762-1 (DHVQFN14) package:  $P_{tot}$  derates linearly with 9.6 mW/K above 98 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74VHC125			74VHCT125			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V $\pm$ 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V $\pm$ 0.5 V	-	-	20	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>For type 74VHC125</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	µA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2.0	-	20	-	40	µA
C <sub>I</sub>	input capacitance		-	3.0	10	-	10	-	10	pF
C <sub>O</sub>	output capacitance		-	4.0	-	-	-	-	-	pF
<b>For type 74VHCT125</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I <sub>OZ</sub>	OFF-state output current	per input pin; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0 A; V <sub>O</sub> = V <sub>CC</sub> or GND; other pins at V <sub>CC</sub> or GND	-	-	±0.25	-	±2.5	-	±10.0	µA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2.0	-	20	-	40	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0 A; other pins at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance		-	3.0	10	-	10	-	10	pF
C <sub>O</sub>	output capacitance		-	4.0	-	-	-	-	-	pF

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

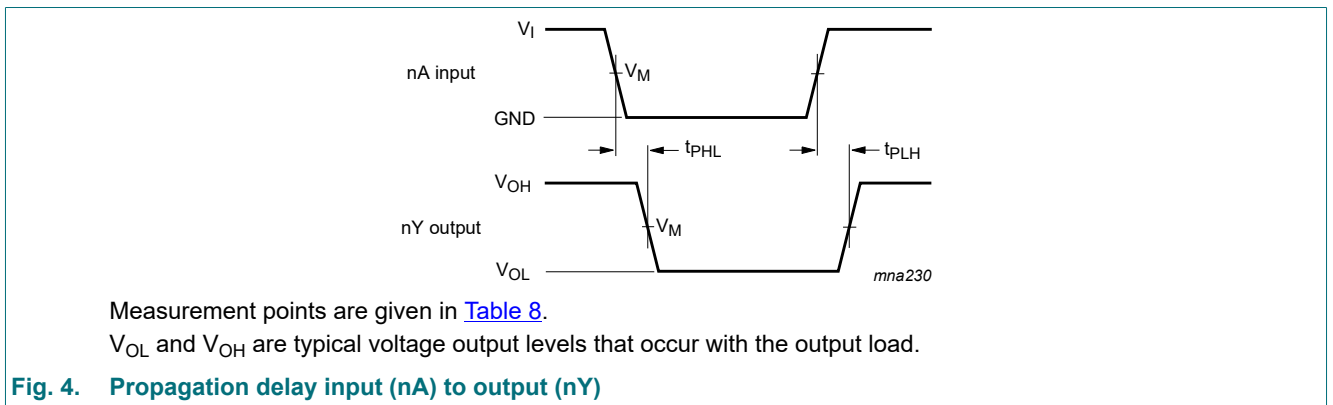
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

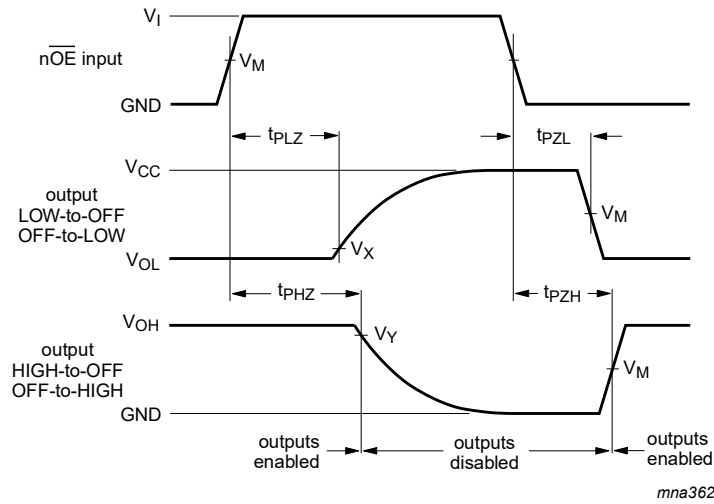
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>For type 74VHC125</b>										
t <sub>pd</sub>	propagation delay	nA to nY; see Fig. 4 [2]								
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF	-	4.4	8.0	1.0	9.5	1.0	11.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 50 pF	-	6.2	11.5	1.0	13.0	1.0	14.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 15 pF	-	3.0	5.5	1.0	6.5	1.0	7.0	ns
t <sub>en</sub>	enable time	nOE to nY; see Fig. 5 [2]								
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF	-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 50 pF	-	6.8	11.5	1.0	13.0	1.0	14.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 15 pF	-	3.3	5.1	1.0	6.0	1.0	6.5	ns
t <sub>dis</sub>	disable time	nOE to nY; see Fig. 5 [2]								
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 15 pF	-	6.7	9.7	1.0	11.5	1.0	12.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V; C <sub>L</sub> = 50 pF	-	9.6	13.2	1.0	15.0	1.0	16.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 15 pF	-	4.8	6.8	1.0	8.0	1.0	8.5	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [3]	-	10	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>For type 74VHCT125</b>										
t <sub>pd</sub>	propagation delay	nA to nY; see Fig. 4 [2]								
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 15 pF	-	3.0	5.5	1.0	6.5	1.0	7.0	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 50 pF	-	4.3	7.5	1.0	8.5	1.0	9.5	ns
t <sub>en</sub>	enable time	n $\overline{O}E$ to nY; see Fig. 5								
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 15 pF	-	3.4	5.1	1.0	6.0	1.0	6.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 50 pF	-	4.9	7.3	1.0	8.3	1.0	9.5	ns
t <sub>dis</sub>	disable time	n $\overline{O}E$ to nY; see Fig. 5 [2]								
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 15 pF	-	4.5	6.8	1.0	8.0	1.0	8.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V; C <sub>L</sub> = 50 pF	-	6.5	8.8	1.0	10.0	1.0	11.0	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [3]	-	12	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage (V<sub>CC</sub> = 3.3 V and V<sub>CC</sub> = 5.0 V).
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:  
f<sub>i</sub> = input frequency in MHz, f<sub>o</sub> = output frequency in MHz  
C<sub>L</sub> = output load capacitance in pF  
V<sub>CC</sub> = supply voltage in Volts  
N = number of inputs switching  
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

### 10.1. Waveforms and test circuit





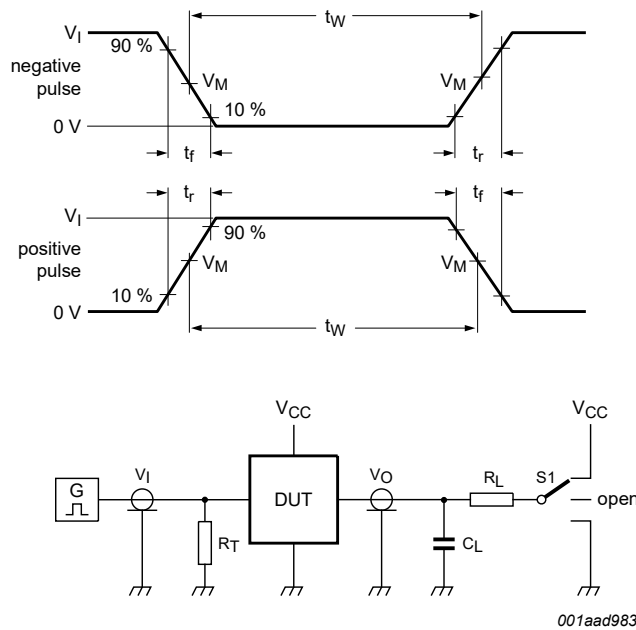
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 5. Enable and disable times**

**Table 8. Measurement points**

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74VHC125	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OL} - 0.3 V$
74VHCT125	1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OL} - 0.3 V$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

S1 = Test selection switch.

**Fig. 6. Test circuit for switching times**

Table 9. Test data

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74VHC125	$V_{CC}$	$\leq 3.0$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74VHCT125	3.0 V	$\leq 3.0$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig. 7. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig. 8. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

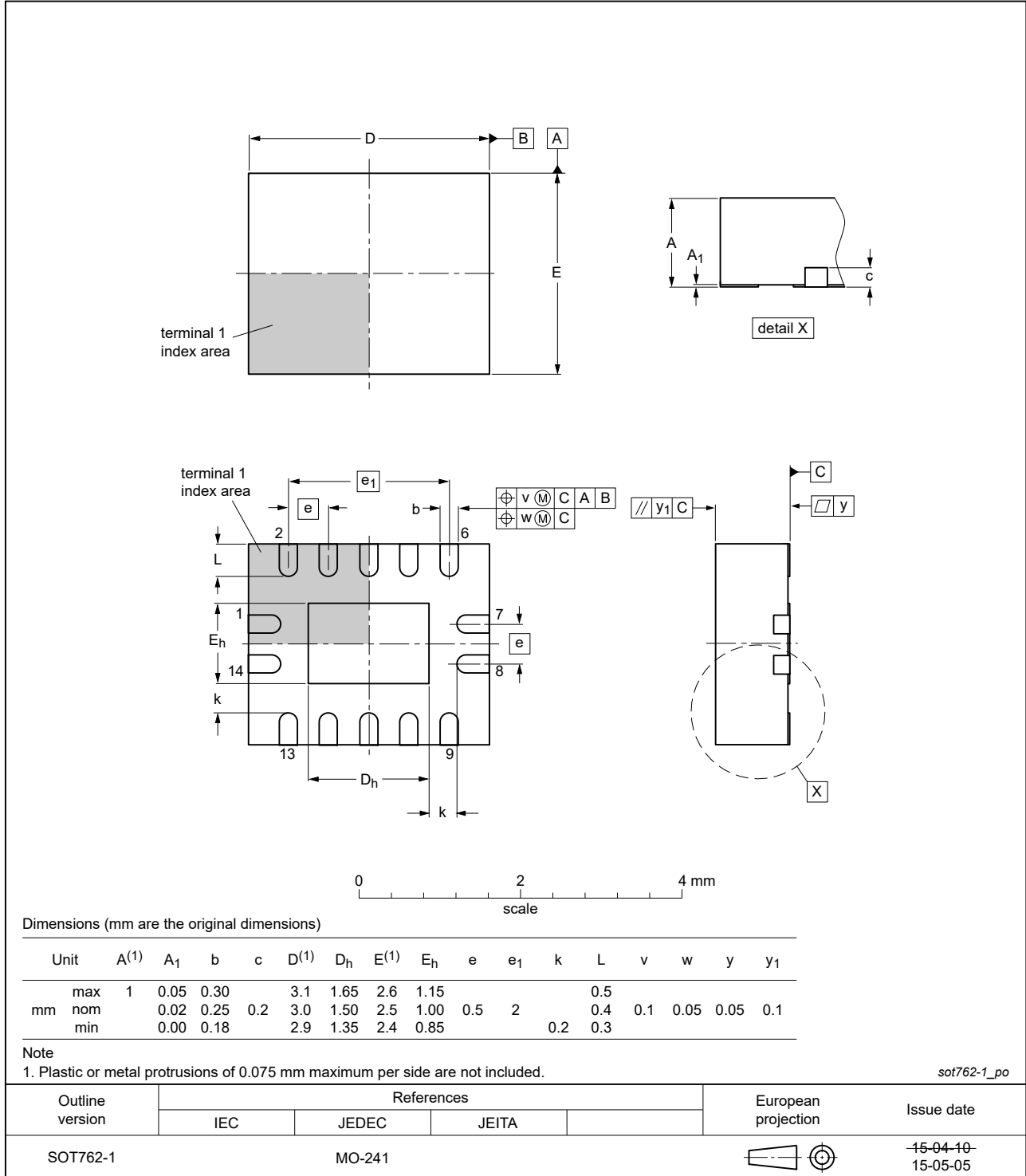


Fig. 9. Package outline SOT762-1 (DHVQFN14)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74VHC_VHCT125 v.4	20240430	Product data sheet	-	74VHC_VHCT125_3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li><a href="#">Fig. 7</a> and <a href="#">Fig. 8</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li> </ul>			
74VHC_VHCT125 v.3	20200408	Product data sheet	-	74VHC_VHCT125_2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> <li>Package outline drawing <a href="#">SOT762-1</a> (DHVQFN14) updated.</li> </ul>			
74VHC_VHCT125_2	20091013	Product data sheet	-	74VHC_VHCT125_1
Modifications:	<ul style="list-style-type: none"> <li>Errata in features list corrected.</li> </ul>			
74VHC_VHCT125_1	20090630	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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