



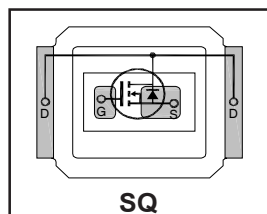
**THE DATASHEET OF  
IRF6811STRPBF**



- RoHS Compliant and Halogen Free ①
- Low Profile (<0.7 mm)
- Dual Sided Cooling Compatible ①
- Ultra Low Package Inductance
- Optimized for High Frequency Switching ①
- Ideal for CPU Core DC-DC Converters
- Optimized for Control FET Application①
- Compatible with existing Surface Mount Techniques ①
- 100% Rg tested
- Footprint compatible to DirectFET

Typical values (unless otherwise specified)

$V_{DS}$	$V_{GS}$	$R_{DS(on)}$	$R_{DS(on)}$		
25V max	$\pm 16V$ max	2.8m $\Omega$ @ 10V	4.1m $\Omega$ @ 4.5V		
$Q_{g\ tot}$	$Q_{gd}$	$Q_{gs2}$	$Q_{rr}$	$Q_{oss}$	$V_{gs(th)}$
11nC	4.2nC	1.4nC	23nC	11nC	1.6V



Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)

<b>SQ</b>	SX	ST		MQ	MX	MT	MP			
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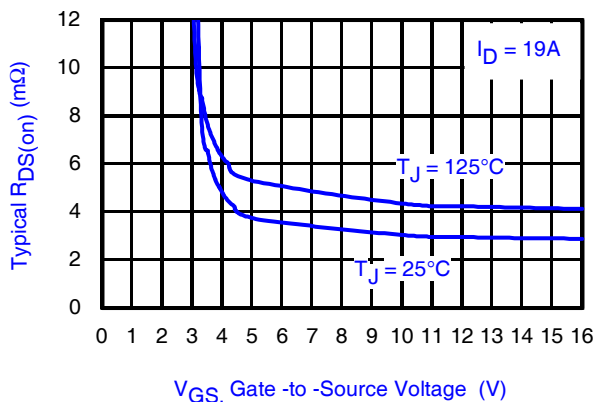
**Description**

The IRF6811STRPbF combines the latest HEXFET<sup>®</sup> Power MOSFET Silicon technology with the advanced DirectFET<sup>®</sup> packaging to achieve improved performance in a package that has the footprint of a MICRO-8 and only 0.7 mm profile. The DirectFET<sup>®</sup> package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET<sup>®</sup> package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

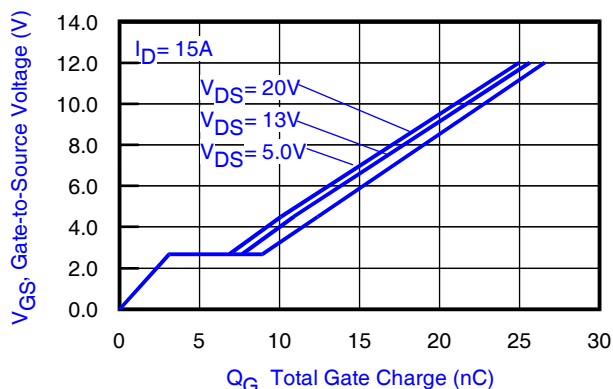
The IRF6811STRPbF has low gate resistance and low charge along with ultra low package inductance providing significant reduction in switching losses. The reduced losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors operating at higher frequencies. The IRF6811STRPbF has been optimized for the control FET socket of synchronous buck operating from 12 volt bus converters.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	25	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	19	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	15	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ④	74	
$I_{DM}$	Pulsed Drain Current ⑤	150	
$E_{AS}$	Single Pulse Avalanche Energy ⑥	32	mJ
$I_{AR}$	Avalanche Current ⑤	15	A



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Typical Total Gate Charge vs Gate-to-Source Voltage

Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

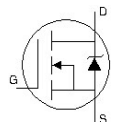
- ④  $T_C$  measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting  $T_J = 25^\circ C$ ,  $L = 0.28mH$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 15A$ .

## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	25	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	22	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.8	3.7	mΩ	$V_{GS} = 10V, I_D = 19A$ ⑦
		—	4.1	5.4		$V_{GS} = 4.5V, I_D = 15A$ ⑦
$V_{GS(th)}$	Gate Threshold Voltage	1.1	1.6	2.1	V	$V_{DS} = V_{GS}, I_D = 35\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-6.2	—	mV/°C	$V_{DS} = V_{GS}, I_D = 25\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
$g_{fs}$	Forward Transconductance	180	—	—	S	$V_{DS} = 13V, I_D = 15A$
$Q_g$	Total Gate Charge	—	11	17	nC	$V_{DS} = 13V$ $V_{GS} = 4.5V$ $I_D = 15A$ See Fig. 2 & 15
$Q_{gs1}$	Pre-Vth Gate-to-Source Charge	—	2.2	—		
$Q_{gs2}$	Post-Vth Gate-to-Source Charge	—	1.4	—		
$Q_{gd}$	Gate-to-Drain Charge	—	4.2	—		
$Q_{godr}$	Gate Charge Overdrive	—	3.2	—		
$Q_{sw}$	Switch Charge ( $Q_{gs2} + Q_{gd}$ )	—	5.6	—		
$Q_{oss}$	Output Charge	—	11	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
$R_G$	Gate Resistance	—	0.4	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	8.7	—	ns	$V_{DD} = 13V, V_{GS} = 4.5V$ ⑦ $I_D = 15A$ $R_G = 1.5\Omega$ See Fig. 17
$t_r$	Rise Time	—	19	—		
$t_{d(off)}$	Turn-Off Delay Time	—	11	—		
$t_f$	Fall Time	—	5.5	—		
$C_{iss}$	Input Capacitance	—	1590	—	pF	$V_{GS} = 0V$ $V_{DS} = 13V$ $f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	460	—		
$C_{rss}$	Reverse Transfer Capacitance	—	110	—		

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	40	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ⑤	—	—	150		
$V_{SD}$	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 15A, V_{GS} = 0V$ ⑦
$t_{rr}$	Reverse Recovery Time	—	18	27	ns	$T_J = 25^\circ\text{C}, I_F = 15A$
$Q_{rr}$	Reverse Recovery Charge	—	23	35	nC	$di/dt = 300A/\mu s$ ⑦



### Notes:

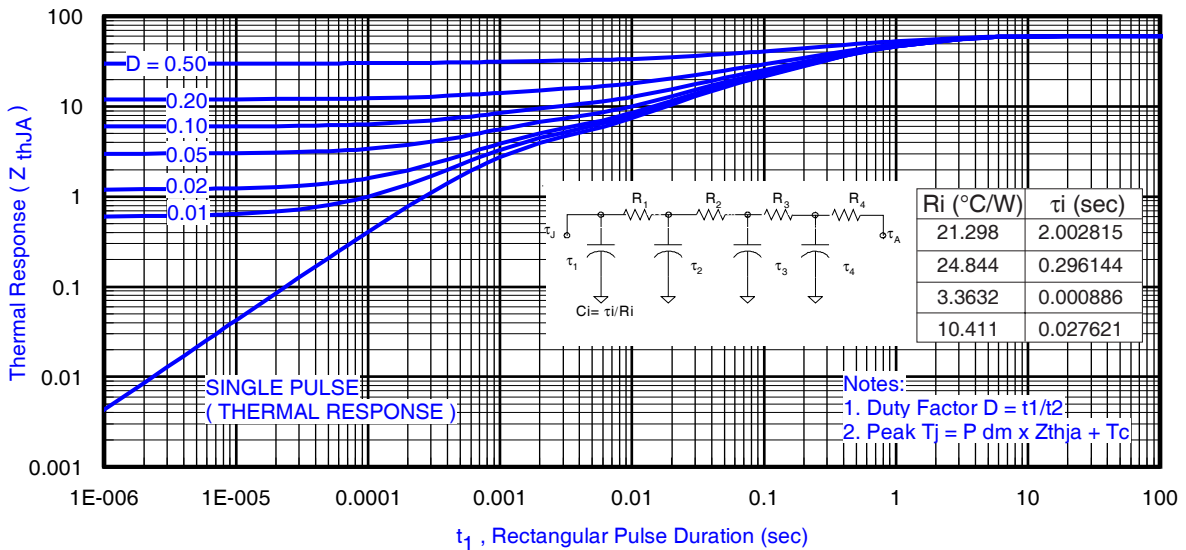
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑦ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③	2.1	W
$P_D @ T_A = 70^\circ\text{C}$	Power Dissipation ③	1.3	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	32	
$T_P$	Peak Soldering Temperature	270	$^\circ\text{C}$
$T_J$	Operating Junction and	-40 to + 150	
$T_{STG}$	Storage Temperature Range		

**Thermal Resistance**

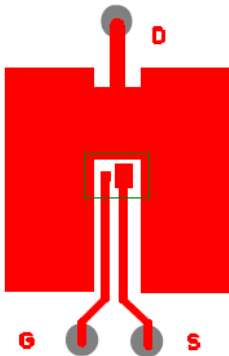
	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③⑩	—	60	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient ⑥⑩	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑨⑩	20	—	
$R_{\theta JC}$	Junction-to-Case ④⑩	—	3.9	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③		0.017	$\text{W}/^\circ\text{C}$



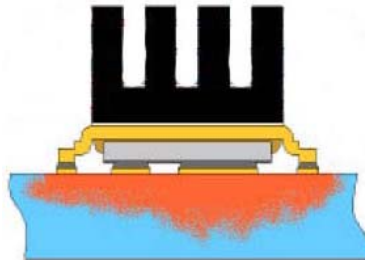
**Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ①**

**Notes:**

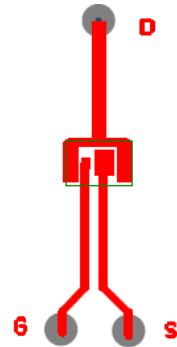
- ③ Used double sided cooling, mounting pad with large heatsink.
- ④ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑥  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .



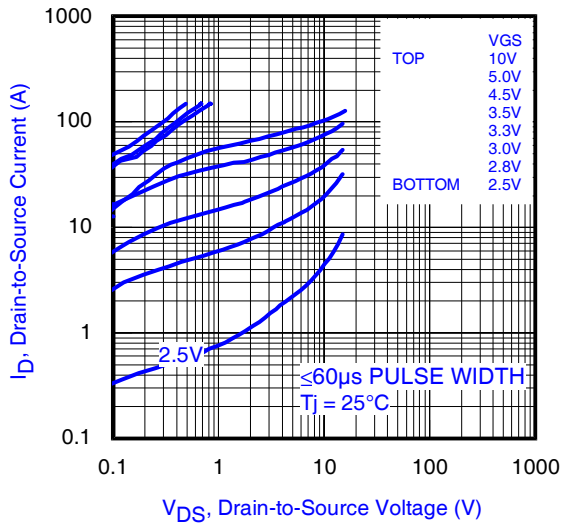
③ Surface mounted on 1 in. square Cu (still air).



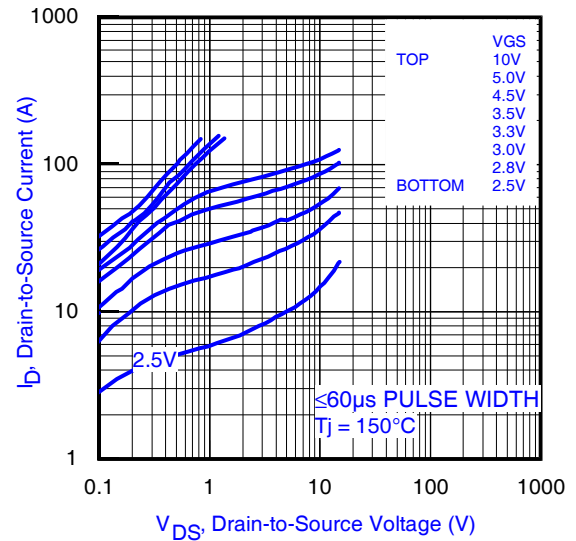
⑥ Mounted to a PCB with small clip heatsink (still air)



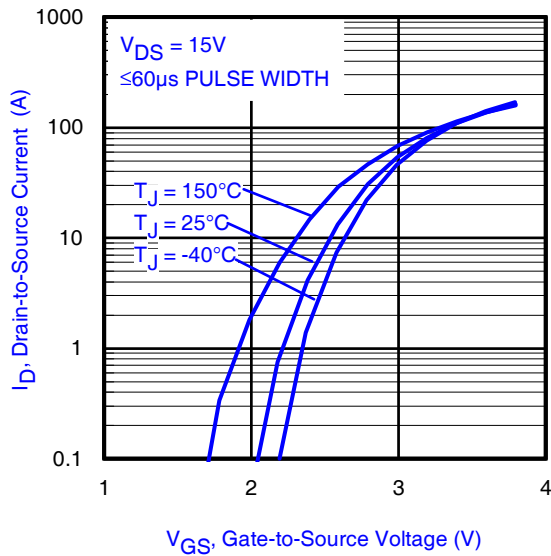
⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)



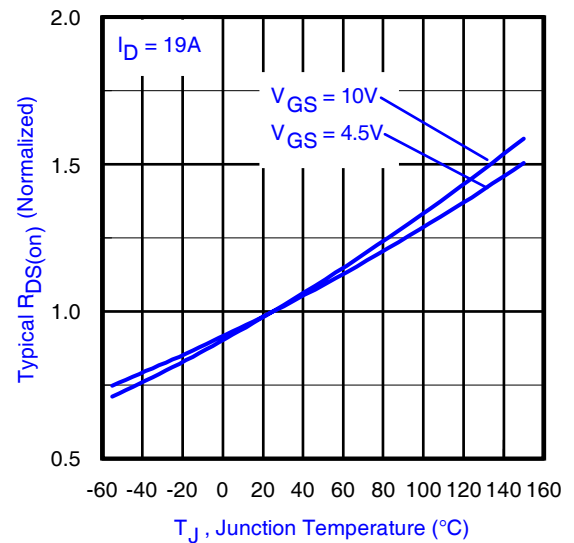
**Fig 4.** Typical Output Characteristics



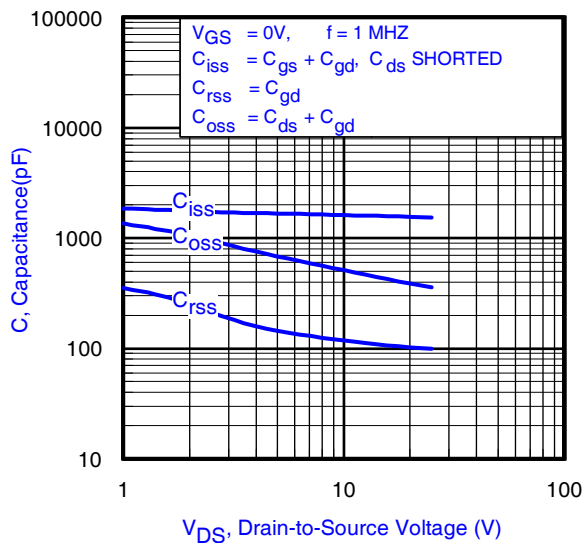
**Fig 5.** Typical Output Characteristics



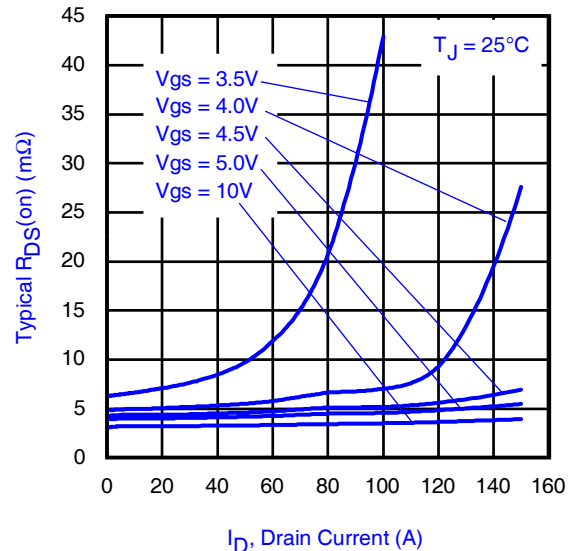
**Fig 6.** Typical Transfer Characteristics



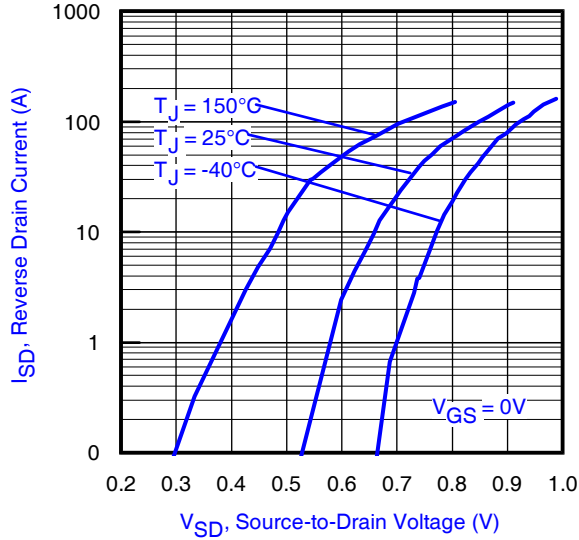
**Fig 7.** Normalized On-Resistance vs. Temperature



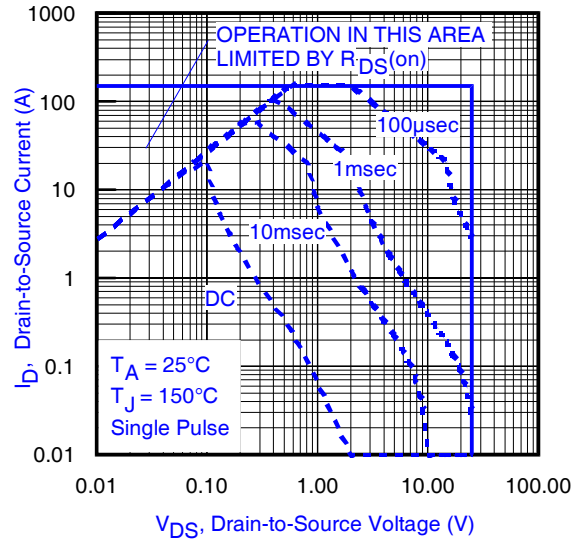
**Fig 8.** Typical Capacitance vs. Drain-to-Source Voltage



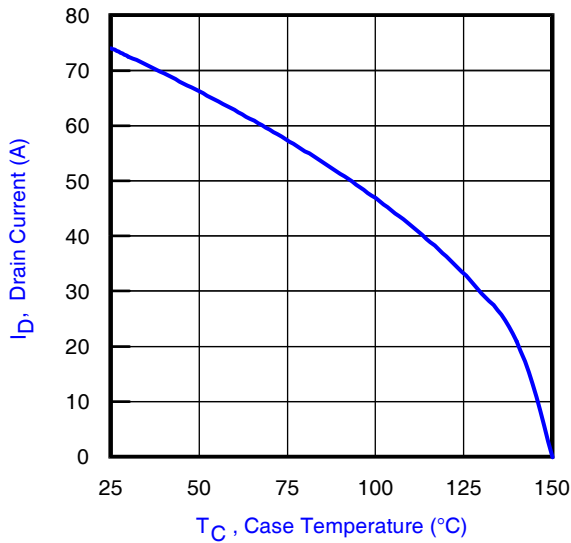
**Fig 9.** Typical On-Resistance vs. Drain Current and Gate Voltage



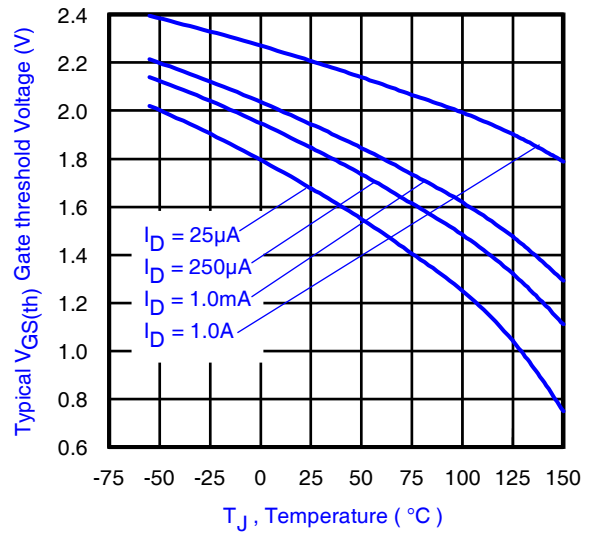
**Fig 10.** Typical Source-Drain Diode Forward Voltage



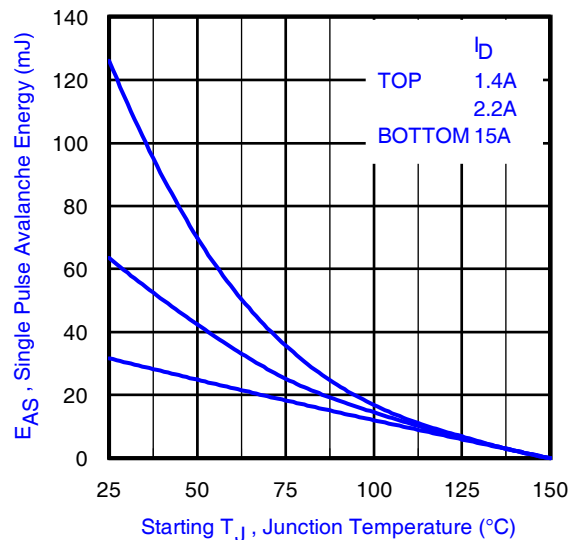
**Fig11.** Maximum Safe Operating Area



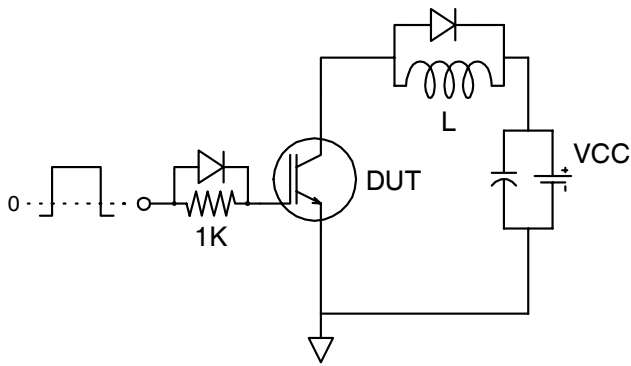
**Fig 12.** Maximum Drain Current vs. Case Temperature



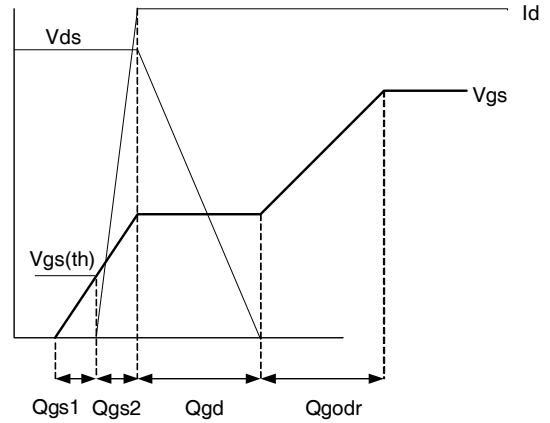
**Fig 13.** Typical Threshold Voltage vs. Junction Temperature



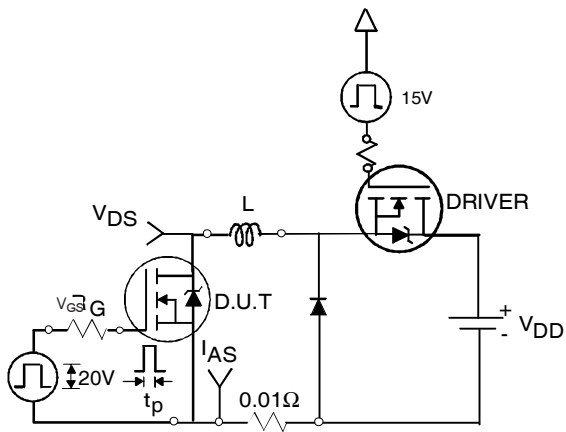
**Fig 14.** Maximum Avalanche Energy vs. Drain Current



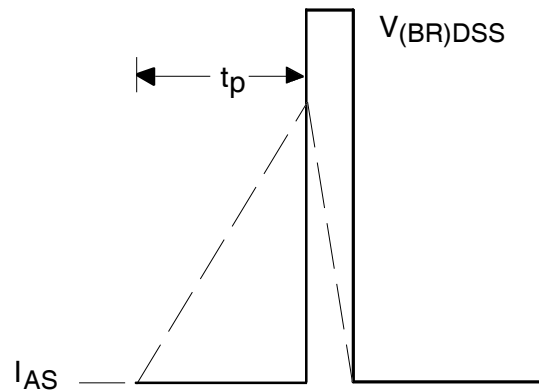
**Fig 15a.** Gate Charge Test Circuit



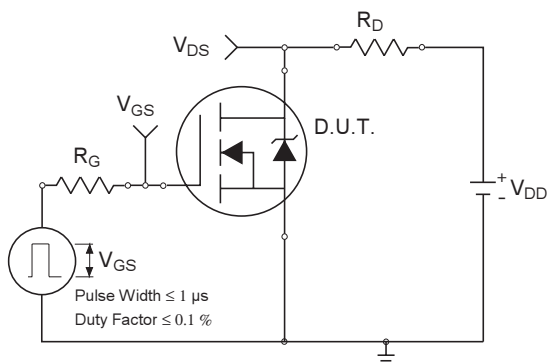
**Fig 15b.** Gate Charge Waveform



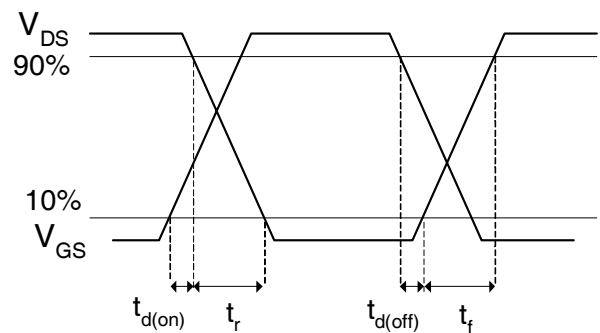
**Fig 16a.** Unclamped Inductive Test Circuit



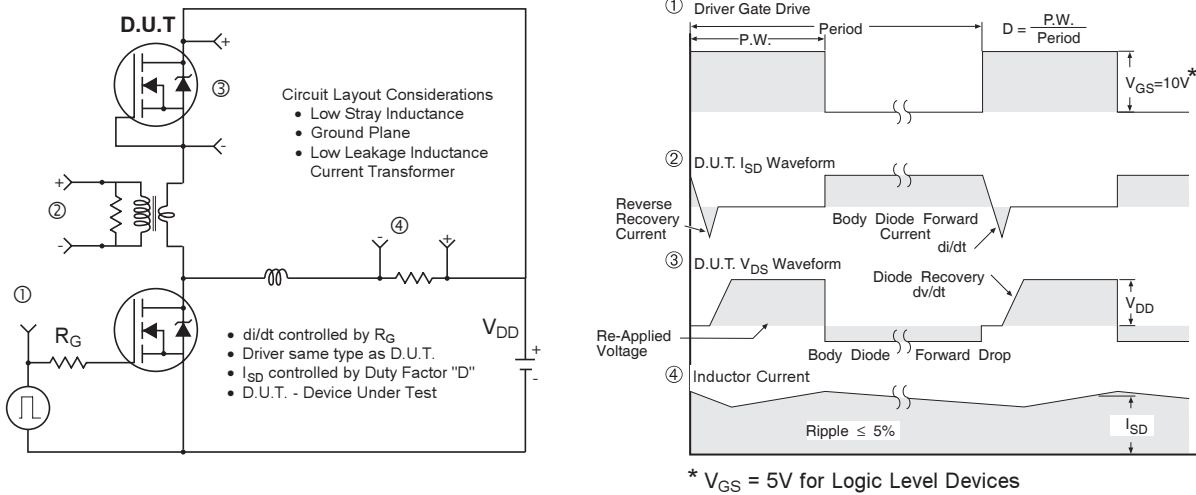
**Fig 16b.** Unclamped Inductive Waveforms



**Fig 17a.** Switching Time Test Circuit



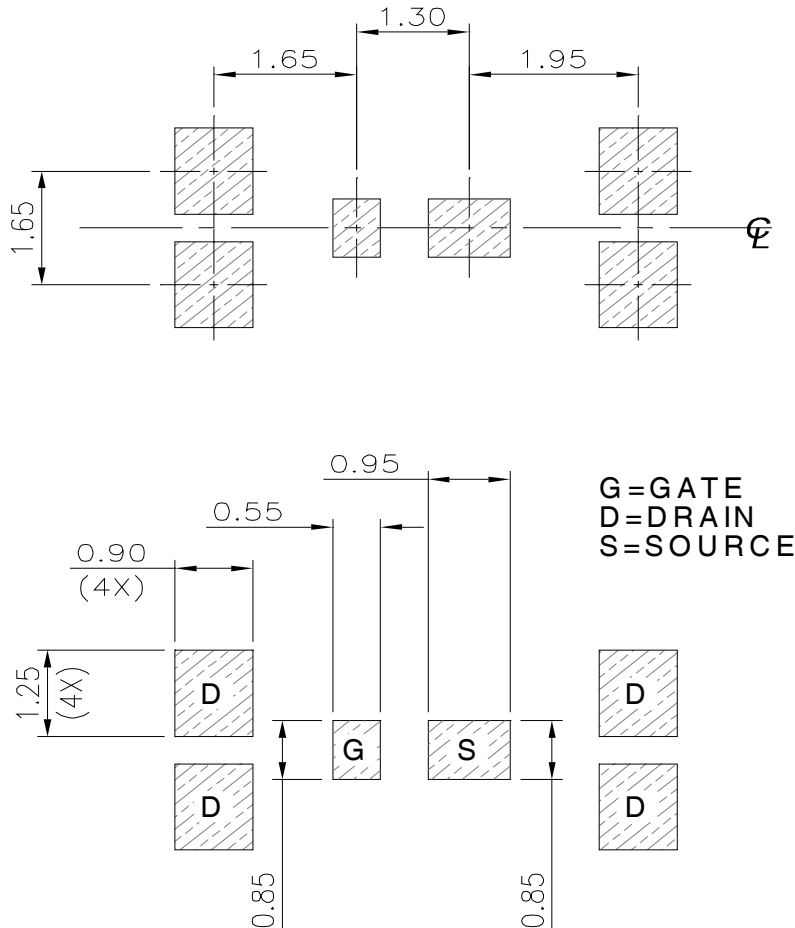
**Fig 17b.** Switching Time Waveforms



**Fig 18. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs**

## DirectFET®*plus* Board Footprint, SQ Outline (Small Size Can, Q-Designation).

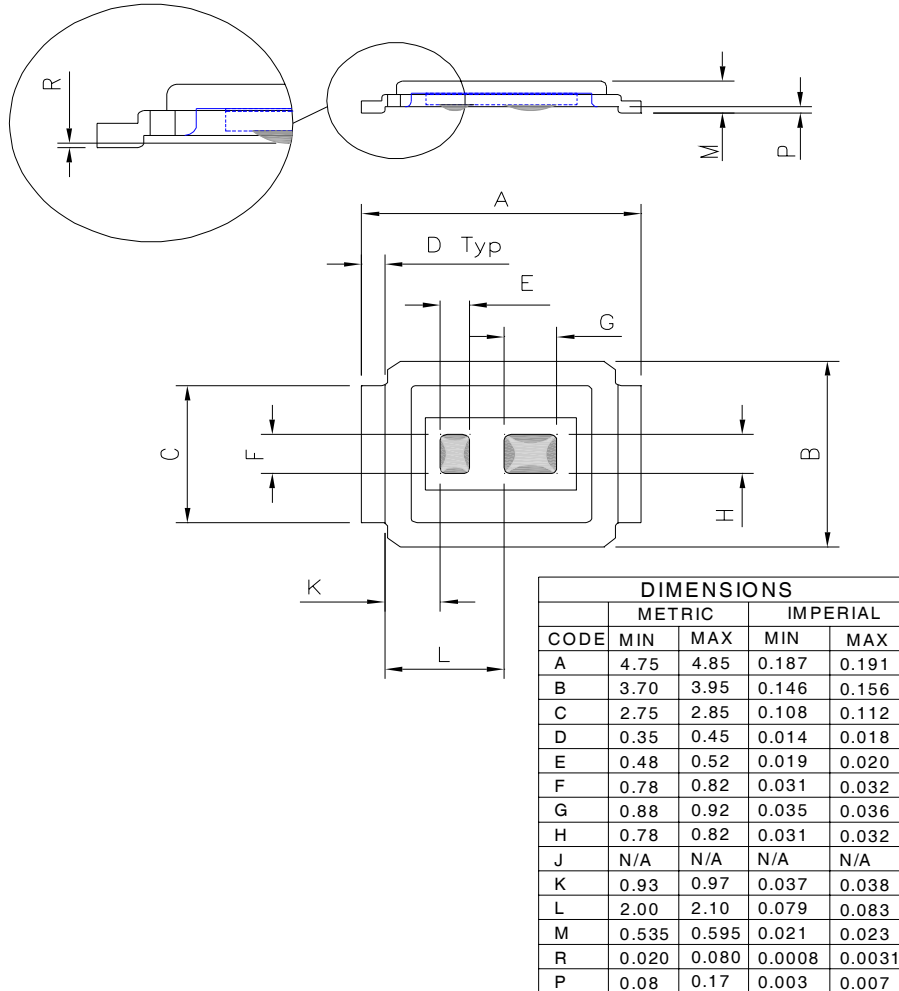
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



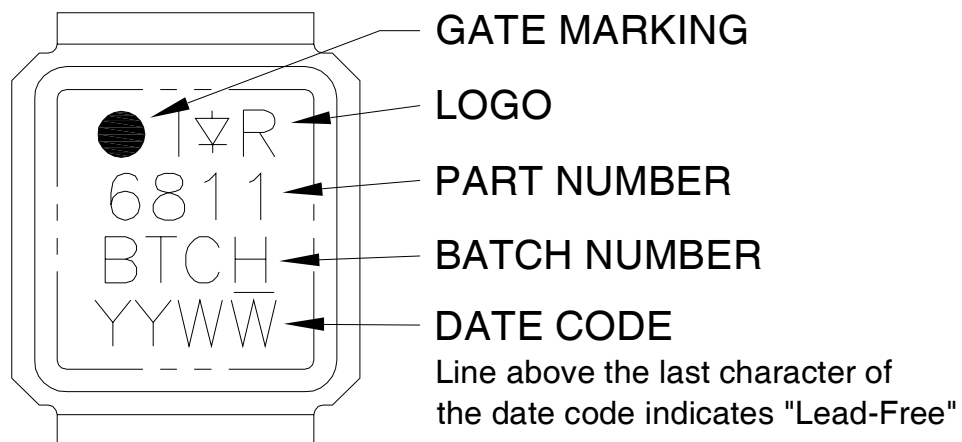
# IRF6811SPbF

## DirectFET<sup>®</sup>*plus* Outline Dimension, SQ Outline (Small Size Can, Q-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.

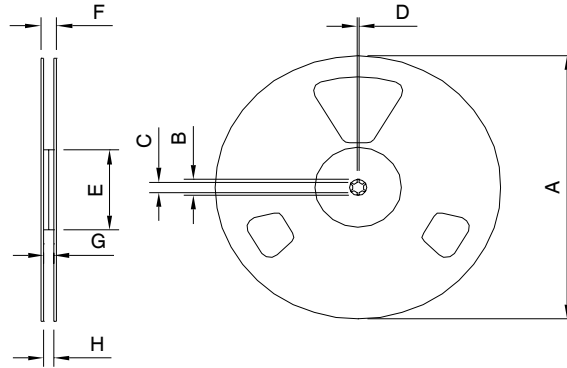


## DirectFET<sup>®</sup>*plus* Part Marking



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>

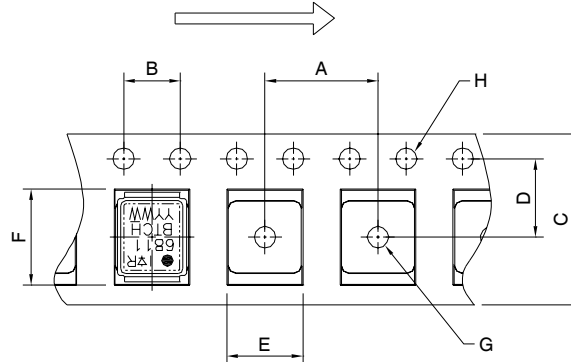
## DirectFET<sup>®</sup>plus Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm  
 Std reel quantity is 4800 parts. (ordered as IRF6811STRPBF). For 1000 parts on 7" reel, order IRF6811STR1PBF

REEL DIMENSIONS									
CODE	STANDARD OPTION (QTY 4800)				TR1 OPTION (QTY 1000)				
	METRIC		IMPERIAL		METRIC		IMPERIAL		
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C	
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C	
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50	
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C	
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C	
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53	
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C	
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C	

LOADED TAPE FEED DIRECTION



NOTE: CONTROLLING DIMENSIONS IN MM

CODE	DIMENSIONS			
	METRIC		IMPERIAL	
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	4.00	4.20	0.158	0.165
F	5.00	5.20	0.197	0.205
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Consumer market.  
 Qualification Standards can be found on IR's Web site.

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