

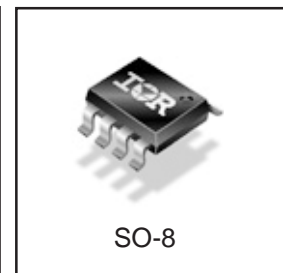
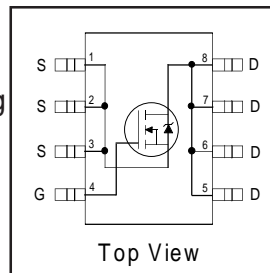
Applications

- High frequency DC-DC converters

V_{DSS}	R_{DS(on)} max	I_D
200V	0.73Ω	1.2A

Benefits

- Low Gate to Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{oss} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	1.2	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	1.0	
I _{DM}	Pulsed Drain Current ①	10	
P _D @ T _A = 25°C	Power Dissipation	2.5	W
	Linear Derating Factor	0.02	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	6.8	V/ns
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topologies

- Telecom 48V input Forward Converter

Notes ① through ⑥ are on page 8
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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.23	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.73	Ω	$V_{GS} = 10V, I_D = 0.72A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 160V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	1.1	—	—	S	$V_{DS} = 50V, I_D = 0.72A$
Q_g	Total Gate Charge	—	9.5	14	nC	$I_D = 0.72A$
Q_{gs}	Gate-to-Source Charge	—	2.5	3.8		$V_{DS} = 160V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	4.6	6.9		$V_{GS} = 10V, \text{④}$
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 100V$
t_r	Rise Time	—	9.5	—		$I_D = 0.72A$
$t_{d(off)}$	Turn-Off Delay Time	—	18	—		$R_G = 24\Omega$
t_f	Fall Time	—	15	—		$V_{GS} = 10V, \text{④}$
C_{iss}	Input Capacitance	—	280	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	52	—		$V_{DS} = 25V$
C_{rSS}	Reverse Transfer Capacitance	—	14	—		$f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	330	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	25	—		$V_{GS} = 0V, V_{DS} = 160V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	48	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V, \text{⑤}$

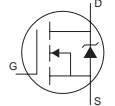
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	68	mJ
I_{AR}	Avalanche Current①	—	1.2	A
E_{AR}	Repetitive Avalanche Energy①	—	0.25	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient⑥	—	50	°C/W

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	10		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 0.72A, V_{GS} = 0V, \text{④}$
t_{rr}	Reverse Recovery Time	—	60	90	ns	$T_J = 25^\circ\text{C}, I_F = 0.72A$
Q_{rr}	Reverse Recovery Charge	—	130	200	nC	$di/dt = 100A/\mu s, \text{④}$

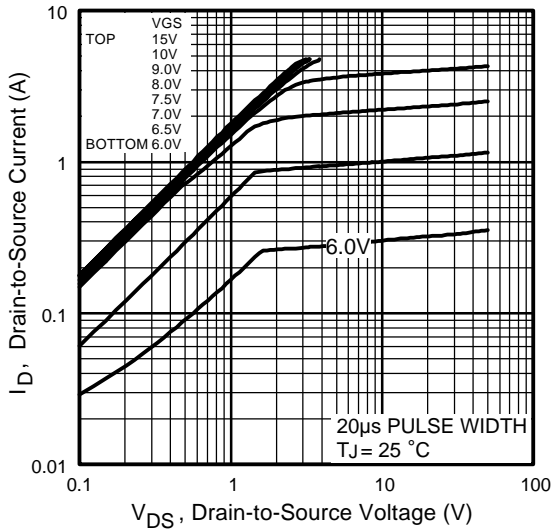


Fig 1. Typical Output Characteristics

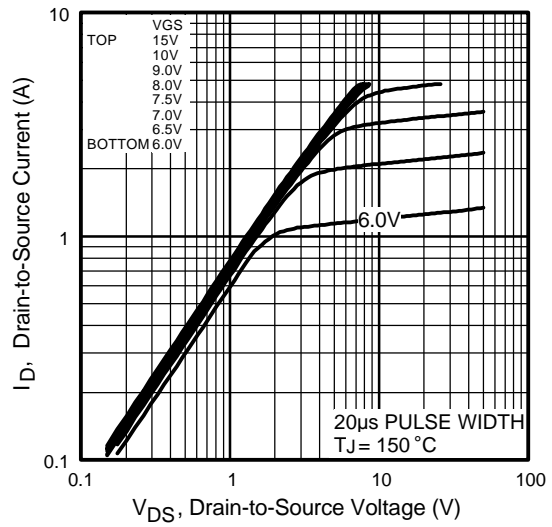


Fig 2. Typical Output Characteristics

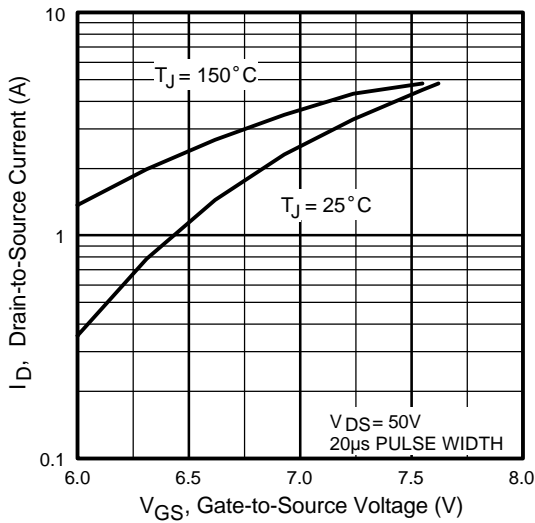


Fig 3. Typical Transfer Characteristics

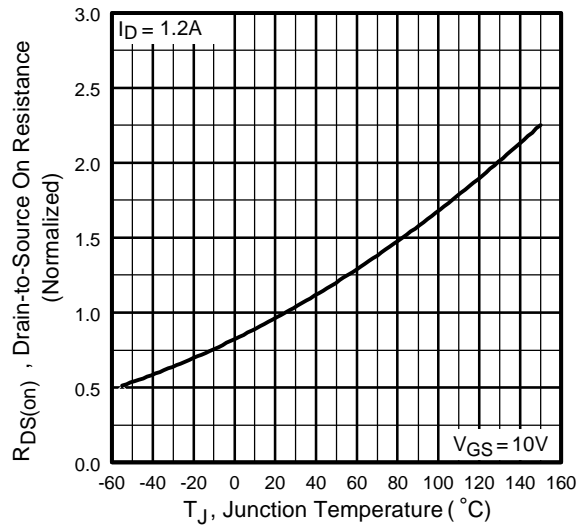


Fig 4. Normalized On-Resistance Vs. Temperature

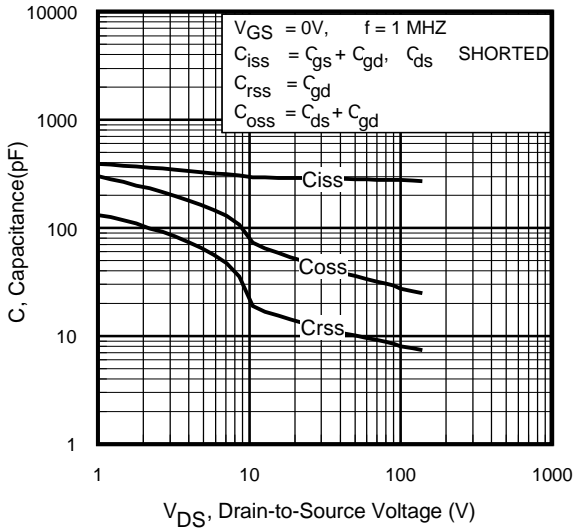


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

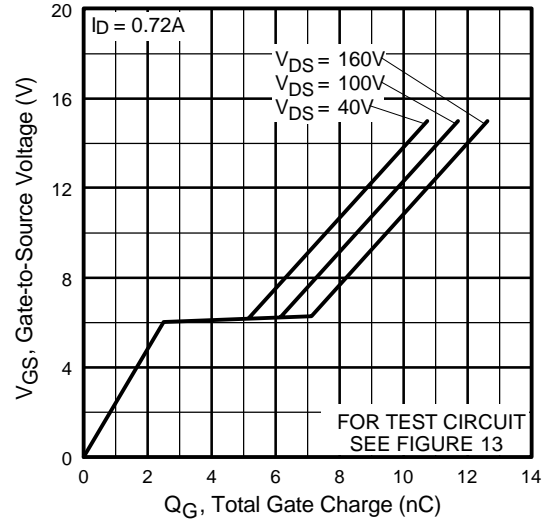


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

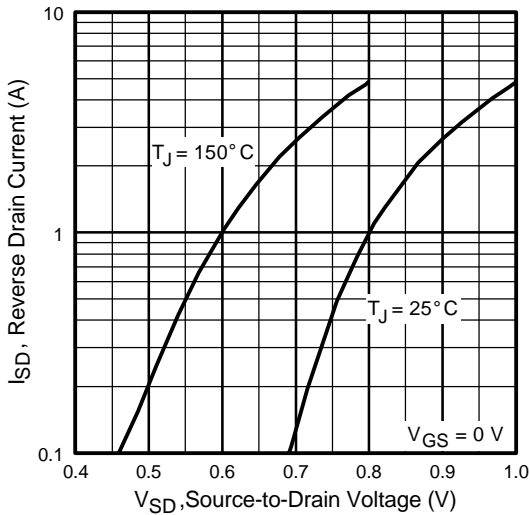


Fig 7. Typical Source-Drain Diode Forward Voltage

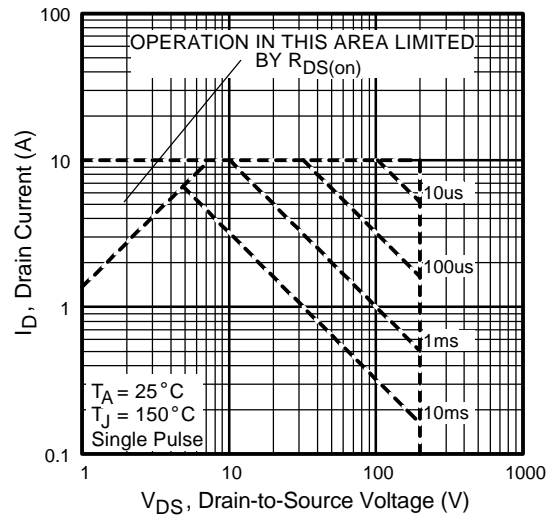


Fig 8. Maximum Safe Operating Area

Fig 6. On-Resistance Vs. Drain Current

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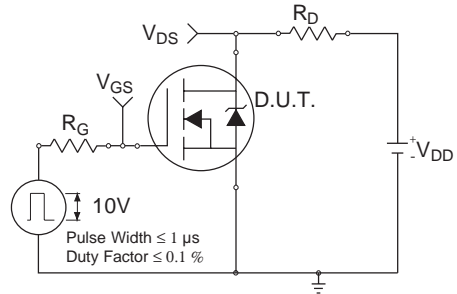
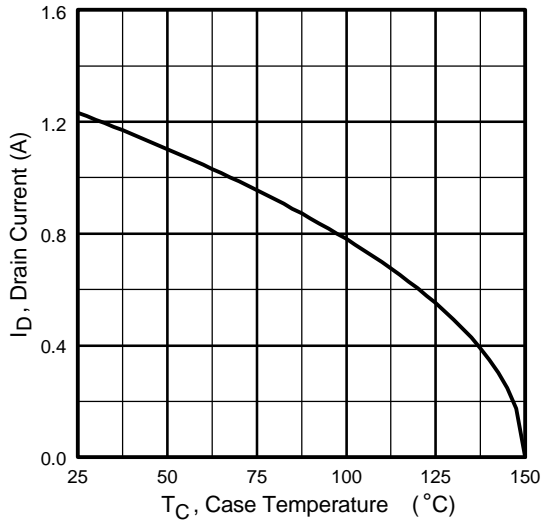


Fig 10a. Switching Time Test Circuit

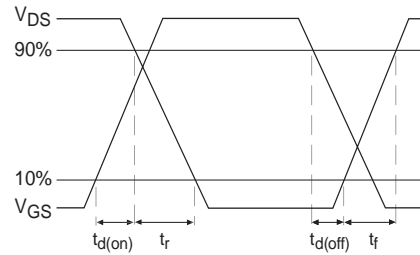


Fig 10b. Switching Time Waveforms

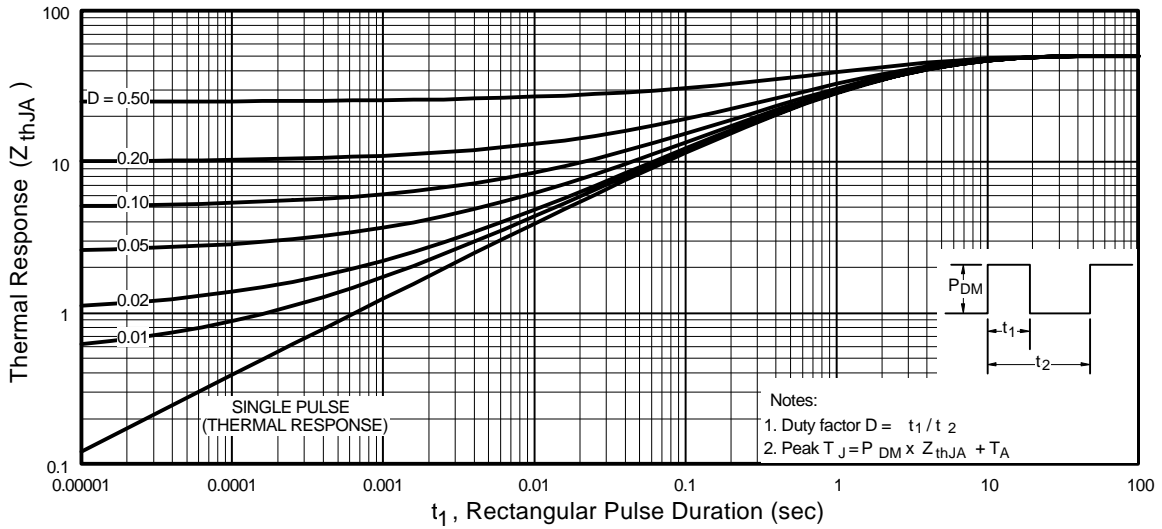


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

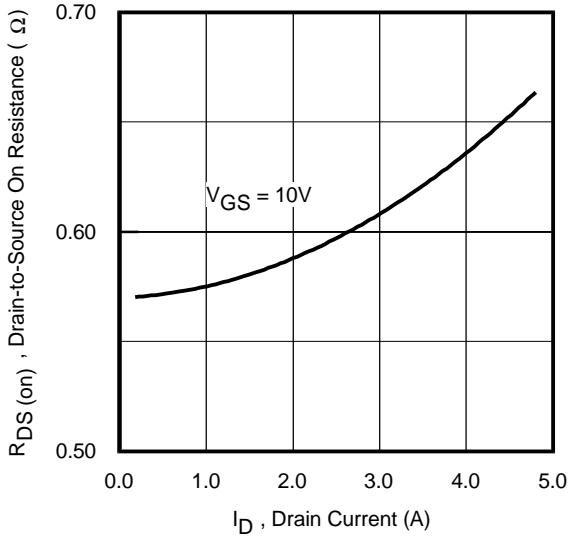


Fig 12. On-Resistance Vs. Drain Current

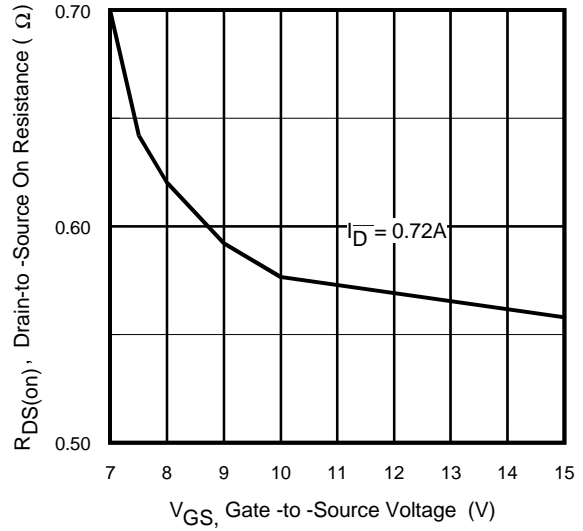


Fig 13. On-Resistance Vs. Gate Voltage

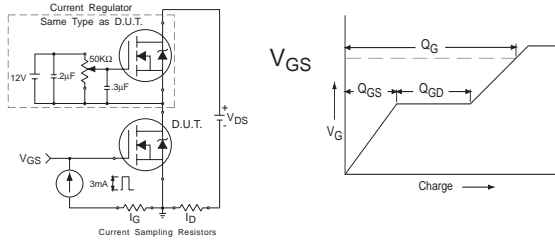


Fig 13a&b. Basic Gate Charge Test Circuit and Waveform

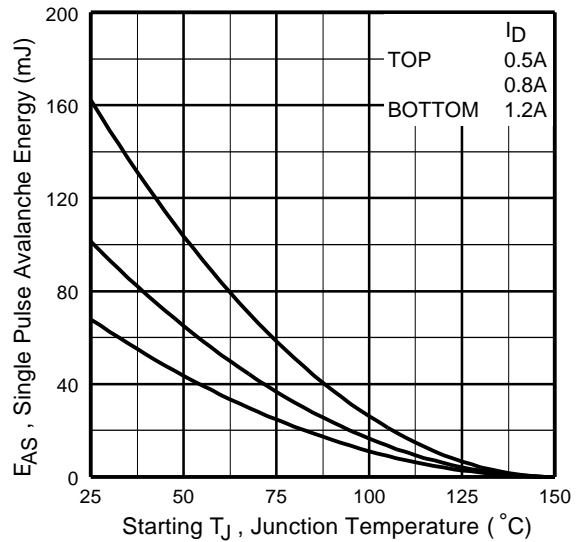


Fig 14c. Maximum Avalanche Energy Vs. Drain Current

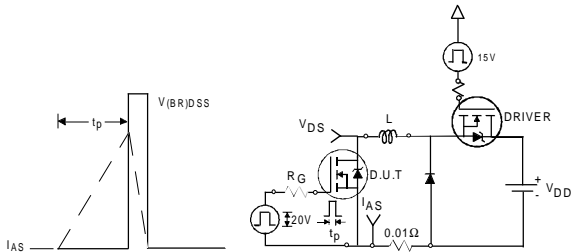
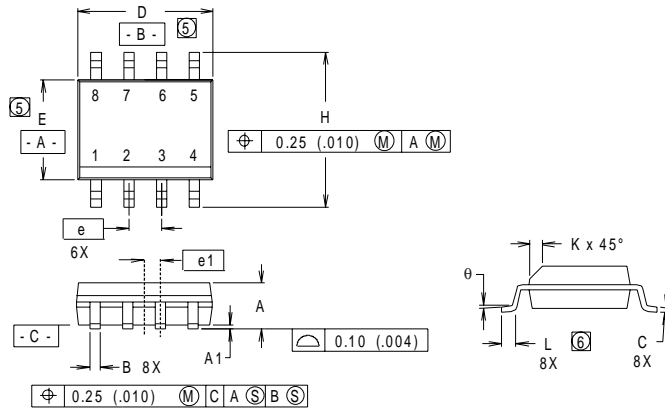


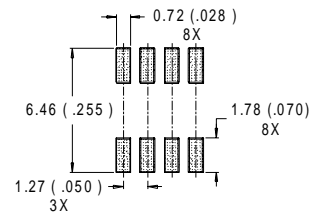
Fig 14a&b. Unclamped Inductive Test circuit and Waveforms

SO-8 Package Details



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	0.16	.050	0.41	1.27
θ	0°	8°	0°	8°

RECOMMENDED FOOTPRINT

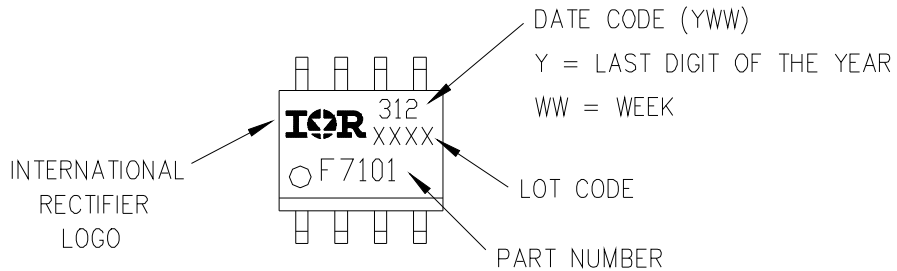


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- (5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS
MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
- (6) DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

SO-8 Part Marking

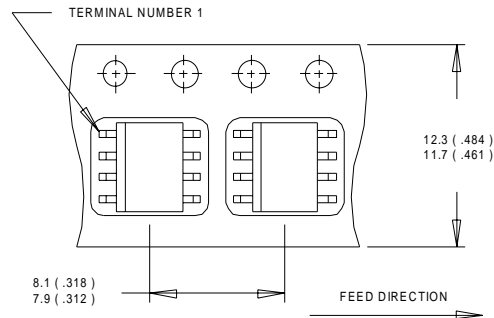
EXAMPLE: THIS IS AN IRF7101



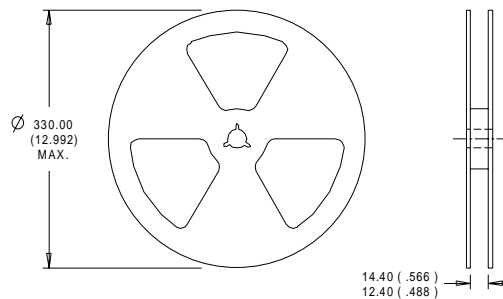
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SO-8 Tape and Reel



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 94\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 1.2\text{A}$.
- ③ $I_{SD} \leq 0.72\text{A}$, $di/dt \leq 130\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ When mounted on 1 inch square copper board, $t < 10$ sec

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IR EUROPEAN REGIONAL CENTER: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 OBL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
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Data and specifications subject to change without notice. 4/00

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- ⊖ [Infineon Technologies](#) Information

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