THE DATASHEET OF

AD5689RTCPZ-EP-RL7

Dual, 16-Bit nanoDAC+ with 4 ppm/°C Reference, SPI Interface

Enhanced Product **AD5689R-EP**

FEATURES

High relative accuracy (INL): ±4 LSB maximum at 16 bits
Low drift 2.5 V reference: 4 ppm/°C typical
Tiny package: 3 mm × 3 mm, 16-lead LFCSP
Total unadjusted error (TUE): ±0.1% of FSR maximum
Offset error: ±1.5 mV maximum
Gain error: ±0.1% of FSR maximum
High drive capability: 15 mA, 0.5 V from supply rails
User-selectable gain of 1 or 2 (GAIN pin)
Reset to zero scale or midscale (RSTSEL pin)
1.8 V logic compatibility
50 MHz SPI with readback or daisy chain
Low glitch: 0.5 nV-sec
Low power: 3.3 mW at 3 V
2.7 V to 5.5 V power supply

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC)
Temperature range: −55°C to +125°C
Controlled manufacturing baseline
1 assembly/test site
1 fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Optical transceivers
Base station power amplifiers
Process control (PLC input/output cards)
Industrial automation
Data acquisition systems

FUNCTIONAL BLOCK DIAGRAM

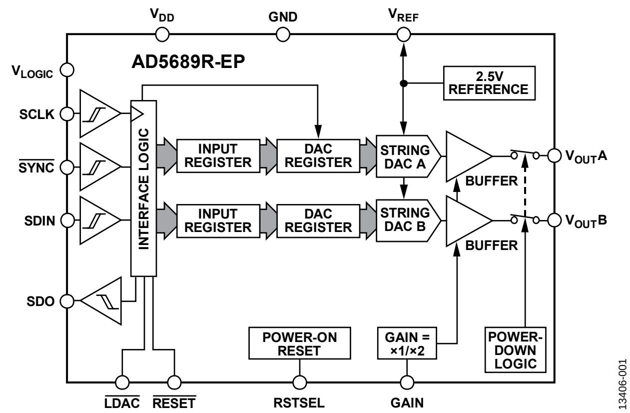

Figure 1.

GENERAL DESCRIPTION

The AD5689R-EP, a member of the *nano*DAC+™ family, is a low power, dual, 16-bit buffered voltage output digital-to-analog converter (DAC). The device includes a 2.5 V, 4 ppm/°C internal reference (enabled by default) and a gain select pin giving a full-scale output of 2.5 V (gain = 1) or 5 V (gain = 2). The device operates from a single 2.7 V to 5.5 V supply, is guaranteed monotonic by design, and exhibits less than 0.1% FSR gain error and 1.5 mV offset error performance.

The AD5689R-EP also incorporates a power-on reset circuit and a RSTSEL pin that ensures that the DAC outputs power up to zero scale or midscale and remains there until a valid write occurs. The device contains a per channel power-down feature that reduces the current consumption of the device to 4 µA at 3 V while in power-down mode.

The AD5689R-EP uses a versatile serial peripheral interface (SPI) that operates at clock rates up to 50 MHz, and contains a V_{LOGIC} pin that is intended for 1.8 V/3 V/5 V logic.

Additional application and technical information can be found in the AD5689R/AD5687R data sheet.

PRODUCT HIGHLIGHTS

1. High Relative Accuracy (INL).
   ±4 LSB maximum
2. Low Drift 2.5 V On-Chip Reference.
   4 ppm/°C typical temperature coefficient
   13 ppm/°C maximum temperature coefficient

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REVISION HISTORY

11/2016—Rev. 0 to Rev. A

Changed 1.8 V ≤ V_{LOGIC} ≤ 5.5 V to 1.62 V ≤ V_{LOGIC} ≤ 5.5 V ..... Throughout
Changes to Features Section 1
Changes to V_{LOGIC} Parameter, Table 1 4
Changes to Table 3 6
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8/2015—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, R_L = 2 kΩ, C_L = 200 pF, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[1]					
Resolution	16			Bits	
Relative Accuracy		±1	±4	LSB	Gain = 2
		±1	±5	LSB	Gain = 1
Differential Nonlinearity (DNL)			±1	LSB	Guaranteed monotonic by design
Zero-Code Error		0.4	1.5	mV	All zeros loaded to DAC register
Offset Error		+0.1	±1.5	mV	
Full-Scale Error		+0.01	±0.1	% of FSR	All ones loaded to DAC register
Gain Error		±0.02	±0.1	% of FSR	Gain = 2
		±0.02	±0.15	% of FSR	Gain = 1
Total Unadjusted Error		±0.01	±0.1	% of FSR	External reference; gain = 2
			±0.2	% of FSR	Internal reference; gain = 1
Offset Error Drift[2]		±1		µV/°C	
Gain Temperature Coefficient (TC)[2]		±1		ppm	Of FSR/°C
DC Power Supply Rejection Ratio[2]		0.15		mV/V	DAC code = midscale, V_{DD} = 5 V ± 10%
DC Crosstalk[2]					
		±2		µV	Due to single channel, full-scale output change
		±3		µV/mA	Due to load current change
		±2		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[2]					
Output Voltage Range	0		V_{REF}	V	Gain = 1
	0		2 × V_{REF}	V	Gain = 2, see Figure 28
Capacitive Load Stability		2		nF	R_L = ∞
		10		nF	R_L = 1 kΩ
Resistive Load[3]	1			kΩ	
Load Regulation		80		µV/mA	5 V ± 10%, DAC code = midscale; −30 mA ≤ I_{OUT} ≤ +30 mA
		80		µV/mA	3 V ± 10%, DAC code = midscale; −20 mA ≤ I_{OUT} ≤ +20 mA
Short-Circuit Current[4]		40		mA	
Load Impedance at Rails[5]		25		Ω	See Figure 28
Power-Up Time		2.5		µs	Coming out of power-down mode; V_{DD} = 5 V
REFERENCE OUTPUT					
Output Voltage[6]	2.4975		2.5025	V	At ambient
Reference TC[7, 8]		4	13	ppm/°C	
Output Impedance[2]		0.04		Ω	
Output Voltage Noise[2]		12		µV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density[2]		240		nV/√Hz	At ambient; f = 10 kHz, C_L = 10 nF
Load Regulation Sourcing[2]		20		µV/mA	At ambient
Load Regulation Sinking[2]		40		µV/mA	At ambient
Output Current Load Capability[2]		±5		mA	V_{DD} ≥ 3 V
Line Regulation[2]		100		µV/V	At ambient
Thermal Hysteresis[2]		125		ppm	First cycle
		25		ppm	Additional cycles
LOGIC INPUTS[2]					
Input Current			±2	µA	Per pin
Input Voltage					
Low (V_{INL})			0.3 × V_{LOGIC}	V	
High (V_{INH})	0.7 × V_{LOGIC}			V	
Pin Capacitance		2		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (SDO)[2]					
Output Voltage					
Low (V_{OL})			0.4	V	I_{SINK} = 200 µA
High (V_{OH})	V_{LOGIC} − 0.4			V	I_{SOURCE} = 200 µA
Floating State Output Capacitance		4		pF	
POWER REQUIREMENTS					
V_{LOGIC}	1.62		5.5	V	
I_{LOGIC}			3	µA	
V_{DD}	2.7		5.5	V	Gain = 1
V_{DD}	V_{REF} + 1.5		5.5	V	Gain = 2
I_{DD}					$V_{IH} = V_{DD}$, V_{IL} = GND, V_{DD} = 2.7 V to 5.5 V
Normal Mode[9]		0.59	0.7	mA	Internal reference off
		1.1	1.3	mA	Internal reference on at full scale
All Power-Down Modes[10]		1	4	µA	−40°C to +85°C
			6	µA	−55°C to +125°C

[1] DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when $V_{REF} = V_{DD}$ with gain = 1 or when $V_{REF}/2 = V_{DD}$ with gain = 2. Linearity is calculated using a reduced code range of 256 to 65,280.
[2] Guaranteed by design and characterization; not production tested.
[3] Channel A can have an output current of up to 15 mA. Similarly, Channel B can have an output current of up to 15 mA, up to a junction temperature of 135°C.
[4] V_{DD} = 5 V. The device includes current limiting that is intended to protect the device during temporary overload conditions. Junction temperature may be exceeded during current limit, but operation above the specified maximum operation junction temperature can impair device reliability.
[5] When drawing a load current at either rail, the output voltage headroom, with respect to that rail, is limited by the 25 Ω typical channel resistance of the output device. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV (see Figure 28).
[6] Initial accuracy presolder reflow is ±750 µV; output voltage includes the effects of preconditioning drift. See the AD5689R/AD5687R data sheet for more information.
[7] Reference is trimmed and tested at two temperatures and is characterized from −55°C to +125°C.
[8] Reference temperature coefficient is calculated as per the box method. See the AD5689R/AD5687R data sheet for more information.
[9] Interface inactive. Both DACs active. DAC outputs unloaded.
[10] Both DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Guaranteed by design and characterization; not production tested.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments[2]
Output Voltage Settling Time		5	8	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		0.8		V/µs	
Digital-to-Analog Glitch Impulse		0.5		nV-sec	1 LSB change around major carry
Digital Feedthrough		0.13		nV-sec	
Digital Crosstalk		0.1		nV-sec	
Analog Crosstalk		0.2		nV-sec	
DAC-to-DAC Crosstalk		0.3		nV-sec	
Total Harmonic Distortion (THD)[3]		−80		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Output Noise Spectral Density (NSD)		300		nV/√Hz	DAC code = midscale, 10 kHz; gain = 2
Output Noise		6		µV p-p	0.1 Hz to 10 Hz
Signal-to-Noise Ratio (SNR)		90		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Spurious Free Dynamic Range (SFDR)		83		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Signal-to-Noise-and-Distortion Ratio (SINAD)		80		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz

[1] See the AD5689R/AD5687R data sheet.
[2] Temperature range is −55°C to +125°C, typical at 25°C.
[3] Digitally generated sine wave at 1 kHz.

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2. $V_{DD} = 2.7$ V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, and $V_{REF} = 2.5$ V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

		1.62 V ≤ V_{LOGIC} < 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		
Parameter[1]	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCLK Cycle Time	t_1	20		20		ns
SCLK High Time	t_2	10		10		ns
SCLK Low Time	t_3	10		10		ns
SYNC to SCLK Falling Edge Setup Time	t_4	15		10		ns
Data Setup Time	t_5	5		5		ns
Data Hold Time	t_6	5		5		ns
SCLK Falling Edge to SYNC Rising Edge	t_7	10		10		ns
Minimum SYNC High Time	t_8	20		20		ns
SYNC Rising Edge to SYNC Rising Edge (DAC Register Update/s)	t_9	870		830		ns
SYNC Falling Edge to SCLK Fall Ignore	t_{10}	16		10		ns
LDAC Pulse Width Low	t_{11}	15		15		ns
SYNC Rising Edge to LDAC Rising Edge	t_{12}	20		20		ns
SYNC Rising Edge to LDAC Falling Edge	t_{13}	30		30		ns
LDAC Falling Edge to SYNC Rising Edge	t_{14}	840		800		ns
Minimum Pulse Width Low	t_{15}	30		30		ns
Pulse Activation Time	t_{16}	30		30		ns
Power-Up Time[2]		4.5		4.5		μs

[1] Guaranteed by design and characterization; not production tested.
[2] Time to exit power-down to normal mode of AD5689R-EP operation, 32nd clock edge to 90% of DAC midscale value, with output unloaded.

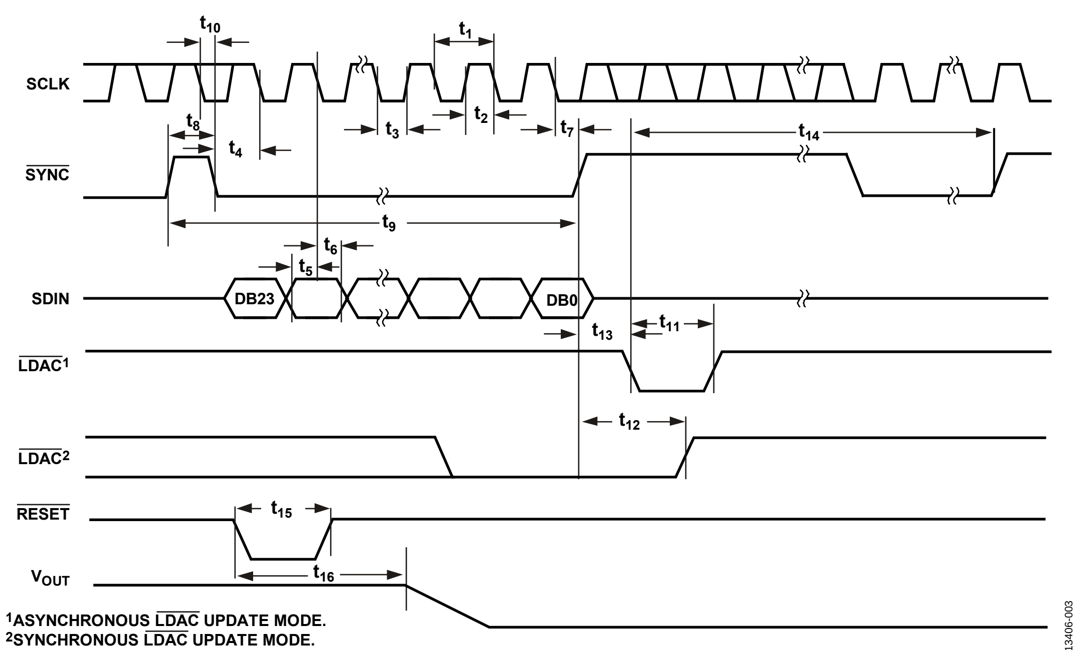

Figure 2. Serial Write Operation

DAISY-CHAIN AND READBACK TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1$ ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 4 and Figure 5. V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, and V_{REF} = 2.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. V_{DD} = 2.7 V to 5.5 V.

Table 4.

Parameter[1]	Symbol	1.62 V ≤ V_{LOGIC} < 2.7 V		2.7 V ≤ V_{LOGIC} ≤ 5.5 V		Unit
		Min	Max	Min	Max	
SCLK Cycle Time	t_1	66		40		ns
SCLK High Time	t_2	33		20		ns
SCLK Low Time	t_3	33		20		ns
$\overline{\text{SYNC}}$ to SCLK Falling Edge	t_4	33		20		ns
Data Setup Time	t_5	5		5		ns
Data Hold Time	t_6	5		5		ns
SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge	t_7	15		10		ns
Minimum $\overline{\text{SYNC}}$ High Time	t_8	60		30		ns
SDO Data Valid from SCLK Rising Edge	t_9		45		30	ns
$\overline{\text{SYNC}}$ Rising Edge to SCLK Rising Edge	t_{10}	15		10		ns
$\overline{\text{SYNC}}$ Rising Edge to SDO Disable	t_{11}	60		60		ns

[1] Guaranteed by design and characterization; not production tested.

Circuit and Timing Diagrams

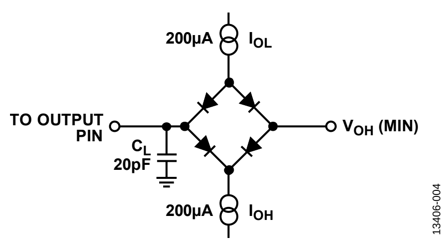

Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications

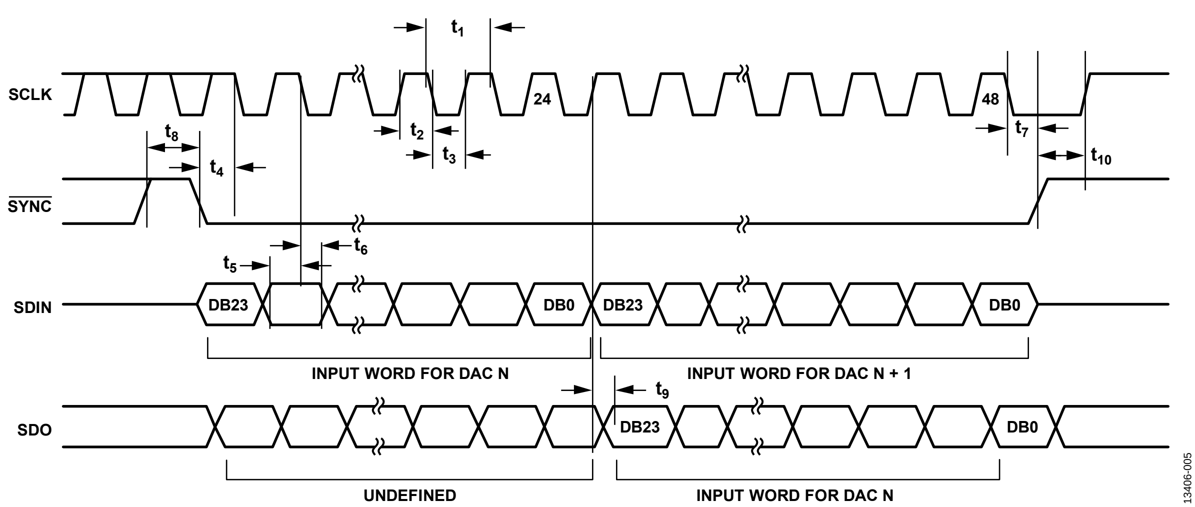

Figure 4. Daisy-Chain Timing Diagram

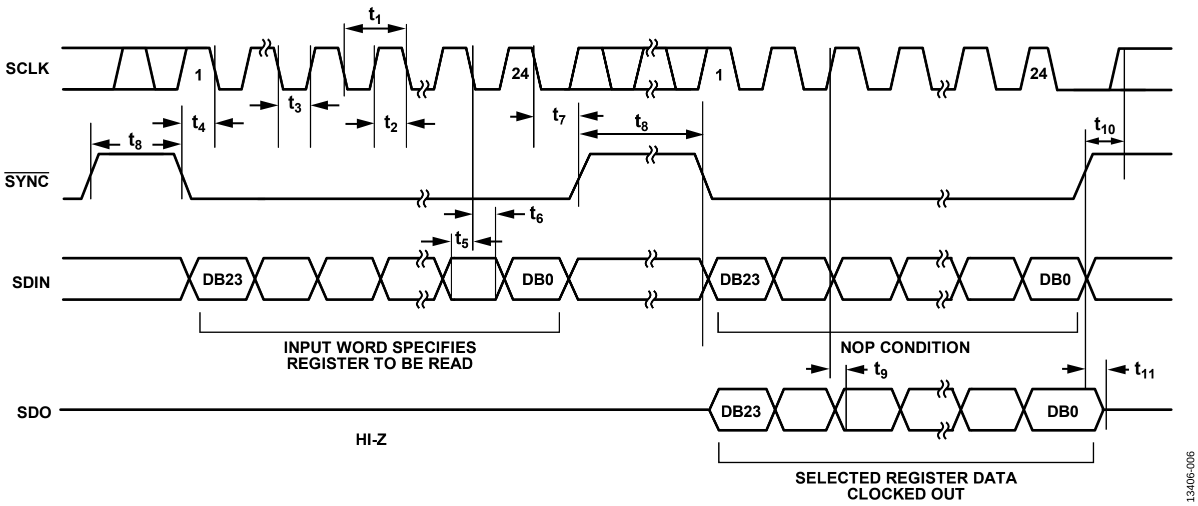

Figure 5. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{LOGIC} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	135°C
16-Lead LFCSP, $θ_{JA}$ Thermal Impedance, 0_{JA} Airflow (4-Layer Board)	70°C/W
Reflow Soldering Peak Temperature, Pb Free (J-STD-020)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

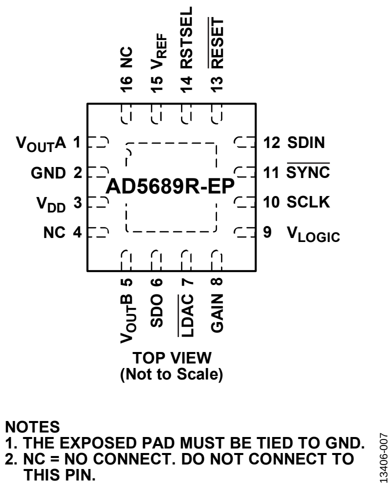

Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No	Mnemonic	Description
1	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
2	GND	Ground Reference Point for All Circuitry on the AD5689R-EP.
3	V_{DD}	Power Supply Input. The AD5689R-EP can be operated from 2.7 V to 5.5 V. Decouple the supply with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	NC	No Connect. Do not connect to this pin.
5	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
6	SDO	Serial Data Output. SDO can be used to daisy-chain a number of AD5689R-EP devices together, or it can be used for readback. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.
7	$\overline{\text{LDAC}}$	$\overline{\text{LDAC}}$ can be operated in two modes: asynchronously and synchronously. Pulsing this pin low allows either or both DAC registers to be updated if the input registers have new data; both DAC outputs can be updated simultaneously. This pin can also be tied permanently low.
8	GAIN	Gain Select. When this pin is tied to GND, both DACs output a span from 0 V to V_{REF}. If this pin is tied to V_{LOGIC}, both DACs output a span of 0 V to 2 × V_{REF}.
9	V_{LOGIC}	Digital Power Supply. Voltage ranges from 1.62 V ≤ V_{LOGIC} ≤ 5.5 V.
10	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
11	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data is transferred in on the falling edges of the next 24 clocks.
12	SDIN	Serial Data Input. This device has a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	$\overline{\text{RESET}}$	Asynchronous Reset Input. The $\overline{\text{RESET}}$ input is falling edge sensitive. When $\overline{\text{RESET}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{RESET}}$ is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin. If this pin is forced low at power-up, the power-on reset (POR) circuit does not initialize the device correctly until this pin is released.
14	RSTSEL	Power-On Reset Select. Tying this pin to GND powers up both DACs to zero scale. Tying this pin to V_{LOGIC} powers up both DACs to midscale.
15	V_{REF}	Reference Voltage. The AD5689R-EP has a common reference pin. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference output.
16	NC	No Connect. Do not connect to this pin.
17	EPAD	Exposed Pad. The exposed pad must be tied to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

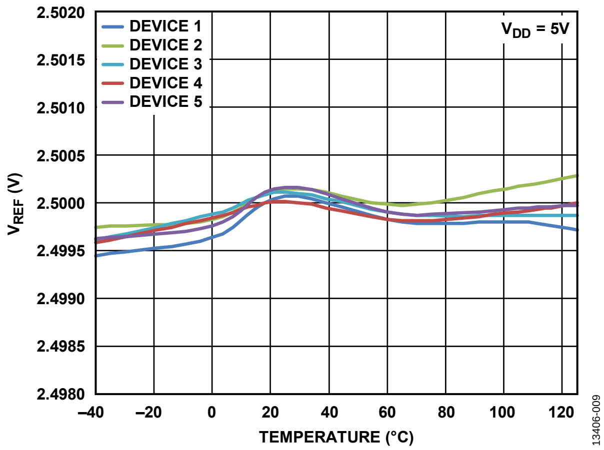

Figure 7. Internal Reference Voltage (V_{REF}) vs. Temperature

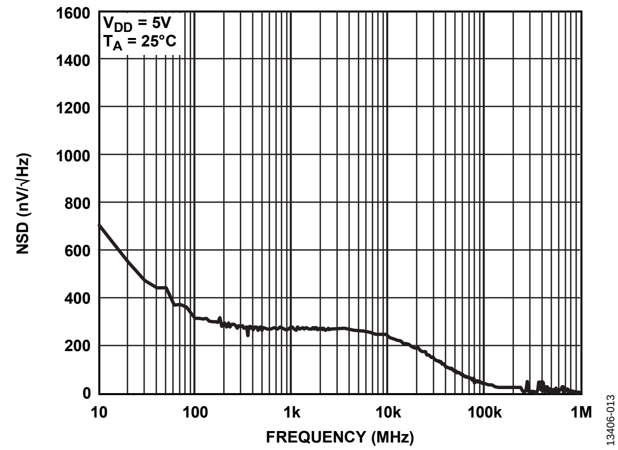

Figure 10. Internal Reference Noise Spectral Density (NSD) vs. Frequency

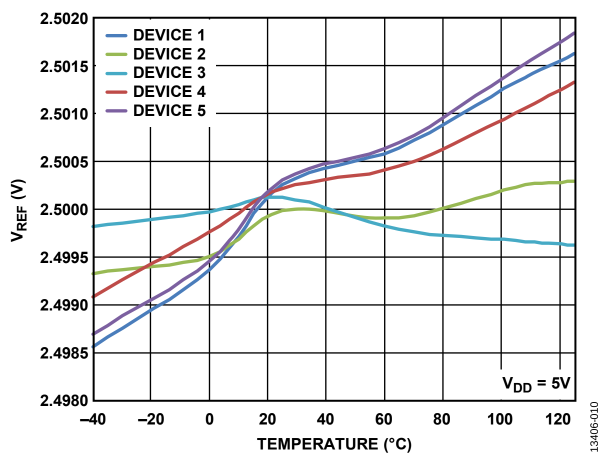

Figure 8. V_{REF} vs. Temperature

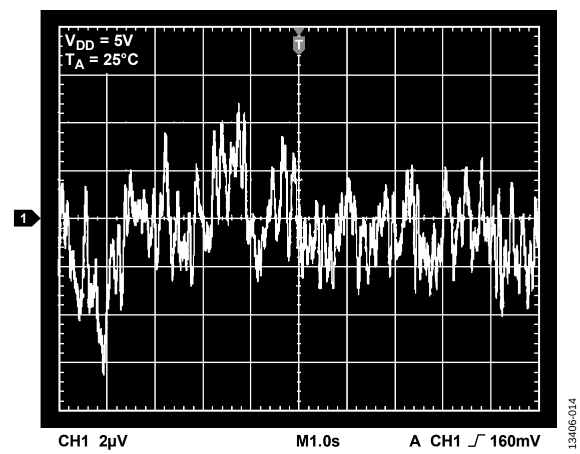

Figure 11. Internal Reference Noise, 0.1 Hz to 10 Hz

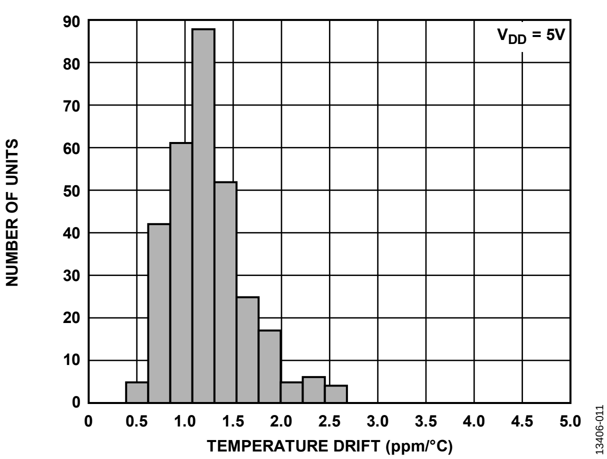

Figure 9. Reference Output Temperature Drift Histogram

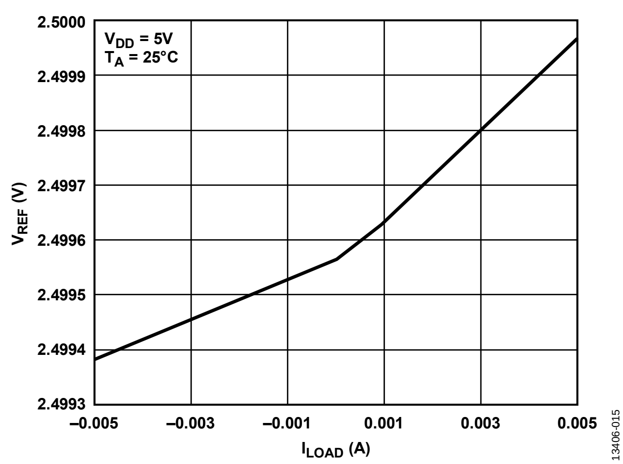

Figure 12. V_{REF} vs. Load Current (I_{LOAD})

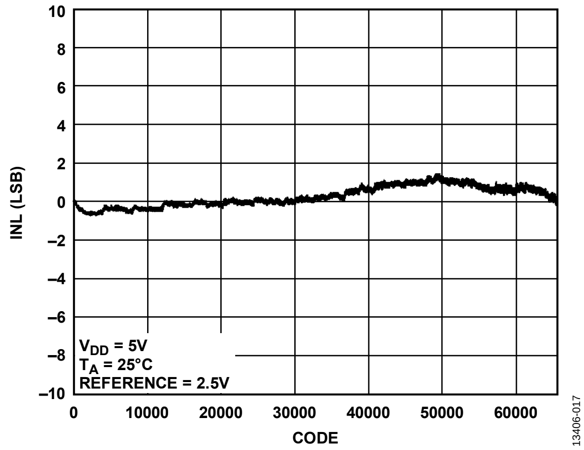

Figure 13. Integral Nonlinearity (INL) vs. Code

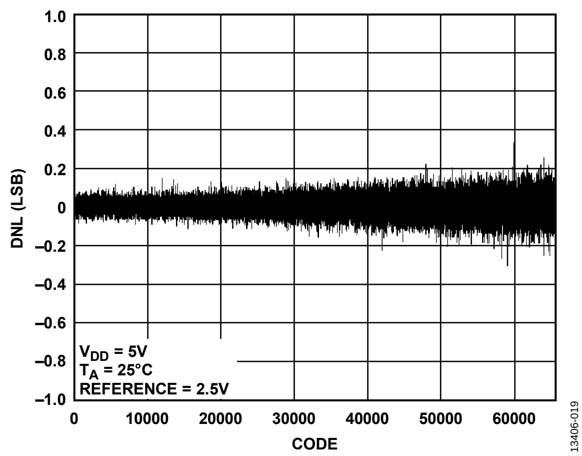

Figure 14. Differential Nonlinearity (DNL) vs. Code

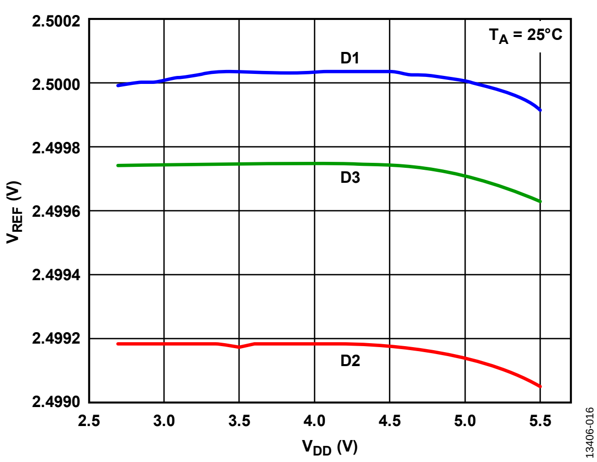

Figure 15. V_{REF} vs. Supply Voltage (V_{DD})

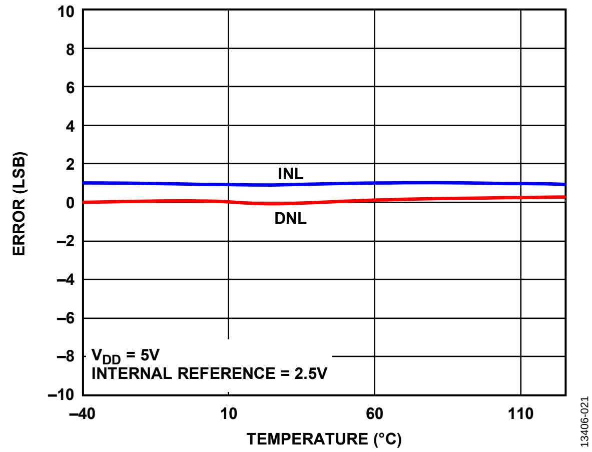

Figure 16. INL Error and DNL Error vs. Temperature

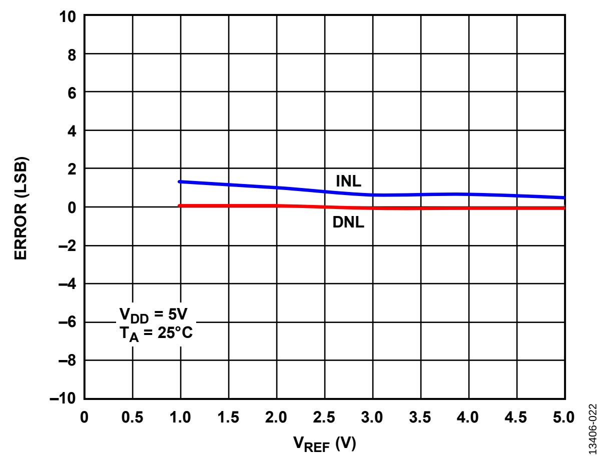

Figure 17. INL Error and DNL Error vs. V_{REF}

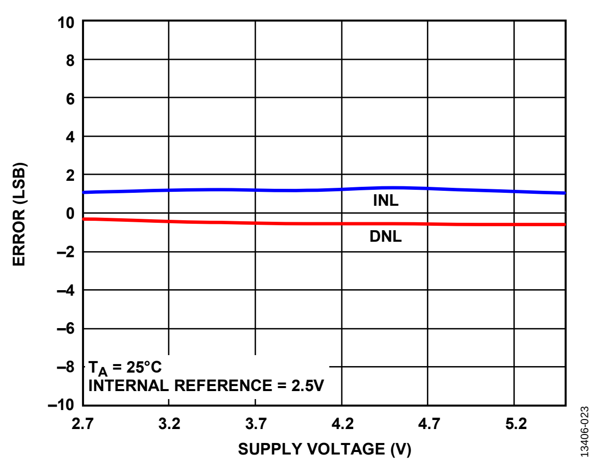

Figure 18. INL Error and DNL Error vs. Supply Voltage

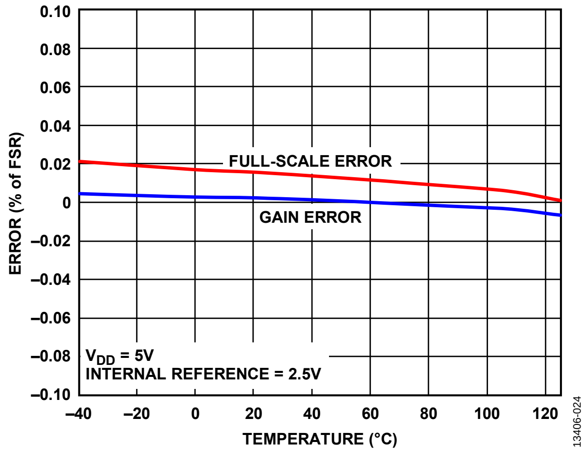

Figure 19. Gain Error and Full-Scale Error vs. Temperature

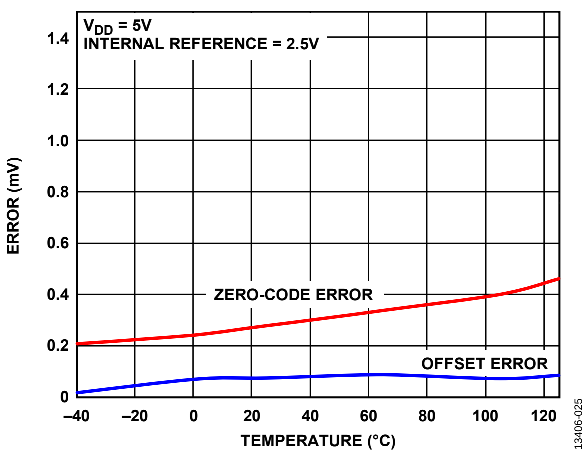

Figure 20. Zero-Code Error and Offset Error vs. Temperature

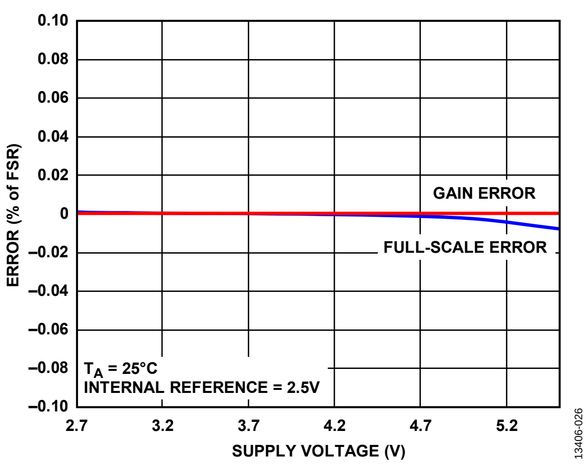

Figure 21. Gain Error and Full-Scale Error vs. Supply Voltage

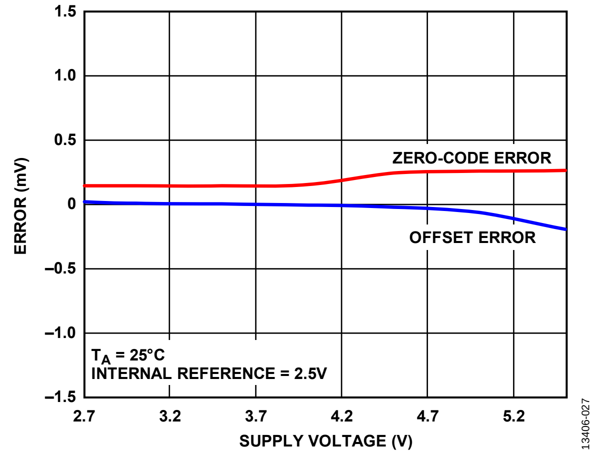

Figure 22. Zero-Code Error and Offset Error vs. Supply Voltage

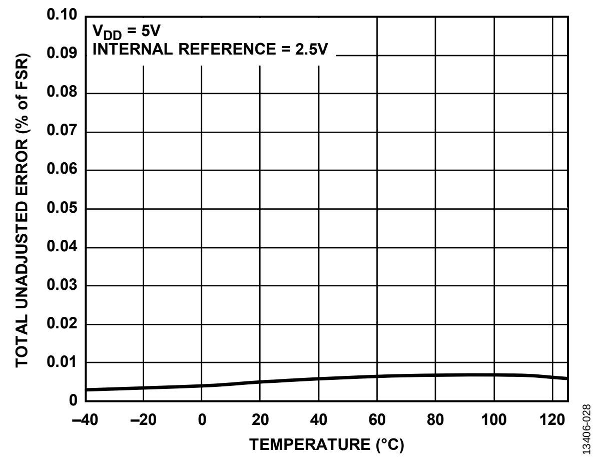

Figure 23. Total Unadjusted Error (TUE) vs. Temperature

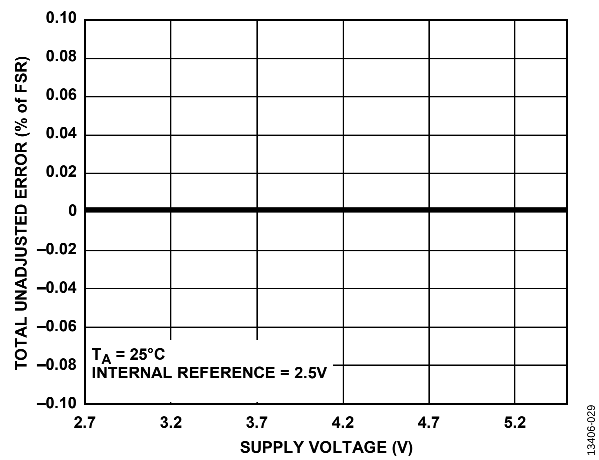

Figure 24. Total Unadjusted Error (TUE) vs. Supply Voltage, Gain = 1

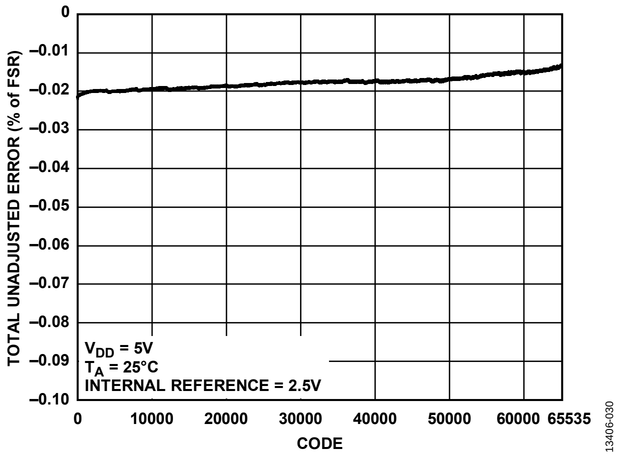

Figure 25. Total Unadjusted Error (TUE) vs. Code

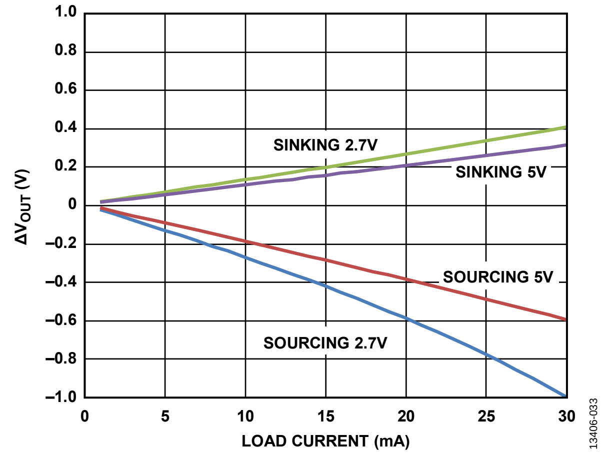

Figure 28. Headroom/Footroom vs. Load Current

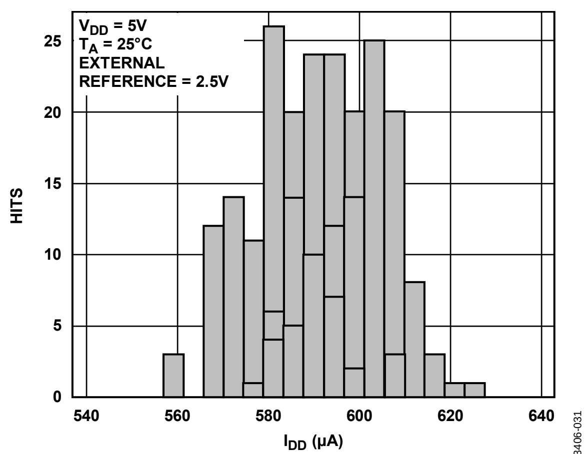

Figure 26. I_{DD} Histogram with External Reference, V_{DD} = 5 V

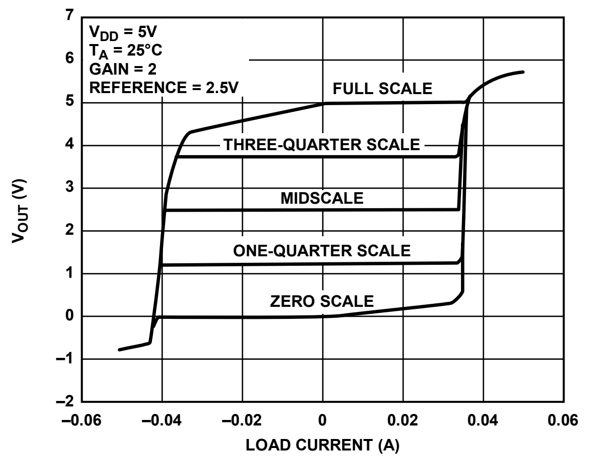

Figure 29. Source and Sink Capability at 5 V, Gain = 2

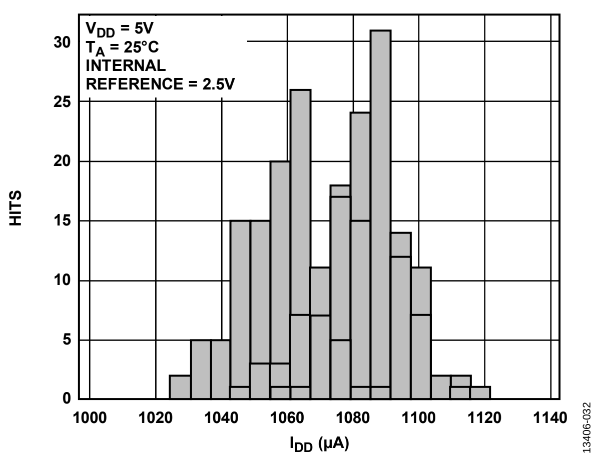

Figure 27. I_{DD} Histogram with Internal Reference, V_{REF} = 2.5 V, Gain = 2

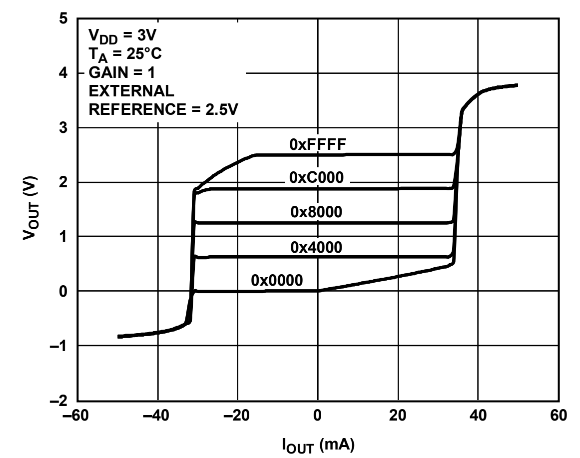

Figure 30. Source and Sink Capability at 3 V, Gain = 1

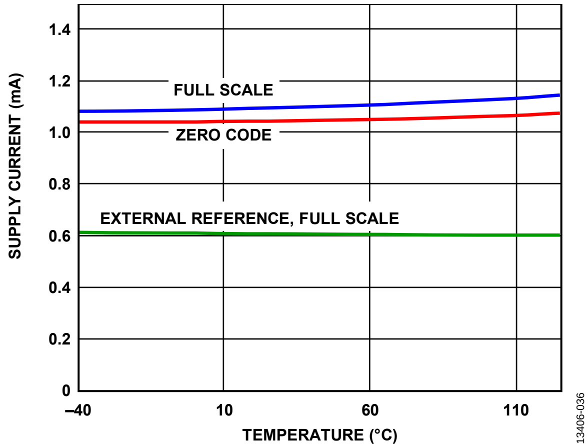

Figure 31. Supply Current vs. Temperature

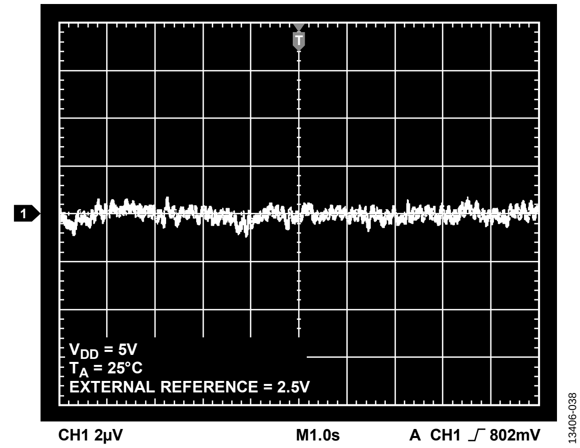

Figure 33. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V External Reference

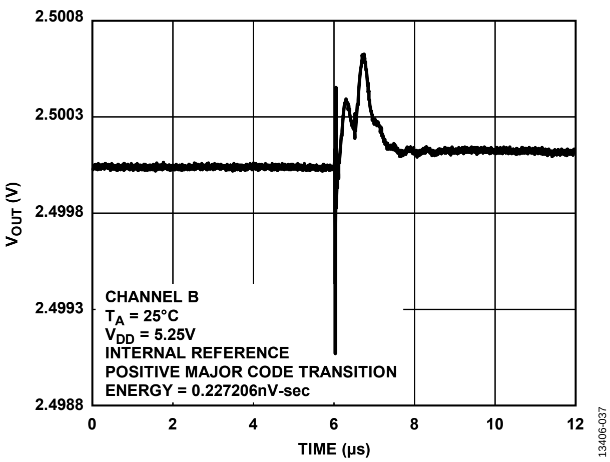

Figure 32. Digital-to-Analog Glitch Impulse

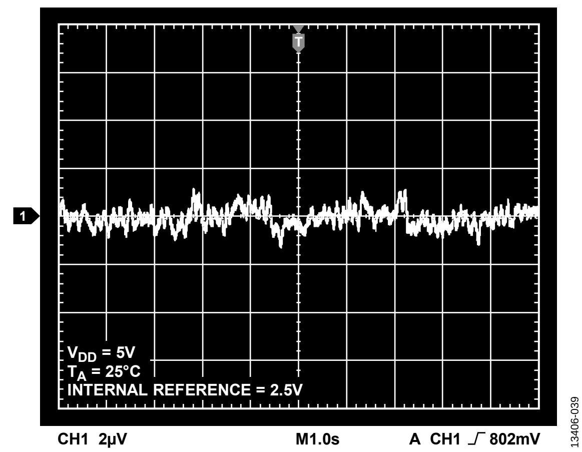

Figure 34. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V Internal Reference

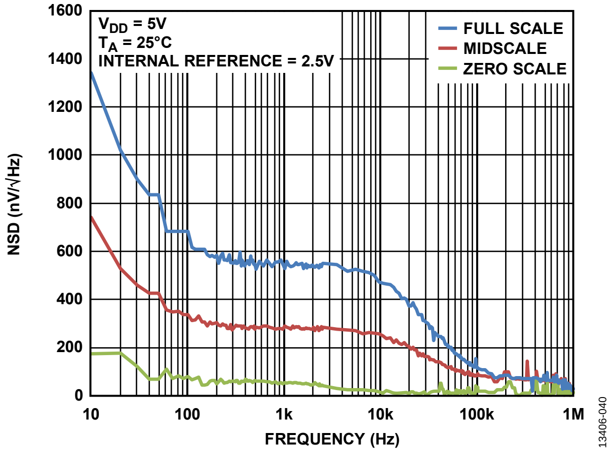

Figure 35. Noise Spectral Density (NSD) vs. Frequency

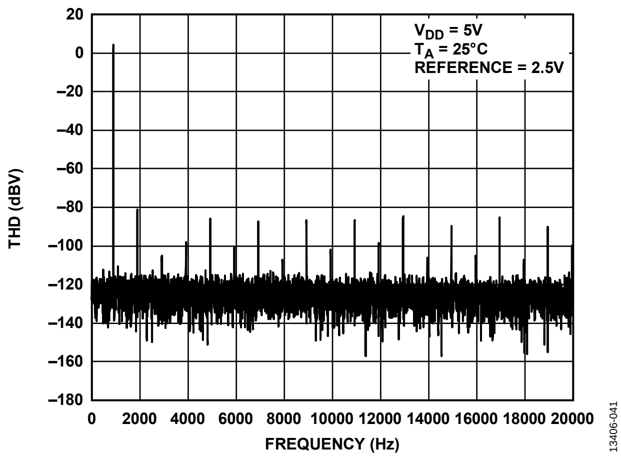

Figure 36. Total Harmonic Distortion at 1 kHz vs. Frequency

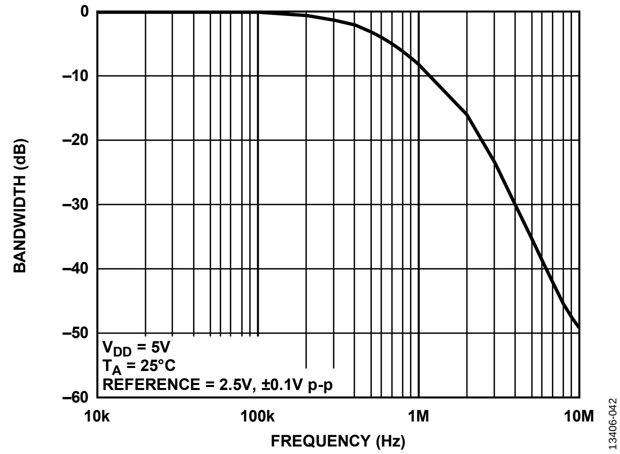

Figure 37. Multiplying Bandwidth, External Reference = 2.5 V, ±0.1 V p-p, 10 kHz to 10 MHz

OUTLINE DIMENSIONS

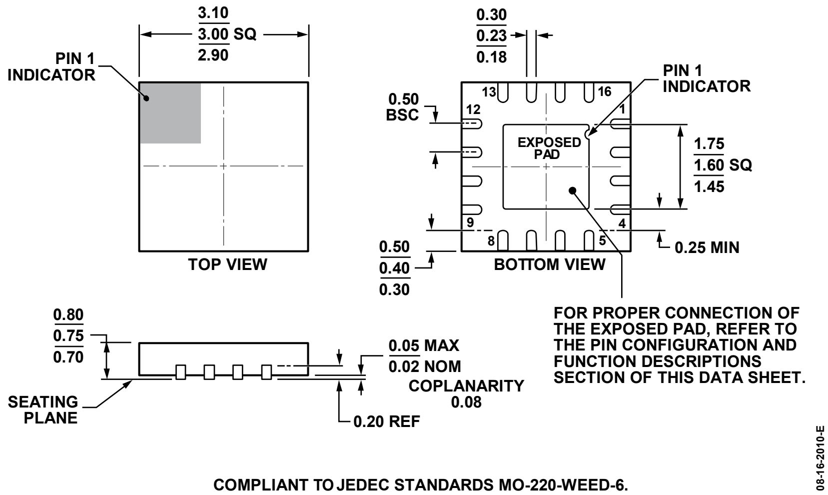

Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution	Temperature Range	Package Description	Package Option
AD5689RTCPZ-EP-RL7	16 Bits	−55°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22

[1] Z = RoHS Compliant Part.