



**THE DATASHEET OF  
IRF9395MTRPBF**



### DirectFET™ dual P-Channel Power MOSFET ②

Typical values (unless otherwise specified)

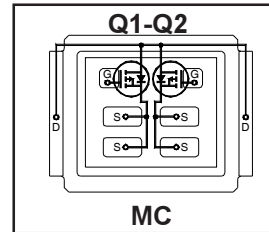
$V_{DSS}$	$V_{GS}$	$R_{DS(on)}$	$R_{DS(on)}$		
-30V max	±20V max	5.3mΩ@-10V	9.0mΩ@-4.5V		
$Q_{g\ tot}$	$Q_{gd}$	$Q_{gs2}$	$Q_{rr}$	$Q_{oss}$	$V_{gs(th)}$
32nC	15nC	3.2nC	62nC	23nC	-1.8V

#### Applications

- Isolation Switch for Input Power or Battery Application

#### Features and Benefits

- Environmentally Friendly Product
- RoHs Compliant Containing no Lead, no Bromide and no Halogen
- Dual Common-Drain P-Channel MOSFETs Provides High Level of Integration and Very Low RDS(on)



Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST		MQ	MX	MT	MP	<b>MC</b>		
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#### Description

The IRF9395MTRPbF combines the latest HEXFET® P-Channel Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.6 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRF9395MTRPbF	DirectFET Medium Can	Tape and Reel	4800	"TR" suffix
IRF9395MTR1PbF	DirectFET Medium Can	Tape and Reel	4000	"TR1" suffix EOL notice # 264

#### Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	-30	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	-14	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	-11	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ④	-75	
$I_{DM}$	Pulsed Drain Current ⑤	-110	

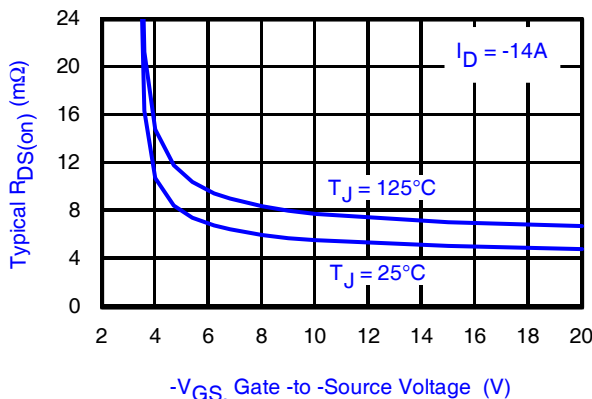


Fig 1. Typical On-Resistance vs. Gate Voltage

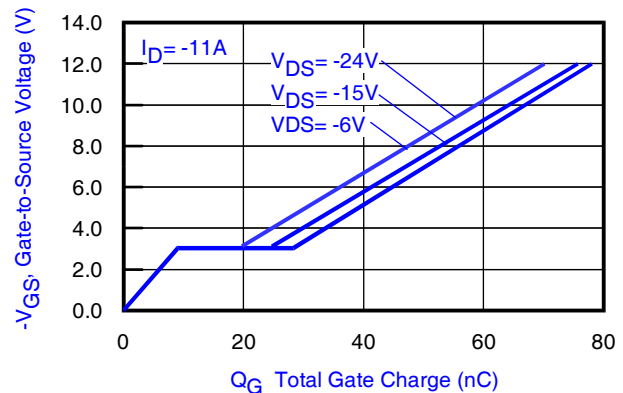


Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

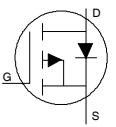
#### Notes:

- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.
- ④  $T_C$  measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.012	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	5.3	7.0	mΩ	V <sub>GS</sub> = -10V, I <sub>D</sub> = -14A ⑥
		—	9.0	11.9		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -11 A ⑥
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.3	-1.8	-2.4	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -50μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-6.1	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-1.0	μA	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V
		—	—	-150		V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	-100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V <sub>GS</sub> = 20V
g <sub>fs</sub>	Forward Transconductance	40	—	—	S	V <sub>DS</sub> = -15V, I <sub>D</sub> = -11A
Q <sub>g</sub>	Total Gate Charge	—	64	—	nC	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -10V, I <sub>D</sub> = -11A
Q <sub>g</sub>	Total Gate Charge	—	32	—		V <sub>DS</sub> = -15V V <sub>GS</sub> = -4.5V I <sub>D</sub> = -11A See Fig.15
Q <sub>gs1</sub>	Pre- V <sub>th</sub> Gate-to-Source Charge	—	6.5	—		
Q <sub>gs2</sub>	Post -V <sub>th</sub> Gate-to-Source Charge	—	3.2	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	15	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	7.3	—		
Q <sub>sw</sub>	Switch charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	18.2	—		
Q <sub>oss</sub>	Output Charge	—	23	—	nC	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V
R <sub>G</sub>	Gate Resistance	—	15	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	16	—	ns	V <sub>DD</sub> = -15V, V <sub>GS</sub> = -4.5V ⑥
t <sub>r</sub>	Rise Time	—	142	—		I <sub>D</sub> = -11A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	76	—		R <sub>G</sub> = 1.8Ω
t <sub>f</sub>	Fall Time	—	121	—		See Fig.17
C <sub>iss</sub>	Input Capacitance	—	3241	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	820	—		V <sub>DS</sub> = -15V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	466	—		f = 1.0KHz

**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-57	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ⑤	—	—	-110		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -11A, V <sub>GS</sub> = 0V ⑥
t <sub>rr</sub>	Reverse Recovery Time	—	43	65	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -11A, V <sub>DD</sub> = -15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	62	93	nC	di/dt = 260A/μs ⑥

**Notes:**

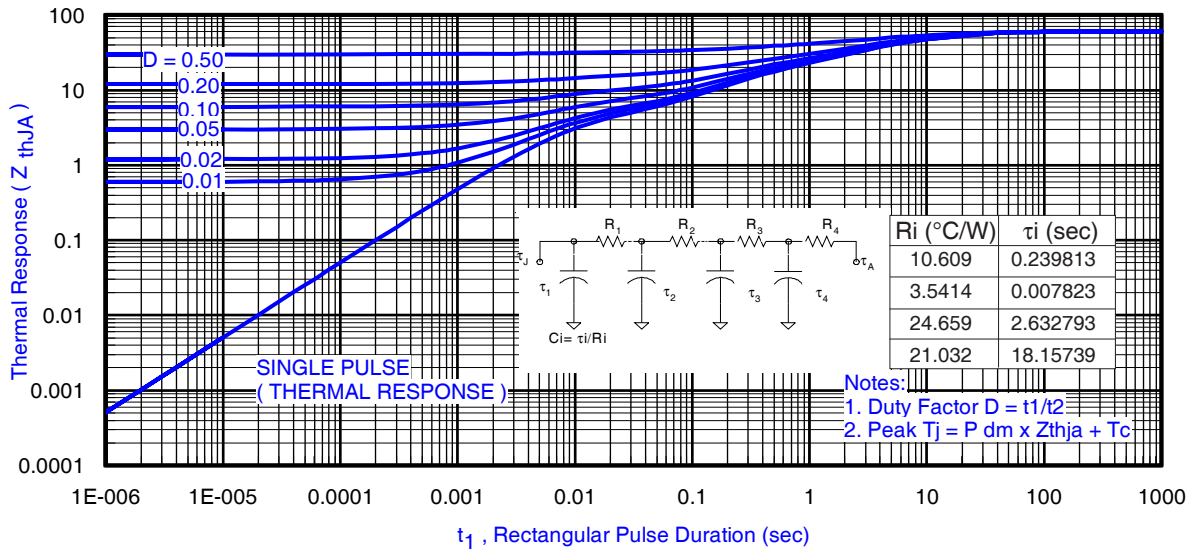
⑥ Pulse width ≤ 400μs; duty cycle ≤ 2%.

**Absolute Maximum Ratings**

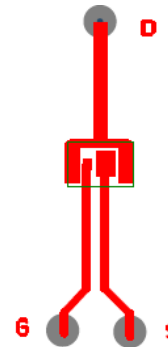
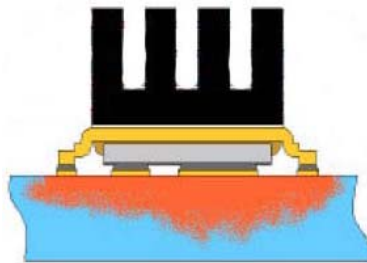
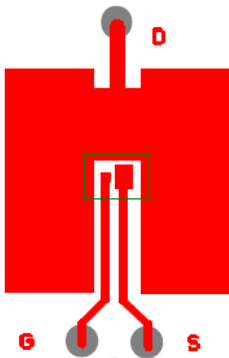
	Parameter	Max.	Units
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③	2.1	W
$P_D @ T_A = 70^\circ\text{C}$	Power Dissipation ③	1.3	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	57	
$T_P$	Peak Soldering Temperature	270	°C
$T_J$	Operating Junction and	-40 to + 150	
$T_{STG}$	Storage Temperature Range		

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③	—	60	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑦	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑧	20	—	
$R_{\theta JC}$	Junction-to-Case ④,⑨	—	2.2	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted	1.0	—	
	Linear Derating Factor ③	0.02		W/°C


**Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ①**
**Notes:**

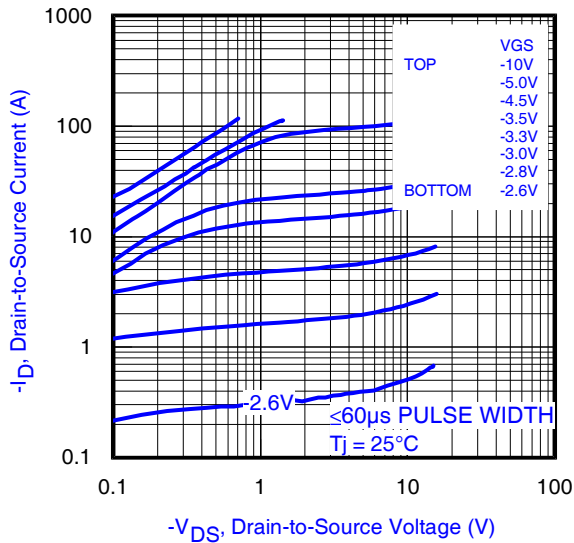
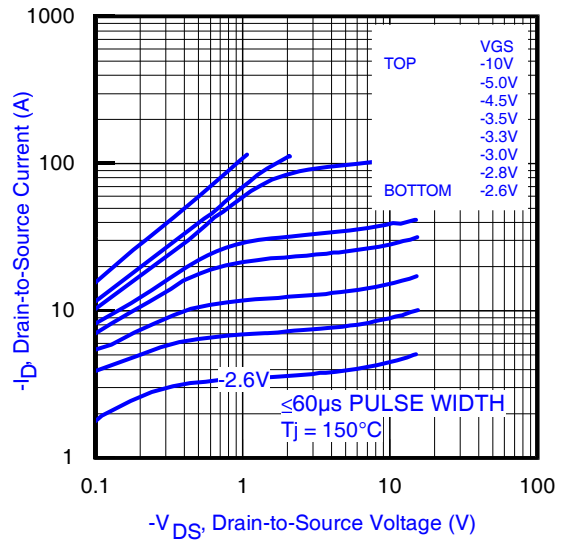
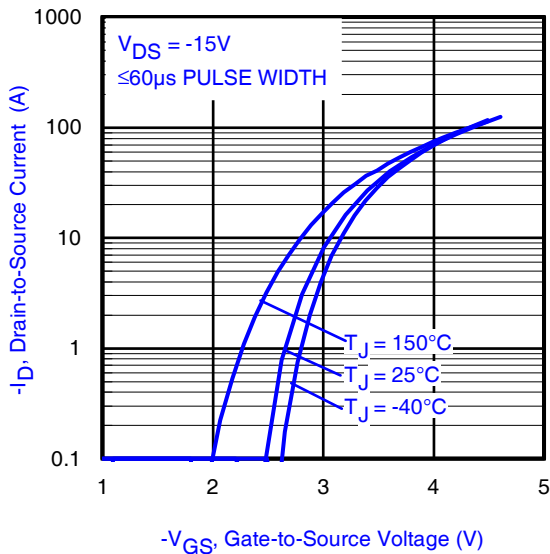
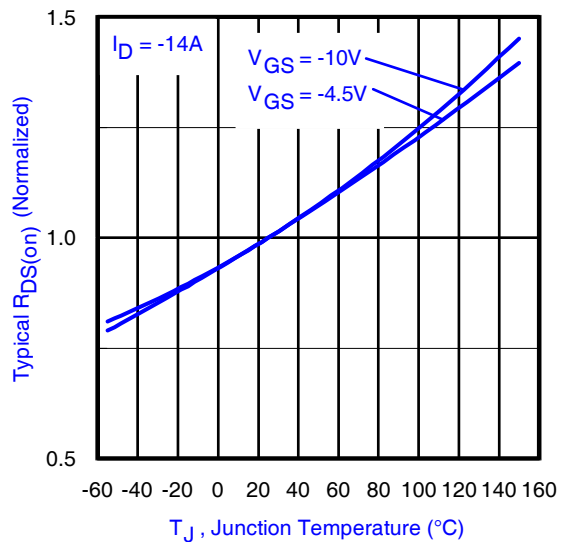
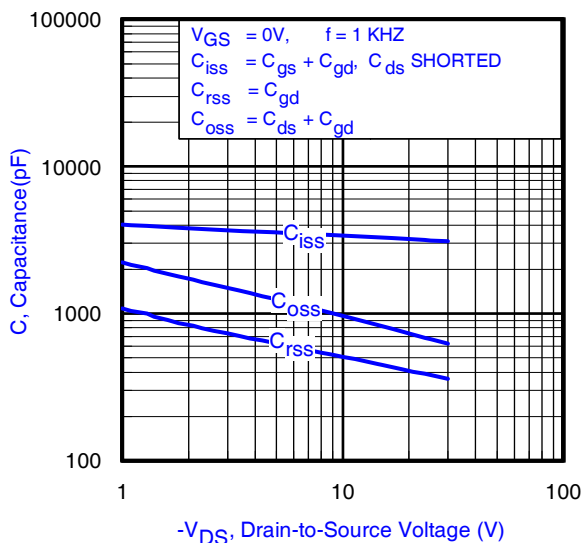
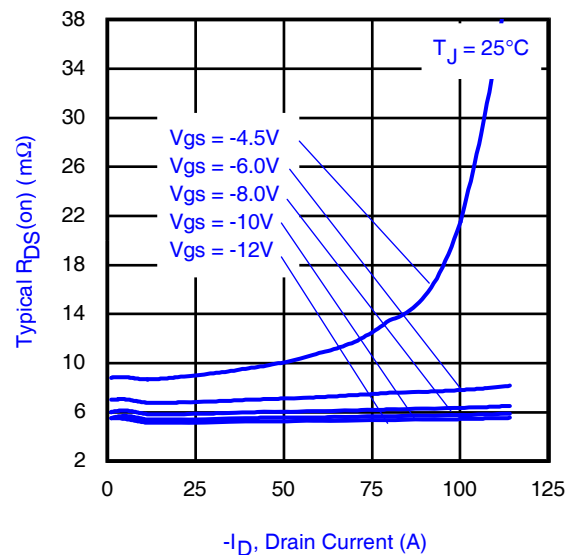
- ⑦ Used double sided cooling, mounting pad with large heatsink.
- ⑧ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ⑨  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .

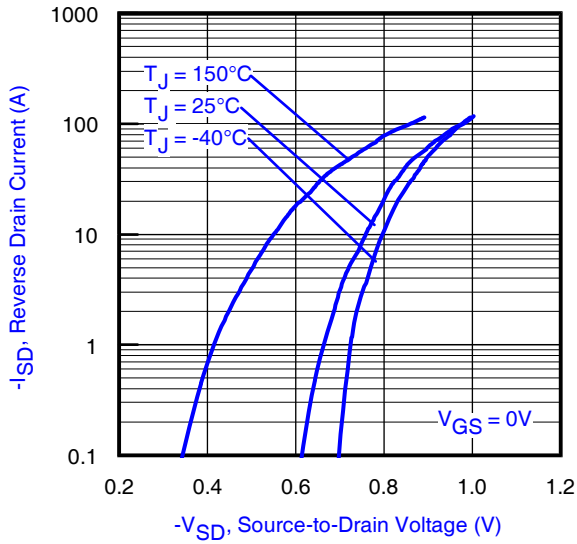
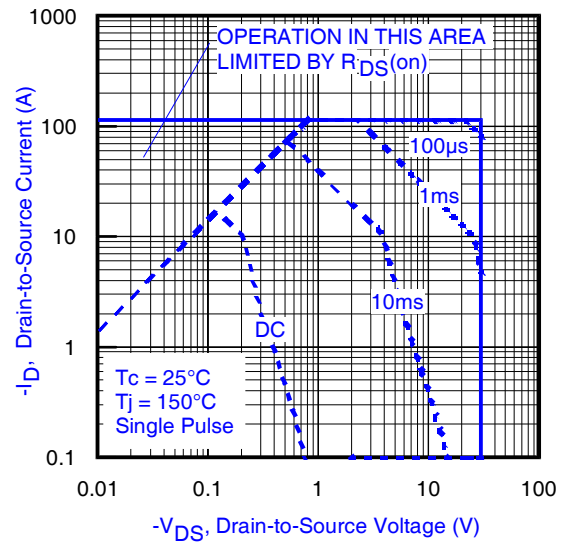
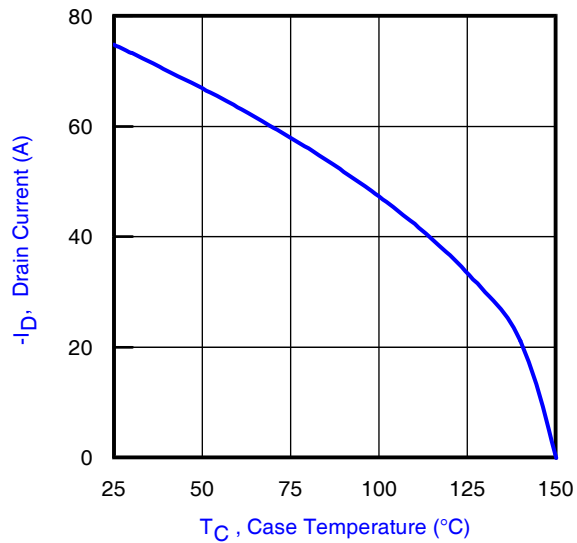
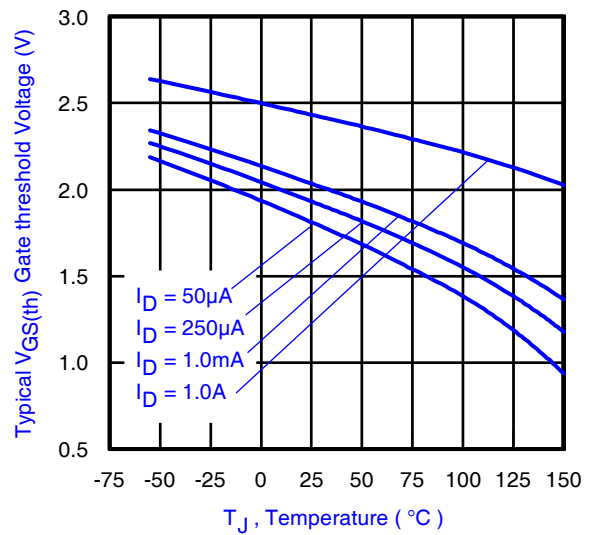
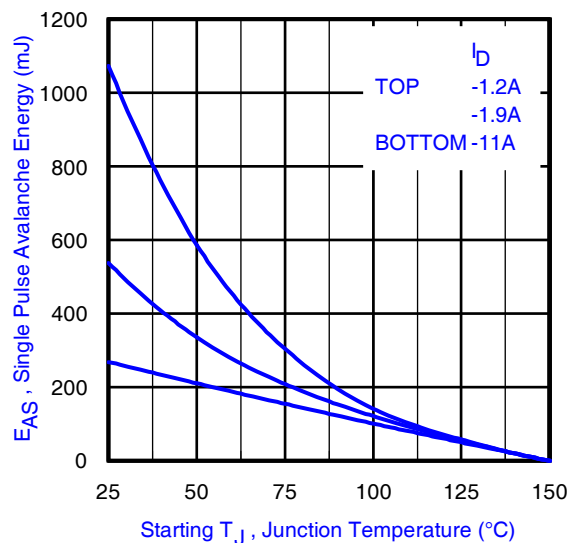


③ Surface mounted on 1 in. square Cu board (still air).

⑧ Mounted to a PCB with small clip heatsink (still air)

⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)


**Fig 4.** Typical Output Characteristics

**Fig 5.** Typical Output Characteristics

**Fig 6.** Typical Transfer Characteristics

**Fig 7.** Normalized On-Resistance vs. Temperature

**Fig 8.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig 9.** Typical On-Resistance vs. Drain Current and Gate Voltage


**Fig 10.** Typical Source-Drain Diode Forward Voltage

**Fig 11.** Maximum Safe Operating Area

**Fig 12.** Maximum Drain Current vs. Case Temperature

**Fig 13.** Typical Threshold Voltage vs. Junction Temperature

**Fig 14.** Maximum Avalanche Energy vs. Drain Current

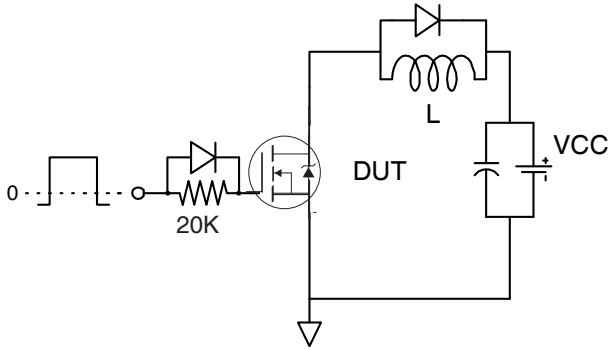


Fig 15a. Gate Charge Test Circuit

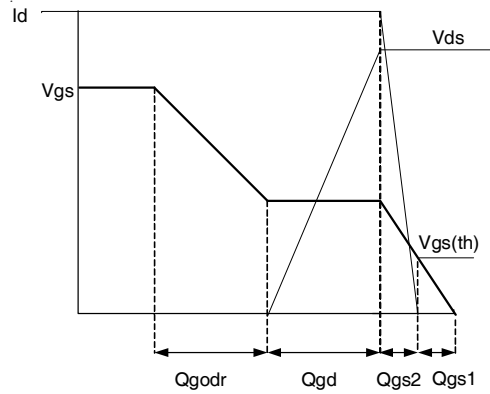


Fig 15b. Gate Charge Waveform

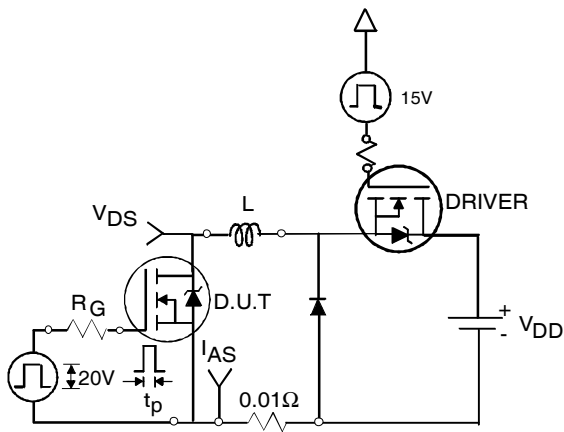


Fig 16a. Unclamped Inductive Test Circuit

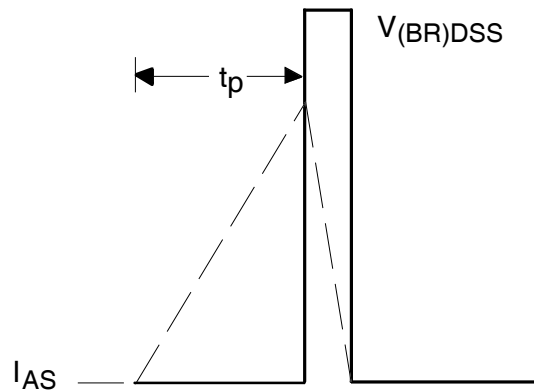


Fig 16b. Unclamped Inductive Waveforms

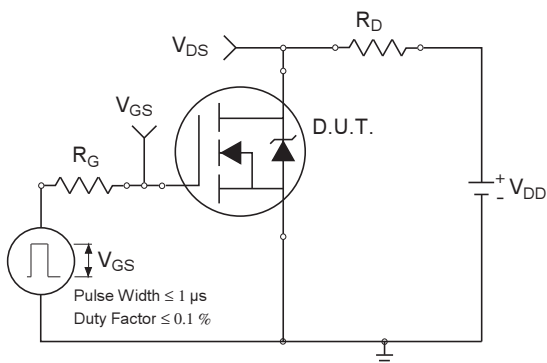


Fig 17a. Switching Time Test Circuit

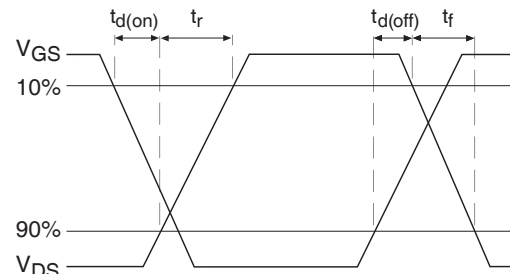
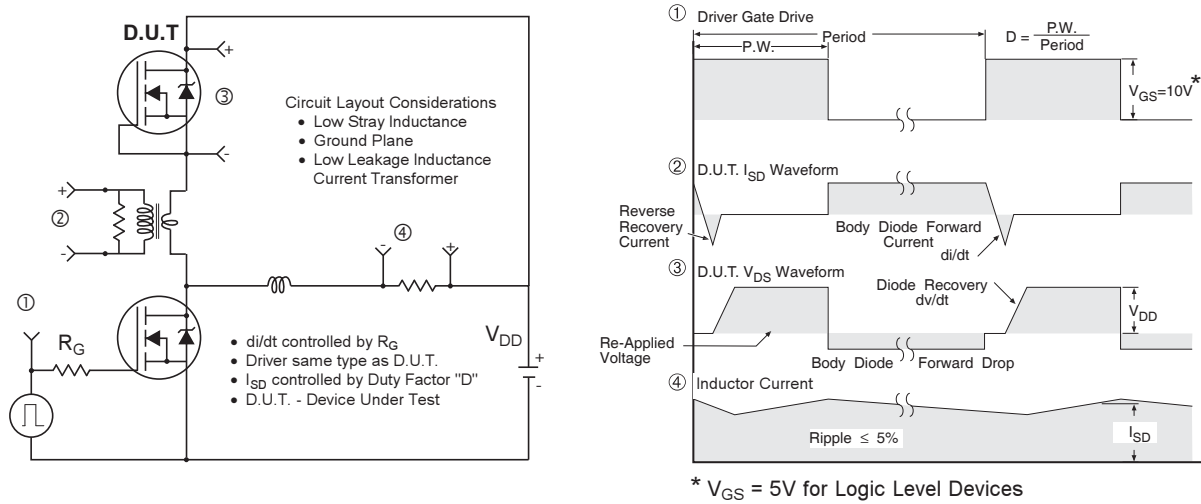


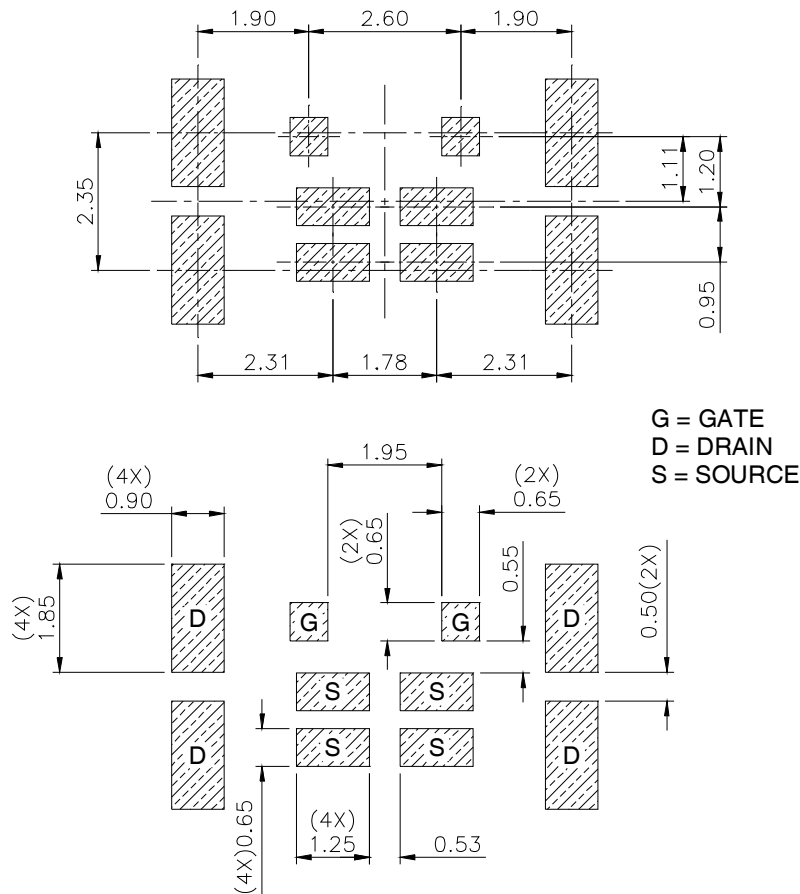
Fig 17b. Switching Time Waveforms



**Fig 18. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs**

**DirectFET™ Board Footprint, MC Outline (Medium Size Can, C-Designation).**

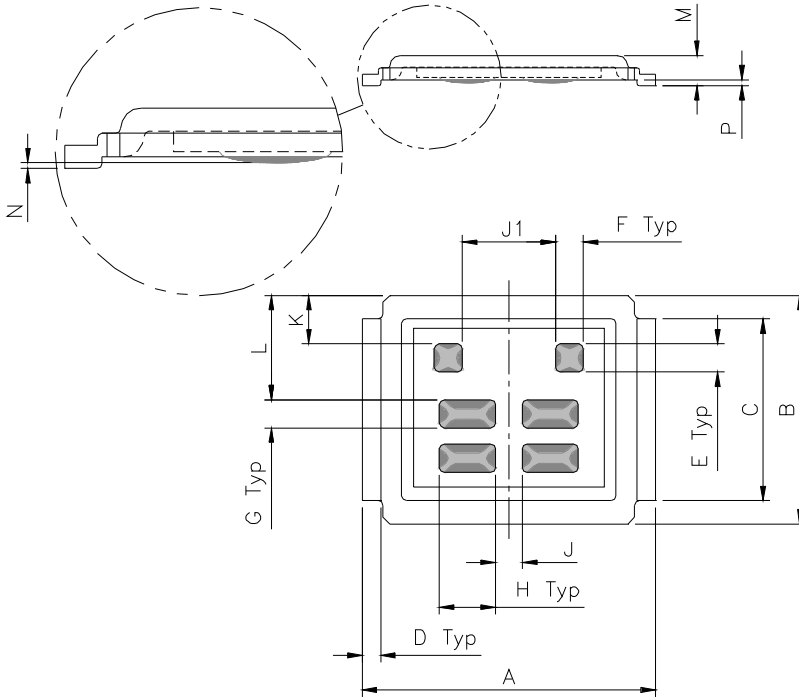
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

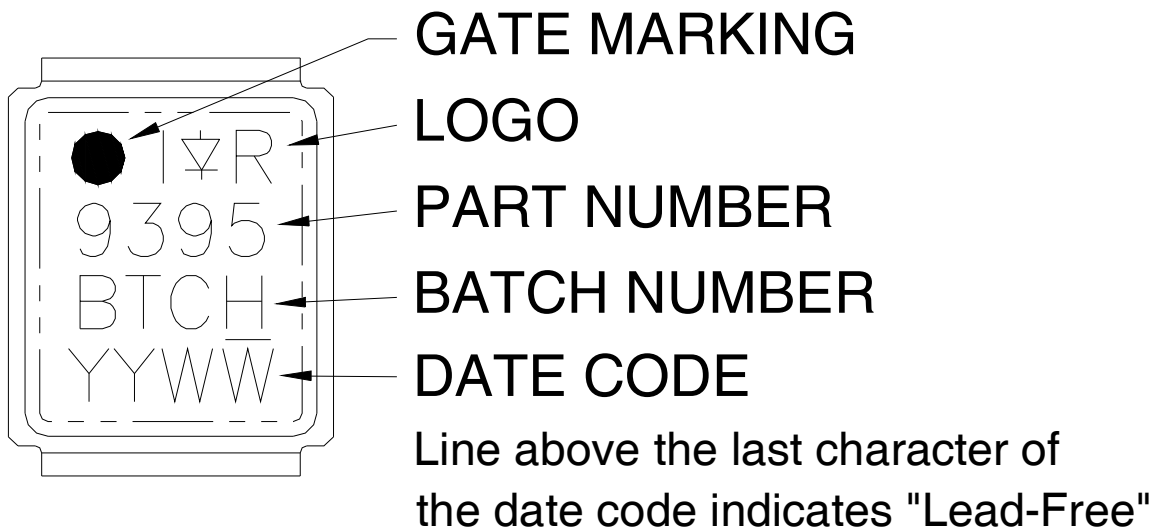
**DirectFET™ Outline Dimension, MC Outline  
(Medium Size Can, C-Designation).**

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.

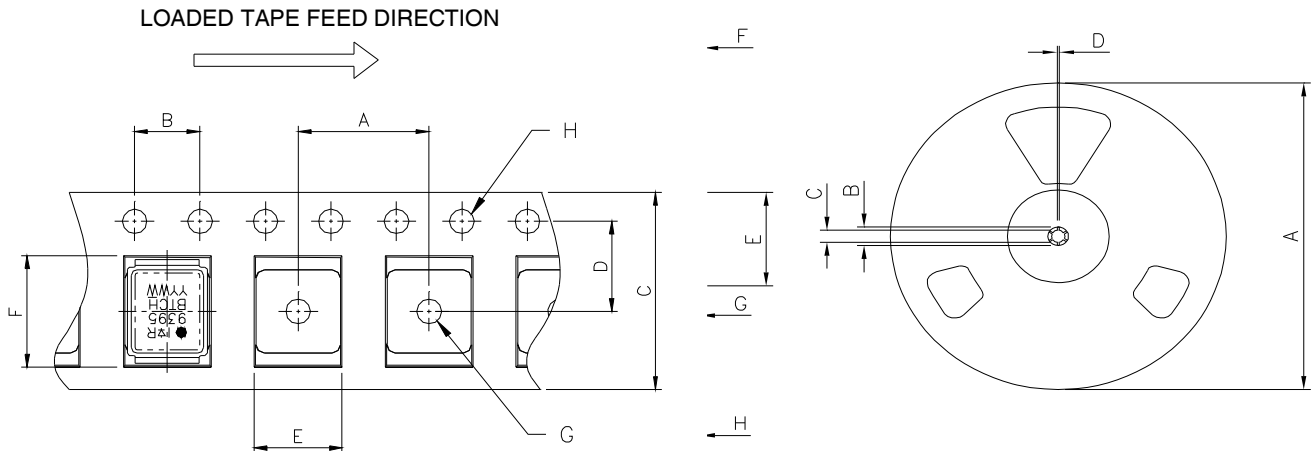


CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.201
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.58	0.62	0.023	0.024
F	0.58	0.62	0.023	0.024
G	0.58	0.62	0.023	0.024
H	1.18	1.22	0.047	0.048
J	0.56	0.60	0.022	0.023
J1	1.98	2.02	0.078	0.079
K	1.02	1.06	0.040	0.041
L	2.22	2.26	0.088	0.089
M	0.59	0.70	0.023	0.028
N	0.03	0.08	0.001	0.003
P	0.08	0.17	0.003	0.007

**DirectFET™ Part Marking**



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**DirectFET™ Tape & Reel Dimension (Showing component orientation).**


NOTE: CONTROLLING DIMENSIONS IN MM

CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

NOTE: Controlling dimensions in mm  
Std reel quantity is 4800 parts (ordered as IRF9395MTRPBF).

REEL DIMENSIONS				
STANDARD OPTION (QTY 4800)				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C
B	20.2	N.C	0.795	N.C
C	12.8	13.2	0.504	0.520
D	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C
F	N.C	18.4	N.C	0.724
G	12.4	14.4	0.488	0.567
H	11.9	15.4	0.469	0.606

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**Qualification Information†**

Qualification level	Industrial† (per JEDEC JESD47F†† guidelines)	
Moisture Sensitivity Level	DirectFET	MSL1 (per JEDEC J-STD-020D††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
10/25/2013	<ul style="list-style-type: none"> <li>Updated Qualification level from "Consumer" to "Industrial" on page 9</li> <li>Updated data sheet with new IR corporate template</li> </ul>
2/24/2014	<ul style="list-style-type: none"> <li>Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #264)</li> </ul>

## Looking for pricing, stock, or lifecycle information?

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 [Infineon Technologies](#) Information

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