

Applications

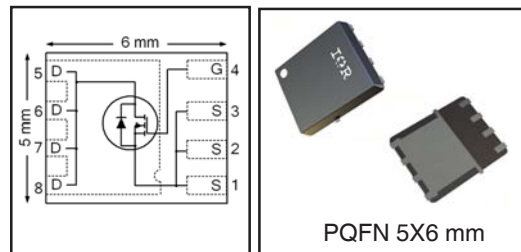
- Control MOSFET of Sync-Buck Converters used for Notebook Processor Power
- Control MOSFET for Isolated DC-DC Converters in Networking Systems

HEXFET® Power MOSFET

V_{DS}	$R_{DS(on)}$ max	Q_g
30V	8.7mΩ @ $V_{GS} = 10V$	8.3nC

Benefits

- Very low $R_{DS(ON)}$ at 4.5V V_{GS}
- Low Gate Charge
- Fully Characterized Avalanche Voltage and Current
- 100% Tested for R_G
- Lead-Free (Qualified up to 260°C Reflow)
- RoHS compliant (Halogen Free)
- Low Thermal Resistance
- Large Source Lead for more reliable Soldering



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	15	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	12	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	35	
I_{DM}	Pulsed Drain Current ①	110	
$P_D @ T_A = 25^\circ C$	Power Dissipation ⑤	3.1	W
$P_D @ T_A = 70^\circ C$	Power Dissipation ⑤	2.0	
	Linear Derating Factor ⑤	0.025	W/°C
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	7.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	40	

Notes ① through ⑤ are on page 9

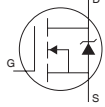
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.022	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	7.5	8.7	mΩ	V _{GS} = 10V, I _D = 14A ③
		—	11.2	13		V _{GS} = 4.5V, I _D = 11A ③
V _{GS(th)}	Gate Threshold Voltage	1.35	1.8	2.35	V	V _{DS} = V _{GS} , I _D = 25μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-6.08	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
g _{fs}	Forward Transconductance	77	—	—	S	V _{DS} = 15V, I _D = 11A
Q _g	Total Gate Charge	—	8.3	12	nC	V _{DS} = 15V V _{GS} = 4.5V I _D = 11A See Fig.17 & 18
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	—	2.1	—		
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	—	1.0	—		
Q _{gd}	Gate-to-Drain Charge	—	2.8	—		
Q _{godr}	Gate Charge Overdrive	—	2.4	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	3.8	—		
Q _{oss}	Output Charge	—	4.8	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	—	1.3	2.2	Ω	
t _{d(on)}	Turn-On Delay Time	—	11	—	ns	V _{DD} = 15V, V _{GS} = 4.5V I _D = 11A R _G = 1.8Ω See Fig.15
t _r	Rise Time	—	11	—		
t _{d(off)}	Turn-Off Delay Time	—	12	—		
t _f	Fall Time	—	4.6	—		
C _{iss}	Input Capacitance	—	1160	—	pF	V _{GS} = 0V V _{DS} = 15V f = 1.0MHz
C _{oss}	Output Capacitance	—	220	—		
C _{rss}	Reverse Transfer Capacitance	—	100	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	17	mJ
I _{AR}	Avalanche Current ①	—	11	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	3.9	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	110		
V _{SD}	Diode Forward Voltage	—	—	1.0	V	T _J = 25°C, I _S = 11A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	14	21	ns	T _J = 25°C, I _F = 11A, V _{DD} = 15V
Q _{rr}	Reverse Recovery Charge	—	9.5	14	nC	di/dt = 200A/μs ③
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

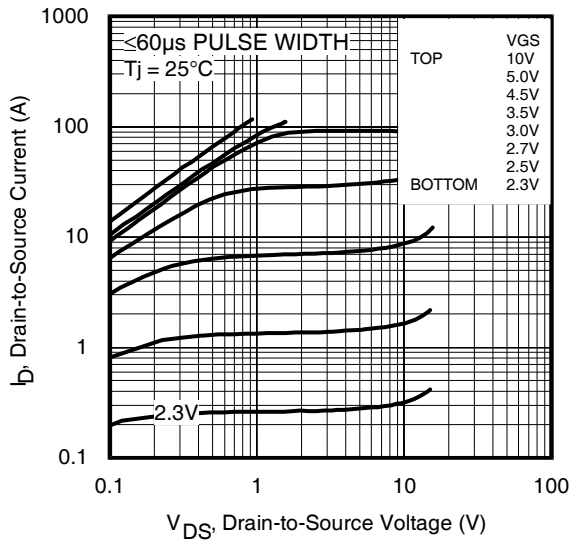


Fig 1. Typical Output Characteristics

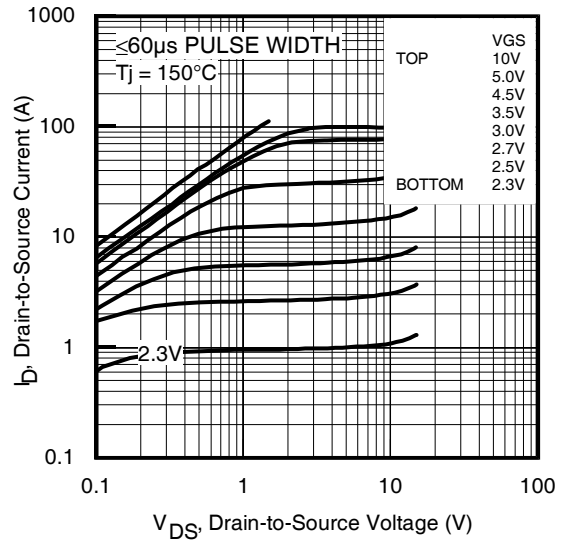


Fig 2. Typical Output Characteristics

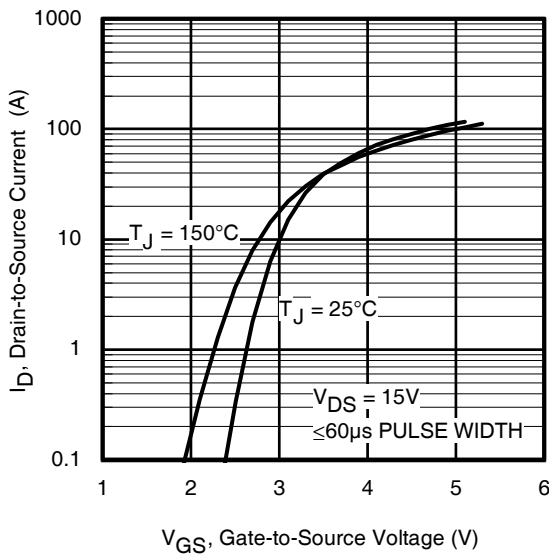


Fig 3. Typical Transfer Characteristics

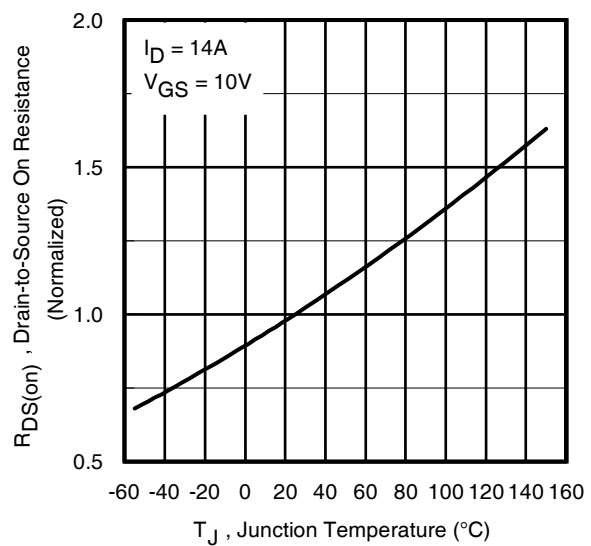


Fig 4. Normalized On-Resistance vs. Temperature

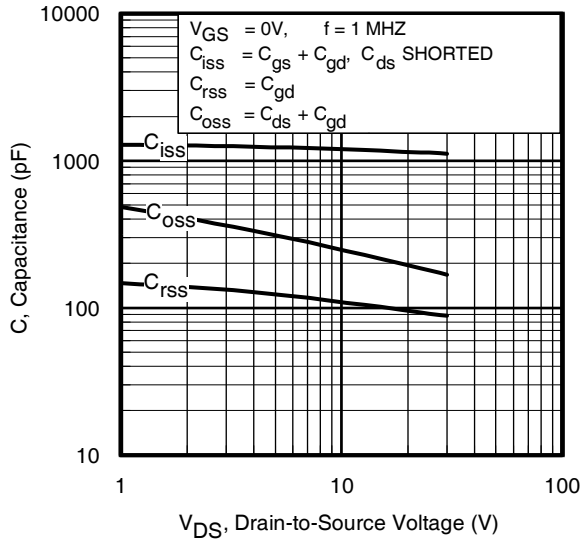


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

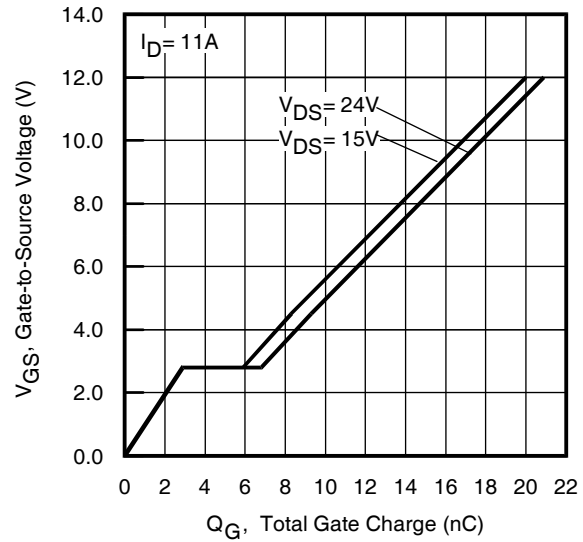


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

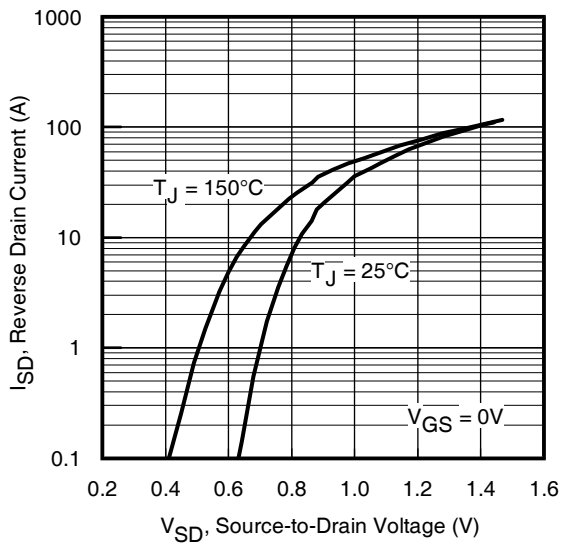


Fig 7. Typical Source-Drain Diode Forward Voltage

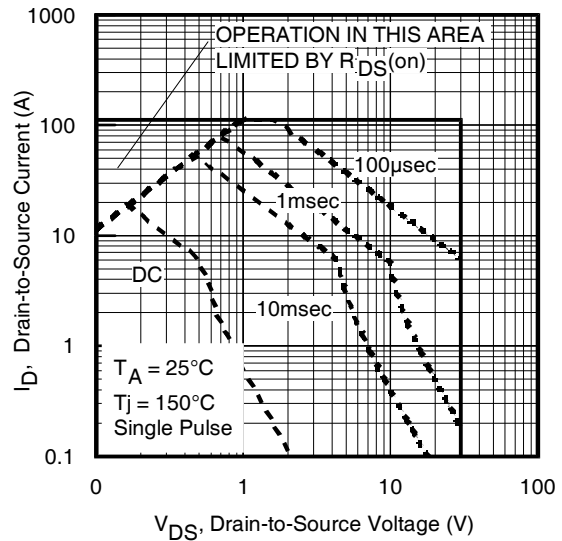
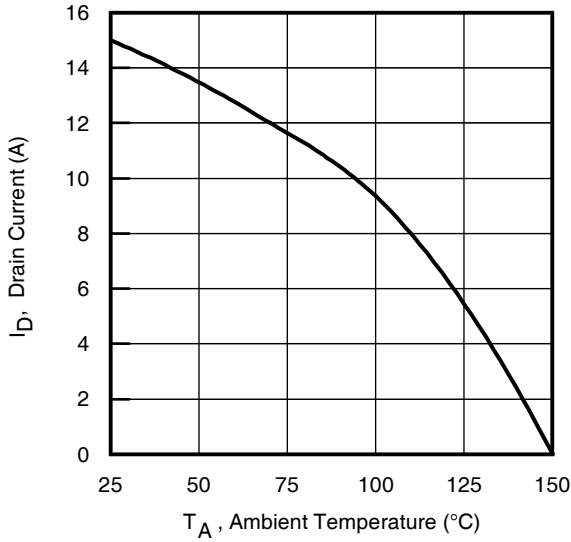
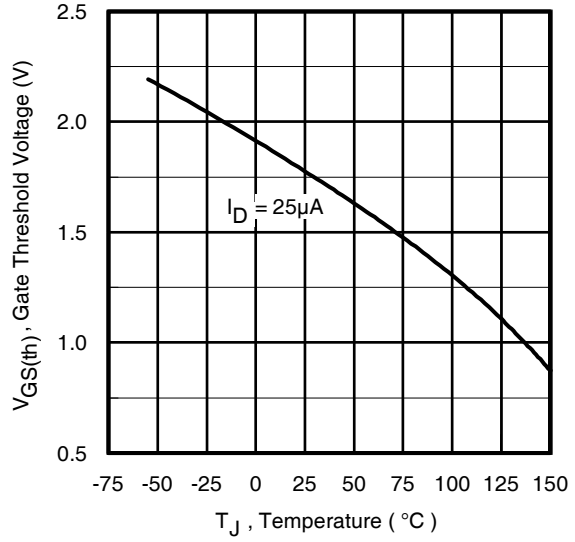
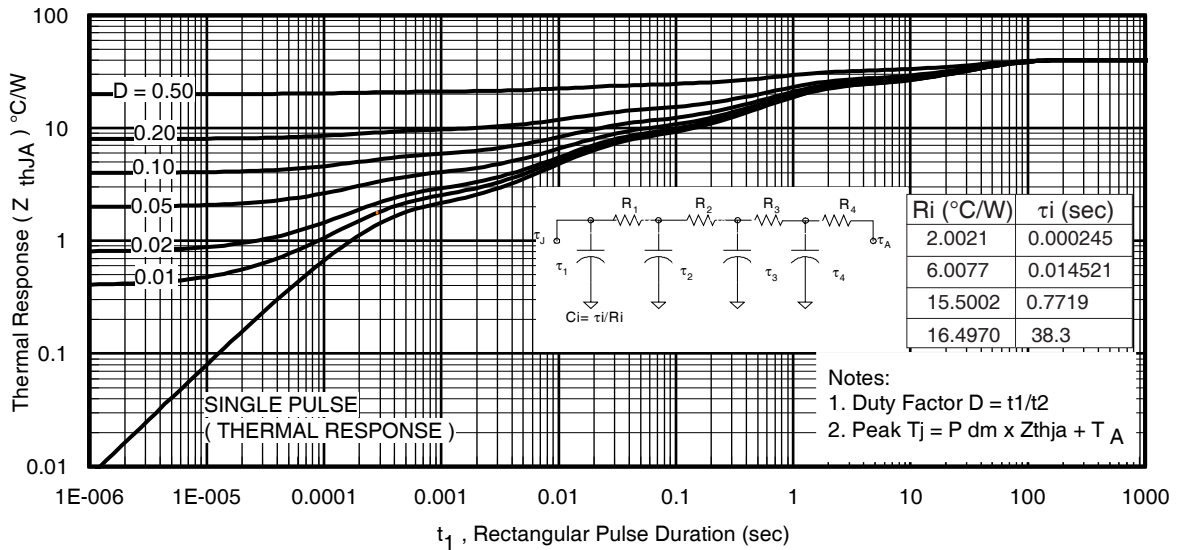
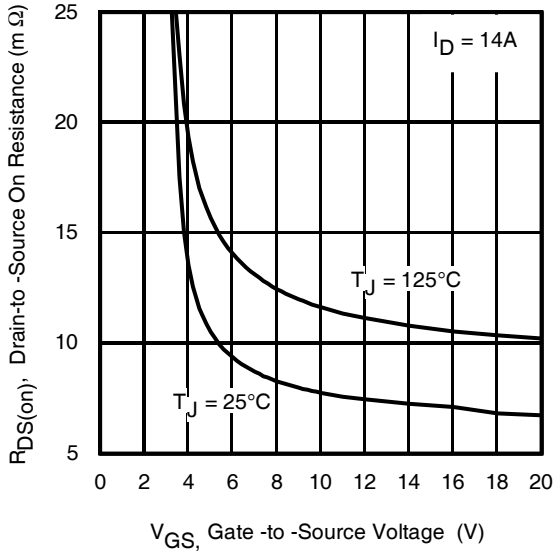
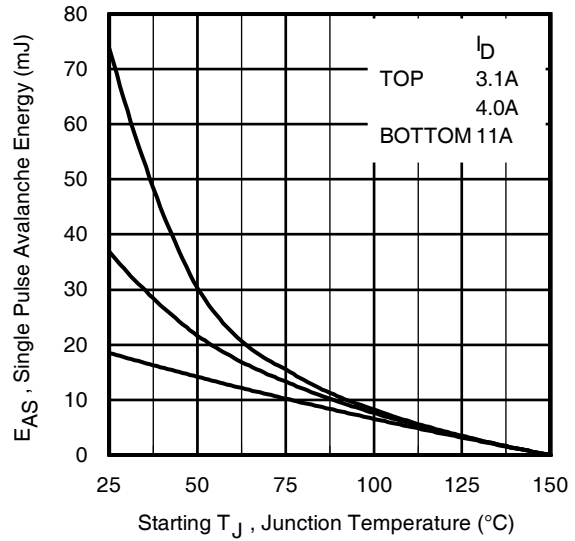
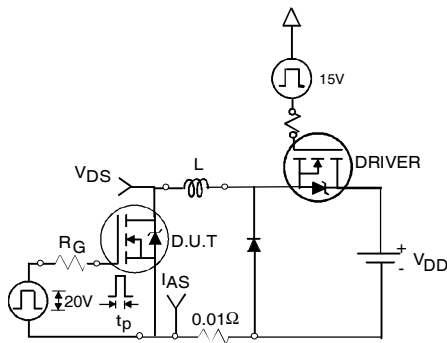
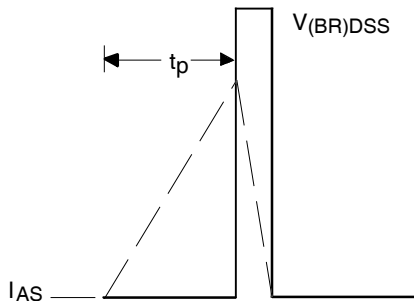
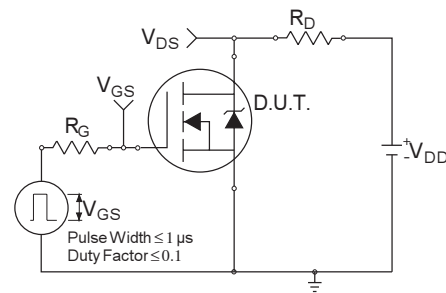
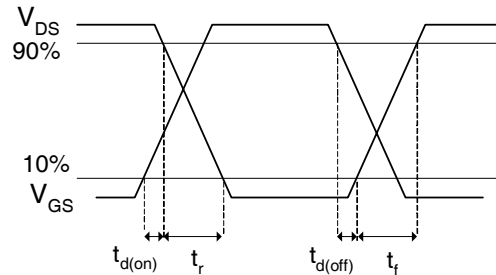


Fig 8. Maximum Safe Operating Area


Fig 9. Maximum Drain Current vs. Ambient Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient


Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14a. Unclamped Inductive Test Circuit

Fig 14b. Unclamped Inductive Waveforms

Fig 15a. Switching Time Test Circuit

Fig 15b. Switching Time Waveforms

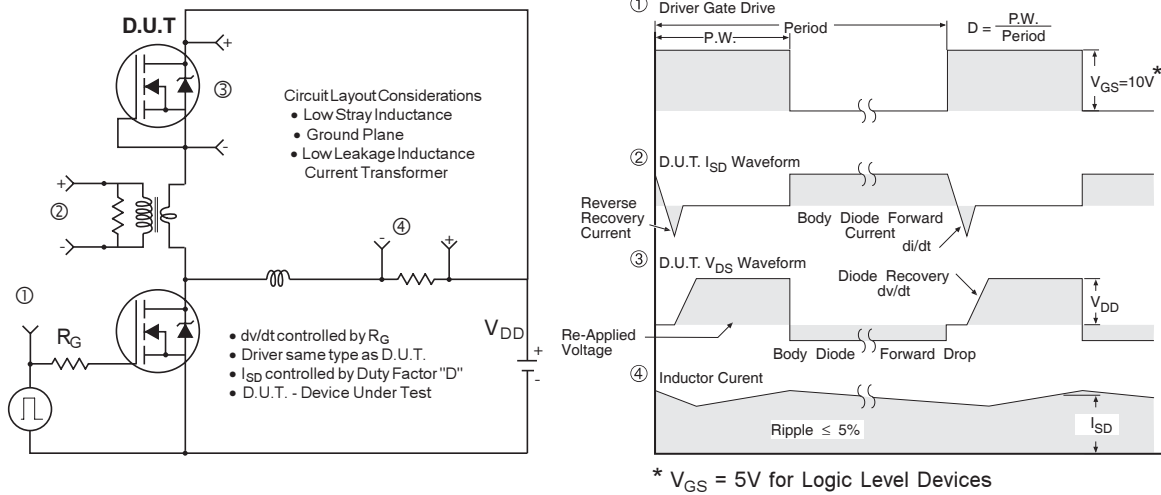


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

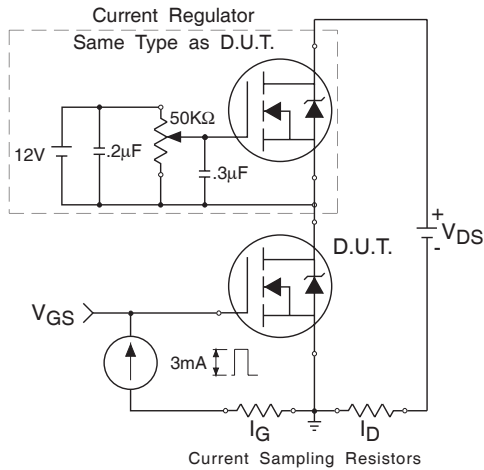


Fig 17. Gate Charge Test Circuit

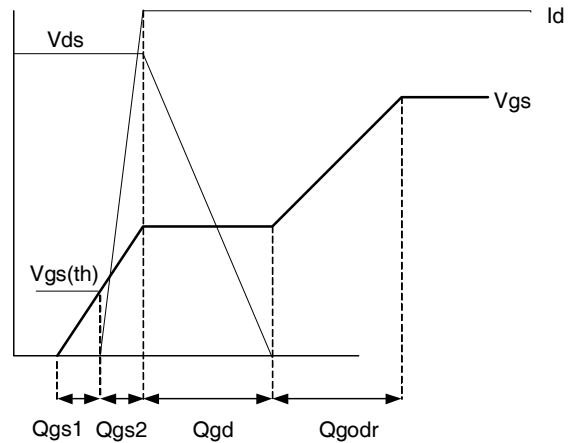
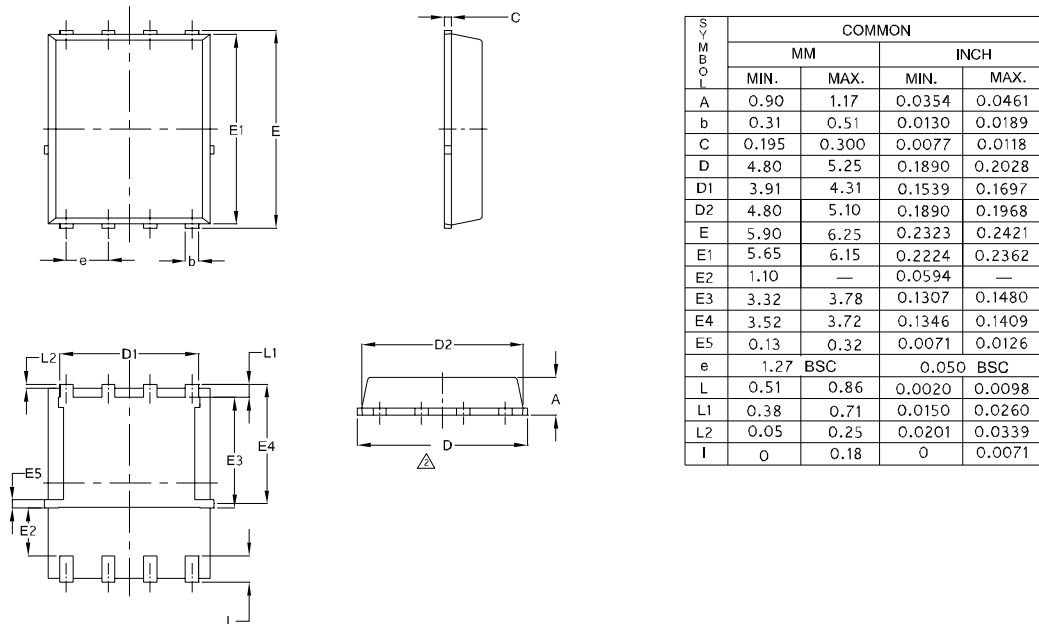
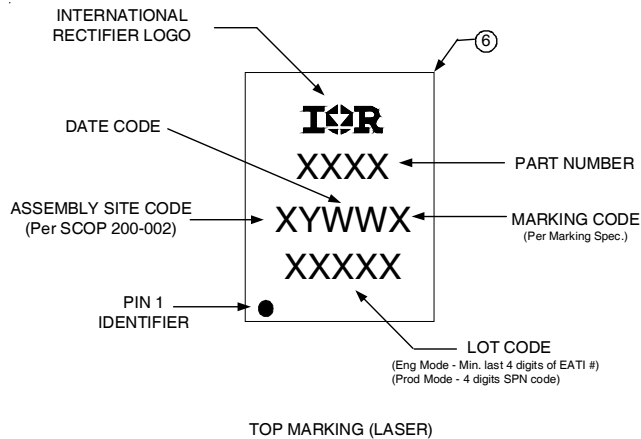


Fig 18. Gate Charge Waveform

PQFN 5x6 Option "E" Package Details

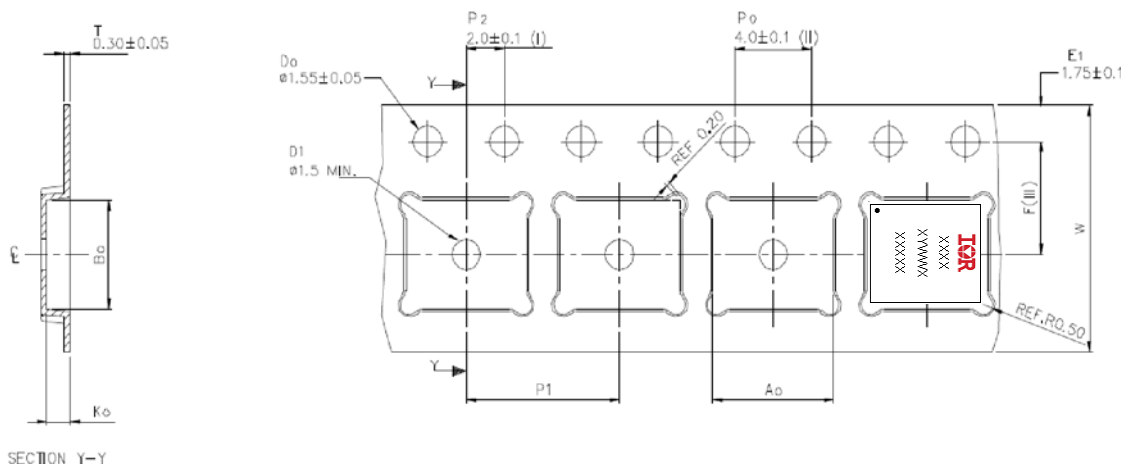


PQFN Part Marking



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

PQFN Tape and Reel



A ₀	6.30 +/− 0.1
B ₀	5.30 +/− 0.1
K ₀	1.20 +/− 0.1
F	5.50 +/− 0.1
P ₁	8.00 +/− 0.1
W	12.00 +/− 0.3

- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.
- (V) Typical SR of form tape Max 10⁹ OHM/SQ

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting T_J = 25°C, L = 0.27mH, R_G = 25Ω, I_{AS} = 11A.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ R_{thjc} is guaranteed by design
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.

Revision History

Date	Comments
08/08/2013	<ul style="list-style-type: none"> • Updated the package drawing, on page 1. • Updated the package outline drawing, on page 8. • This drawing change is related to PCN "Hana-GTBF-GEM 5x6 PQFN Public."

International
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