



THE DATASHEET OF IRFP4710



IRFP4710PbF

HEXFET® Power MOSFET

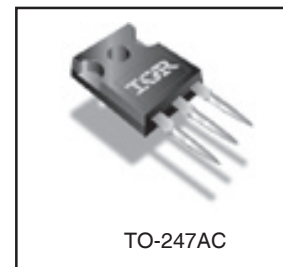
Applications

- High frequency DC-DC converters
- Motor Control
- Uninterruptible Power Supplies
- Lead-Free

V_{DSS}	R_{DS(on)} max	I_D
100V	0.014Ω	72A

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	72	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	51	
I _{DM}	Pulsed Drain Current ①	300	
P _D @ T _C = 25°C	Power Dissipation	190	W
	Linear Derating Factor	1.2	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	8.2	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.81	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface	0.24	—	
R _{θJA}	Junction-to-Ambient	—	40	

Notes ① through ③ are on page 8

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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	0.011	0.014	Ω	V _{GS} = 10V, I _D = 45A ④
V _{GS(th)}	Gate Threshold Voltage	3.5	—	5.5	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V _{DS} = 95V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V

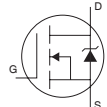
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	35	—	—	S	V _{DS} = 50V, I _D = 45A
Q _g	Total Gate Charge	—	110	170	nC	I _D = 45A
Q _{gs}	Gate-to-Source Charge	—	43	—		V _{DS} = 50V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	40	—		V _{GS} = 10V,
t _{d(on)}	Turn-On Delay Time	—	35	—	ns	V _{DD} = 50V
t _r	Rise Time	—	130	—		I _D = 45A
t _{d(off)}	Turn-Off Delay Time	—	41	—		R _G = 4.5Ω
t _f	Fall Time	—	38	—		V _{GS} = 10V ④
C _{iss}	Input Capacitance	—	6160	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	440	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	250	—		f = 1.0MHz
C _{oss}	Output Capacitance	—	1580	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	280	—		V _{GS} = 0V, V _{DS} = 80V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	430	—		V _{GS} = 0V, V _{DS} = 0V to 80V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	190	mJ
I _{AR}	Avalanche Current①	—	45	A
E _{AR}	Repetitive Avalanche Energy①	—	20	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	72	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	300		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 45A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	74	110	ns	T _J = 25°C, I _F = 45A
Q _{rr}	Reverse Recovery Charge	—	180	260	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

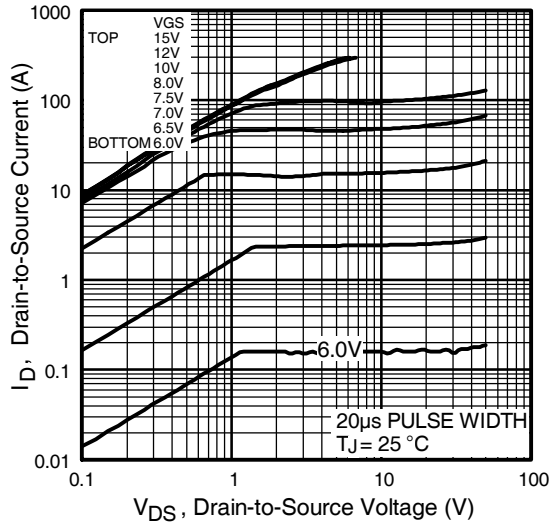


Fig 1. Typical Output Characteristics

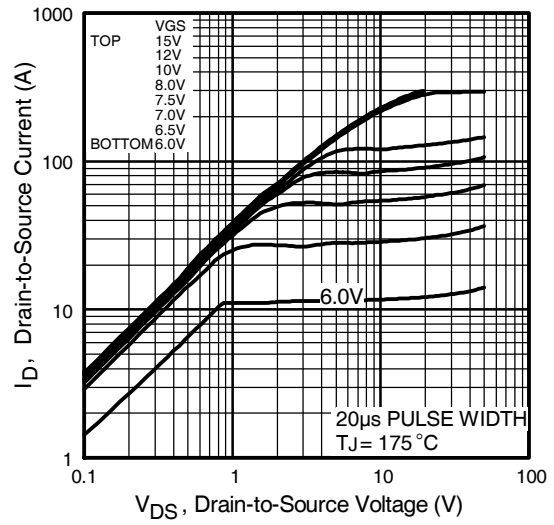


Fig 2. Typical Output Characteristics

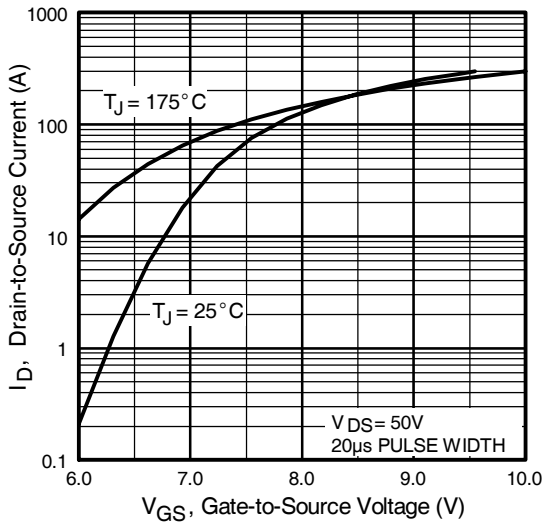


Fig 3. Typical Transfer Characteristics

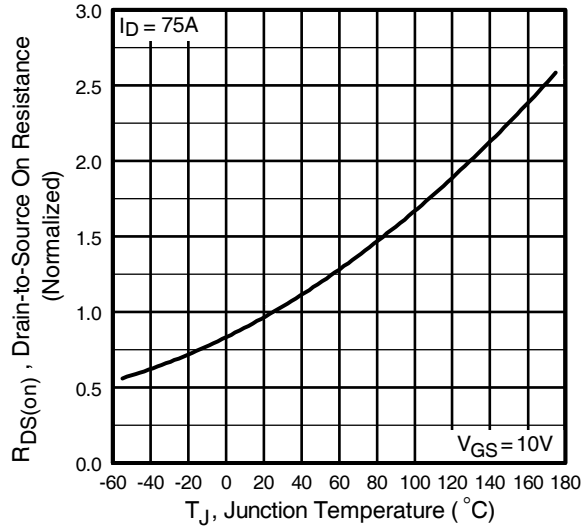


Fig 4. Normalized On-Resistance Vs. Temperature

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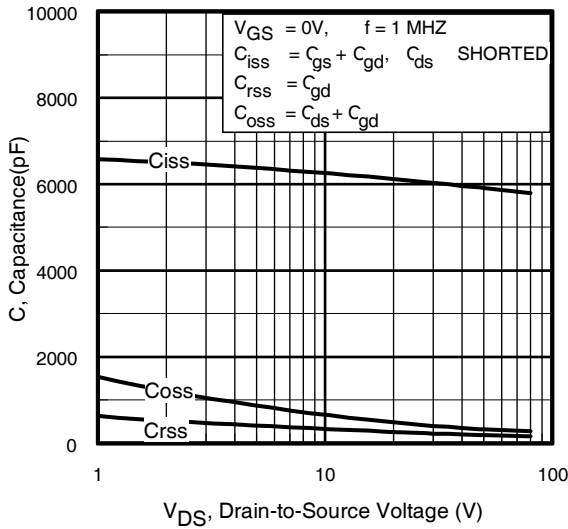


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

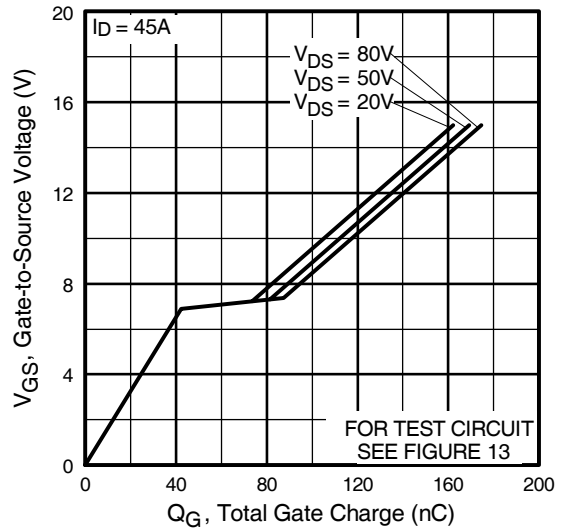


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

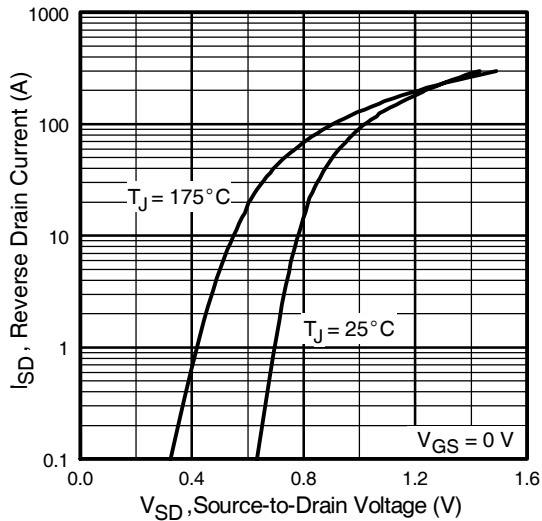


Fig 7. Typical Source-Drain Diode Forward Voltage

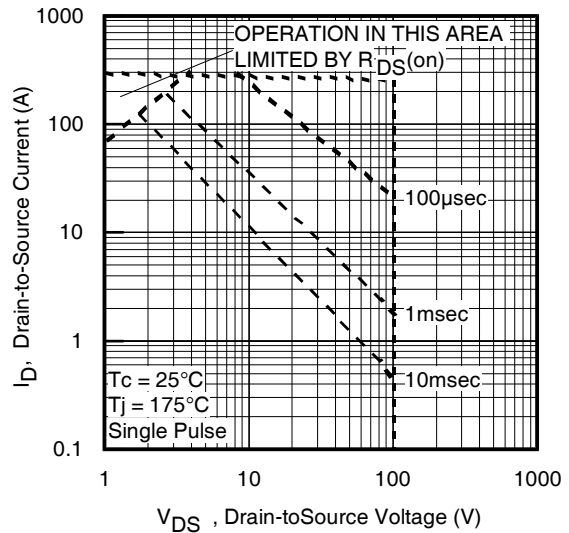


Fig 8. Maximum Safe Operating Area

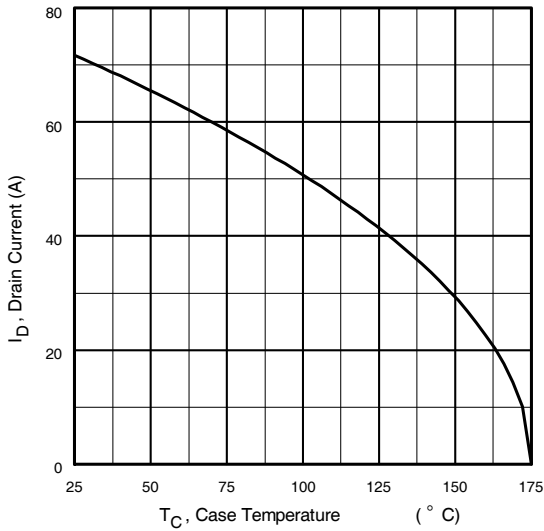


Fig 9. Maximum Drain Current Vs. Case Temperature

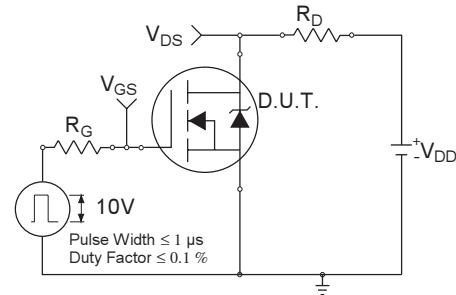


Fig 10a. Switching Time Test Circuit

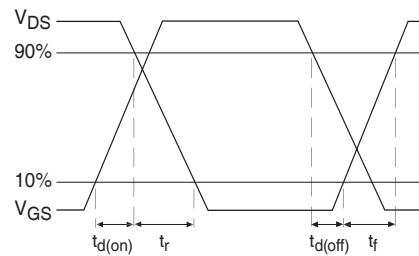


Fig 10b. Switching Time Waveforms

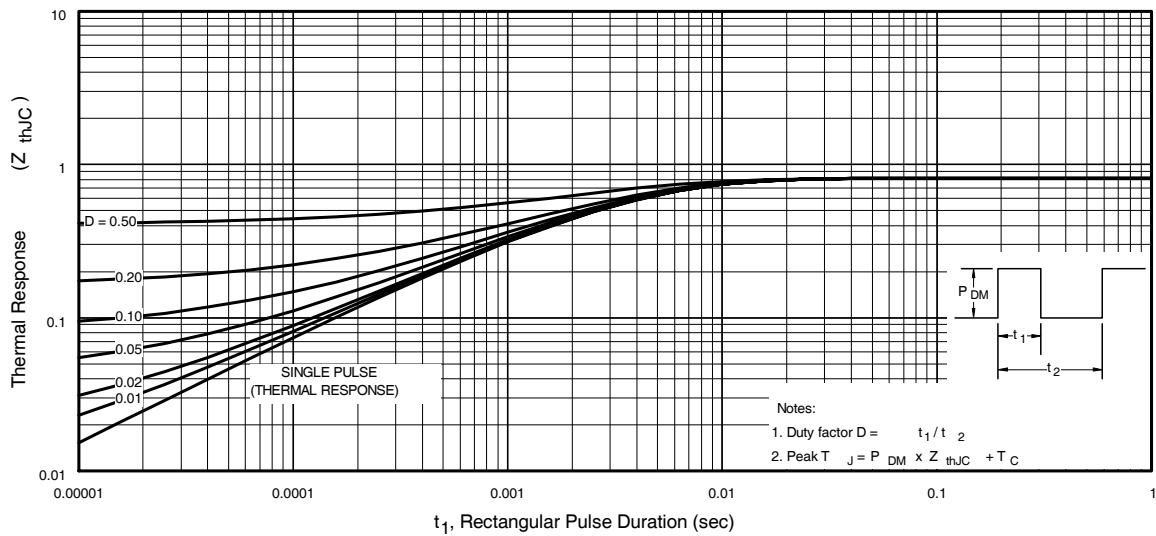


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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IR Rectifier

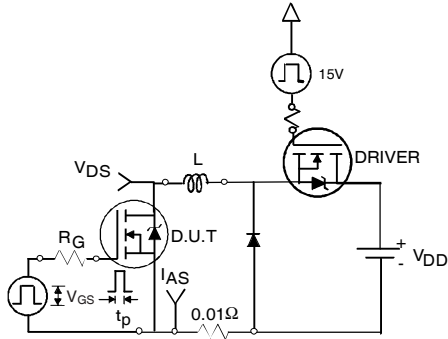


Fig 12a. Unclamped Inductive Test Circuit

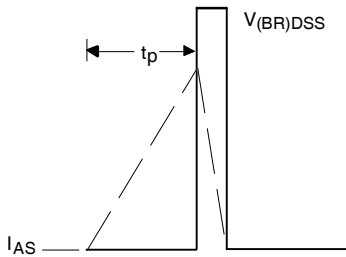


Fig 12b. Unclamped Inductive Waveforms

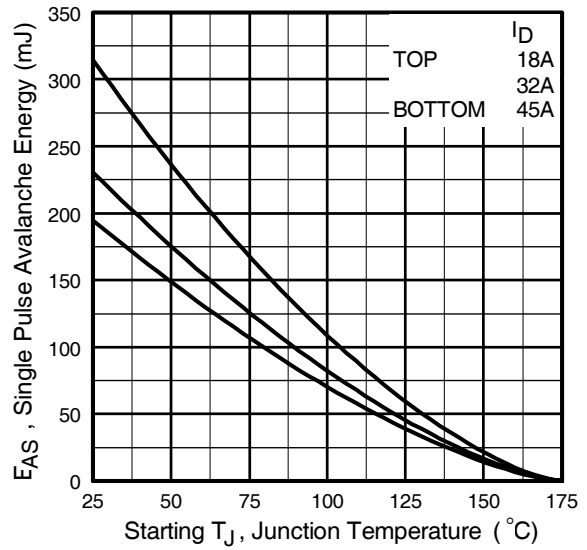


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

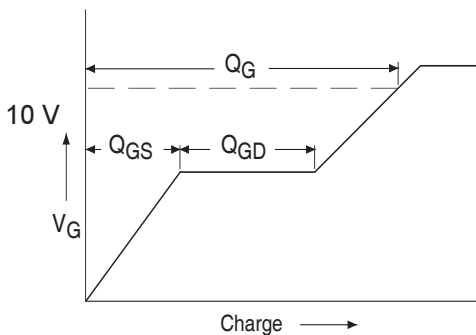


Fig 13a. Basic Gate Charge Waveform

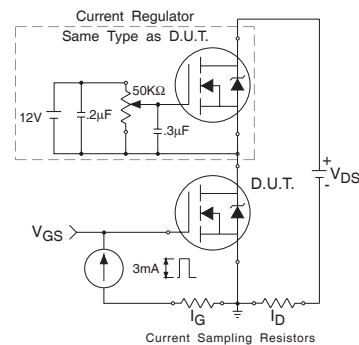
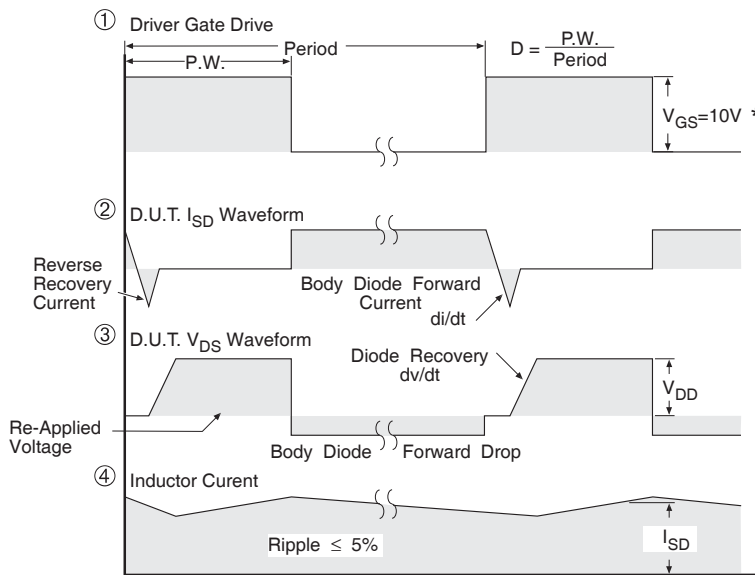
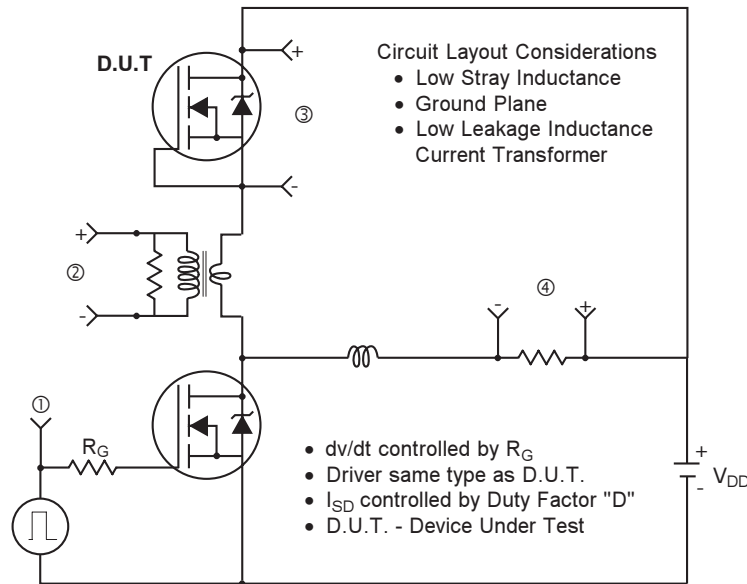


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

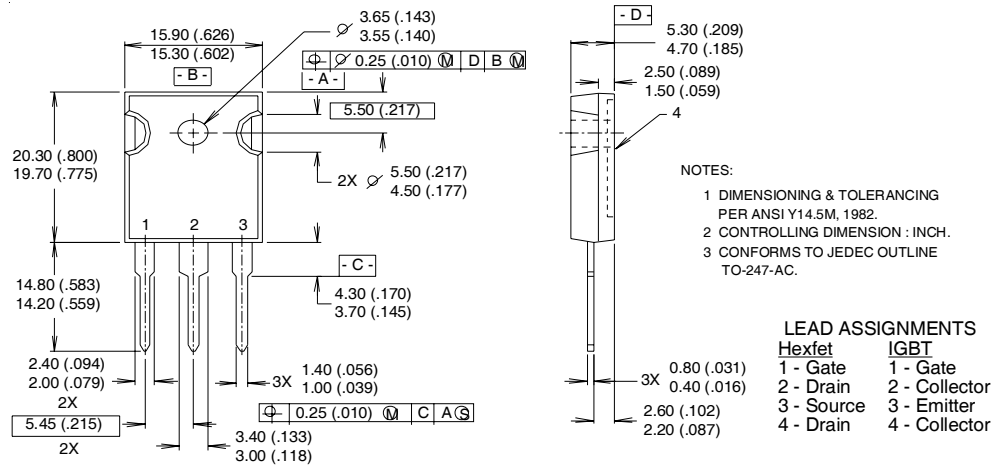
Fig 14. For N-Channel HEXFET® Power MOSFETs

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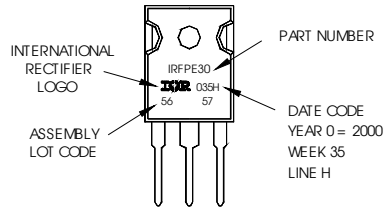
TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5667
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"
Note: "P" in assembly line
position indicates "Lead-Free"



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 190\mu\text{H}$
 $R_G = 25\Omega$, $I_{AS} = 45\text{A}$, $V_{GS} = 10\text{V}$.
- ③ $I_{SD} \leq 45\text{A}$, $di/dt \leq 420\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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Note: For the most current drawings please refer to the IR website at:
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