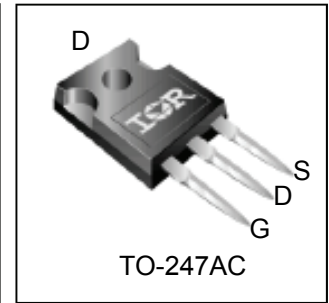
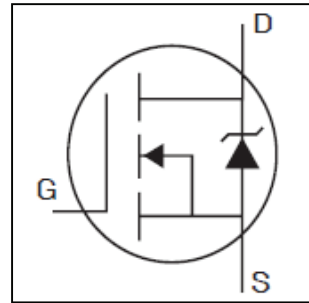




THE DATASHEET OF IRFP4868



V_{DSS}	300V
$R_{DS(on)}$ typ.	25.5mΩ
max.	32mΩ
I_D	70A


Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free

G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP4868PbF	TO-247AC	Tube	25	IRFP4868PbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	70	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	49	
I_{DM}	Pulsed Drain Current ①	280	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	517	W
	Linear Derating Factor	3.4	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf.in (1.1N.m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	1093	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦ ⑧	—	0.29	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

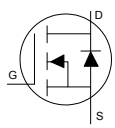
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	300	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.29	—	V/°C	Reference to 25°C, I _D = 5mA①
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	25.5	32	mΩ	V _{GS} = 10V, I _D = 42A ④
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 300V, V _{GS} = 0V
		—	—	250		V _{DS} = 300V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
R _G	Internal Gate Resistance	—	1.1	—	Ω	

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	80	—	—	S	V _{DS} = 50V, I _D = 42A
Q _g	Total Gate Charge	—	180	270	nC	I _D = 42A
Q _{gs}	Gate-to-Source Charge	—	60	—		V _{DS} = 150V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	57	—		V _{GS} = 10V ④
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})	—	123	—		I _D = 42A, V _{DS} = 0V, V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	24	—	ns	V _{DD} = 195V
t _r	Rise Time	—	16	—		I _D = 42A
t _{d(off)}	Turn-Off Delay Time	—	62	—		R _G = 1.0Ω
t _f	Fall Time	—	45	—		V _{GS} = 10V ④
C _{iss}	Input Capacitance	—	10774	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	612	—		V _{DS} = 50V
C _{rss}	Reverse Transfer Capacitance	—	193	—		f = 1.0 MHz, See Fig. 5
C _{oss} eff. (ER)	Effective Output Capacitance (Energy Related) ⑥	—	406	—		V _{GS} = 0V, V _{DS} = 0V to 240V ⑥, See Fig. 11
C _{oss} eff. (TR)	Effective Output Capacitance (Time Related) ⑤	—	710	—		V _{GS} = 0V, V _{DS} = 0V to 240V ⑤

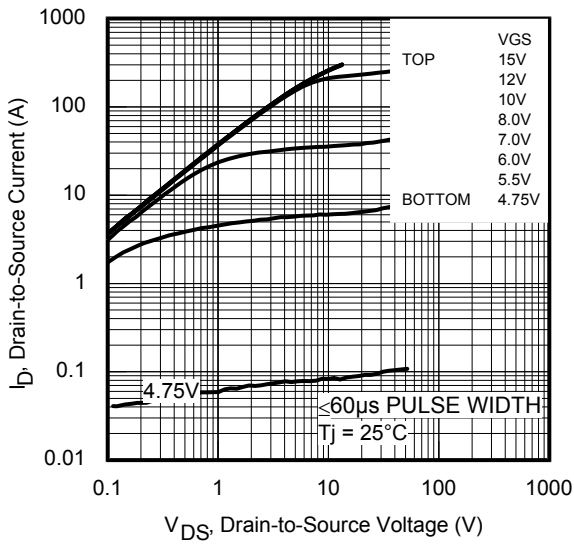
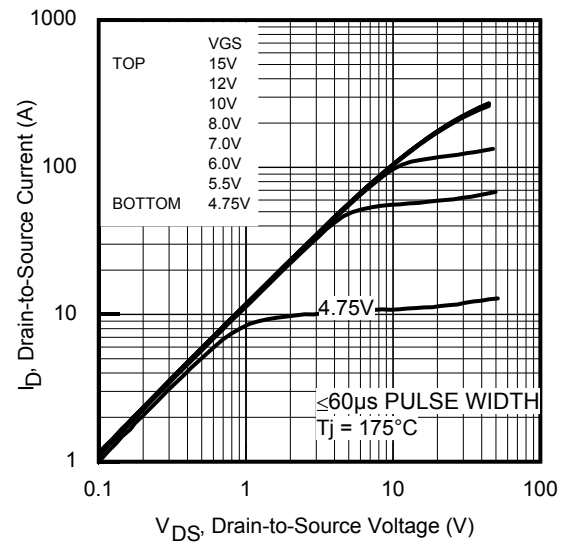
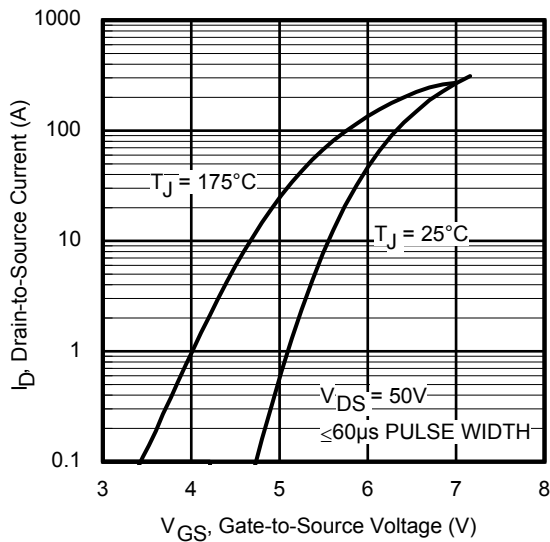
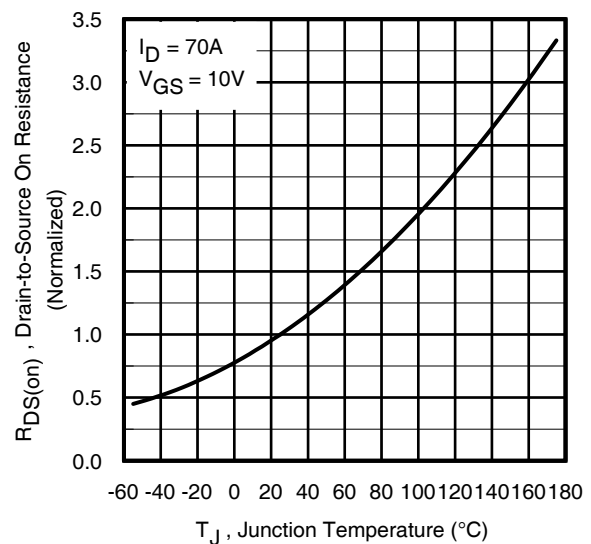
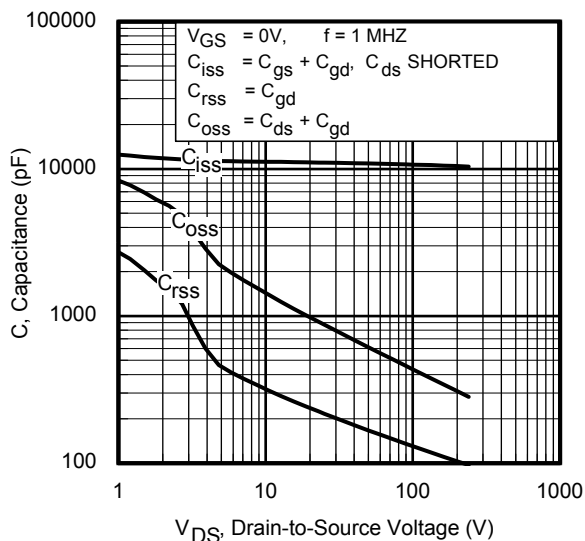
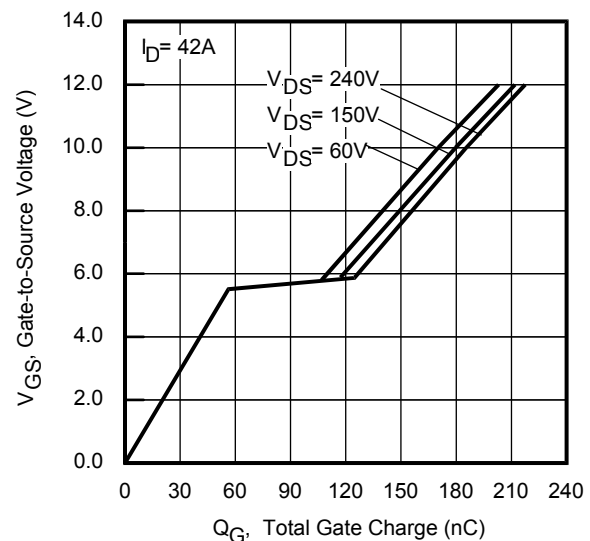
Diode Characteristics

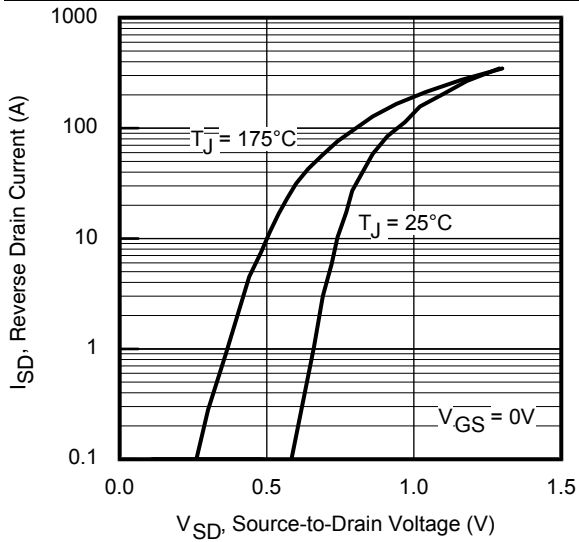
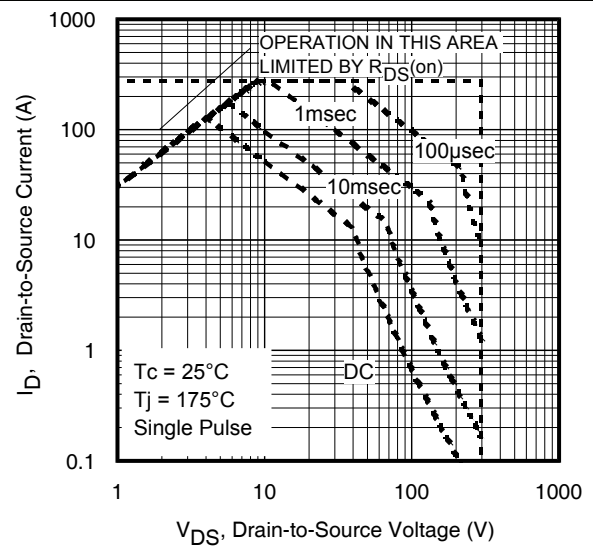
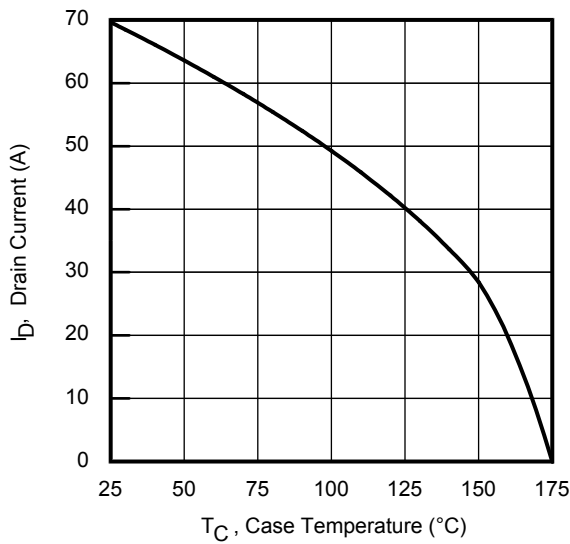
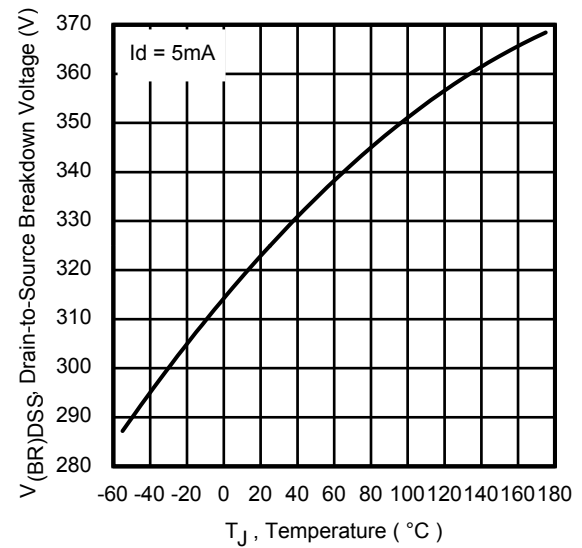
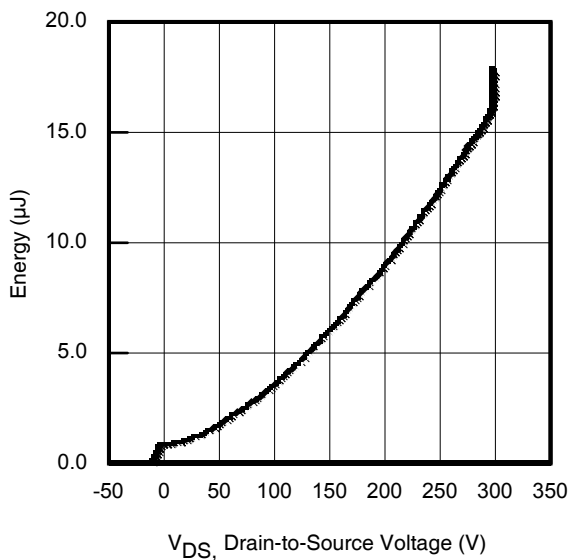
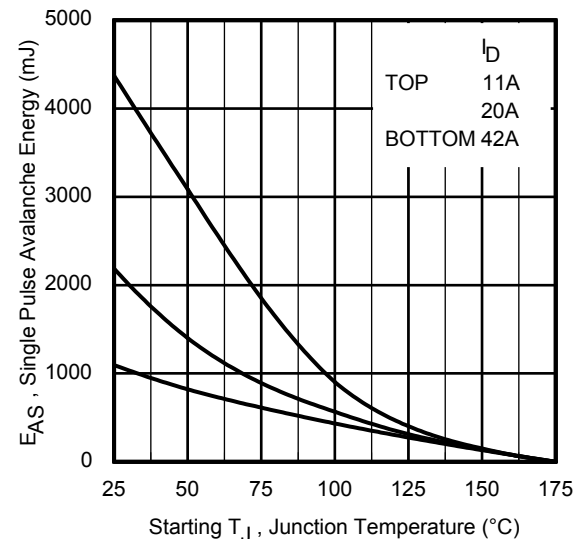
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	70	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	280	A	
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 42A, V _{GS} = 0V ④
dv/dt	Peak Diode Recovery ③	—	7.3	—	V/ns	T _J = 25°C, I _S = 42A, V _{DS} = 300V
t _{rr}	Reverse Recovery Time	—	351	—	ns	T _J = 25°C
		—	454	—		T _J = 125°C
Q _{rr}	Reverse Recovery Charge	—	2520	—	nC	T _J = 25°C
		—	3686	—		T _J = 125°C
I _{RRM}	Reverse Recovery Current	—	16	—	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

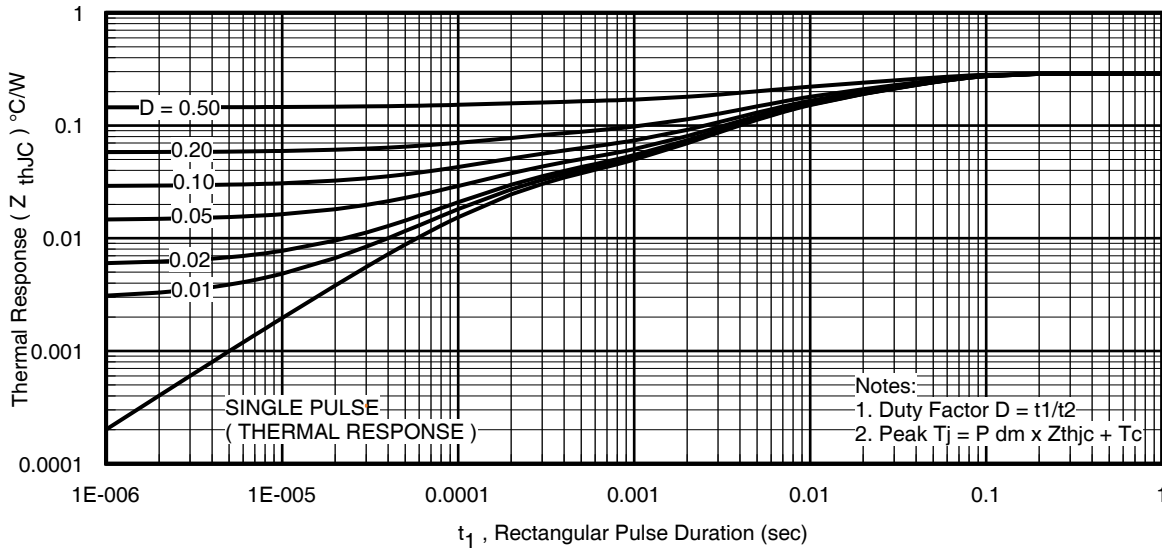
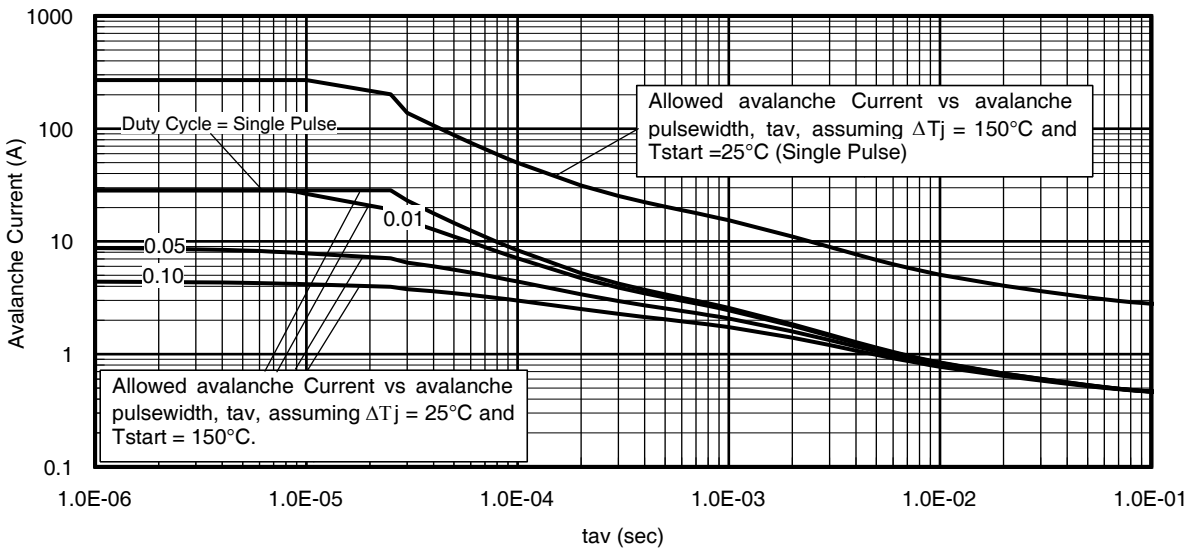
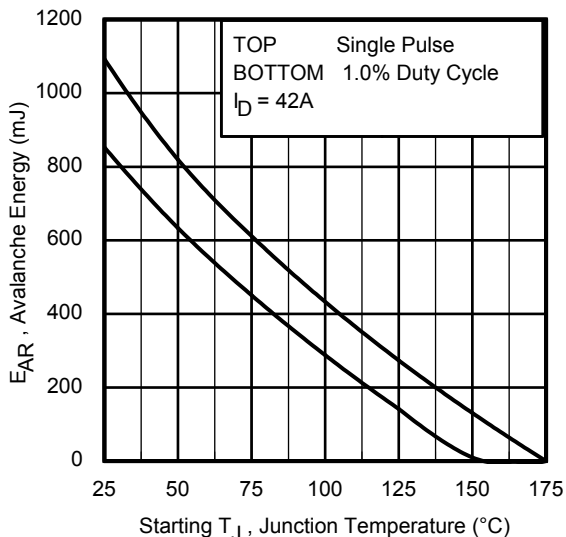
Notes:

- ① Repetitive rating; pulse width limited by max. Junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 1.2mH
R_G = 50Ω, I_{AS} = 42A, V_{GS} = 10V. Part not recommended for use above this value.
- ③ I_{SD} ≤ 42A, di/dt ≤ 1706A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

- ⑤ Coss eff. (TR) is a fixed capacitance that gives the same charging time as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ Coss eff. (ER) is a fixed capacitance that gives the same energy as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ R_θ is measured at T_J approximately 90°C.
- ⑧ R_{θJC} value shown is at time zero.


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-to-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage

Fig 11. Typical Coss Stored Energy

Fig 12. Maximum Avalanche Energy vs. Drain Current

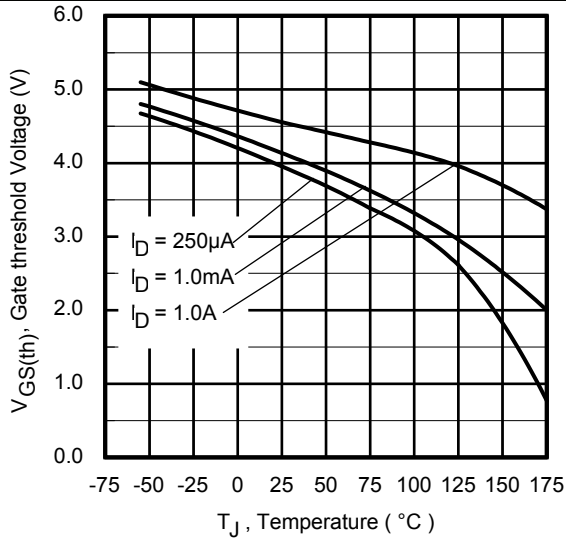
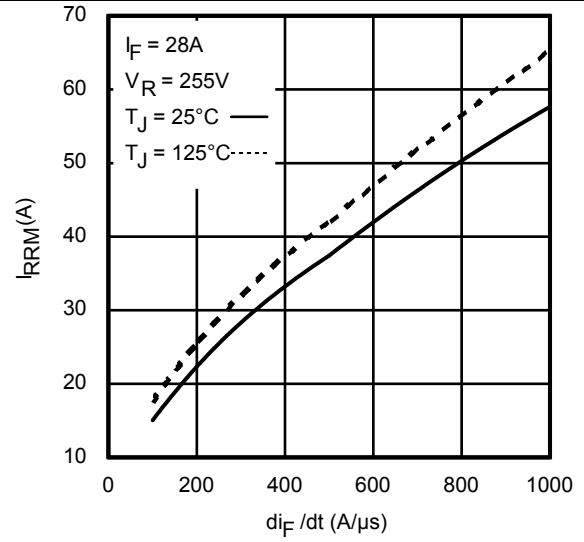
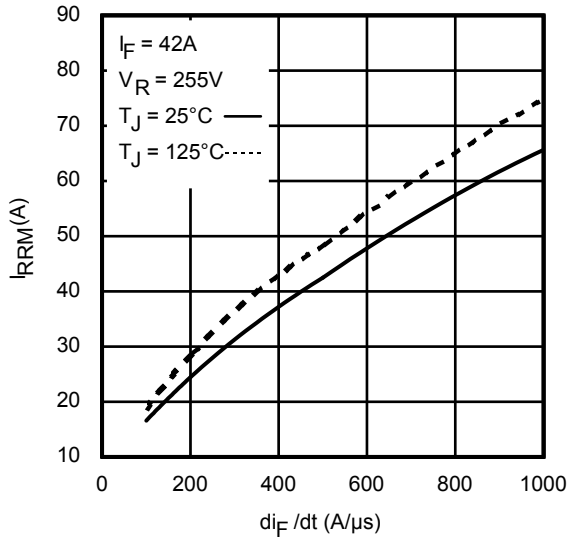
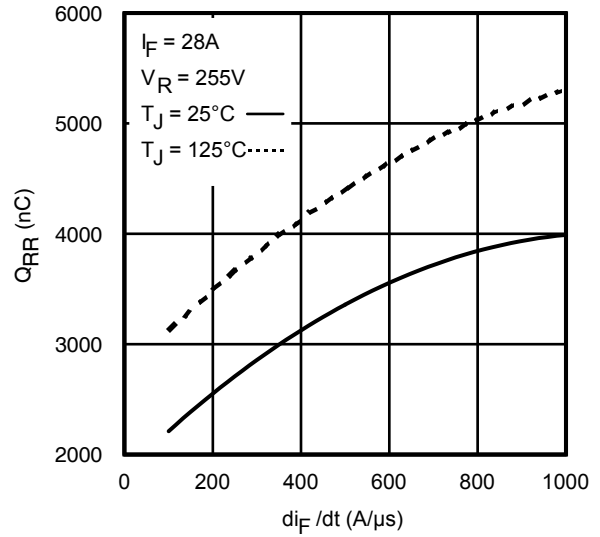
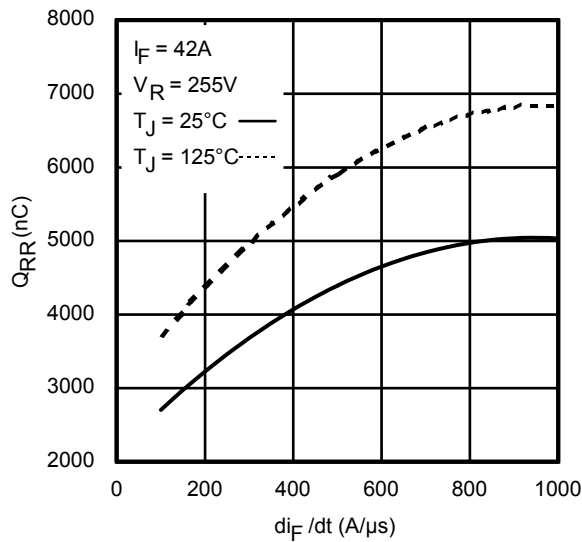

Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Avalanche Current vs. Pulsewidth

Fig 15. Maximum Avalanche Energy vs. Temperature
**Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)**

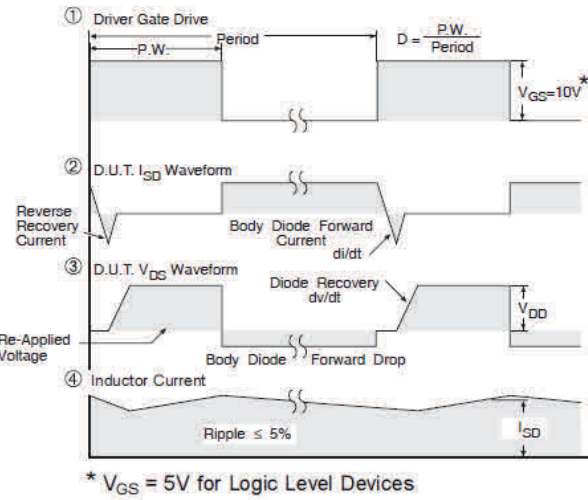
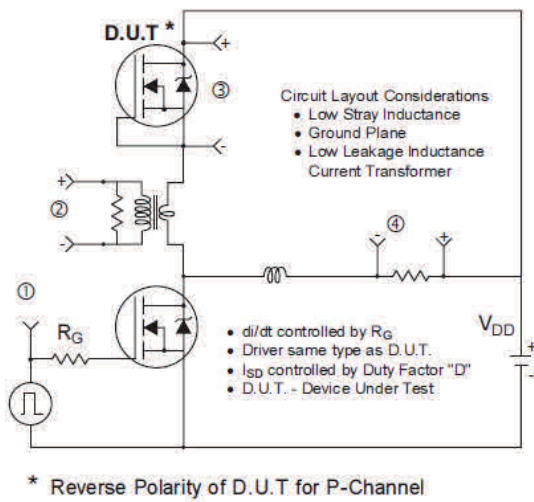
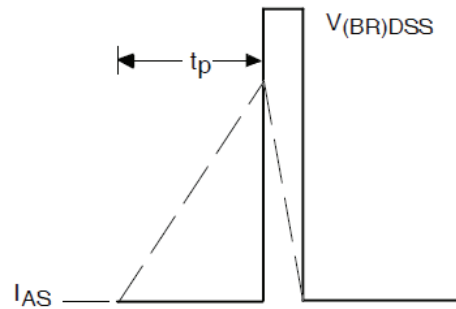
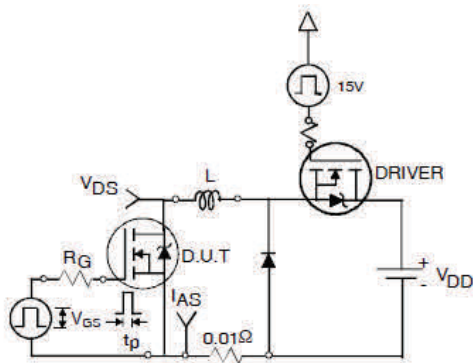
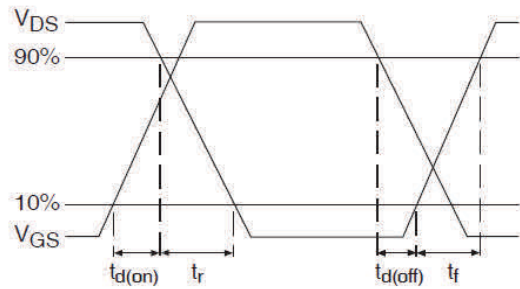
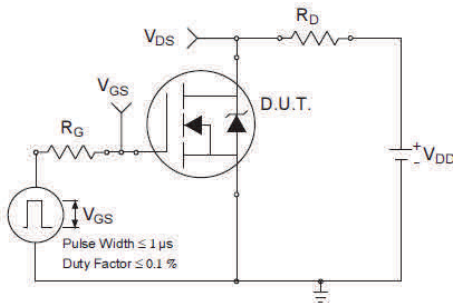
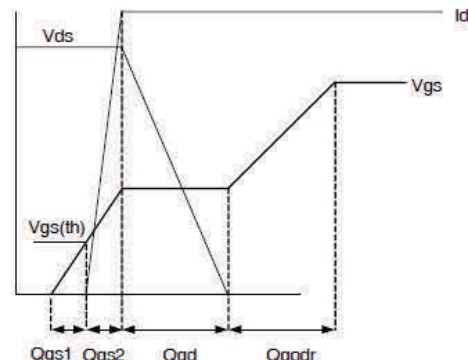
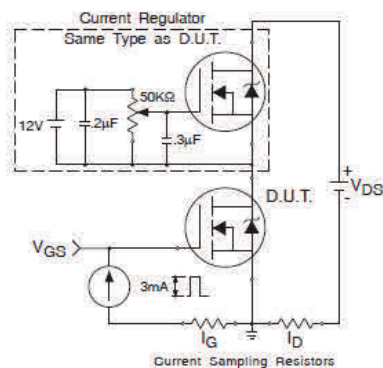
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as $25^\circ C$ in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $tav \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

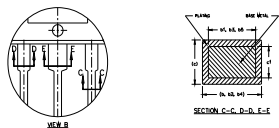
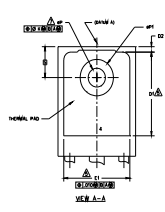
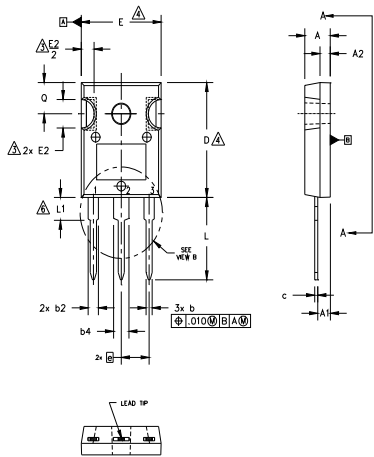
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


Fig. 16 Threshold Voltage vs. Temperature

Fig. 17 Typical Recovery Current vs. di_F/dt

Fig 18. Typical Recovery Current vs. di_F/dt

Fig 19. Typical Stored Charge vs. di_F/dt

Fig 20. Typical Stored Charge vs. di_F/dt


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 22a. Unclamped Inductive Test Circuit
Fig 22b. Unclamped Inductive Waveforms

Fig 23a. Switching Time Test Circuit
Fig 23b. Switching Time Waveforms

Fig 24a. Gate Charge Test Circuit
Fig 24b. Gate Charge Waveform

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

DIODES

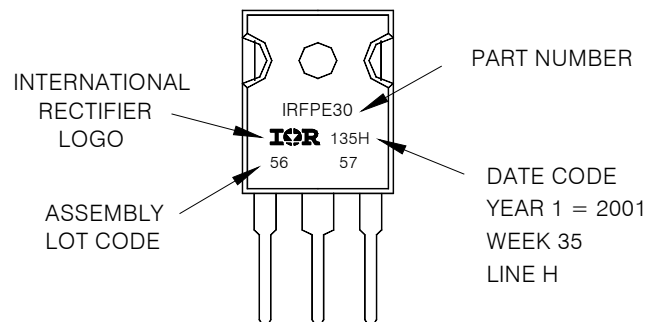
- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247 package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to website at <http://www.irf.com/package/>

Qualification information

Qualification level	Industrial (per JEDEC JESD47F) [†]	
Moisture Sensitivity Level	TO-247AC	N/A
RoHS compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
06/21/2017	<ul style="list-style-type: none"> • Changed datasheet with Infineon logo-all pages • Corrected Package outline on page 8. • Added disclaimer on last page.

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