

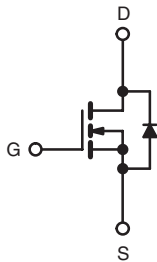


**THE DATASHEET OF
IRFPS35N50LPBF**



Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	500
R _{DS(on)} (Ω)	V _{GS} = 10 V 0.125
Q _g (Max.) (nC)	230
Q _{gs} (nC)	65
Q _{gd} (nC)	110
Configuration	Single



N-Channel MOSFET



FEATURES

- Super Fast Body Diode Eliminates the Need for External Diodes in ZVS Applications
- Lower Gate Charge Results in Simpler Drive Requirements
- Enhanced dV/dt Capabilities Offer Improved Ruggedness
- Higher Gate Voltage Threshold Offers Improved Noise Immunity
- Lead (Pb)-free Available



Available
RoHS*
COMPLIANT

APPLICATIONS

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control Applications

ORDERING INFORMATION	
Package	SUPER-247™
Lead (Pb)-free	IRFPS35N50LPbF
	SiHFPS35N50L-E3
SnPb	IRFPS35N50L
	SiHFPS35N50L

ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	500	V	
Gate-Source Voltage	V _{GS}	± 30		
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	A	
		T _C = 100 °C		22
Pulsed Drain Current ^a	I _{DM}	140		
Linear Derating Factor		3.6	W/°C	
Single Pulse Avalanche Energy ^b	E _{AS}	560	mJ	
Repetitive Avalanche Current ^a	I _{AR}	34	A	
Repetitive Avalanche Energy ^a	E _{AR}	45	mJ	
Maximum Power Dissipation	T _C = 25 °C	P _D	450	W
Peak Diode Recovery dV/dt ^c	dV/dt	15	V/ns	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d		
Mounting Torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting T_J = 25 °C, L = 0.97 mH, R_G = 25 Ω, I_{AS} = 34 A (see fig. 12).
- I_{SD} ≤ 34 A, di/dt ≤ 765 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.28	

Note

a. R_{th} is measured at T_J approximately 90 °C.

SPECIFICATIONS $T_J = 25\text{ °C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	500	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1\text{ mA}$	-	0.12	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.0	-	5.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	50	μA	
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ °C}$	-	-	2.0	mA	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 20\text{ A}^b$	-	0.125	0.145	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 20\text{ A}^b$	18	-	-	S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5	-	5580	-	pF	
Output Capacitance	C_{oss}		-	590	-		
Reverse Transfer Capacitance	C_{rss}		-	58	-		
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$	-	7290	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 400\text{ V}$, $f = 1.0\text{ MHz}$	-	160	-	
Effective Output Capacitance (Energy Related)	$C_{oss\text{ eff. (ER)}}$	$V_{DS} = 0\text{ V to }400\text{ V}^c$	-	320	-		
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 34\text{ A}$, $V_{DS} = 400\text{ V}$, see fig. 7 and 13 ^b	-	-	230	nC
Gate-Source Charge	Q_{gs}			-	-	65	
Gate-Drain Charge	Q_{gd}			-	-	110	
Internal Gate Resistance	R_G	$f = 1\text{ MHz}$, open drain		-	1.1	-	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$, $I_D = 34\text{ A}$, $R_G = 1.2\text{ }\Omega$, see fig. 10 ^b	-	24	-	ns	
Rise Time	t_r		-	100	-		
Turn-Off Delay Time	$t_{d(off)}$		-	42	-		
Fall Time	t_f		-	42	-		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	34	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	140		
Body Diode Voltage	V_{SD}	$T_J = 25\text{ °C}$, $I_S = 34\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.5	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}$, $I_F = 34\text{ A}$	-	170	250	ns	
		$T_J = 125\text{ °C}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	220	330		
Body Diode Reverse Recovery Charge	Q_{rr}	$T_J = 25\text{ °C}$, $I_S = 34\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	670	1010	μC	
		$T_J = 125\text{ °C}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	1500	2200		
Reverse Recovery Current	I_{RRM}	$T_J = 25\text{ °C}$	-	8.5	-	A	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 400\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .
 $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

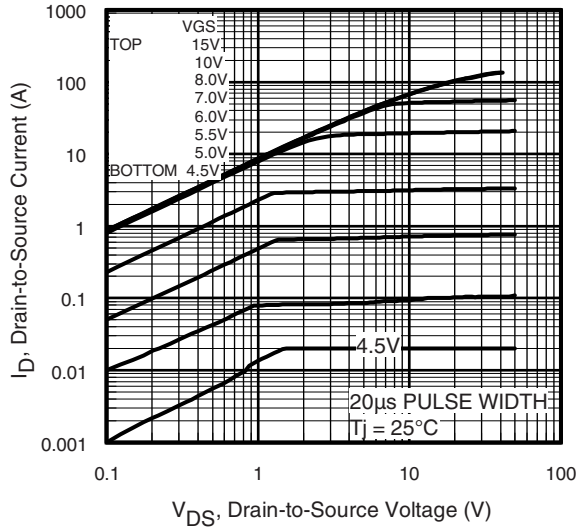


Fig. 1 - Typical Output Characteristics

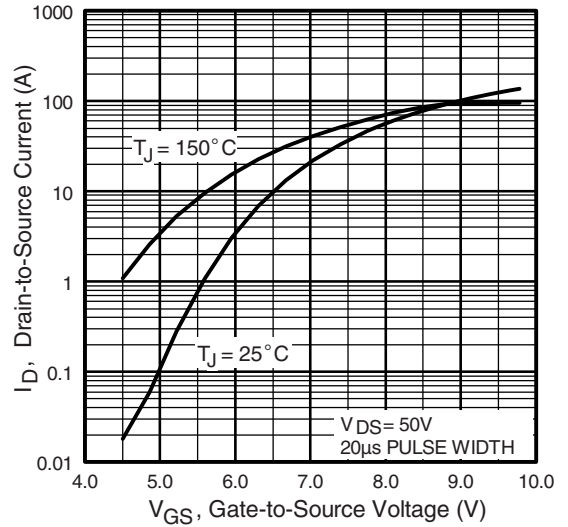


Fig. 3 - Typical Transfer Characteristics

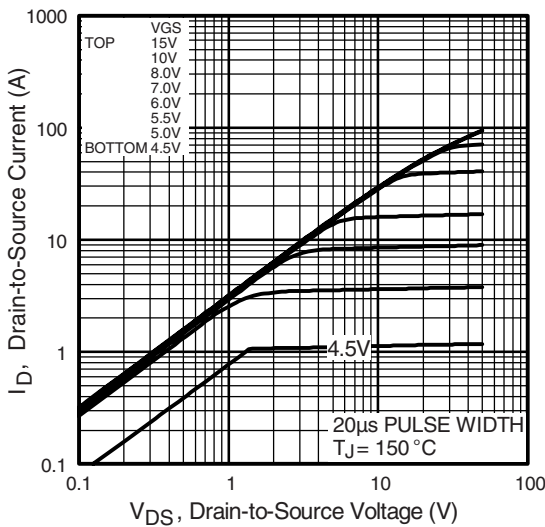


Fig. 2 - Typical Output Characteristics

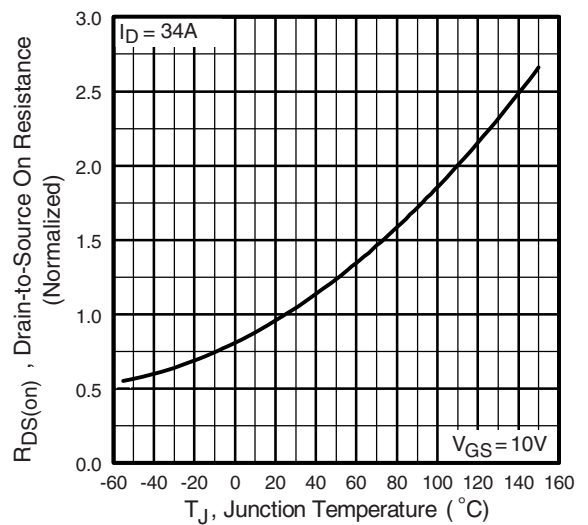


Fig. 4 - Normalized On-Resistance vs. Temperature

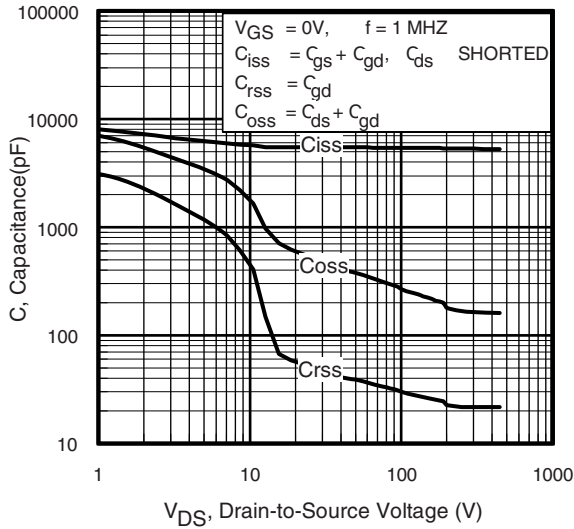


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

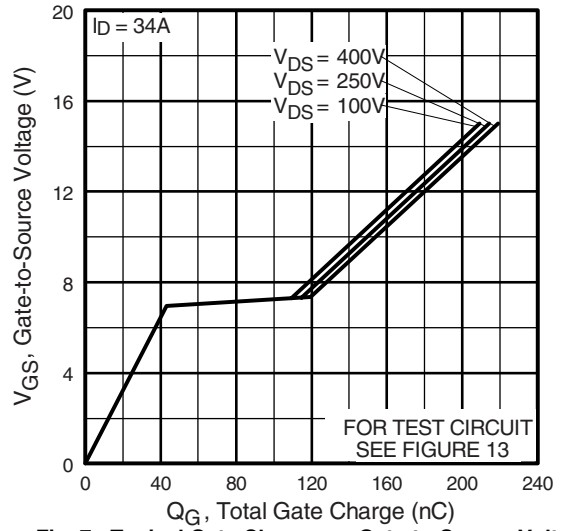


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

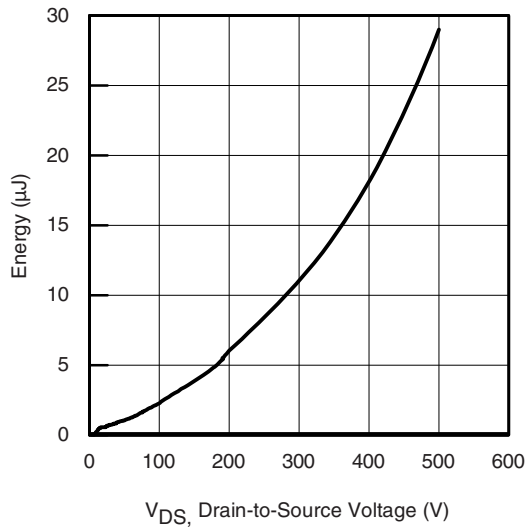


Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

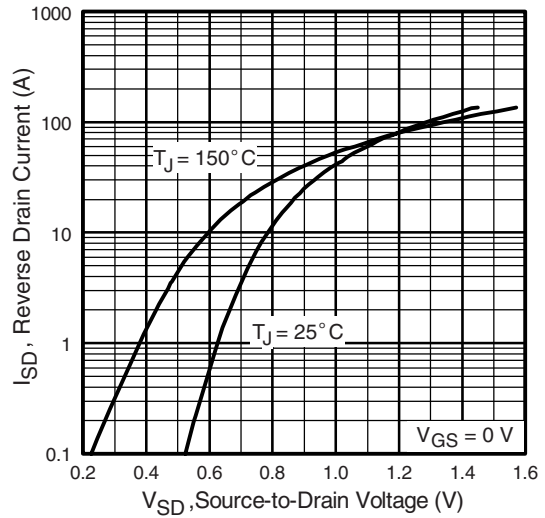


Fig. 8 - Typical Source Drain Diode Forward Voltage

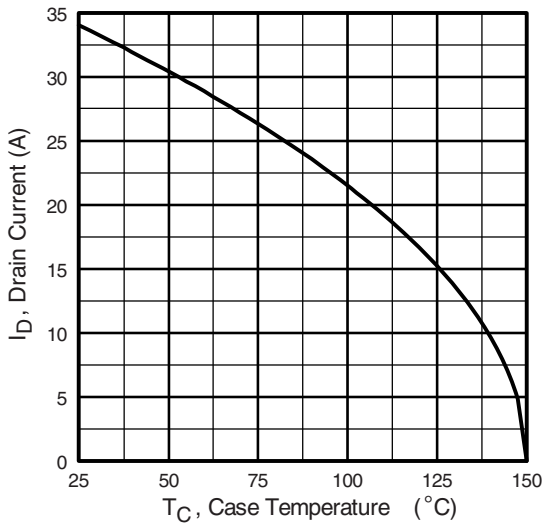


Fig. 9 - Maximum Drain Current vs. Case Temperature

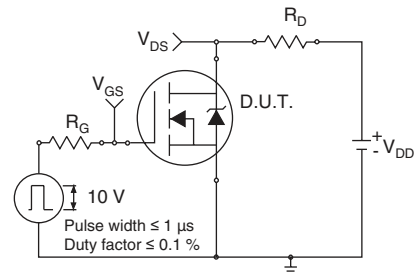


Fig. 10a - Switching Time Test Circuit

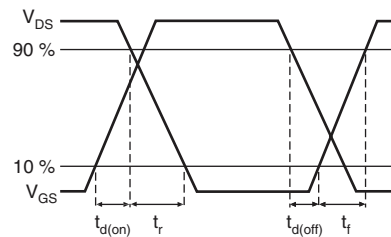


Fig. 10b - Switching Time Waveforms

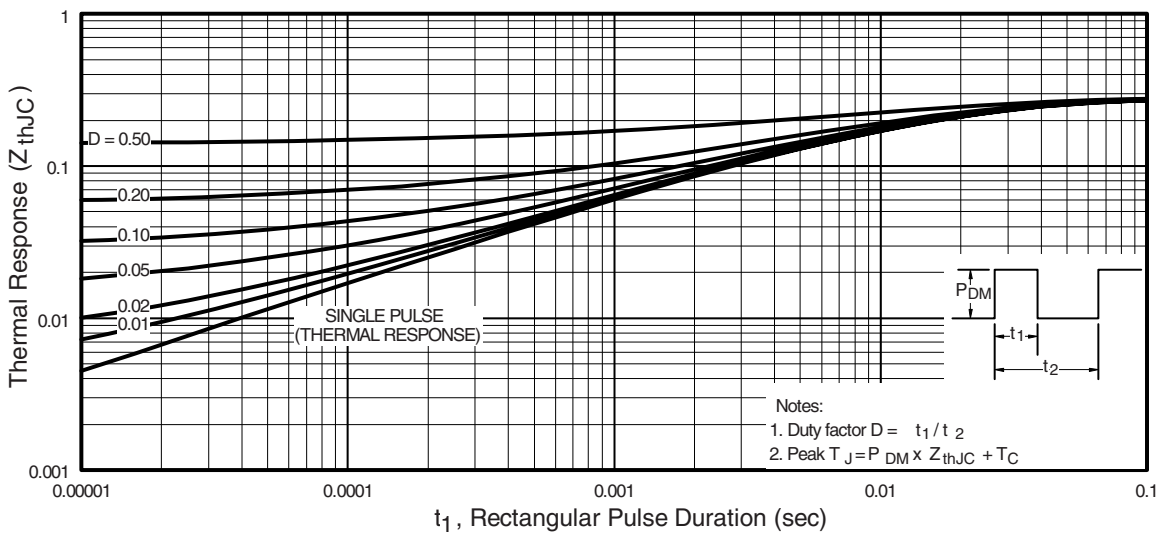


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

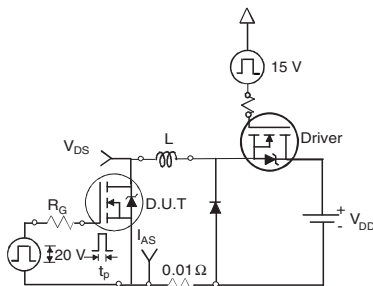


Fig. 12a - Unclamped Inductive Test Circuit

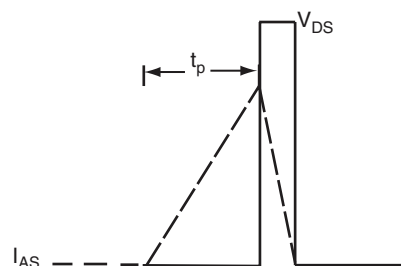


Fig. 12b - Unclamped Inductive Waveforms

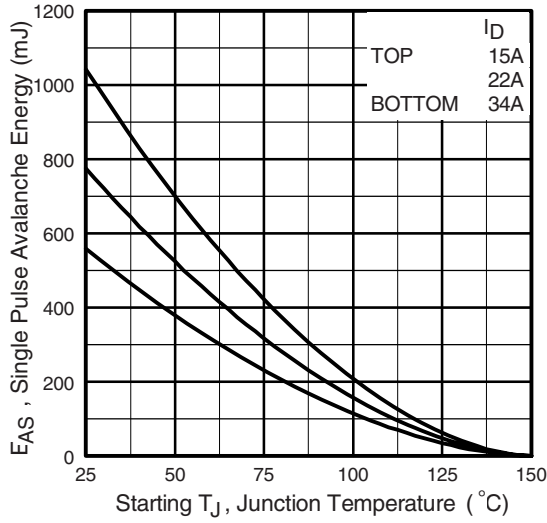


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

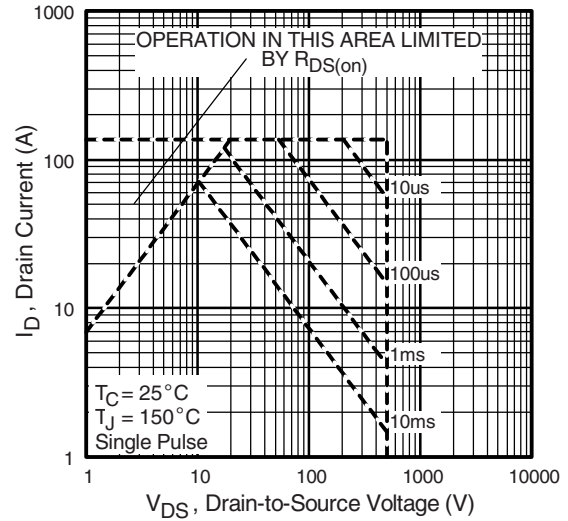


Fig. 12d - Maximum Safe Operating Area

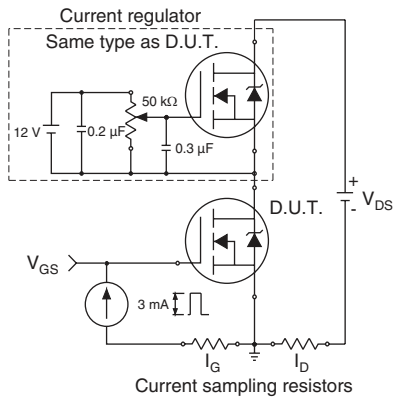


Fig. 13a - Gate Charge Test Circuit

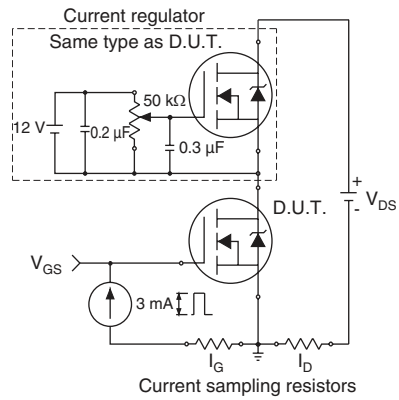
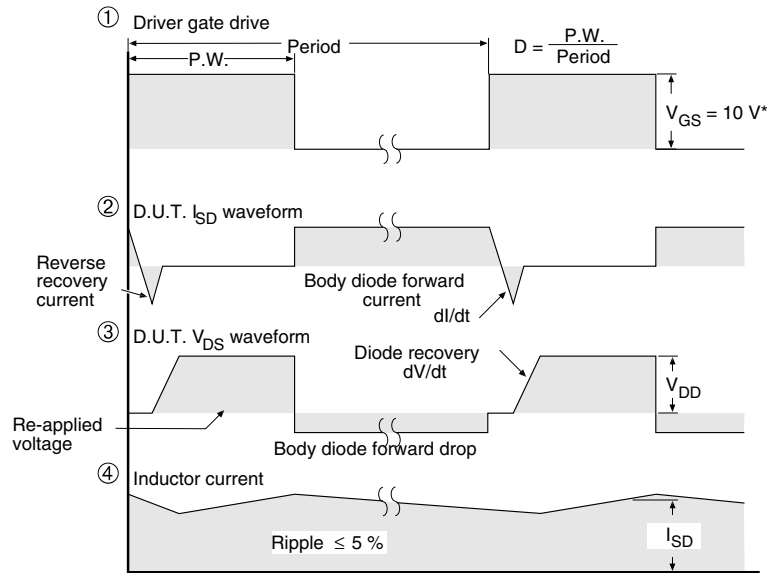
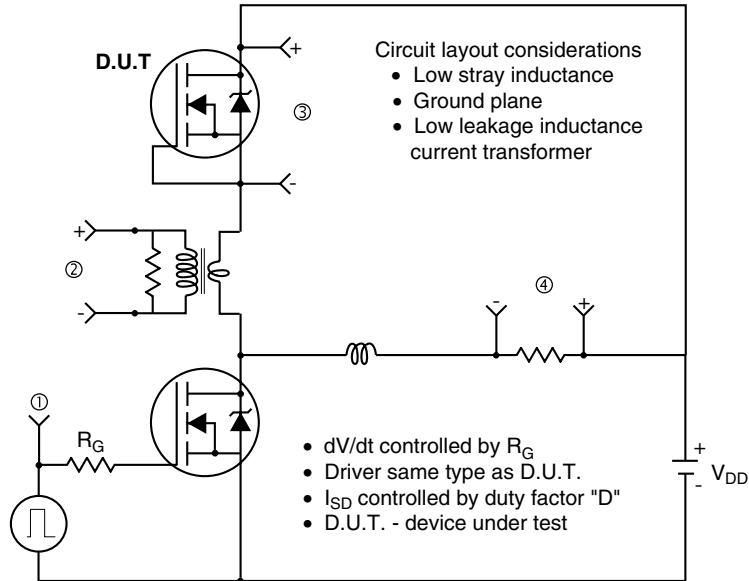


Fig. 13b - Basic Gate Charge Waveform

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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