



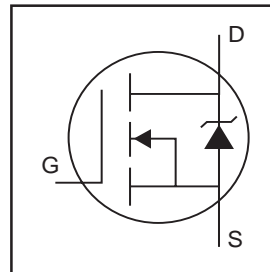
**THE DATASHEET OF
IRFPS3815PBF**



IRFPS3815PbF

HEXFET® Power MOSFET

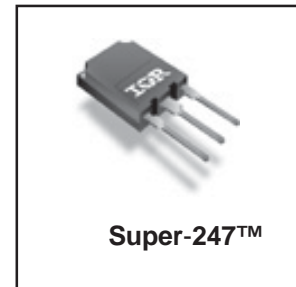
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



$V_{DSS} = 150V$
$R_{DS(on)} = 0.015\Omega$
$I_D = 105A$

Description

The HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.



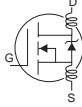
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	105	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	74	
I_{DM}	Pulsed Drain Current ①	390	
$P_D @ T_C = 25^\circ C$	Power Dissipation	441	W
	Linear Derating Factor	2.9	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy ②	1610	mJ
I_{AR}	Avalanche Current ③	58	A
E_{AR}	Repetitive Avalanche Energy ④	38	mJ
dv/dt	Peak Diode Recovery dv/dt ⑤	3.0	V/ns
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.34	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.015	Ω	$V_{GS} = 10V, I_D = 63A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = 10V, I_D = 250\mu A$
g_{fs}	Forward Transconductance	47	—	—	S	$V_{DS} = 50V, I_D = 58A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$
Q_g	Total Gate Charge	—	260	390	nC	$I_D = 58A$
Q_{gs}	Gate-to-Source Charge	—	53	80		$V_{DS} = 120V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	150	230		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	22	—		$V_{DD} = 75V$
t_r	Rise Time	—	130	—	ns	$I_D = 58A$
$t_{d(off)}$	Turn-Off Delay Time	—	51	—		$R_G = 1.03\Omega$
t_f	Fall Time	—	60	—		$V_{GS} = 10V$ ④
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	6810	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1570	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	480	—		$f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	9820	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	670	—		$V_{GS} = 0V, V_{DS} = 120V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance ⑤	—	1270	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	105	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	390		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 58A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	270	410	ns	$T_J = 25^\circ\text{C}, I_F = 58A$
Q_{rr}	Reverse Recovery Charge	—	2990	4490	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.96\text{mH}$
 $R_G = 25\Omega, I_{AS} = 58A$. (See Figure 12)
- ③ $I_{SD} \leq 58A, di/dt \leq 450A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss\ eff.}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

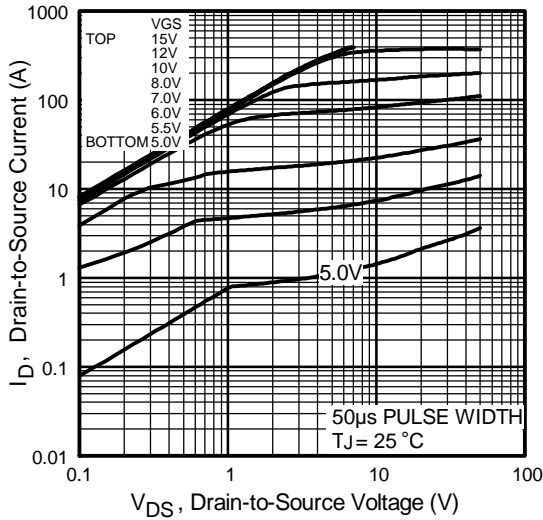


Fig 1. Typical Output Characteristics

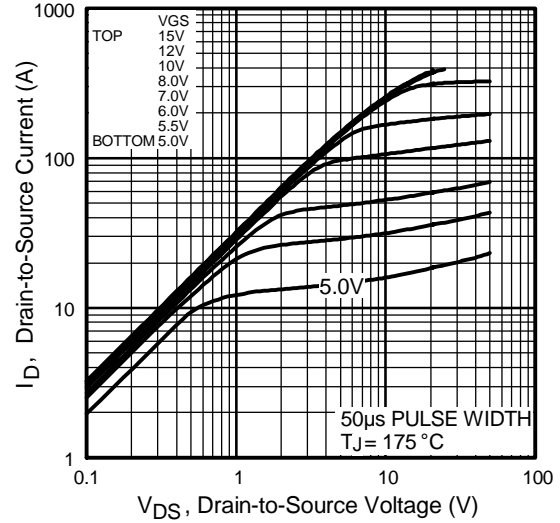


Fig 2. Typical Output Characteristics

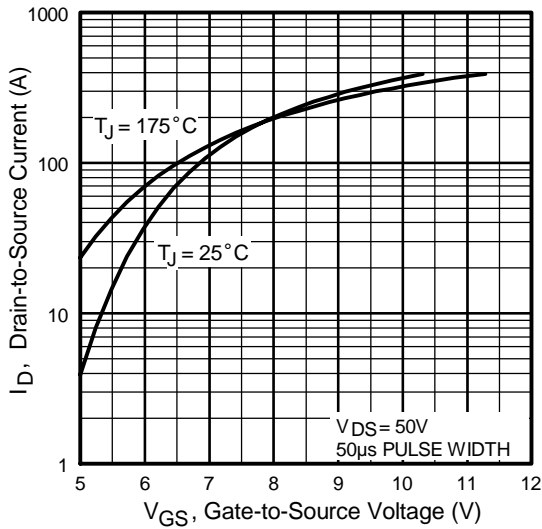


Fig 3. Typical Transfer Characteristics

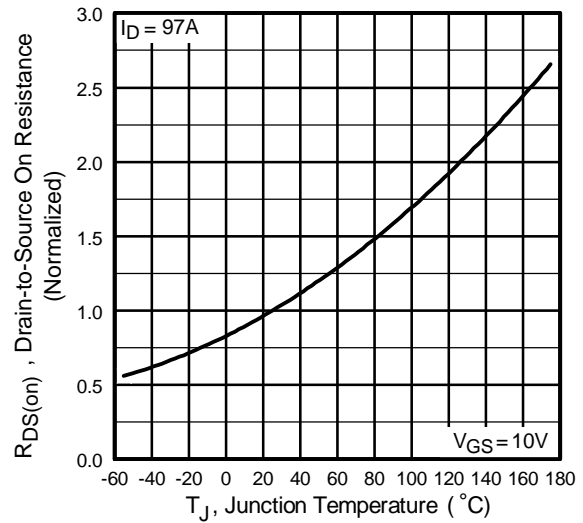


Fig 4. Normalized On-Resistance Vs. Temperature

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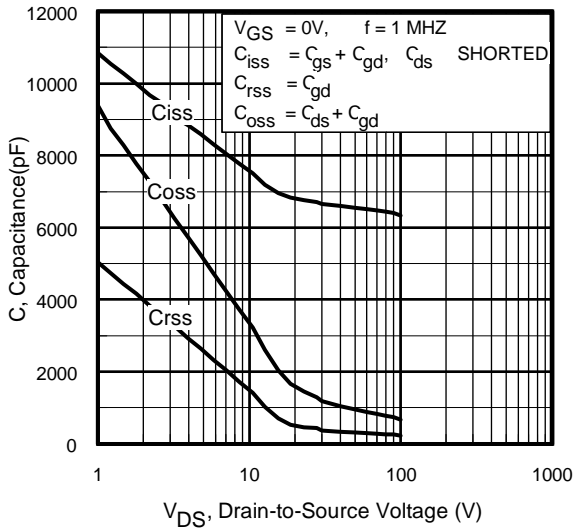


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

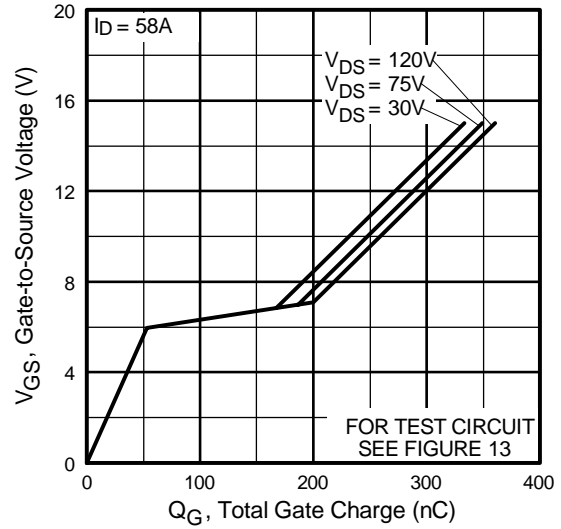


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

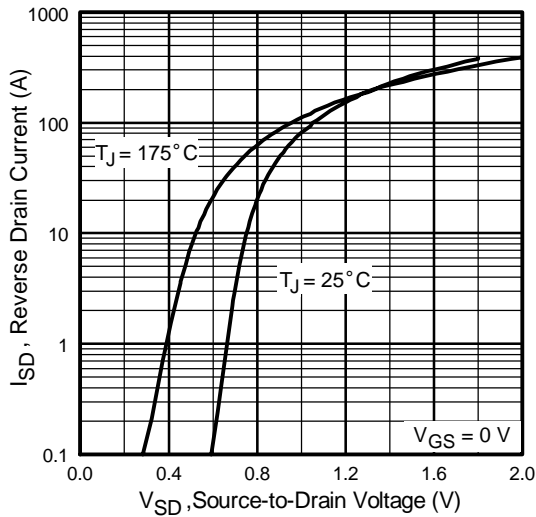


Fig 7. Typical Source-Drain Diode Forward Voltage

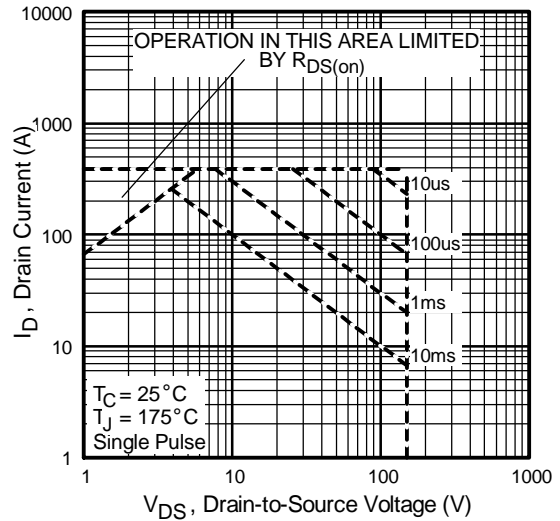


Fig 8. Maximum Safe Operating Area

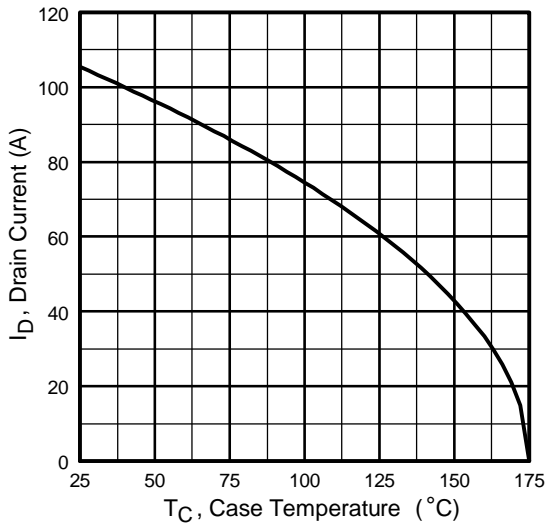


Fig 9. Maximum Drain Current Vs. Case Temperature

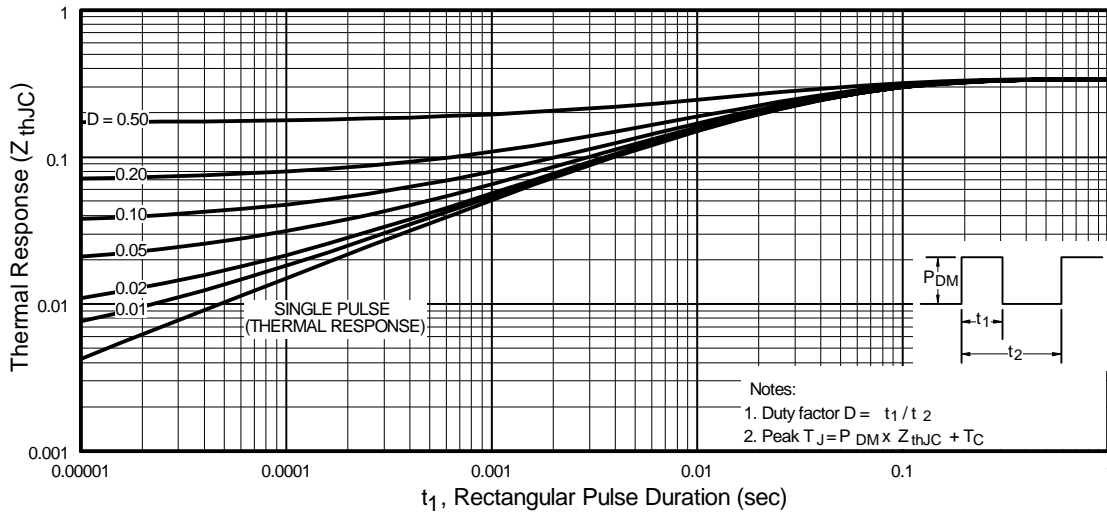
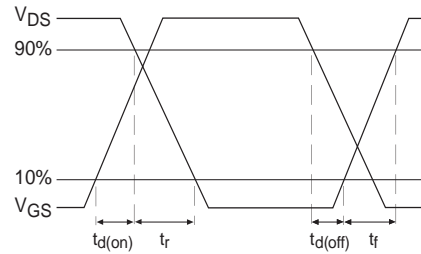
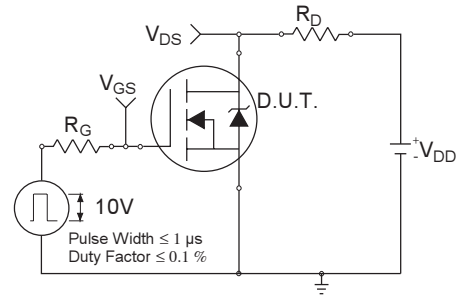


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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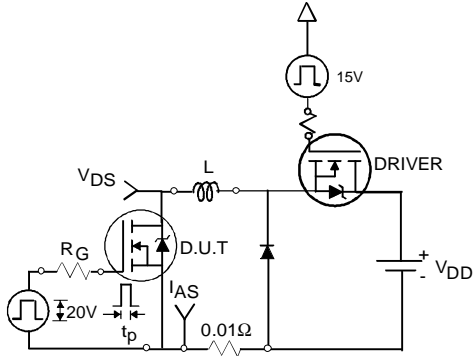


Fig 12a. Unclamped Inductive Test Circuit

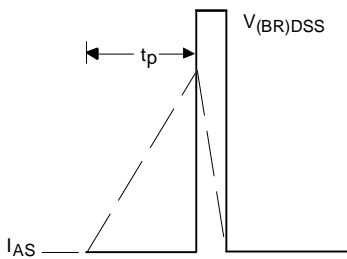


Fig 12b. Unclamped Inductive Waveforms

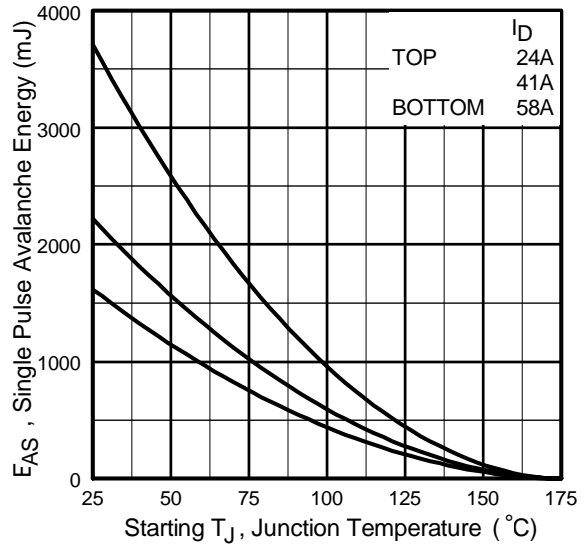


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

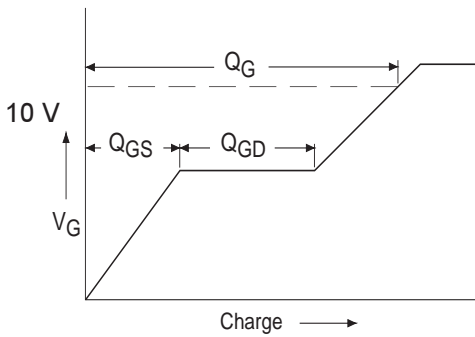


Fig 13a. Basic Gate Charge Waveform

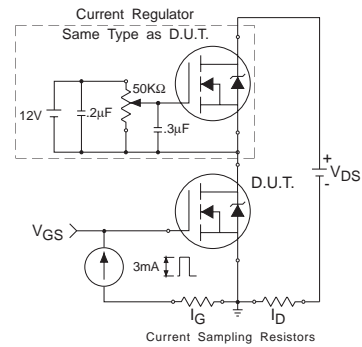
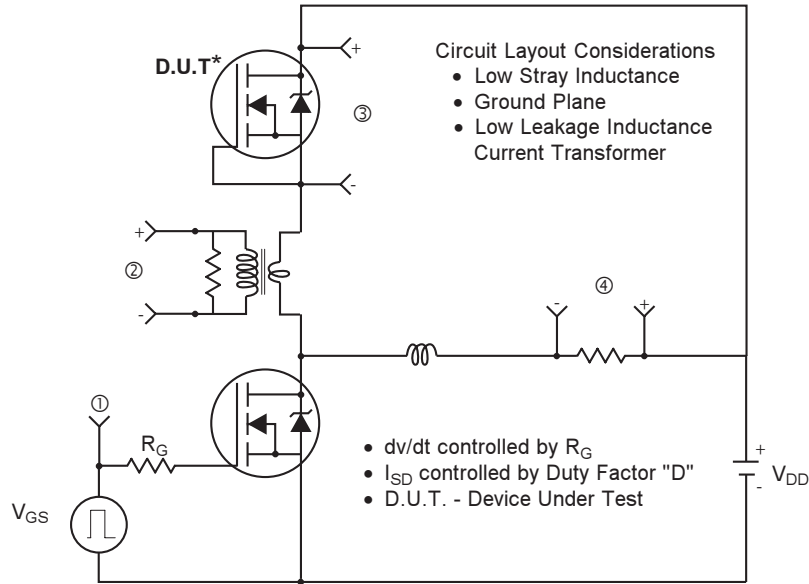
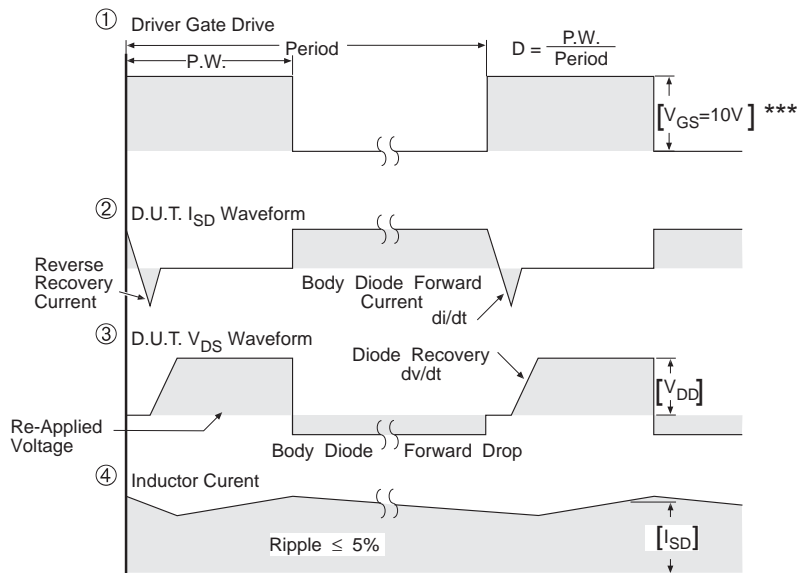


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



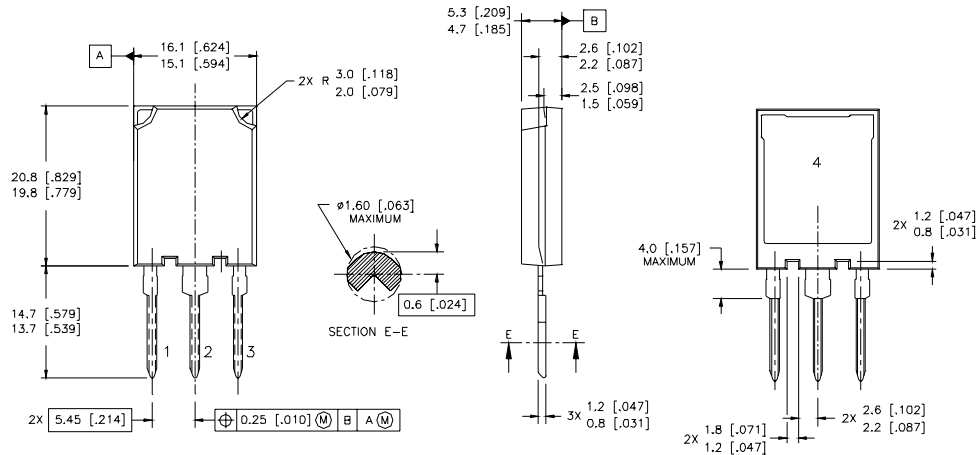
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

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Case Outline and Dimensions — Super-247

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NOTES:

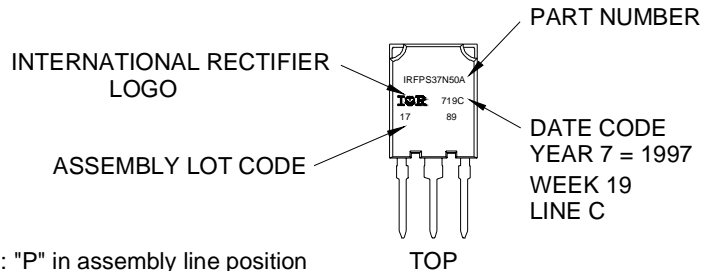
1. DIMENSIONS & TOLERANCING PER ASME Y14.5M-1994
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETRES [INCHES]

LEAD ASSIGNMENTS

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

Super-247 (TO-274AA) Part Marking Information

EXAMPLE: THIS IS AN IRFPS37N50A WITH
ASSEMBLY LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Note: "P" in assembly line position indicates "Lead-Free"

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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