



**THE DATASHEET OF
IRFR3711TRLPBF**



SMPS MOSFET

IRFR3711PbF
IRFU3711PbF

Applications

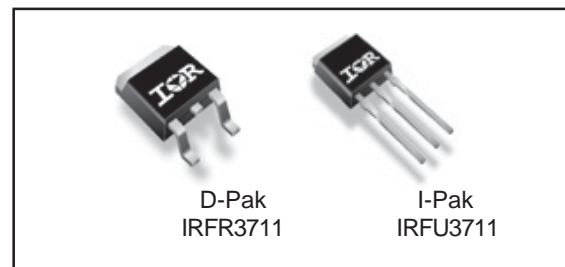
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Server Processor Power Synchronous FET
- Optimized for Synchronous Buck Converters Including Capacitive Induced Turn-on Immunity
- 100% R_G Tested
- Lead-Free

Benefits

- Ultra-Low Gate Impedance
- Very Low R_{DS(on)} at 4.5V V_{GS}
- Fully Characterized Avalanche Voltage and Current

HEXFET® Power MOSFET

V _{DSS}	R _{DS(on)} max	I _D
20V	6.5mΩ	110A ^④



Absolute Maximum Ratings

Symbol	Parameter	Max	Units
V _{DS}	Drain-Source Voltage	20	V
V _{GS}	Gate-Source Voltage	± 20	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	100 ^④	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	69 ^④	
I _{DM}	Pulsed Drain Current ^①	440	
P _D @ T _A = 25°C	Maximum Power Dissipation ^⑤	2.5	W
P _D @ T _C = 25°C	Maximum Power Dissipation	120	
	Linear Derating Factor	0.96	W/°C
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

Symbol	Parameter	Typ	Max	Units
R _{θJC}	Junction-to-Case ^⑥	—	1.04	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mount) ^{⑥⑦}	—	50	
R _{θJA}	Junction-to-Ambient ^⑥	—	110	

Notes ① through ⑦ are on page 10

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.022	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	5.2	6.5	m Ω	$V_{GS} = 10V, I_D = 15A$ ③
		—	6.7	8.5		$V_{GS} = 4.5V, I_D = 12A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	140	μA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	20		$V_{DS} = 16V, V_{GS} = 0V$
		—	—	100		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$

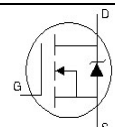
Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
g_{fs}	Forward Transconductance	53	—	—	S	$V_{DS} = 16V, I_D = 30A$
Q_g	Total Gate Charge	—	29	44	nC	$I_D = 15A$
Q_{gs}	Gate-to-Source Charge	—	7.3	—		$V_{DS} = 10V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	8.9	—		$V_{GS} = 4.5V$ ③
Q_{oss}	Output Gate Charge	—	33	—		$V_{GS} = 0V, V_{DS} = 10V$
R_G	Gate Resistance	0.3	—	2.5	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 10V$
t_r	Rise Time	—	220	—		$I_D = 30A$
$t_{d(off)}$	Turn-Off Delay Time	—	17	—		$R_G = 1.8\Omega$
t_f	Fall Time	—	12	—		$V_{GS} = 4.5V$ ③
C_{iss}	Input Capacitance	—	2980	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1770	—		$V_{DS} = 10V$
C_{riss}	Reverse Transfer Capacitance	—	280	—		$f = 1.0MHz$

Avalanche Characteristics

Symbol	Parameter	Typ	Max	Units
E_{AS}	Single Pulse Avalanche Energy②	—	460	mJ
I_{AR}	Avalanche Current ①	—	30	A

Diode Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	110 ④	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	440		
V_{SD}	Diode Forward Voltage	—	0.88	1.3	V	$T_J = 25^\circ\text{C}, I_S = 30A, V_{GS} = 0V$ ③
		—	0.82	—		$T_J = 125^\circ\text{C}, I_S = 30A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	50	75	ns	$T_J = 25^\circ\text{C}, I_F = 16A, V_R = 10V$
Q_{rr}	Reverse Recovery Charge	—	61	92	nC	$di/dt = 100A/\mu s$ ③
t_{rr}	Reverse Recovery Time	—	48	72	ns	$T_J = 125^\circ\text{C}, I_F = 16A, V_R = 10V$
Q_{rr}	Reverse Recovery Charge	—	65	98	nC	$di/dt = 100A/\mu s$ ③

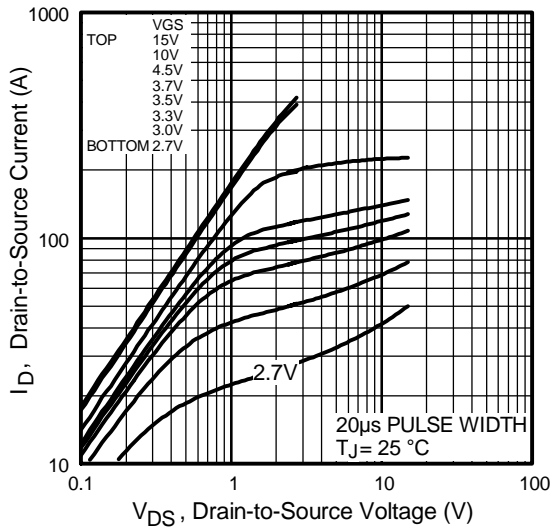


Fig 1. Typical Output Characteristics

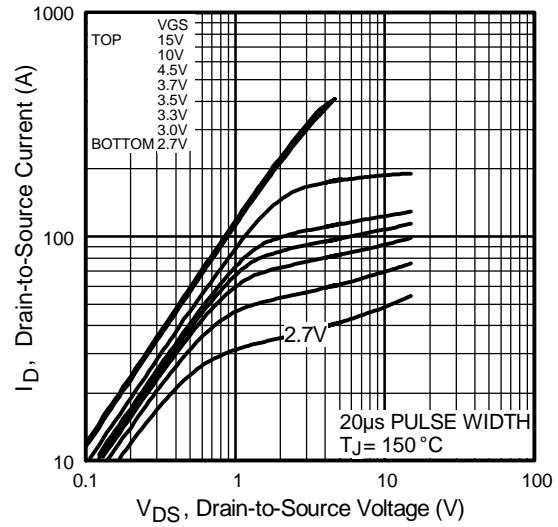


Fig 2. Typical Output Characteristics

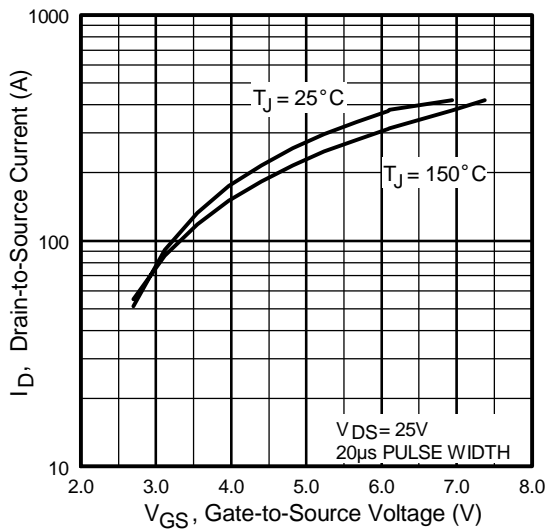


Fig 3. Typical Transfer Characteristics

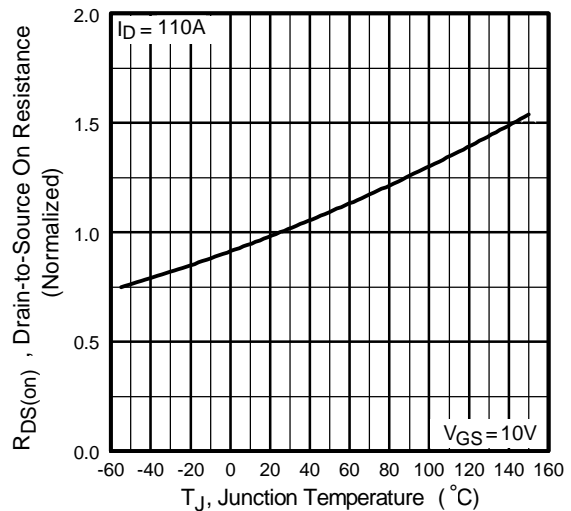


Fig 4. Normalized On-Resistance Vs. Temperature

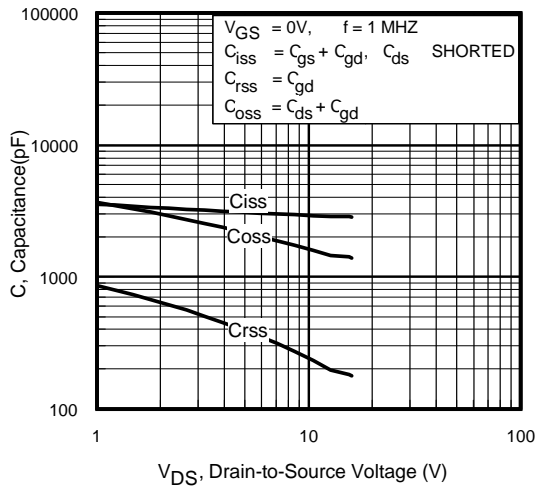


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

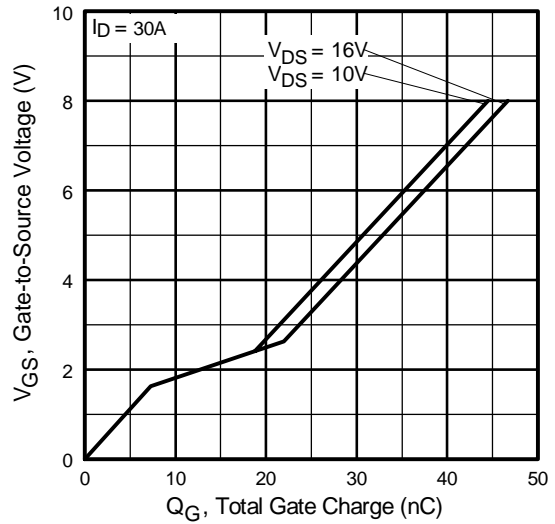


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

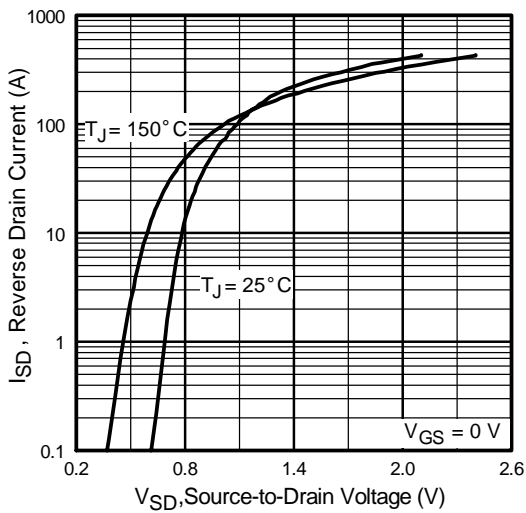


Fig 7. Typical Source-Drain Diode Forward Voltage

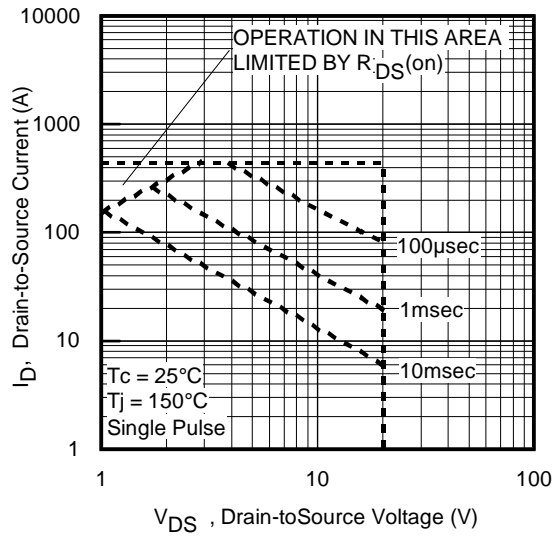


Fig 8. Maximum Safe Operating Area

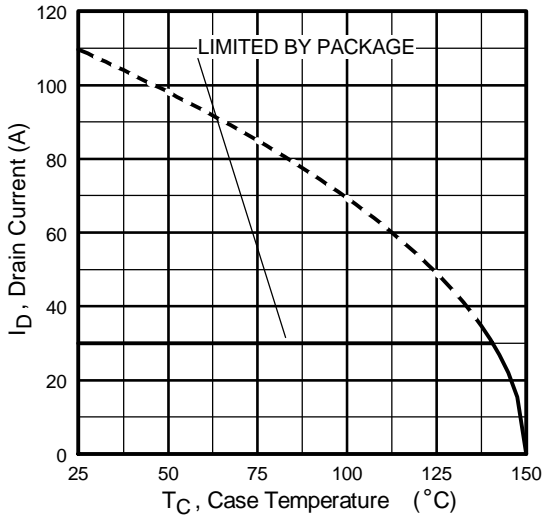


Fig 9. Maximum Drain Current Vs. Case Temperature

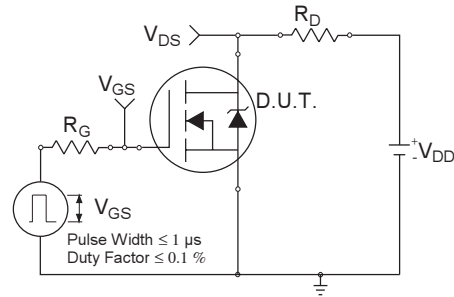


Fig 10a. Switching Time Test Circuit

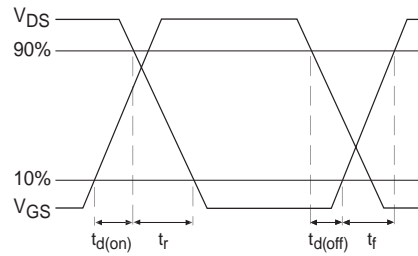


Fig 10b. Switching Time Waveforms

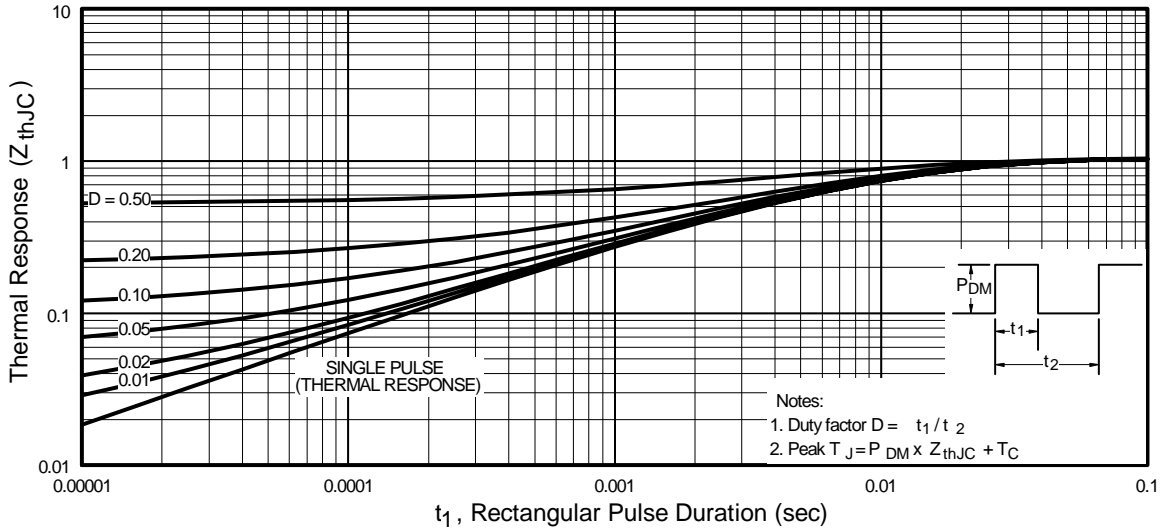


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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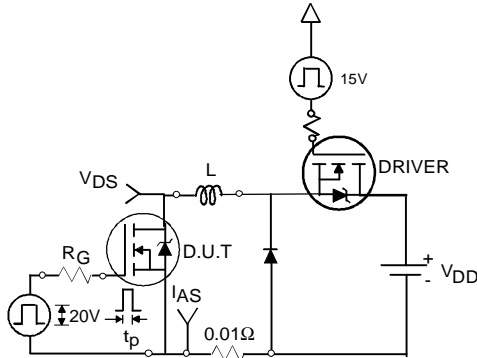


Fig 12a. Unclamped Inductive Test Circuit

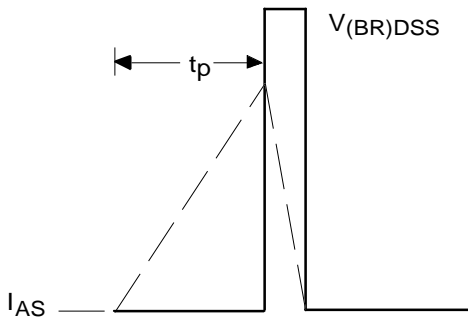


Fig 12b. Unclamped Inductive Waveforms

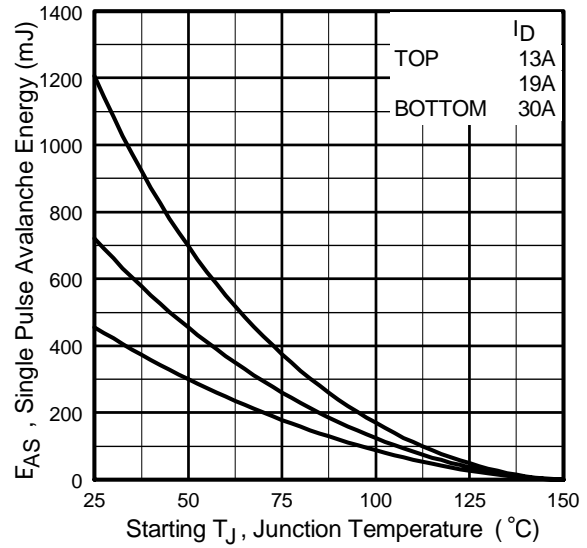


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

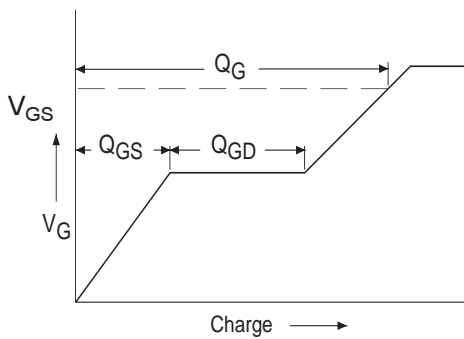


Fig 13a. Basic Gate Charge Waveform

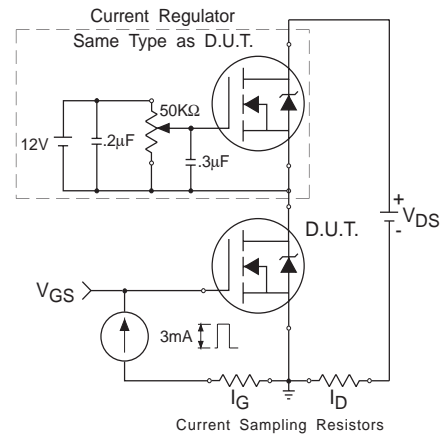


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

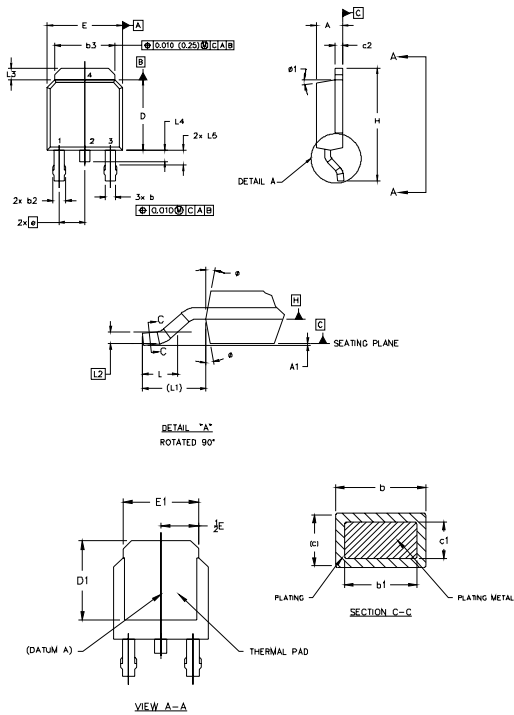
Fig 14. For N-Channel HEXFET® Power MOSFETs

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D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
 - 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
 - 3.0 LEAD DIMENSION UNCONTROLLED IN L5
 - 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
 - 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
 - 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.13		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	4.35	5.46	.190	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5.97	6.22	.236	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.52	-	.170	-	4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.14 REF.		.08 REF.		
L2	0.051 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	3
e	0"	10"	0"	10"	
e1	0"	15"	0"	15"	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

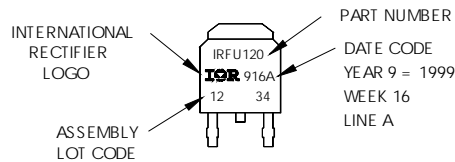
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

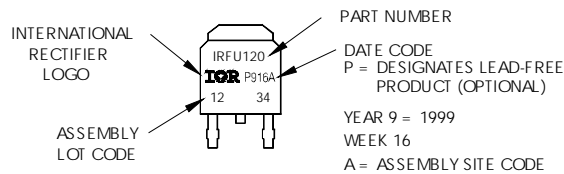
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"



OR

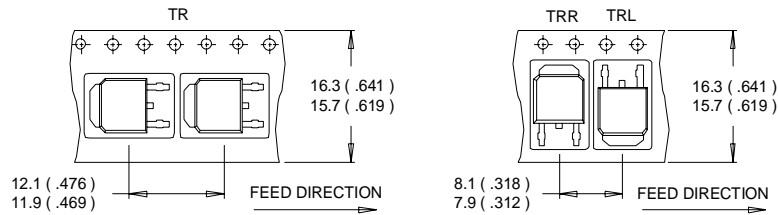


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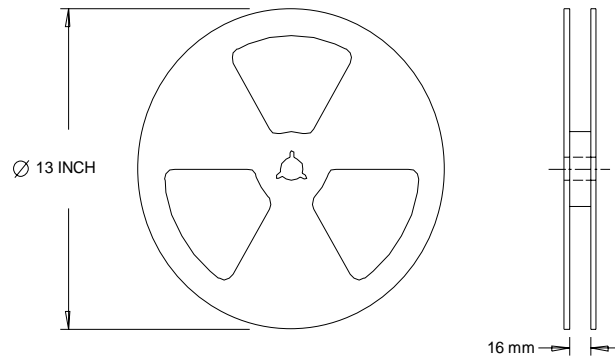
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D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.0\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 30\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994
- ⑥ R_θ is measured at T_J approximately at 90°C

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management