



**THE DATASHEET OF
IRFR7446TRPBF**



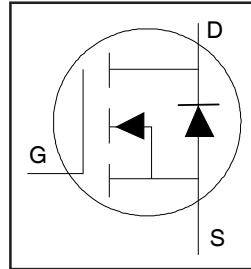
Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- PWM Inverterized topologies
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters

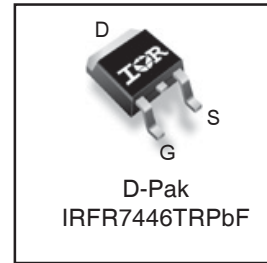
Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- Lead-Free

HEXFET® Power MOSFET



V_{DS}		40V
$R_{DS(on)}$	typ.	3.0mΩ
	max.	3.9mΩ
I_D (Silicon Limited)		120A Ⓢ
I_D (Package Limited)		56A



G	D	S
Gate	Drain	Source

Ordering Information

Orderable part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRFR7446PBF	D-PAK	Tube/Bulk	75	IRFR7446PBF
IRFR7446TRPBF	D-PAK	Tape and Reel	2000	IRFR7446TRPBF

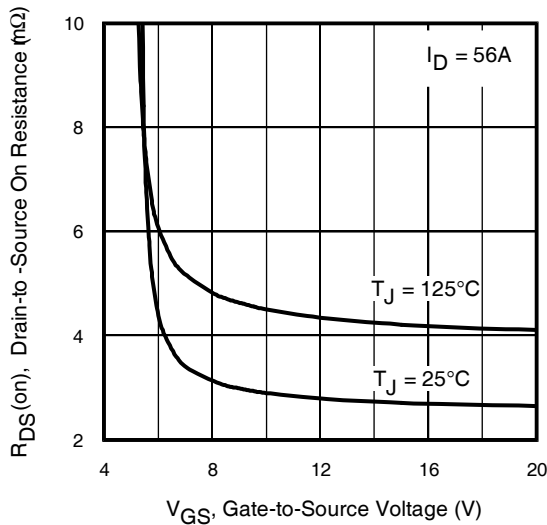


Fig 1. Typical On-Resistance vs. Gate Voltage

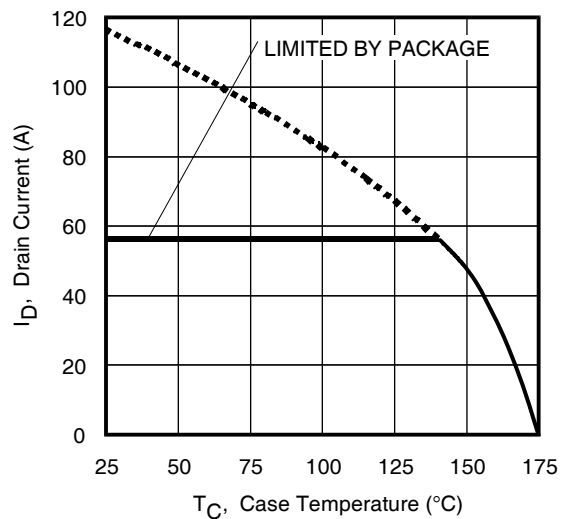


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	120 ^①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	84 ^①	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	56	
I_{DM}	Pulsed Drain Current ^②	520	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	98	W
	Linear Derating Factor	0.66	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^③	125	mJ
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^④	251	
I_{AR}	Avalanche Current ^②	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ^②		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ^⑤	—	1.52	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ^⑥	—	50	
$R_{\theta JA}$	Junction-to-Ambient ^⑥	—	110	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$ ^⑦
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	26	—	mV/°C	Reference to 25°C , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.0	3.9	mΩ	$V_{GS} = 10\text{V}$, $I_D = 56\text{A}$ ^⑧
		—	4.4	—	mΩ	$V_{GS} = 6.0\text{V}$, $I_D = 28\text{A}$ ^⑧
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	$V_{DS} = V_{GS}$, $I_D = 100\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40\text{V}$, $V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
R_G	Internal Gate Resistance	—	1.5	—	Ω	

Notes:

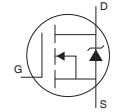
- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.08\text{mH}$
 $R_G = 50\Omega$, $I_{AS} = 56\text{A}$, $V_{GS} = 10\text{V}$.
- ④ $I_{SD} \leq 100\text{A}$, $di/dt \leq 1306\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ C_{OSS} eff. (TR) is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ C_{OSS} eff. (ER) is a fixed capacitance that gives the same energy as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C .
- ⑩ Limited by T_{Jmax} starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 22\text{A}$, $V_{GS} = 10\text{V}$.
- * L_D and L_S are Internal Drain Inductance and Internal Source Inductance

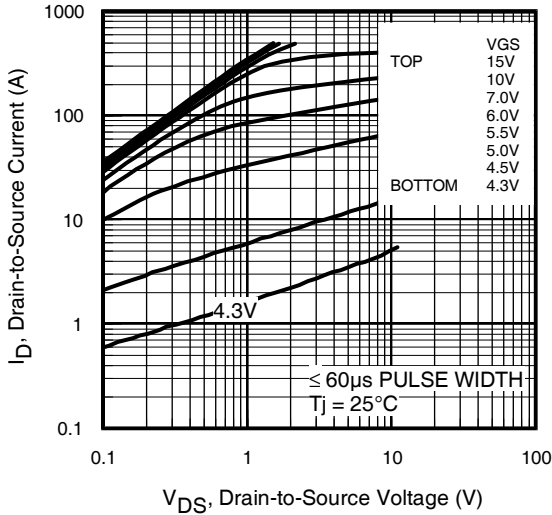
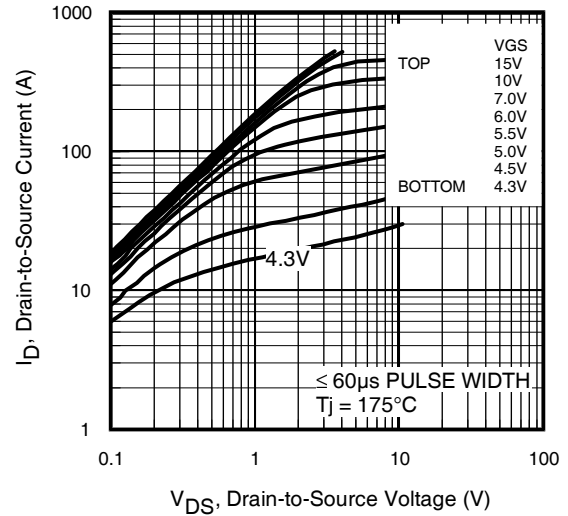
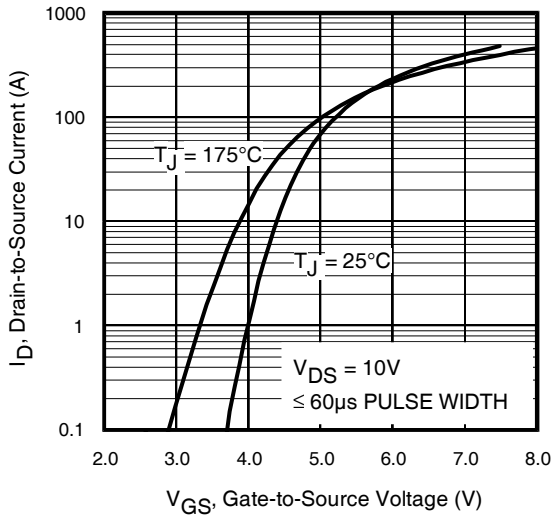
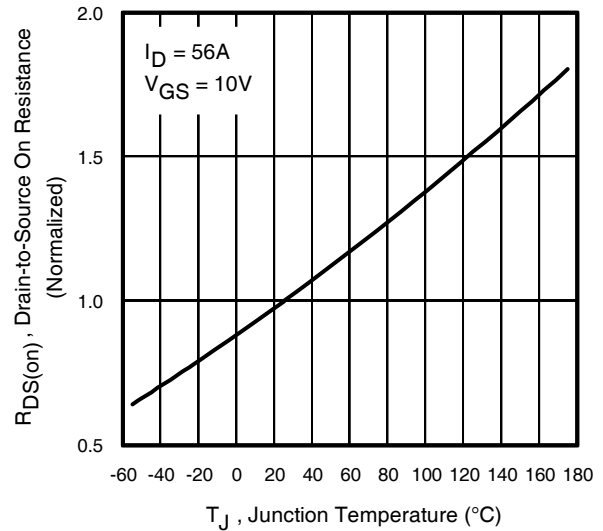
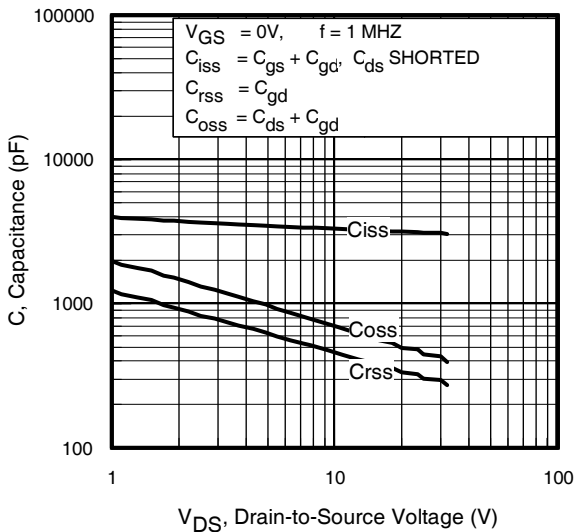
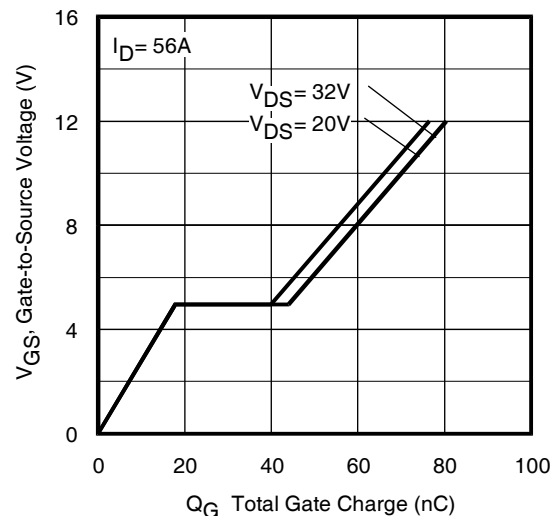
Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	170	—	—	S	V _{DS} = 10V, I _D = 56A
Q _g	Total Gate Charge	—	65	130	nC	I _D = 56A V _{DS} = 20V V _{GS} = 10V ⑤
Q _{gs}	Gate-to-Source Charge	—	18	—		
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	22	—		
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})	—	43	—		
t _{d(on)}	Turn-On Delay Time	—	9.8	—	ns	V _{DD} = 20V I _D = 30A R _G = 2.7Ω V _{GS} = 10V ⑤
t _r	Rise Time	—	13	—		
t _{d(off)}	Turn-Off Delay Time	—	32	—		
t _f	Fall Time	—	20	—		
C _{iss}	Input Capacitance	—	3150	—	pF	V _{GS} = 0V V _{DS} = 25V f = 1.0 MHz, See Fig. 5
C _{oss}	Output Capacitance	—	480	—		
C _{rss}	Reverse Transfer Capacitance	—	330	—		
C _{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	570	—		
C _{oss} eff. (TR)	Effective Output Capacitance (Time Related)	—	680	—		

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	120 ①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ②	—	—	480	A	
V _{SD}	Diode Forward Voltage	—	0.9	1.3	V	T _J = 25°C, I _S = 56A, V _{GS} = 0V
dv/dt	Peak Diode Recovery ④	—	4.8	—	V/ns	T _J = 175°C, I _S = 56A, V _{DS} = 40V ⑤
t _{rr}	Reverse Recovery Time	—	20	—	ns	T _J = 25°C V _R = 34V, T _J = 125°C I _F = 56A
Q _{rr}	Reverse Recovery Charge	—	13	—		
I _{RRM}	Reverse Recovery Current	—	1.8	—	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) *				




Fig 3. Typical Output Characteristics

Fig 4. Typical Output Characteristics

Fig 5. Typical Transfer Characteristics

Fig 6. Normalized On-Resistance vs. Temperature

Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

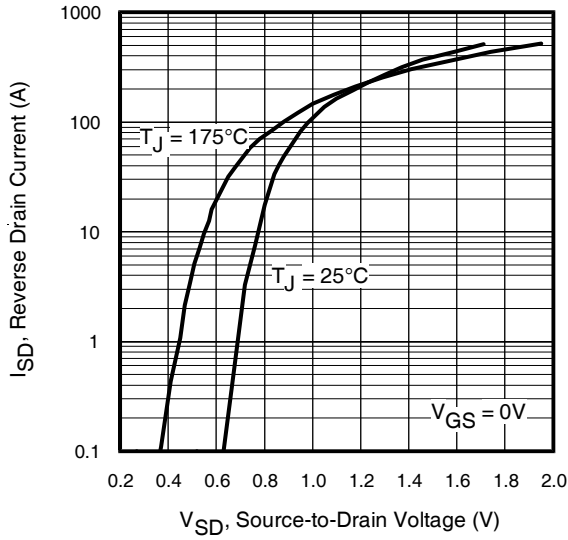


Fig 9. Typical Source-Drain Diode Forward Voltage

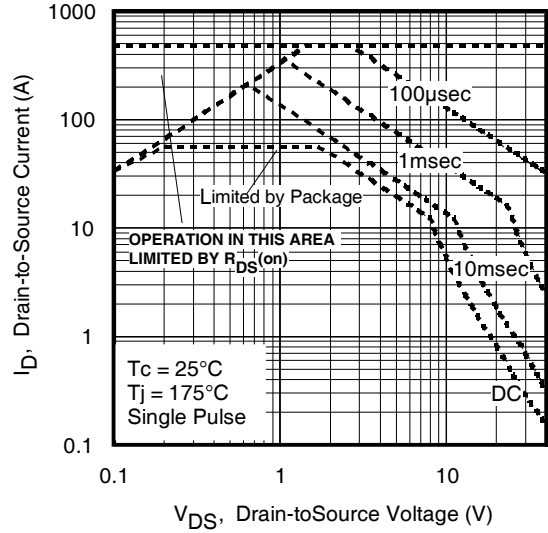


Fig 10. Maximum Safe Operating Area

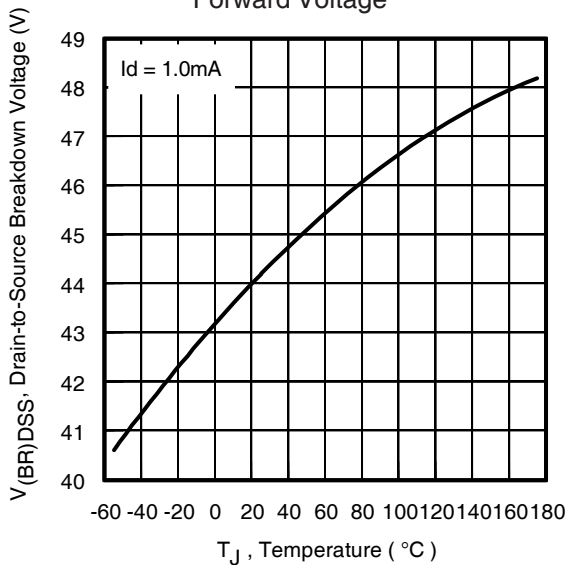


Fig 11. Drain-to-Source Breakdown Voltage

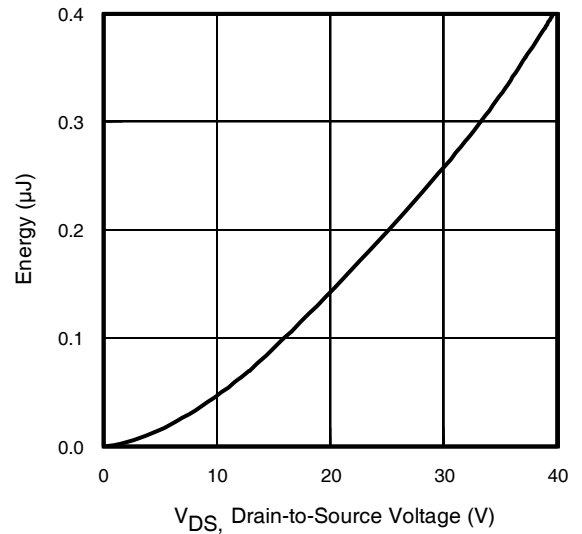


Fig 12. Typical C_{OSS} Stored Energy

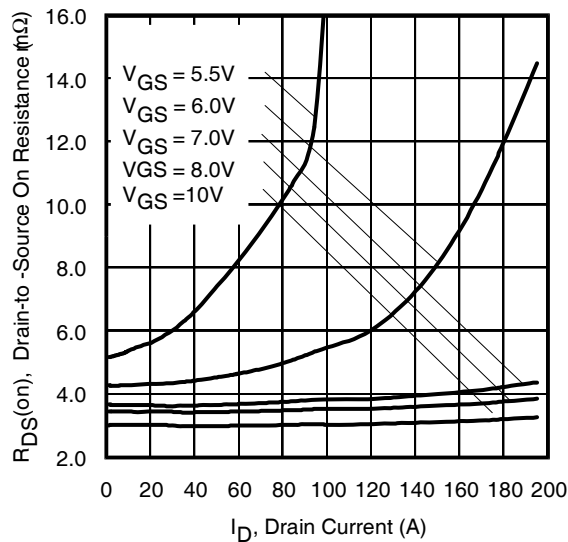
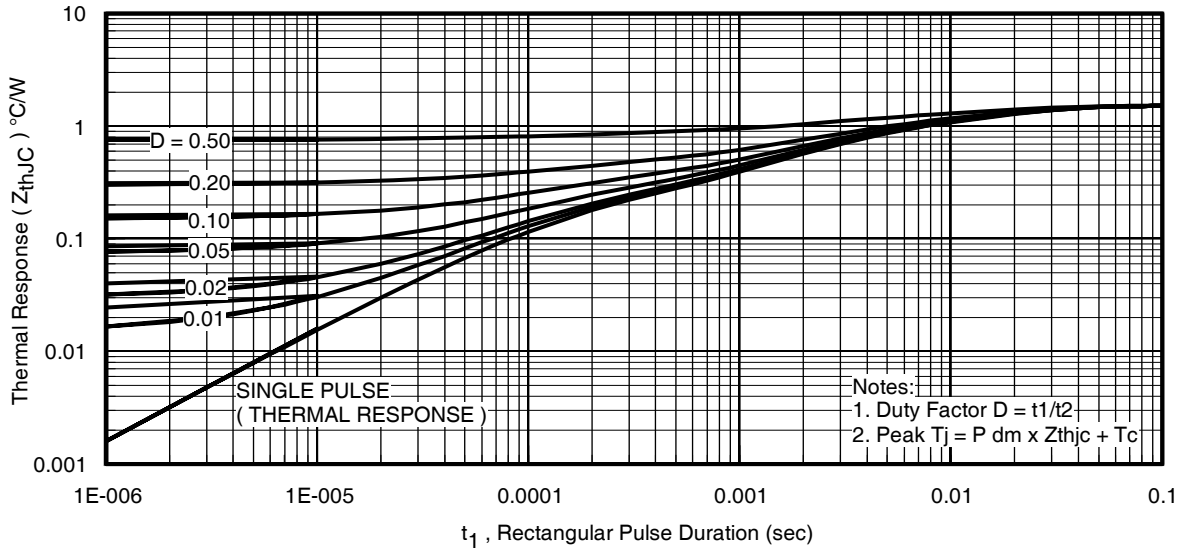
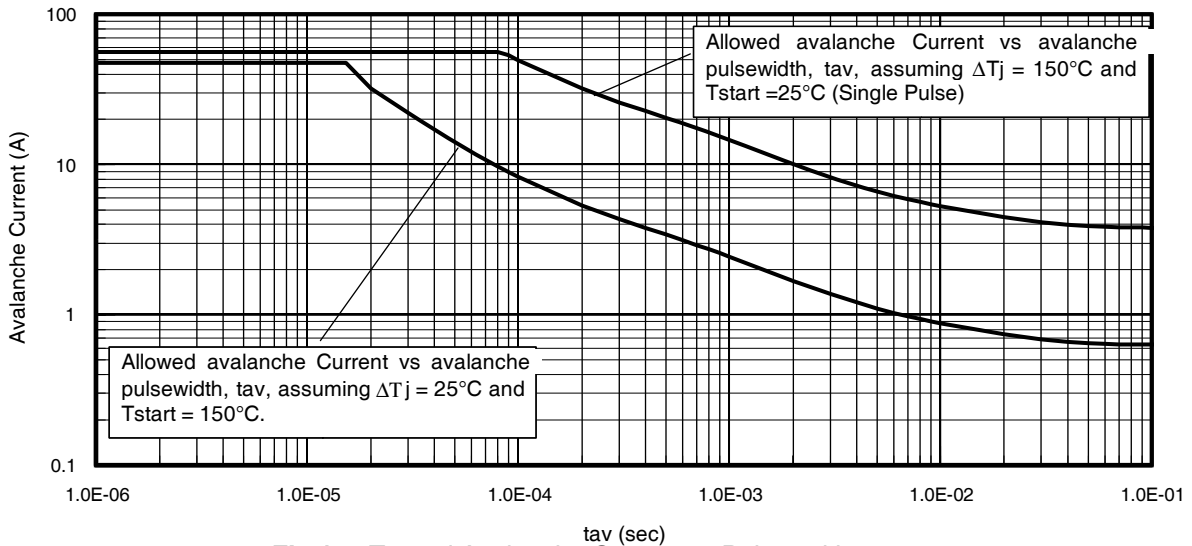
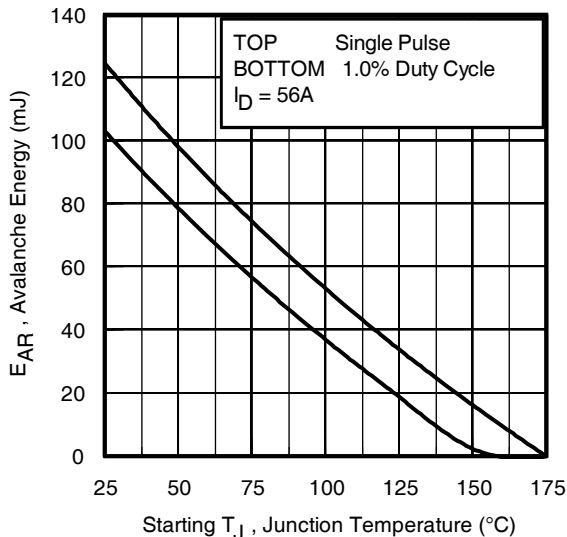


Fig 13. Typical On-Resistance vs. Drain Current

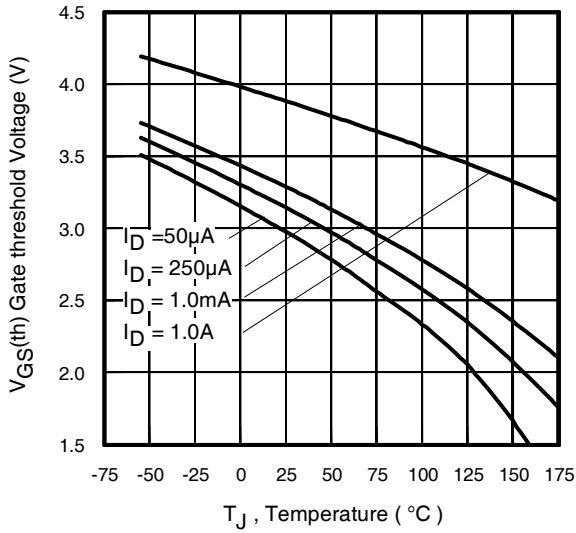
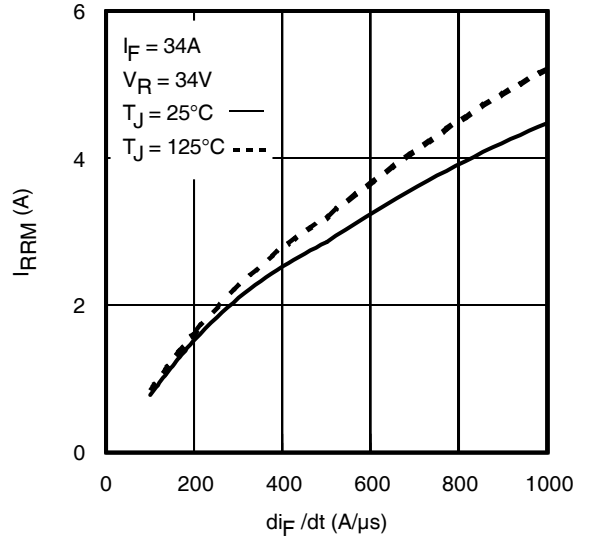
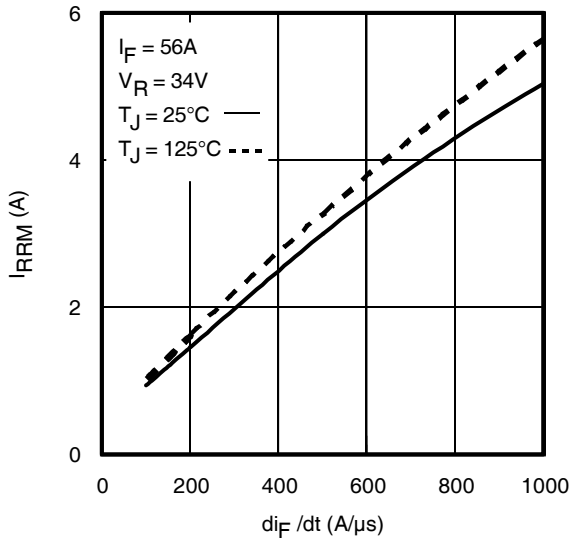
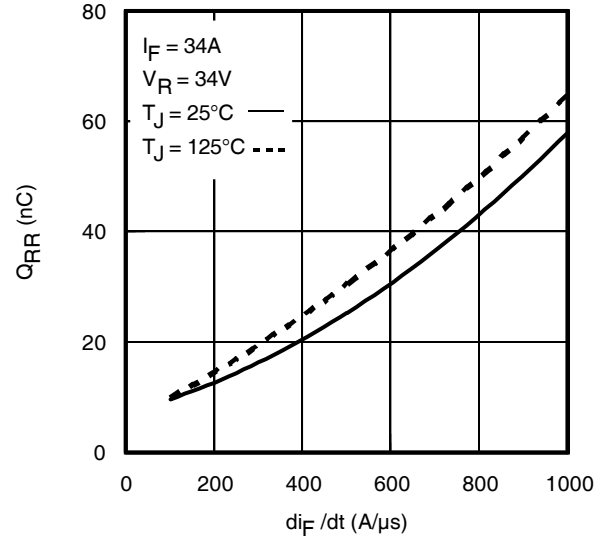
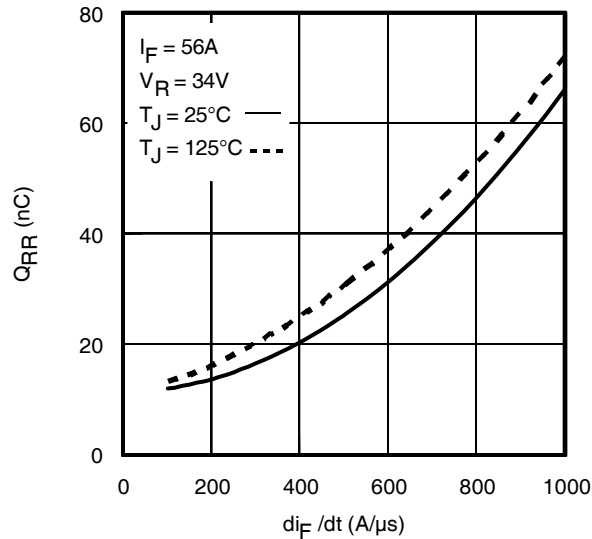

Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 15. Typical Avalanche Current vs. Pulsewidth

Fig 16. Maximum Avalanche Energy vs. Temperature
**Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)**

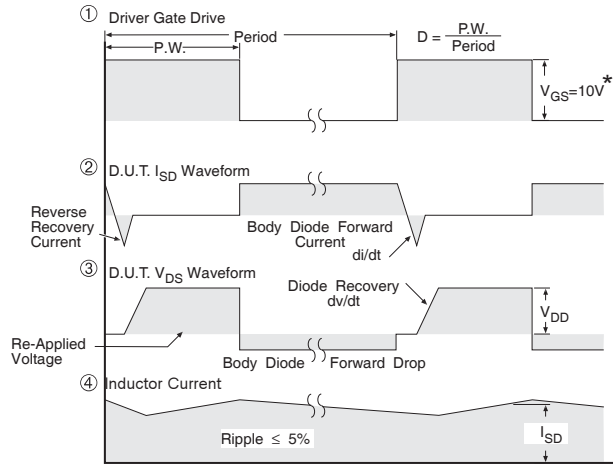
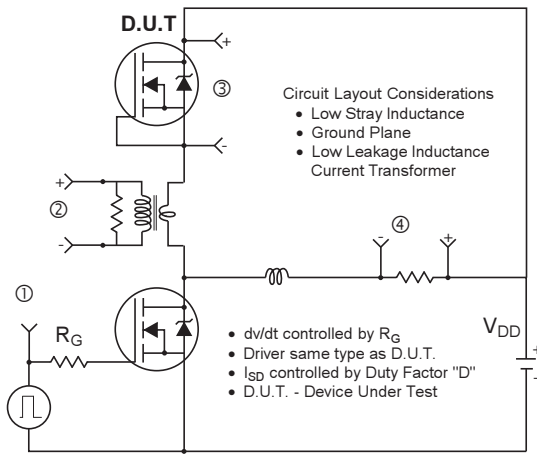
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


Fig 17. Threshold Voltage vs. Temperature

Fig. 18 - Typical Recovery Current vs. di_F/dt

Fig. 19 - Typical Recovery Current vs. di_F/dt

Fig. 20 - Typical Stored Charge vs. di_F/dt

Fig. 21 - Typical Stored Charge vs. di_F/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET[®] Power MOSFETs

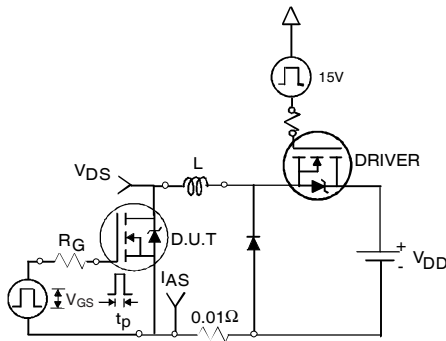


Fig 23a. Unclamped Inductive Test Circuit

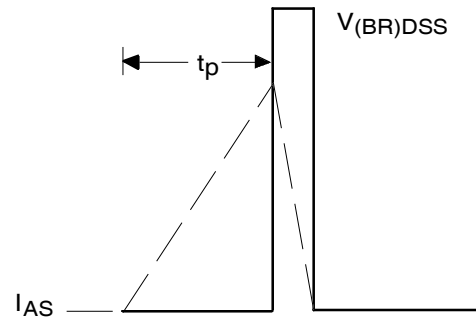


Fig 23b. Unclamped Inductive Waveforms

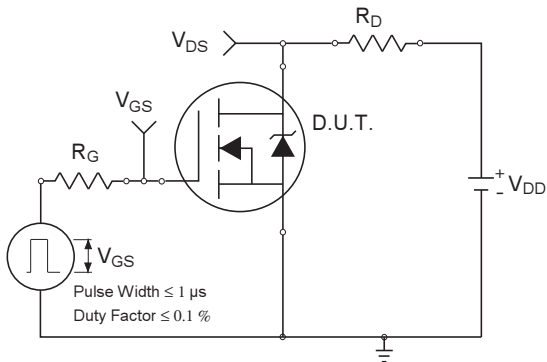


Fig 24a. Switching Time Test Circuit

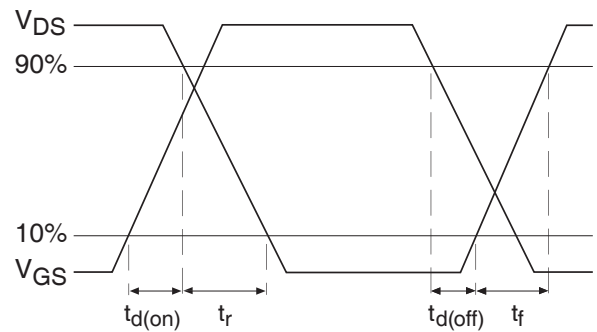


Fig 24b. Switching Time Waveforms

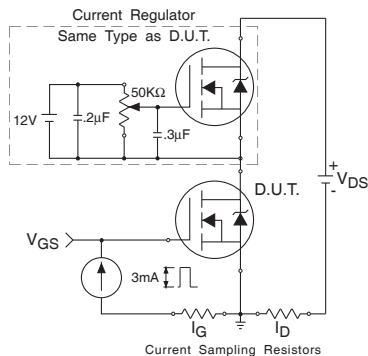


Fig 25a. Gate Charge Test Circuit

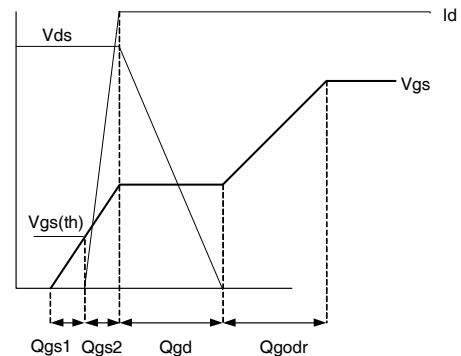
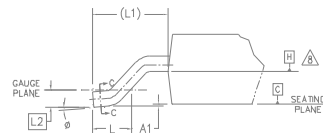
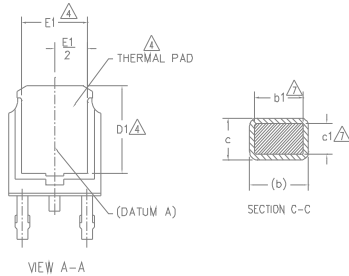
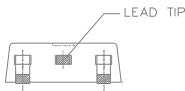
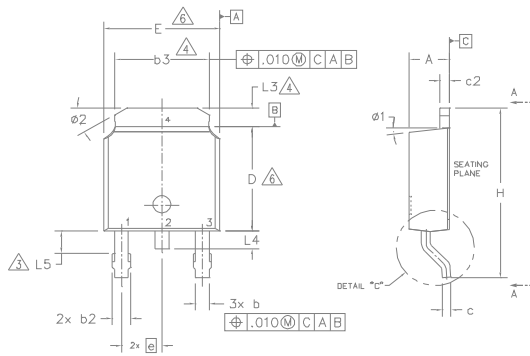


Fig 25b. Gate Charge Waveform

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
phi	0*	10*	0*	10*	
phi 1	0*	15*	0*	15*	
phi 2	25*	35*	25*	35*	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

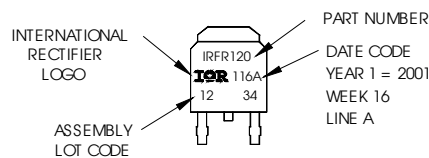
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information

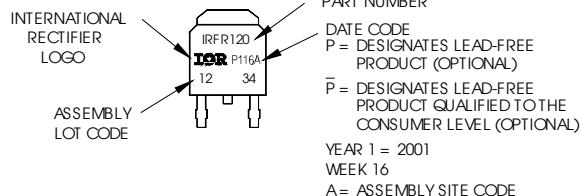
EXAMPLE: THIS IS AN IRFR120 WITH ASSEMBLY LOT CODE 1234 ASSEMBLED ON WW 16, 2001 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

"P" in assembly line position indicates "Lead-Free" qualification to the consumer-level



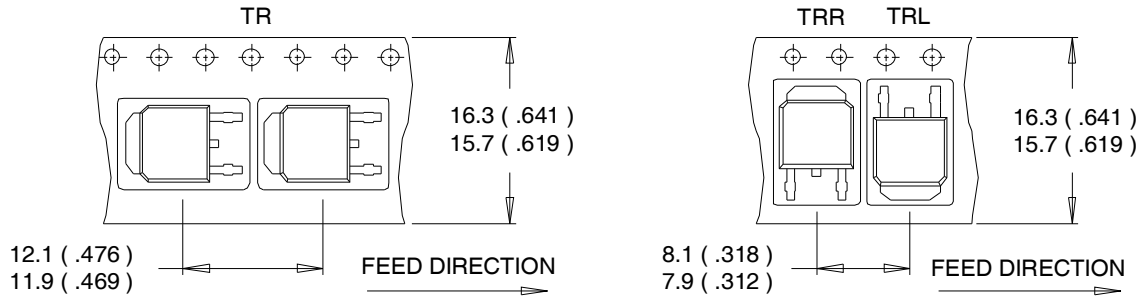
OR



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

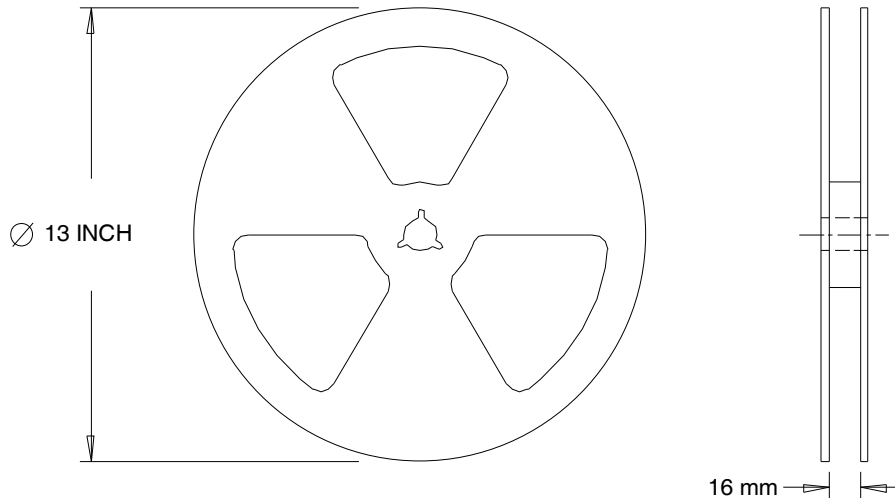
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification information[†]

Qualification level	Industrial ^{††}	
	(per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	D-PAK	MSL1
		(per JEDEC J-STD-020D ^{†††})
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: <http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comment
1/6/2015	<ul style="list-style-type: none"> • Updated $E_{AS(L=1mH)} = 251mJ$ on page 2 • Updated note 10 "Limited by T_{Jmax}, starting $T_J = 25^{\circ}C$, $L = 1mH$, $R_G = 50\Omega$, $I_{AS} = 22A$, $V_{GS} = 10V$". on page 2 • Updated package outline on page 9.

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