

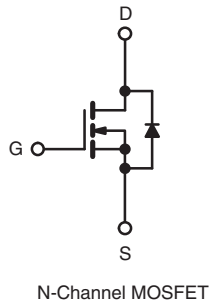
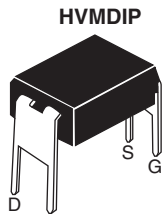


**THE DATASHEET OF
IRLD014PBF**



Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ (Ω)	$V_{GS} = 5\text{ V}$ 0.20
Q_g (Max.) (nC)	8.4
Q_{gs} (nC)	2.6
Q_{gd} (nC)	6.4
Configuration	Single



FEATURES

- Dynamic dV/dt Rating
- For Automatic Insertion
- End Stackable
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS} = 4\text{ V}$ and 5 V
- $175\text{ }^\circ\text{C}$ Operating Temperature
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertible case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain servers as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRLD014PbF
	SiHLD014-E3
SnPb	IRLD014
	SiHLD014

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 10	
Continuous Drain Current	V_{GS} at 5.0 V	I_D	$T_A = 25\text{ }^\circ\text{C}$	A
			$T_A = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a		I_{DM}	14	
Linear Derating Factor			0.0083	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b		E_{AS}	490	mJ
Maximum Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	P_D	1.3	W
Peak Diode Recovery dV/dt^c		dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d	

Notes

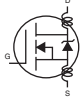
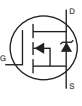
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 197\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 1.7\text{ A}$ (see fig. 12).
- $I_{SD} \leq 10\text{ A}$, $dI/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^\circ\text{C}$.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	60	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C , $I_D = 1\text{ mA}$	-	0.070	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.0	-	2.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 10\text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	25	μA	
		$V_{DS} = 48\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 150\text{ °C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}$	-	-	0.20	Ω	
		$V_{GS} = 4.0\text{ V}$	-	-	0.28		
Forward Transconductance	g_{fs}	$V_{DS} = 25\text{ V}$, $I_D = 1.0\text{ A}^b$	1.9	-	-	S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}$ $f = 1.0\text{ MHz}$, see fig. 5	-	400	-	pF	
Output Capacitance	C_{oss}		-	170	-		
Reverse Transfer Capacitance	C_{rss}		-	42	-		
Total Gate Charge	Q_g	$V_{GS} = 5.0\text{ V}$	$I_D = 10\text{ A}$, $V_{DS} = 48\text{ V}$ see fig. 6 and 13 ^b	-	-	8.4	nC
Gate-Source Charge	Q_{gs}			-	-	2.6	
Gate-Drain Charge	Q_{gd}			-	-	6.4	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}$, $I_D = 10\text{ A}$ $R_g = 12\text{ }\Omega$, $R_D = 2.8\text{ }\Omega$, see fig. 10 ^b	-	9.3	-	ns	
Rise Time	t_r		-	110	-		
Turn-Off Delay Time	$t_{d(off)}$		-	17	-		
Fall Time	t_f		-	26	-		
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal Source Inductance	L_S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	1.7	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	14	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ °C}$, $I_S = 1.7\text{ A}$, $V_{GS} = 0\text{ V}^b$	-	-	1.6	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}$, $I_F = 10\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	93	130	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.34	0.65	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

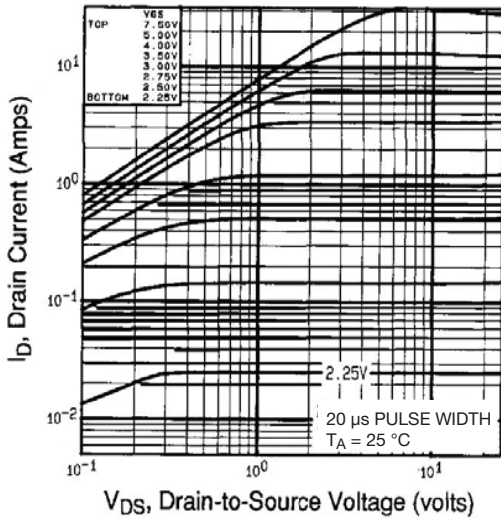


Fig. 1 - Typical Output Characteristics, $T_A = 25\text{ }^\circ\text{C}$

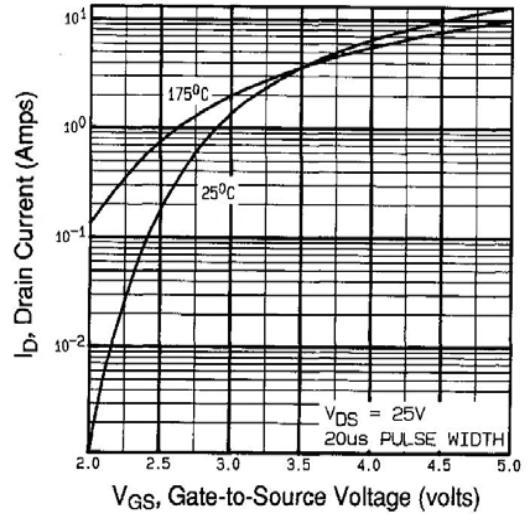


Fig. 3 - Typical Transfer Characteristics

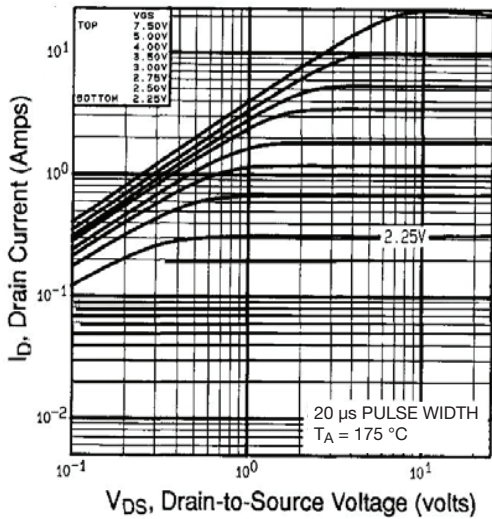


Fig. 2 - Typical Output Characteristics, $T_A = 175\text{ }^\circ\text{C}$

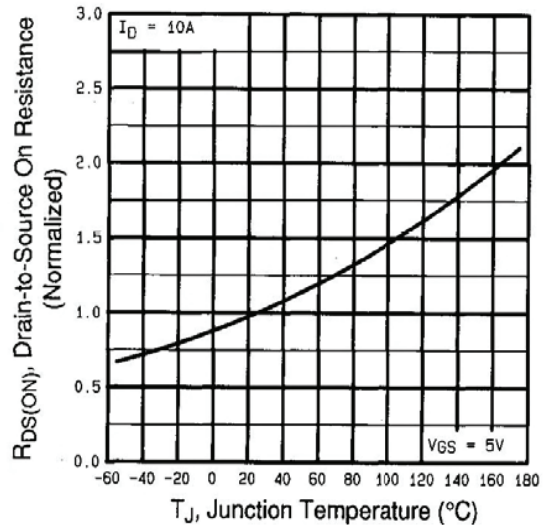


Fig. 4 - Normalized On-Resistance vs. Temperature

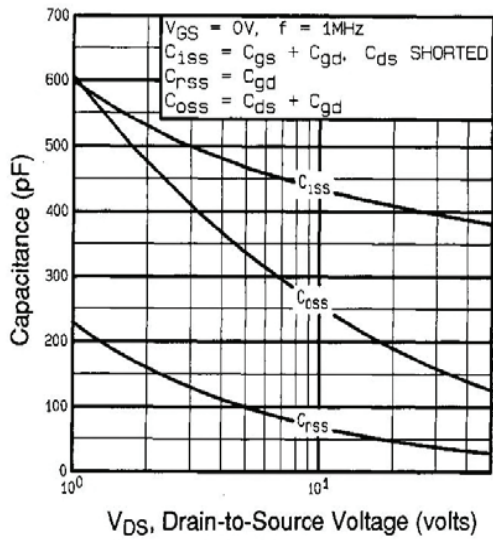


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

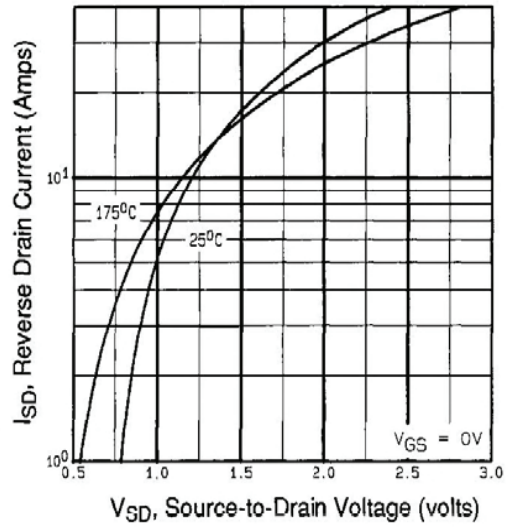


Fig. 7 - Typical Source-Drain Diode Forward Voltage

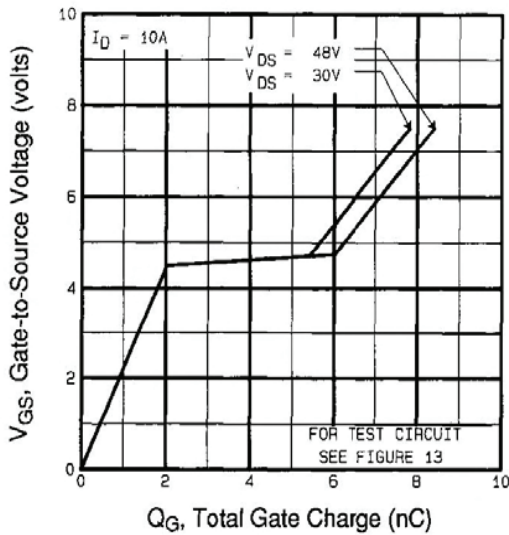


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

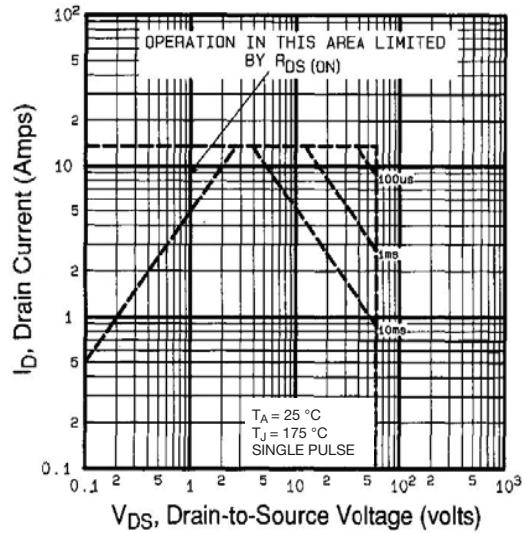


Fig. 8 - Maximum Safe Operating Area

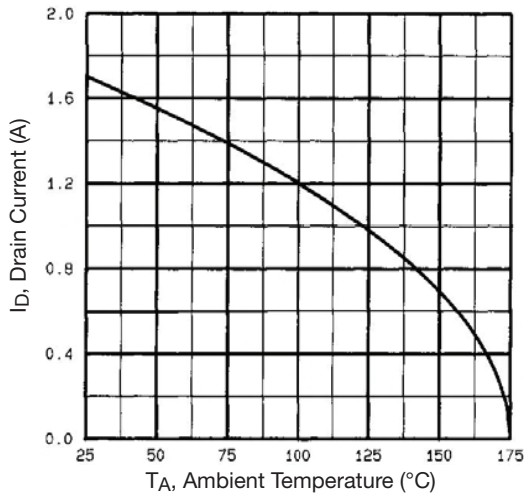


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

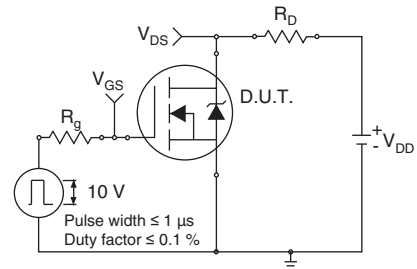


Fig. 10a - Switching Time Test Circuit

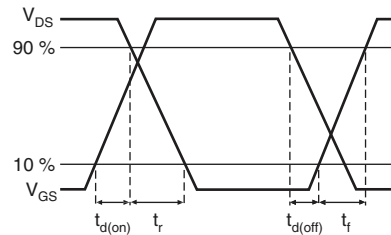


Fig. 10b - Switching Time Waveforms

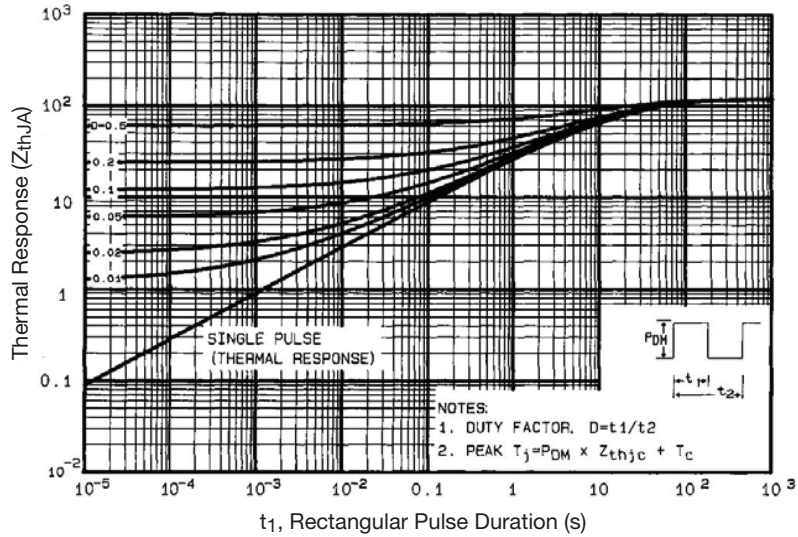


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

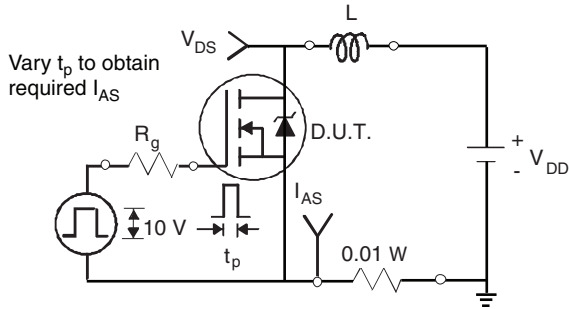


Fig. 12a - Unclamped Inductive Test Circuit

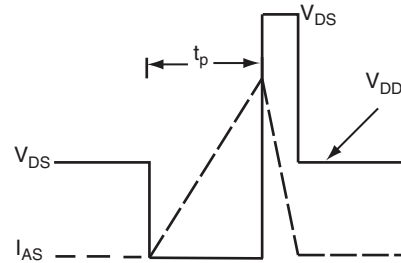


Fig. 12b - Unclamped Inductive Waveforms

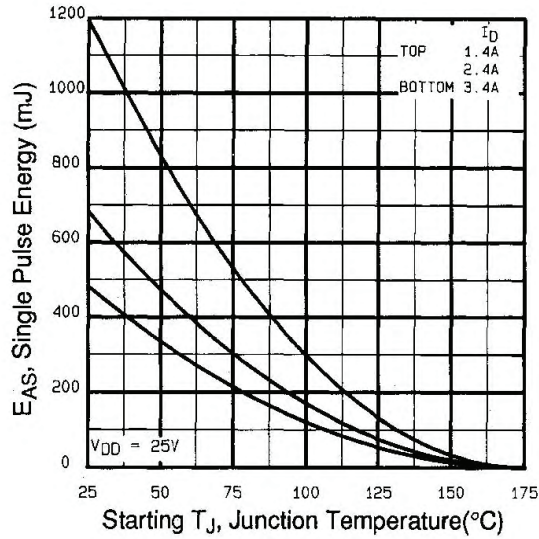


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

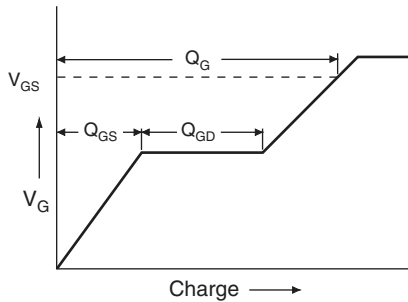


Fig. 13a - Basic Gate Charge Waveform

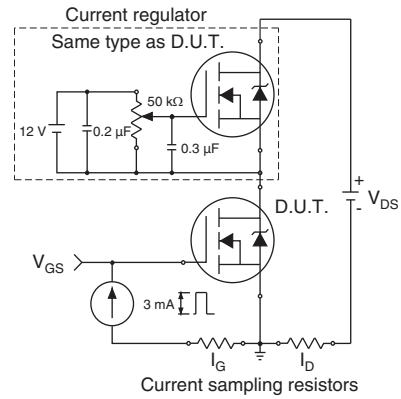
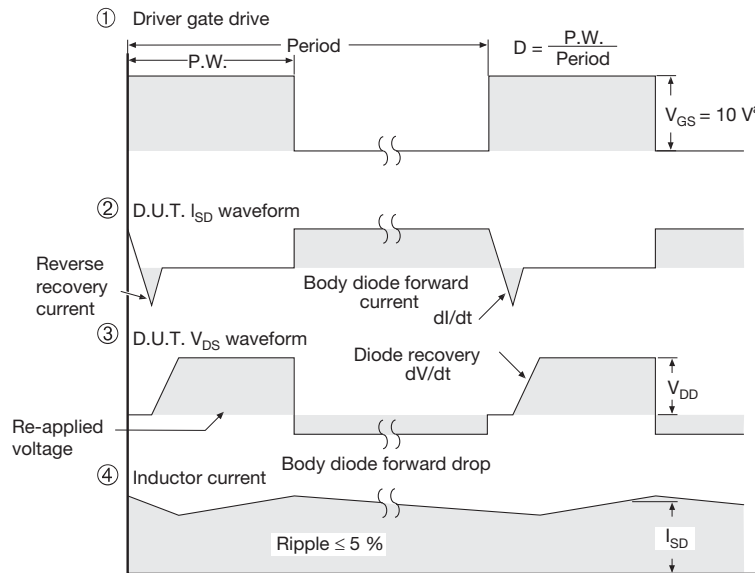
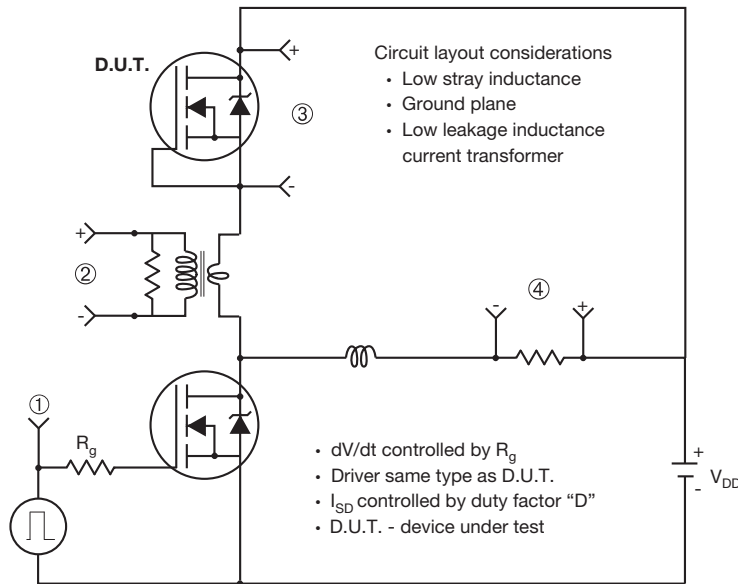


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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