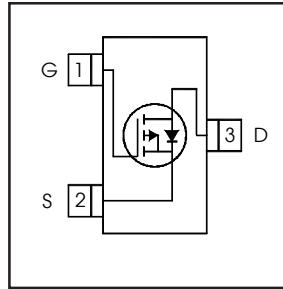




- Generation V Technology
- Ultra Low On-Resistance
- P-Channel MOSFET
- SOT-23 Footprint
- Low Profile (<1.1mm)
- Available in Tape and Reel
- Fast Switching
- Lead-Free
- RoHS Compliant, Halogen-Free

HEXFET® Power MOSFET

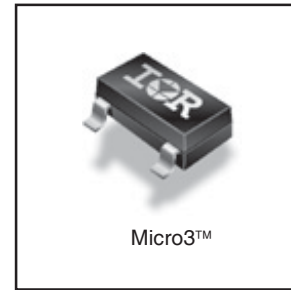


$V_{DSS} = -30V$   
 $R_{DS(on)} = 0.60\Omega$

**Description**

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

A customized leadframe has been incorporated into the standard SOT-23 package to produce a HEXFET Power MOSFET with the industry's smallest footprint. This package, dubbed the Micro3, is ideal for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the Micro3 allows it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.



Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLML5103TRPbF	Micro3™ (SOT-23)	Tape and Reel	3000	IRLML5103TRPbF

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-0.76	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-0.61	
$I_{DM}$	Pulsed Drain Current ①	-4.8	
$P_D @ T_A = 25^\circ C$	Power Dissipation	540	mW
	Linear Derating Factor	4.3	mW/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ②	-5.0	V/ns
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to + 150	°C

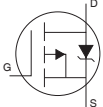
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	230	°C/W

**Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

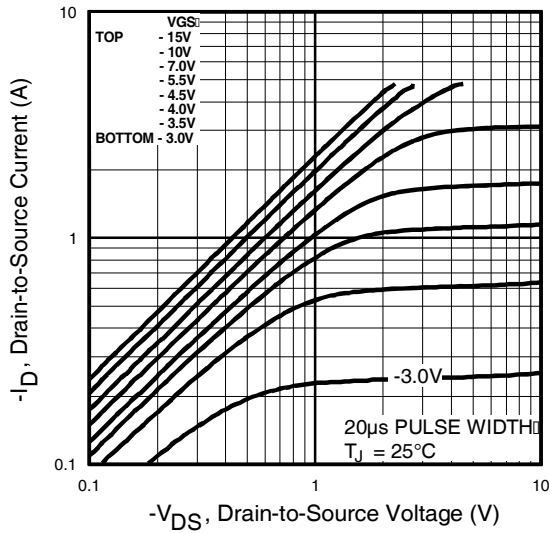
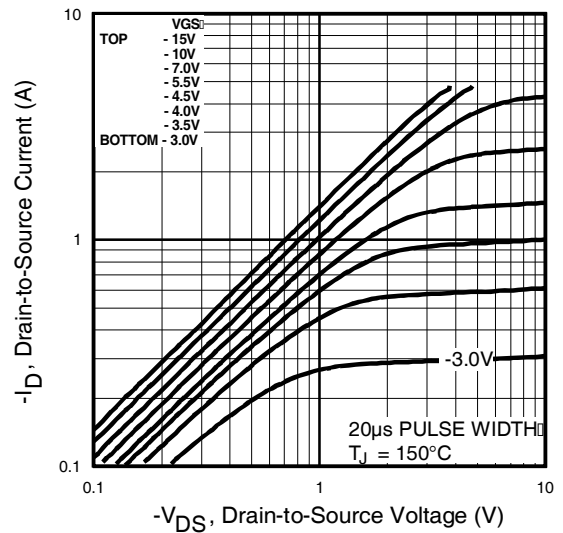
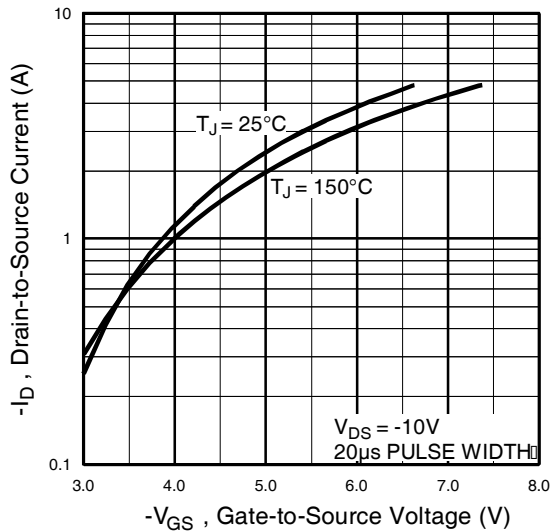
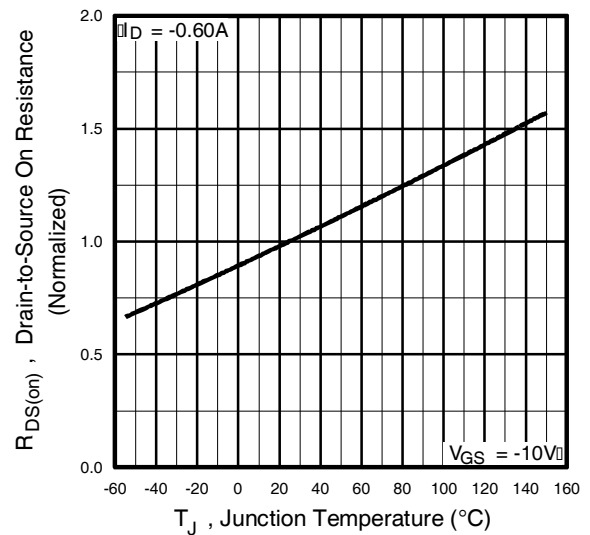
	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	-30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	-0.029	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1mA
R <sub>DS(ON)</sub>	Static Drain-to-Source On-Resistance	—	—	0.60	Ω	V <sub>GS</sub> = -10V, I <sub>D</sub> = -0.60A ③
		—	—	1.0		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -0.30A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.0	—	—	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
g <sub>fs</sub>	Forward Transconductance	0.44	—	—	S	V <sub>DS</sub> = -10V, I <sub>D</sub> = -0.30A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-1.0	μA	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V
		—	—	-25		V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	-100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V <sub>GS</sub> = 20V
Q <sub>g</sub>	Total Gate Charge	—	3.4	5.1	nC	I <sub>D</sub> = -0.60A
Q <sub>gs</sub>	Gate-to-Source Charge	—	0.52	0.78		V <sub>DS</sub> = -24V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	1.1	1.7		V <sub>GS</sub> = -10V, See Fig. 6 and 9 ③
t <sub>d(on)</sub>	Turn-On Delay Time	—	10	—	ns	V <sub>DD</sub> = -15V
t <sub>r</sub>	Rise Time	—	8.2	—		I <sub>D</sub> = -0.60A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	23	—		R <sub>G</sub> = 6.2Ω
t <sub>f</sub>	Fall Time	—	16	—		R <sub>D</sub> = 25Ω, See Fig. 10 ③
C <sub>iss</sub>	Input Capacitance	—	75	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	37	—		V <sub>DS</sub> = -25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	18	—		f = 1.0MHz, See Fig. 5

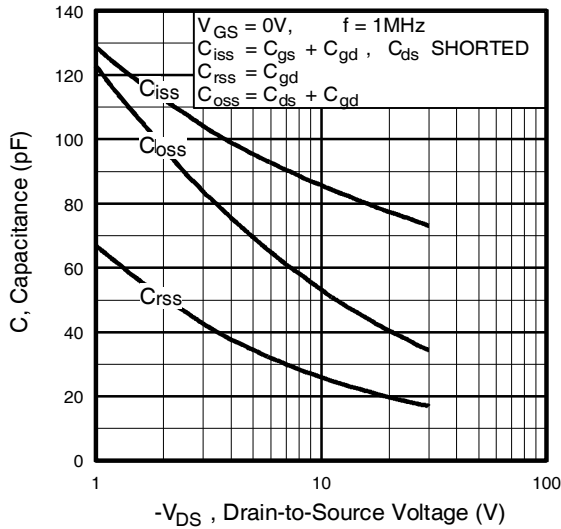
**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-0.54	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	-4.8		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -0.60A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	26	39	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -0.60A
Q <sub>rr</sub>	Reverse Recovery Charge	—	20	30	nC	di/dt = 100A/μs ③

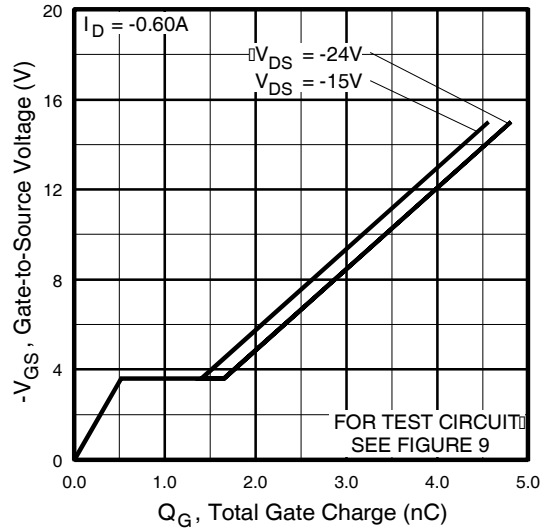
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② I<sub>SD</sub> ≤ -0.60A, di/dt ≤ 110A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 150°C
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ④ Surface mounted on FR-4 board, t ≤ 5sec.

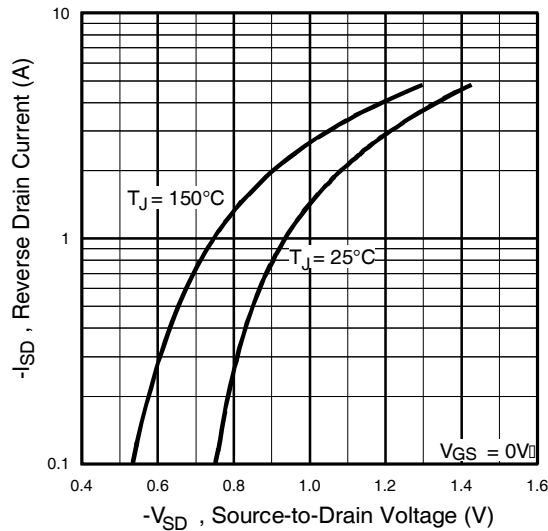

**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance Vs. Temperature**



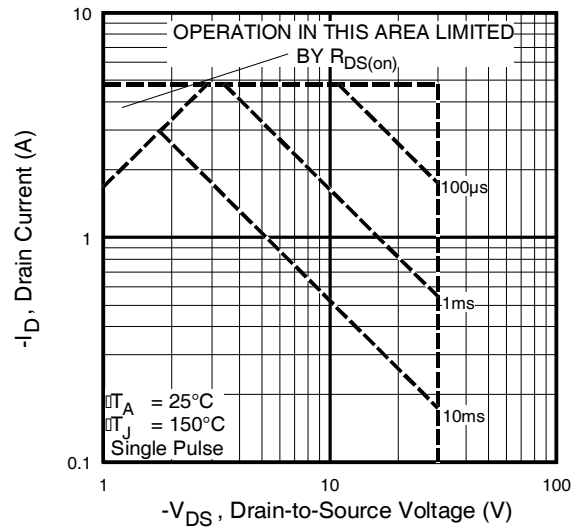
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



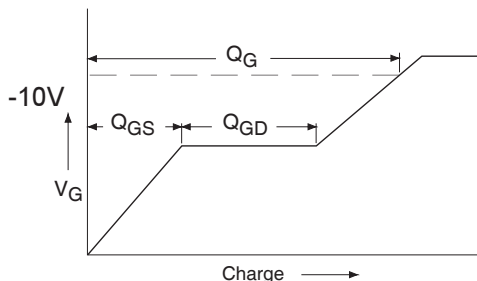
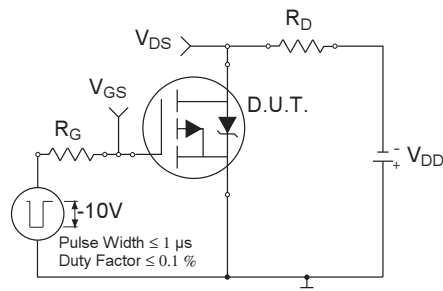
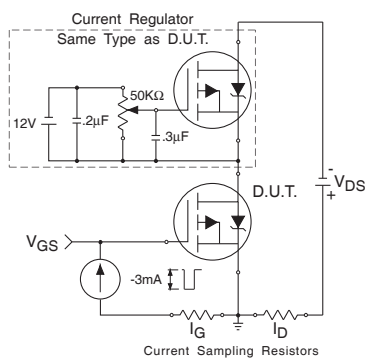
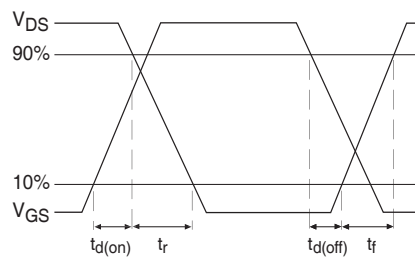
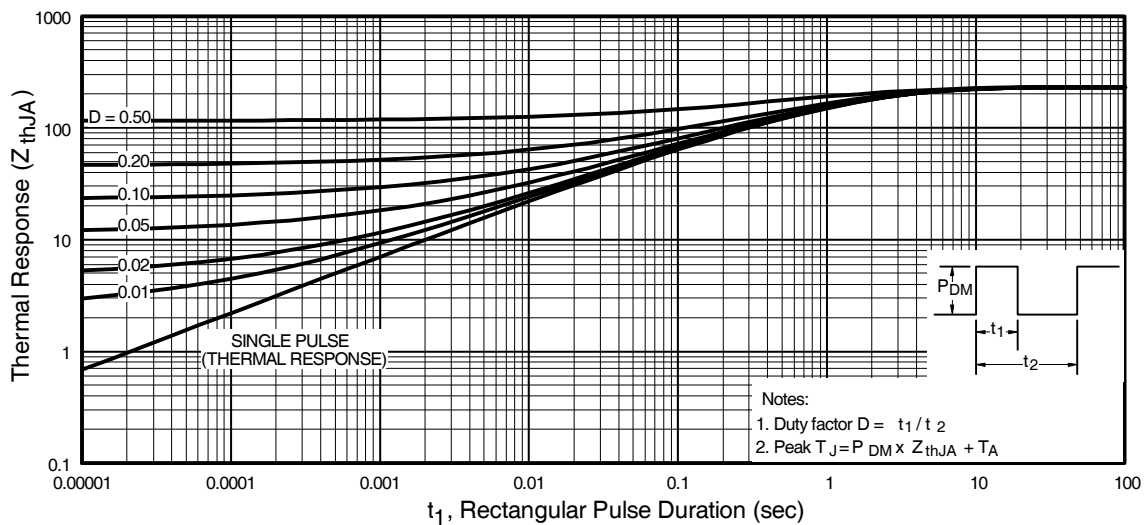
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



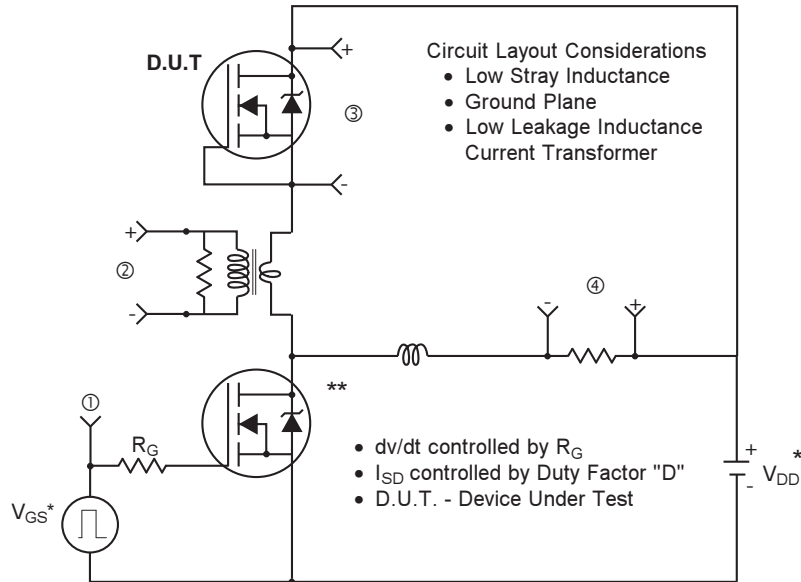
**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

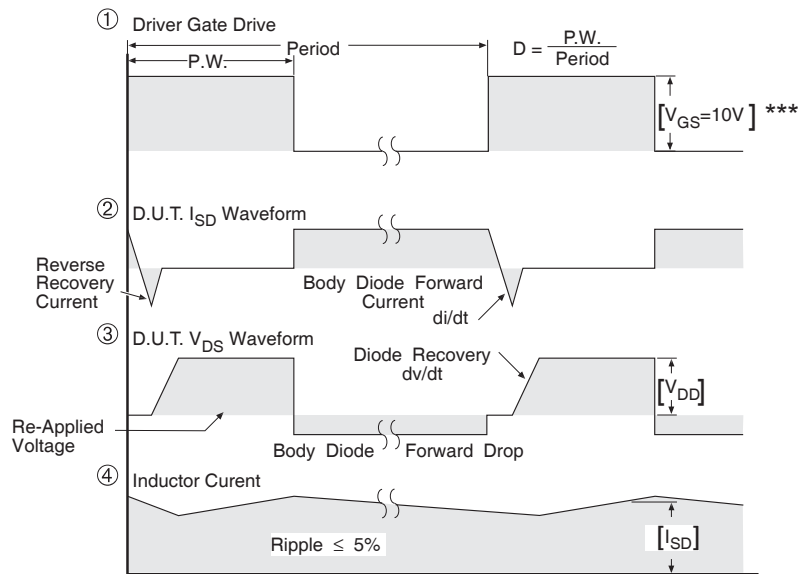

**Fig 9a. Basic Gate Charge Waveform**

**Fig 10a. Switching Time Test Circuit**

**Fig 9b. Gate Charge Test Circuit**

**Fig 10b. Switching Time Waveforms**

**Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**

### Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements

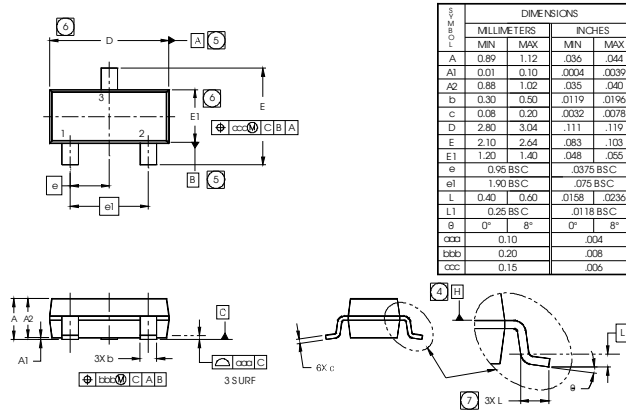


\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

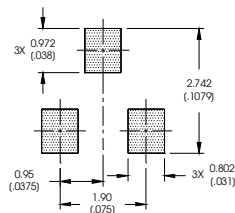
**Fig 13. For P-Channel HEXFETS**

### Micro3 (SOT-23) (Lead-Free) Package Outline

Dimensions are shown in millimeters (inches)



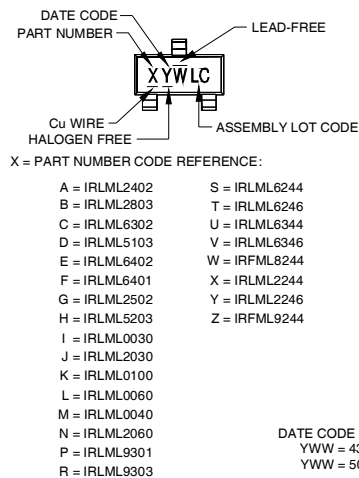
RECOMMENDED FOOTPRINT



- NOTES
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
  3. CONTROLLING DIMENSION: MILLIMETER.
  4. DATUM PLANE H IS LOCATED AT THE MOLD PARTING LINE.
  5. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
  6. DIMENSIONS D AND E1 ARE MEASURED AT DATUM PLANE H.
  7. DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
  8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-236AB.

### Micro3 (SOT-23 / TO-236AB) Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001



W = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

YEAR	Y	WORK WEEK	W
2011	2001	1 01	A
2012	2002	2 02	B
2013	2003	3 03	C
2014	2004	4 04	D
2015	2005	5	
2016	2006	6	
2017	2007	7	
2018	2008	8	
2019	2009	9	
2020	2010	0 24	X
		25	Y
		26	Z

W = (27-52) IF PRECEDED BY A LETTER

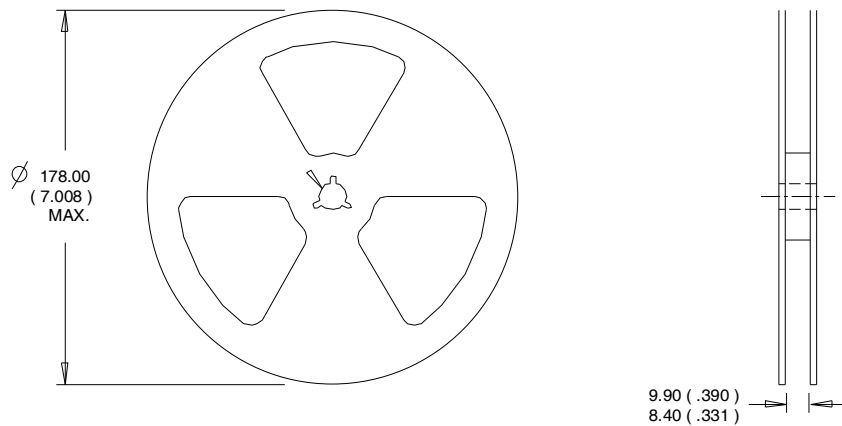
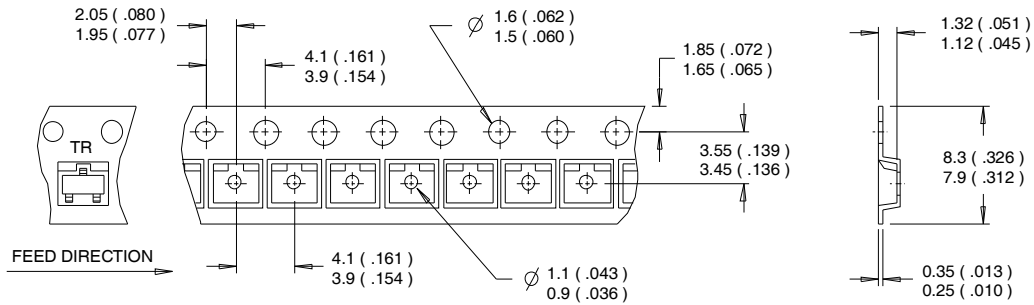
YEAR	Y	WORK WEEK	W
2011	2001	A 27	A
2012	2002	B 28	B
2013	2003	C 29	C
2014	2004	D 30	D
2015	2005	E	
2016	2006	F	
2017	2007	G	
2018	2008	H	
2019	2009	J	
2020	2010	K 50	X
		51	Y
		52	Z

DATE CODE EXAMPLE:  
 YWW = 432 = DF  
 YWW = 503 = 5C

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>

### Micro3™ Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
  2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>

**Qualification information<sup>†</sup>**

Qualification level	Consumer (per JEDEC JESD47F <sup>††</sup> guidelines)	
Moisture Sensitivity Level	Micro3 <sup>™</sup> (SOT-23)	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
RoHS compliant	Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability>

<sup>††</sup> Applicable version of JEDEC standard at the time of product release

**Revision History**

Date	Comment
4/24/2014	<ul style="list-style-type: none"> <li>• Updated data sheet with new IR corporate template.</li> <li>• Updated package outline &amp; part marking on page 7.</li> <li>• Added Qualification table -Qual level "Consumer" on page 9.</li> <li>• Added bullet point in the Benefits "RoHS Compliant, Halogen -Free" on page 1.</li> </ul>

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