

IRLR7811WPbF

HEXFET® Power MOSFET

Applications

- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- Lead-Free

V _{DSS}	R _{DS(on)} max	Q _g
30V	10.5mΩ	19nC

Benefits

- Very Low RDS(on) at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	64 ^④	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	45 ^④	
I _{DM}	Pulsed Drain Current ^①	260	
P _D @ T _C = 25°C	Power Dissipation	71	W
P _D @ T _A = 100°C	Power Dissipation*	1.5	
	Linear Derating Factor	0.48	W/°C
V _{GS}	Gate-to-Source Voltage	±12	V
T _J	Operating Junction and	-55 to +175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	2.1	°C/W
R _{θJA}	Junction-to-Ambient (PCB mount)*	—	50	
R _{θJA}	Junction-to-Ambient	—	110	

Notes ^① through ^④ are on page 9
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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	27	—	mV/°C	Reference to 25°C, I _D = 1mA ⑥
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	5.8	10.5	mΩ	V _{GS} = 10V, I _D = 15A ④
		—	7.0	15		V _{GS} = 4.5V, I _D = 12A
V _{GS(th)}	Gate Threshold Voltage	—	1.5	2.5	V	V _{DS} = V _{GS} , I _D = 250μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-5.0	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	30	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 12V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -12V
g _{fs}	Forward Transconductance	58	—	—	S	V _{DS} = 15V, I _D = 12A
Q _g	Total Gate Charge Control Fet	—	21	31	nC	
Q _{gs1}	Pre-V _{th} Gate-Source Charge	—	5.0	—		
Q _{gs2}	Post-V _{th} Gate-Source Charge	—	1.7	—		
Q _{gd}	Gate-to-Drain Charge	—	6.6	—		
Q _{gdtr}	Gate Charge Overdrive	—	5.5	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	8.3	—		
Q _g	Total Gate Charge Sync Fet	—	17	—		
Q _{oss}	Output Charge	—	10	—		
R _g	Gate Resistance	—	1.6	—		
t _{d(on)}	Turn-On Delay Time	—	18	—	ns	V _{DD} = 16V, V _{GS} = 4.5V ④ I _D = 12A Clamped Inductive Load
t _r	Rise Time	—	4.8	—		
t _{d(off)}	Turn-Off Delay Time	—	11	—		
t _f	Fall Time	—	23	—		
C _{iss}	Input Capacitance	—	2260	—	pF	V _{GS} = 0V V _{DS} = 15V f = 1.0MHz
C _{oss}	Output Capacitance	—	420	—		
C _{rss}	Reverse Transfer Capacitance	—	180	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	140	mJ
I _{AR}	Avalanche Current③	—	12	A
E _{AR}	Repetitive Avalanche Energy③	—	7.1	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	64 ④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	260		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 12A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	30	45	ns	T _J = 25°C, I _F = 12A
Q _{rr}	Reverse Recovery Charge	—	27	41	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

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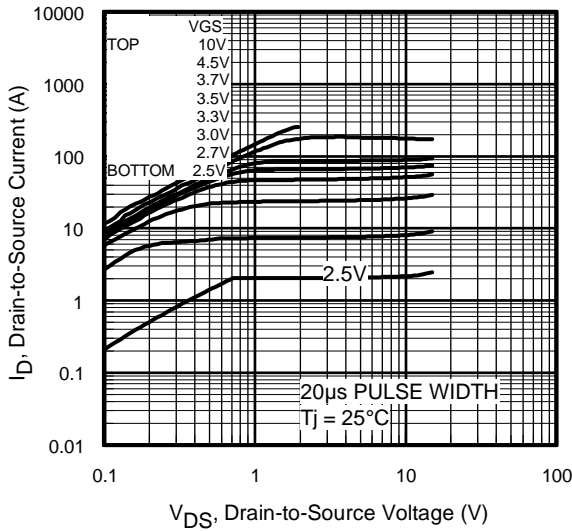


Fig 1. Typical Output Characteristics

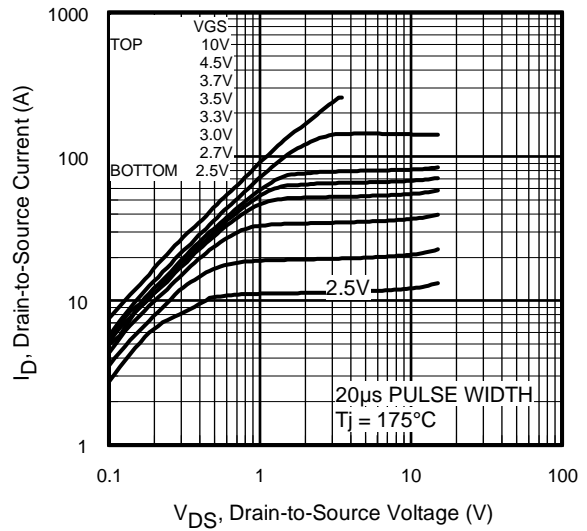


Fig 2. Typical Output Characteristics

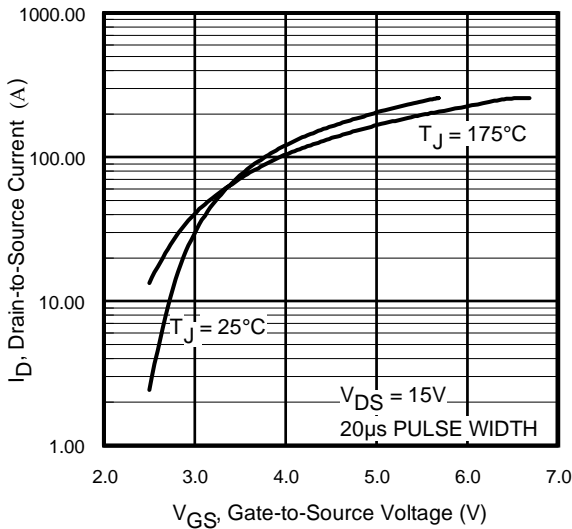


Fig 3. Typical Transfer Characteristics

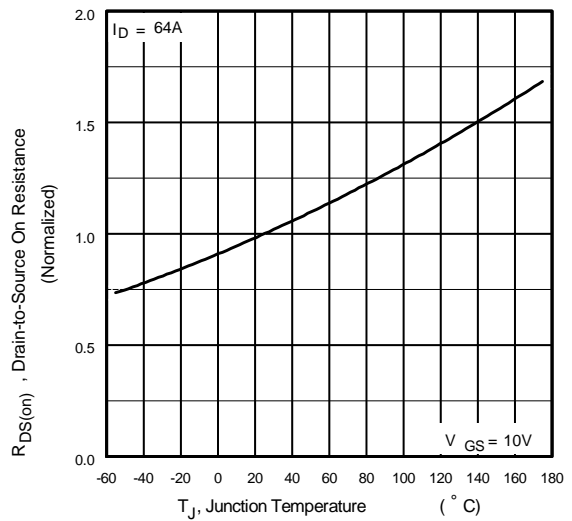


Fig 4. Normalized On-Resistance Vs. Temperature

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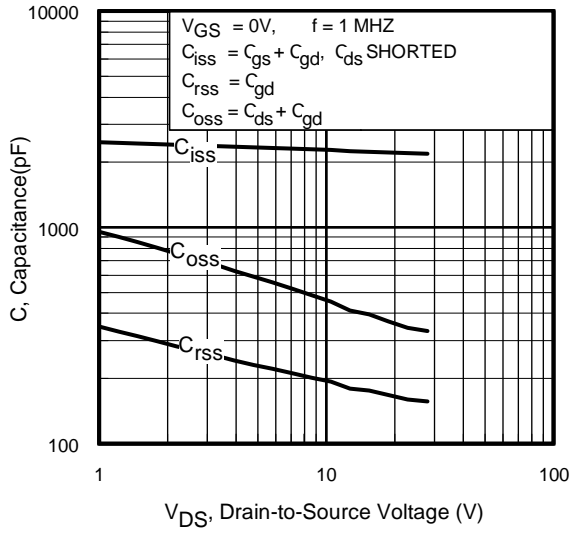


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

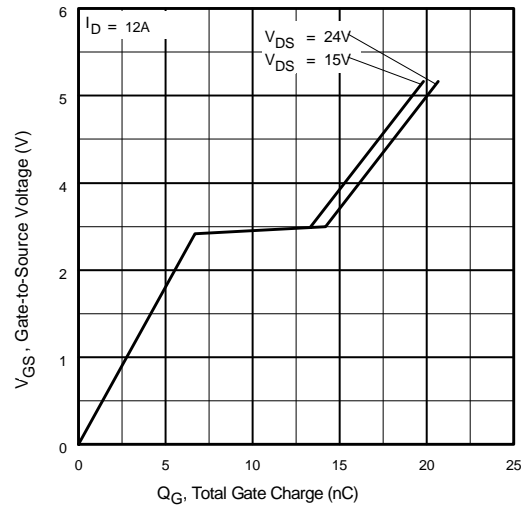


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

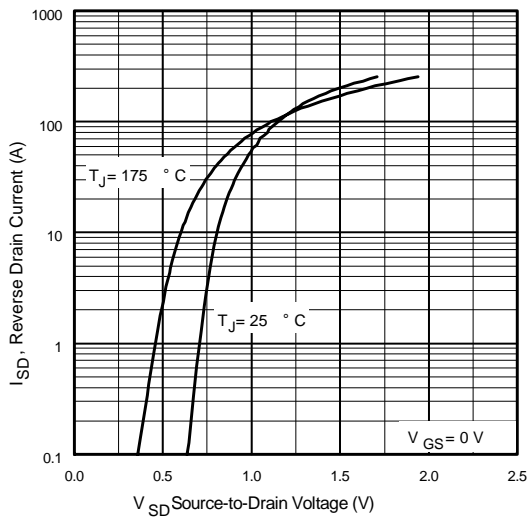


Fig 7. Typical Source-Drain Diode Forward Voltage

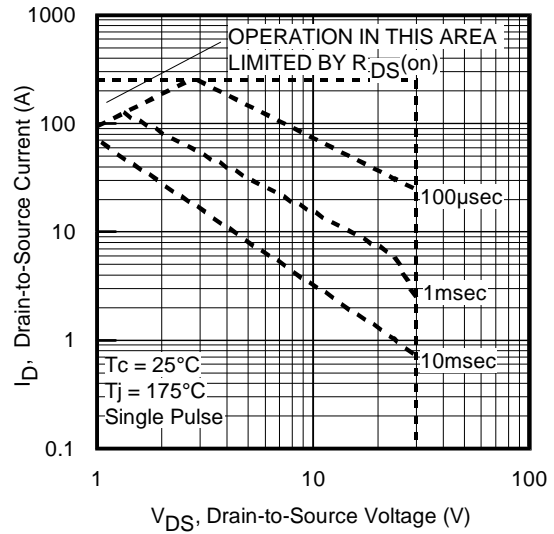


Fig 8. Maximum Safe Operating Area

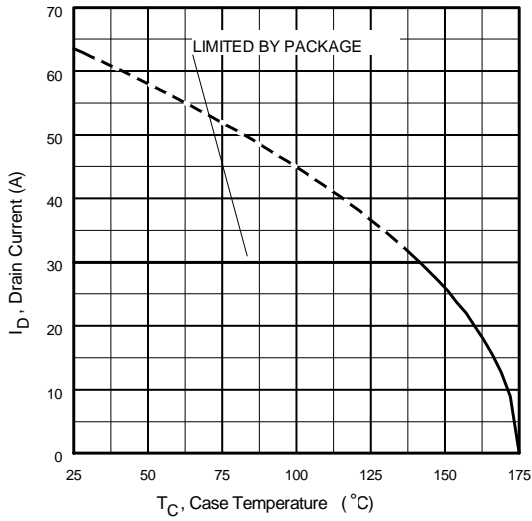


Fig 9. Maximum Drain Current Vs. Case Temperature

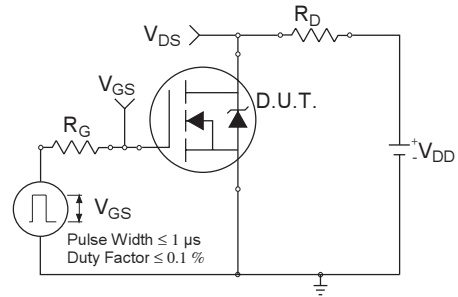


Fig 10a. Switching Time Test Circuit

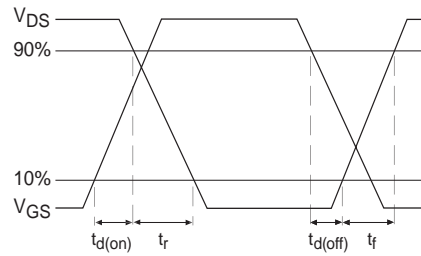


Fig 10b. Switching Time Waveforms

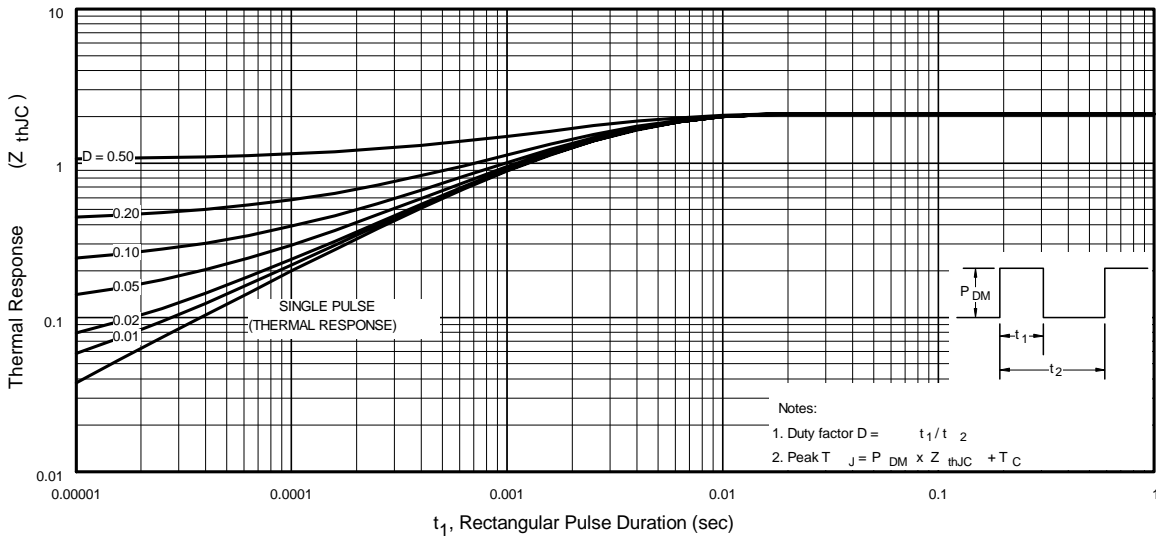


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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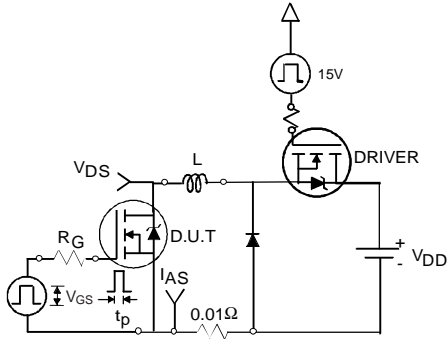


Fig 12a. Unclamped Inductive Test Circuit

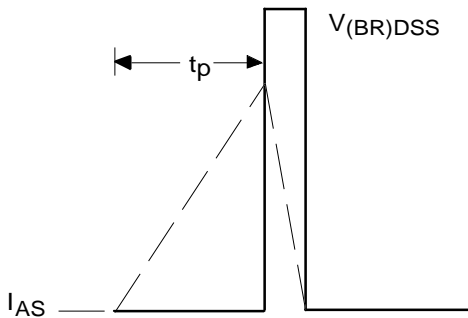


Fig 12b. Unclamped Inductive Waveforms

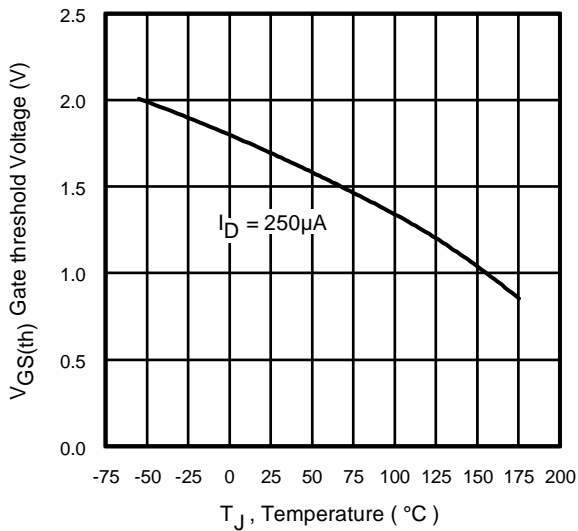


Fig 13. Threshold Voltage Vs. Temperature

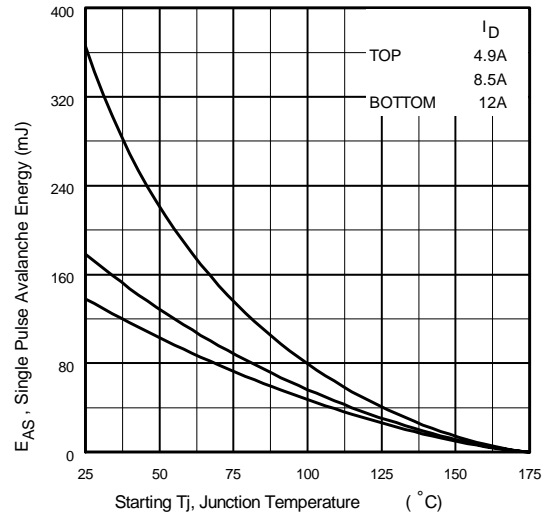


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

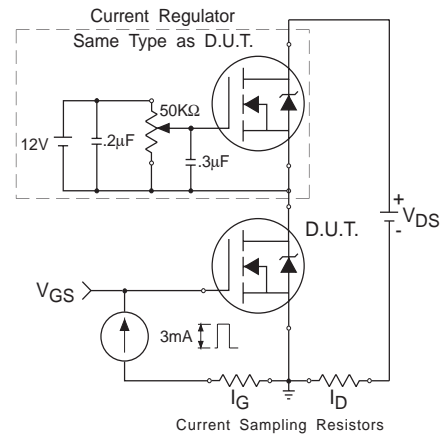
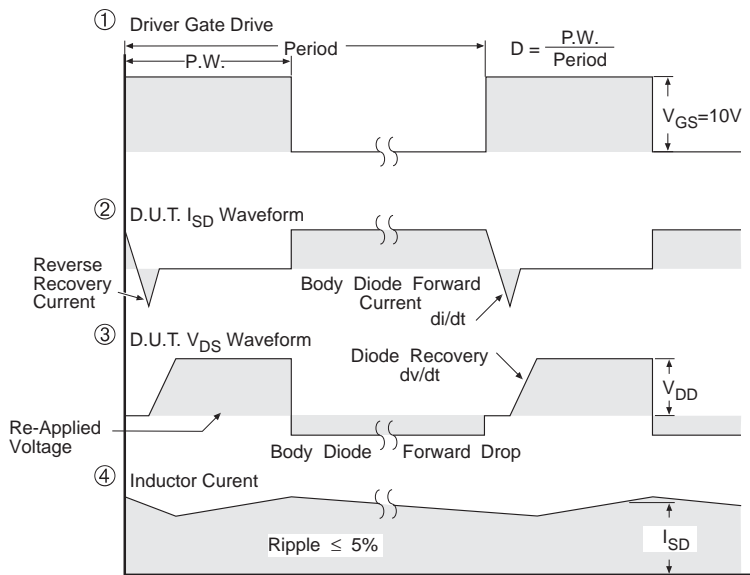
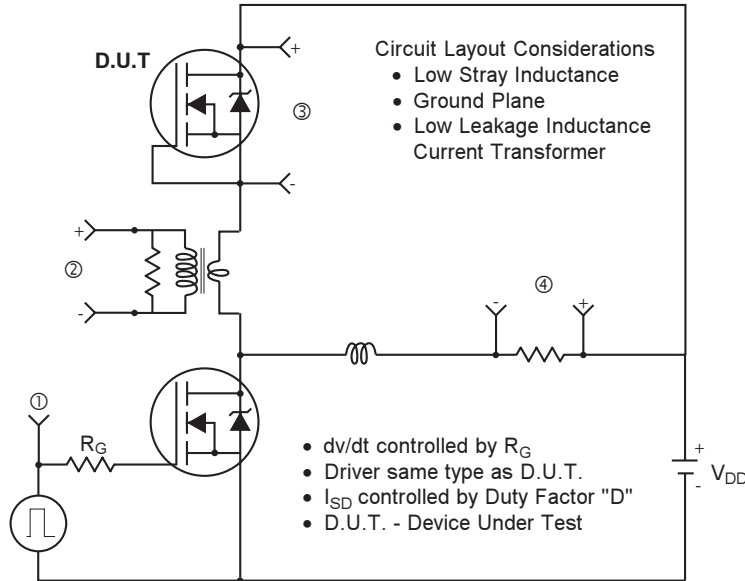


Fig 14. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

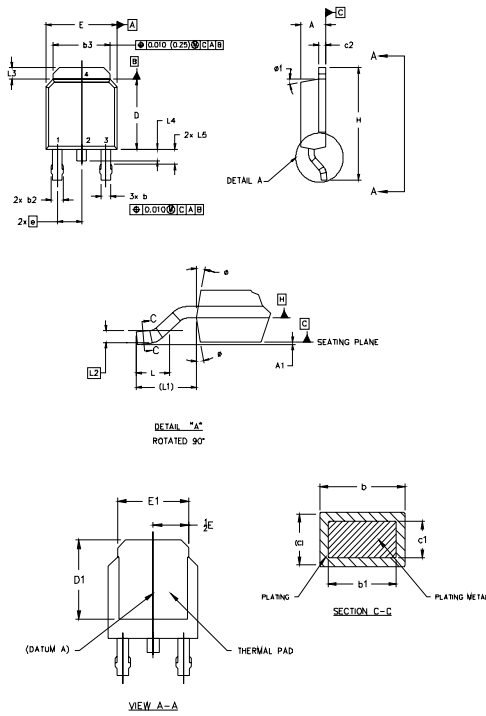
Fig 15. For N-Channel HEXFET® Power MOSFETs

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D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
 - 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
 - 3.0 LEAD DIMENSION UNCONTROLLED IN L5
 - 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
 - 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
 - 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.15		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	.0051 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	
ø	0"	10"	0"	10"	3
ø1	0"	15"	0"	15"	

LEAD ASSIGNMENTS

- HEXFET**
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
 - 4.- DRAIN

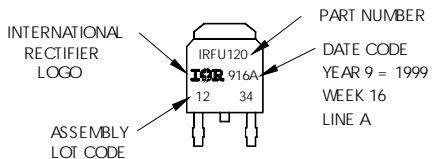
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

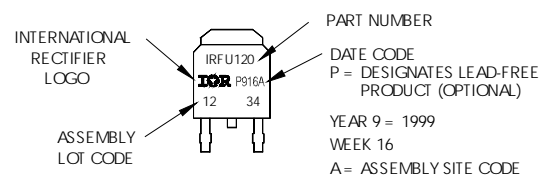
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"

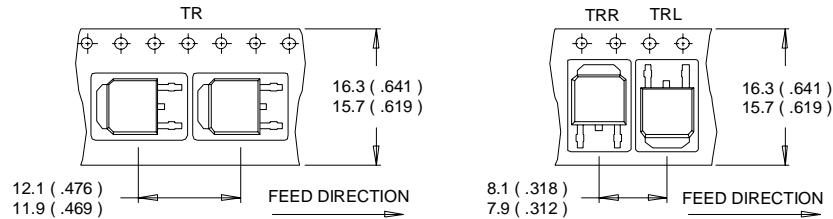


OR

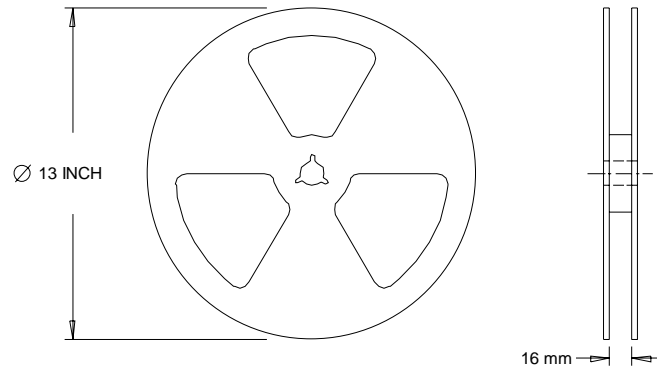


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
 - ② Starting $T_J = 25^\circ\text{C}$, $L = 1.9\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 12\text{A}$.
 - ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
 - ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.
- * When mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Consumer market.
 Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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