THE DATASHEET OF

IRS2093MTR

Datasheet No - PD97380
June 22, 2009

International
IOR Rectifier

IRS2093MPbF

4 CH Digital Audio Amplifier

Features

- 4 channel integrated analog input Class D audio amplifier drivers in a 48 pin MLPQ package
- Programmable over current protection
- Programmable dead-time generation
- Versatile protection control enabling latched, non-latched, or host controlled shutdown function
- Versatile input structure for self-oscillating PWM, external clock synchronization, or natural carrier based PWM modulations
- Start and stop click noise reduction
- Under voltage protection
- High noise immunity

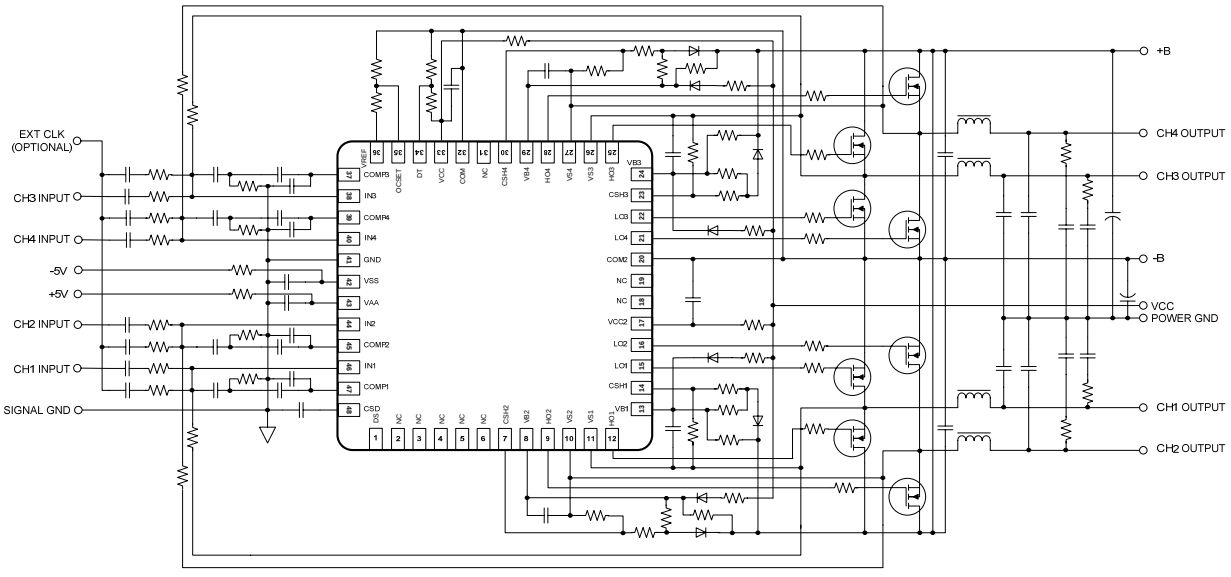
Product Summary

Topology	Half-Bridge and Full-Bridge
$V_{OFFSET\ (max)}$	+/- 100 V
I_{O+} & I_{O-} (typical)	0.5 A & 0.6 A
Selectable deadtime	45/65/85/105ns
DC offset	<18 mV
OC protection delay	500ns (max)
Shutdown propagation delay	250ns (max)
Error amplifier open loop gain	>60 dB

Package

MLPQ48 (7x7mm, 0.50mm pitch)

Typical Connection



Description

The IRS2093 integrates four channels of high voltage, high performance Class D audio amplifier drivers with PWM modulators and protections. In conjunction with external MOSFET and external components, a complete 4 channel Class D audio amplifier can be realized. The IRS2093 is designed with floating analog inputs and protection control interface pin especially for half bridge topology. High and low side MOSFET are protected from over current conditions by a programmable bi-directional current sensing. Essential elements of PWM modulator section allow flexible system design. A small MLPQ48 package enhances the benefit of smaller size of Class D topology.

Qualification Information†

Qualification Level	Industrial††
	Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level	MSL2†††, 260°C (per IPC/JEDEC J-STD-020)
IC Latch-Up Test	Class I, Level A (per JESD78A)
RoHS Compliant	Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_{Bn}	High side floating supply voltage	-0.3	215	V
V_{Sn}	High side floating supply voltage††, n=1-4	V_{Bn} -15	V_{Bn} +0.3	V
V_{Hon}	High side floating output voltage, n=1-4	V_{Sn} -0.3	V_{Bn} +0.3	V
V_{CSHn}	CSH pin input voltage, n=1-4	V_{Sn} -0.3	V_{Bn} +0.3	V
V_{CCn}	Low side fixed supply voltage††, n=1-2	-0.3	20	V
V_{LOn}	Low side output voltage, n=1-4	-0.3	VCC2 +0.3	V
V_{AA}	Floating input positive supply voltage††	(See I_{AAZ})	210	V
V_{SS}	Floating input negative supply voltage††	-1 (See I_{SSZ})	GND +0.3	V
V_{GND}	Floating input supply ground voltage	V_{SS} -0.3 (See I_{SSZ})	V_{AA} +0.3 (See I_{AAZ})	V
COM2	Low side output supply return	-0.3	+0.3	V
I_{IN-n}	Inverting input current †, n=1-4	-	±3	mA
V_{CSD}	SD pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{COMPn}	COMP pin input voltage, n=1-4	V_{SS} -0.3	V_{AA} +0.3	V
V_{DS}	DS pin input voltage	V_{SS} -0.3	V_{AA} +0.3	V
V_{DT}	DT pin input voltage	-0.3	V_{CC} +0.3	V
V_{OCSET}	OCSET pin input voltage	-0.3	V_{CC}+0.3	V
I_{AAZ}	Floating input positive supply zener clamp current	-	20	mA
I_{SSZ}	Floating input negative supply zener clamp current	-	20	mA
I_{CCZn}	Low side supply zener clamp current†††, n=1-2	-	10	mA
I_{BSZn}	Floating supply zener clamp current†††, n=1-4	-	10	mA
I_{OREF}	Reference output current	-	5	mA
dV_{Sn}/dt	Allowable Vs voltage slew rate, n=1-4	-	50	V/ns
dV_{SSn}/dt	Allowable Vss voltage slew rate†††, n=1-4	-	50	V/ms
Pd	Maximum power dissipation @ $T_A \leq +25°C$††††	-	6.2	W
Rth_{JA}	Thermal resistance, Junction to ambient††††	-	20	°C/W
T_J	Junction Temperature	-	150	°C
T_S	Storage Temperature	-55	150	°C
T_L	Lead temperature (Soldering, 10 seconds)	-	300	°C

† IN-1-4 contains clamping diode to GND.
†† VAA-VSS, Vcc1-COM, Vcc2-COM2, VB1-VS1, VB2-VS2, VB3-VS3 and VB4-VS4 contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.
††† For the rising and falling edges of step signal of 10V. Vss=15V to 200V.
†††† According to JESD51-5. JEDEC still air chamber.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The Vs and COM offset ratings are tested with supplies biased at V_{AA}-V_{SS}=10V, V_{CC}=12V and V_B-V_S=12V. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

Symbol	Definition	Min.	Max.	Units
V_{Bn}	High side floating supply absolute voltage, n=1-4	V_{Sn} +10	V_{Sn} +14	V
V_{Sn}	High side floating supply offset voltage	†	200	V
I_{AAZ}	Floating input positive supply zener clamp current	1	11	mA
I_{SSZ}	Floating input negative supply zener clamp current	1	11	mA
V_{SS}	Floating input supply absolute voltage	0	200	V
V_{HOn}	High side floating output voltage, n=1-4	Vs	V_B	V
V_{CC}, V_{CC2}	Low side fixed supply voltage	10	15	V
V_{LOn}	Low side output voltage, n=1-4	0	V_{CC}2	V
V_{GND}	GND pin input voltage	V_{SS} †††	V_{AA} †††	V
V_{IN-n}	Inverting input voltage, n=1-4	V_{GND} -0.5	V_{GND} +0.5	V
V_{CSD}	CSD pin input voltage	V_{SS}	V_{AA}	V
V_{COMPn}	COMP pin input voltage, n=1-4	V_{SS}	V_{AA}	V
C_{COMPn}	COMP pin phase compensation capacitor to GND, n=1-4	1	-	nF
V_{DT}	DT pin input voltage	0	V_{CC}	V
I_{OREF}	Reference output current to COM ††	0.3	0.8	mA
V_{OCSET}	OCSET pin input voltage	0.5	5	V
V_{CSHn}	CSH pin input voltage, n=1-4	V_{Sn}	V_{Bn}	V
dVss/dt	Allowable Vss voltage slew rate upon power-up ††††	-	50	V/ms
f_{SW}	Switching Frequency	-	800	kHz
T_A	Ambient Temperature	-40	125	°C

† Logic operational for Vsn equal to –5V to +200V. Logic state held for Vsn equal to –5V to –V_{BSn}.
†† Nominal voltage for V_{REF} is 5.1V. I_{OREF} of 0.3 – 0.8mA dictates total external resistor value on VREF to be 6.3k to 16.7k ohm.
††† GND input voltage is limited by I_{IN-n}.
†††† Vss ramps up from 0V to 200V.

Electrical Characteristics

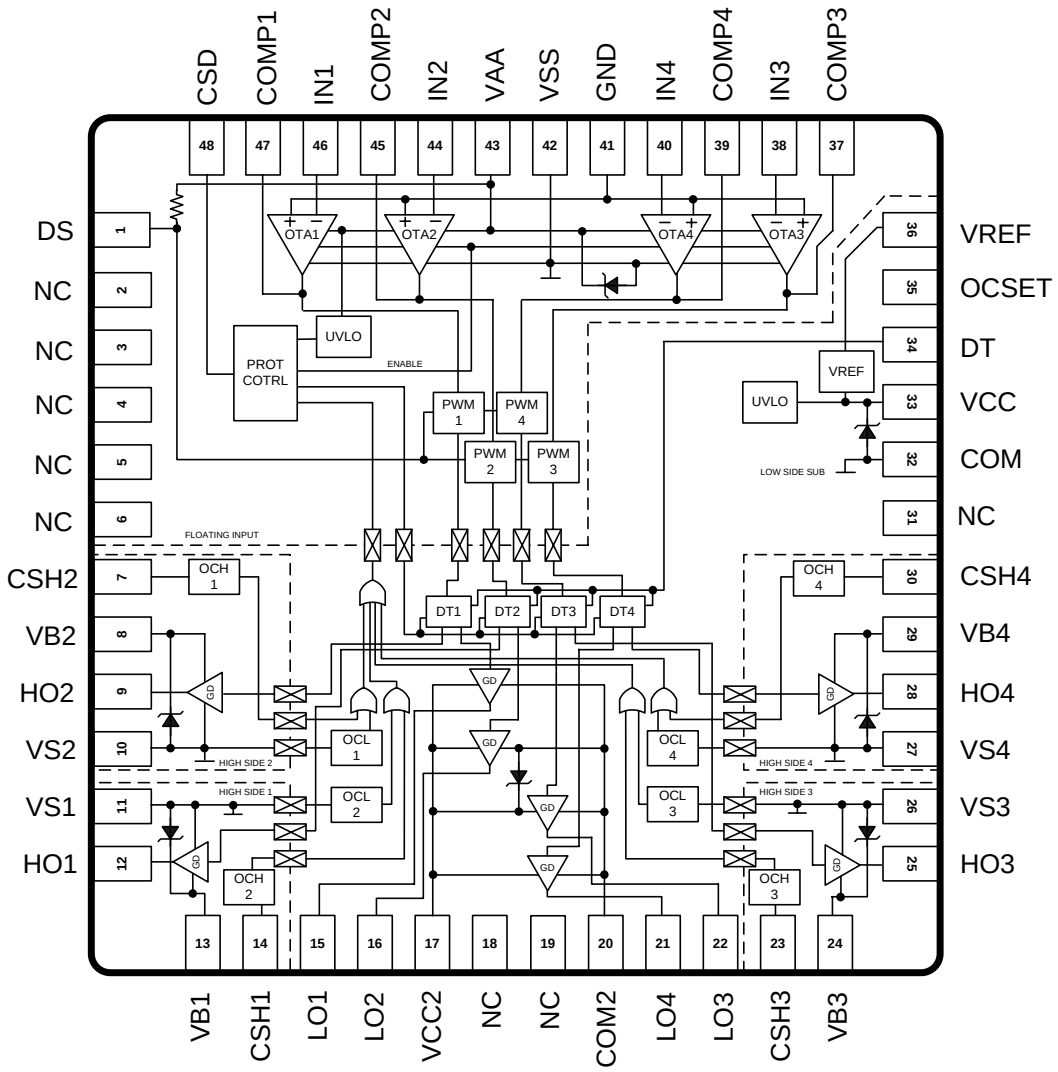
V_{CC}= V_{CC2}=V_{BS1}=V_{BS2},=V_{BS3}=V_{BS4} =12V, V_{SS}=V_{S1}=V_{S2}=V_{S3}=V_{S4}=COM=0V, V_{GND}=5V, V_{AA}=10V, C_L=1nF and T_A=25°C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Side Supply 1						
UV_{CC+}	Vcc supply UVLO positive threshold	8.4	8.9	9.4	V	
UV_{CC-}	Vcc supply UVLO negative threshold	8.2	8.7	9.2	V	
UV_{CCHYS}	UV_{CC} hysteresis	-	0.2	-	V	
I_{QCC_DT}	Low side quiescent current	-	3.3	6.6	mA	V_{DT}=V_{CC}
$V_{CLAMPL1}$	Low side zener diode clamp voltage	19.0	20.4	21.6	V	I_{CC1}=5mA
Low Side Supply 2						
I_{QCC2}	Low side quiescent current	-	2.4	5.0	mA	V_{DT}=COM
$V_{CLAMPL2}$	Low side zener diode clamp voltage	19.6	20.4	21.6	V	I_{CC2}=5mA
High Side Floating Supply						
UV_{BS+n}	High side well UVLO positive threshold, n=1-4	8.0	8.5	9.0	V	
UV_{BS-n}	High side well UVLO negative threshold, n=1-4	7.8	8.3	8.8	V	
UV_{BSHYSn}	UV_{BS} hysteresis, n=1-4	-	0.2	-	V	
I_{QBSn}	High side quiescent current, n=1-4	-	0.5	1	mA	
I_{LKHn}	High to Low side leakage current, n=1-4	-	-	50	µA	V_{Bn}=V_{Sn} =200V
$V_{CLAMPHn}$	High side zener diode clamp voltage, n=1-4	14.7	15.3	16.2	V	I_{BSn}=5mA
Floating Input Supply						
UV_{AA+}	VA+, VA- floating supply UVLO positive threshold from V_{SS}	8.2	8.7	9.2	V	GND pin floating
UV_{AA-}	VA+, VA- floating supply UVLO negative threshold from V_{SS}	7.7	8.2	8.7	V	GND pin floating
UV_{AAHYS}	UV_{AA} hysteresis	-	0.5	-	V	GND pin floating
I_{QAA0}	Floating Input positive quiescent supply current	-	1	3	mA	V_{CSD} =VSS
I_{QAA10}	Floating Input positive quiescent supply current	-	12	25	mA	
I_{QAA11}	Floating Input positive quiescent supply current		9	20	mA	
I_{QAA2}	Floating Input positive quiescent supply current	-	20	40	mA	V_{CSD} =VSS+5V
I_{LKM}	Floating input side to Low side leakage current	-	-	50	µA	V_{AA}=V_{SS}=V_{GND}= 100V
V_{CLAMPM}	Floating supply zener diode clamp voltage	19.6	20.4	22.5	V	I_{AA}=5mA, V_{CSD} =VSS
Audio Input (V_{GND}=0, V_{AA}=5V, V_{SS}=-5V, COM=COM2=VCC=VCC2=-5V, VS1=VS2=VS3=VS4=-5V, CSH1=CSH2=CHS3=CSH4=-5V, DT=OCSET=-5V)						
V_{OSn}	CHn input offset voltage, n=1-4	-18	0	18	mV	
I_{BINn}	CHn input bias current, n=1-4	-	-	40	nA	
GBWn	CHn small signal bandwidth	-	9	-	MHz	C_{COMPn}=1nF,

						Rfn=0
V_{COMPn}	CHn OTA Output voltage, n=1-4	VAA-1	-	VSS+1	V	
g_{mn}	CHn OTA transconductance, n=1-4	-	100	-	mS	V_{IN-n}=10mV
G_{Vn}	CHn OTA gain, n=1-4	60	-	-	dB	
V_{Nrmsn}	CHn OTA input noise voltage, n=1-4	-	250	-	mVrms	BW=20kHz, Resolution BW=22Hz Fig.5
SRn	CHn slew rate, n=1-4	-	±5	-	V/us	C_{COMPn}=1nF
CMRRn	CHn common-mode rejection ratio, n=1-4	-	60	-	dB	
PSRRn	CHn supply voltage rejection ratio, n=1-4	-	65	-	dB	
PWM comparator						
Vth_{PWM}	PWM comparator threshold in COMP	-	(V_{AA} - V_{SS})/2	-	V	
f_{OTAn}	CHn COMP pin star-up local oscillation frequency, n=1-4	0.7	1.0	1.5	MHz	V_{CSD} =VSS+5V
Protection						
V_{REF}	Reference output voltage	4.8	5.1	5.4	V	I_{OREF} =0.5mA
Vth_{OCLn}	CHn low side OC threshold in Vsn, n=1-4	1.1	1.2	1.3	V	OCSET=1.2V
Vth_{OCHn}	CHn high side OC threshold in V_{CSHn}, n=1-4	1.1+ Vs	1.2+ Vs	1.3+ Vs	V	Vs=200V,
Vth_{DS}	DS pin input threshold	$0.4xV_{AA}$	$0.5xV_{AA}$	$0.6xV_{AA}$	V	V_{SS} =0V
Vth1	CSD pin shutdown release threshold	$0.62xV_{AA}$	$0.70xV_{AA}$	$0.78xV_{AA}$	V	
Vth2	CSD pin self reset threshold	$0.26xV_{AA}$	$0.30xV_{AA}$	$0.34xV_{AA}$	V	
I_{CSD+}	CSD pin discharge current	70	100	130	µA	V_{CSD} = V_{SS} +5V
I_{CSD-}	CSD pin charge current	70	100	130	µA	V_{CSD} = V_{SS} +5V
t_{SDn}	CHn shutdown propagation delay from V_{CSD} > V_{SS} + Vth_{OCH} to Shutdown	-	-	250	ns	
t_{OCHn}	CHn propagation delay time from V_{CSHn} > Vth_{OCHn} to Shutdown, n=1-4	-	-	500	ns	Fig.4
t_{OCLn}	CHn propagation delay time from Vsn> Vth_{OCL} to Shutdown, n=1-4	-	-	500	ns	Fig.3
Gate Driver						
Io+n	CHn output high short circuit current (Source) , n=1-4	-	0.5	-	A	Vo=0V, PW≤10µS
Io-n	CHn output low short circuit current (Sink) , n=1-4	-	0.6	-	A	Vo=12V, PW≤10µS
V_{OLn}	CHn low level out put voltage LO – COM, HO - VS, n=1-4	-	-	0.1	V	Io=0A
V_{OHn}	CHn high level out put voltage VCC – LO, VB - HO, n=1-4	-	-	1.4	V	
Ton0n	CHn high and low side turn-on propagation delay, n=1-4	-	350	-	ns	V_{DT} = V_{CC}, V_{DS}=V_{AA}
Toff0n	CHn high and low side turn-off propagation delay, n=1-4	-	325	-	ns	
Ton1n	CHn high and low side turn-on	-	145	-	ns	V_{DT} = V_{CC}, V_{DS}=V_{SS}

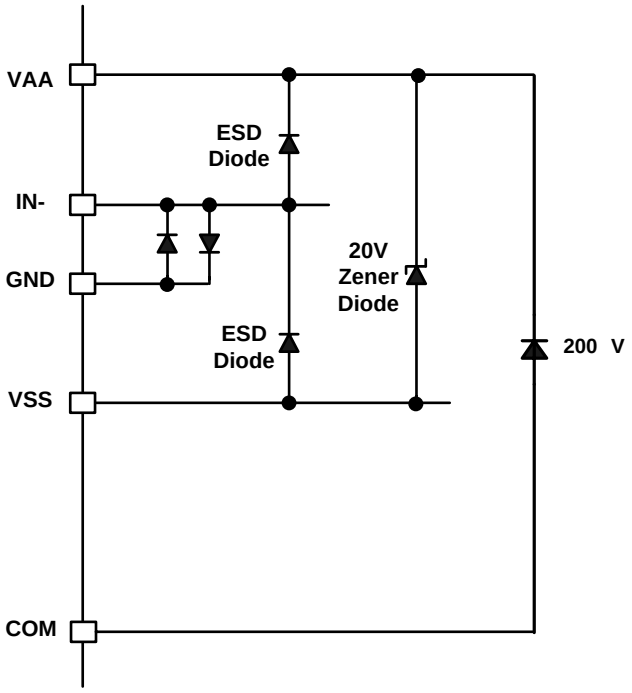
	propagation delay, n=1-4					
Toff1n	CHn high and low side turn-off propagation delay, n=1-4	-	100	-	ns	
tr	Turn-on rise time	-	25	50	ns	
tf	Turn-off fall time	-	20	40	ns	
DT1n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LnO turn-on (DT_{HO-LO})	30	45	60	ns	$V_{DT}>V_{DT1,}$
DT2n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LOn turn-on (DT_{HO-LO})	45	65	85	ns	$V_{DT1}>V_{DT}> V_{DT2,}$
DT3n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LOn turn-on (DT_{HO-LO})	65	85	105	ns	$V_{DT2}>V_{DT}> V_{DT3,}$
DT4n	CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HO turn-off to LOn turn-on (DT_{HO-LO})$V_{DT}= V_{DT4}$	85	105	145	ns	$V_{DT}<V_{DT3}$
V_{DT1}	DT mode select threshold 1	0.51xVcc	0.57xVcc	0.63xVcc	V	
V_{DT2}	DT mode select threshold 2	0.32xVcc	0.36xVcc	0.40xVcc	V	
V_{DT3}	DT mode select threshold 3	0.21xVcc	0.23xVcc	0.25xVcc	V	

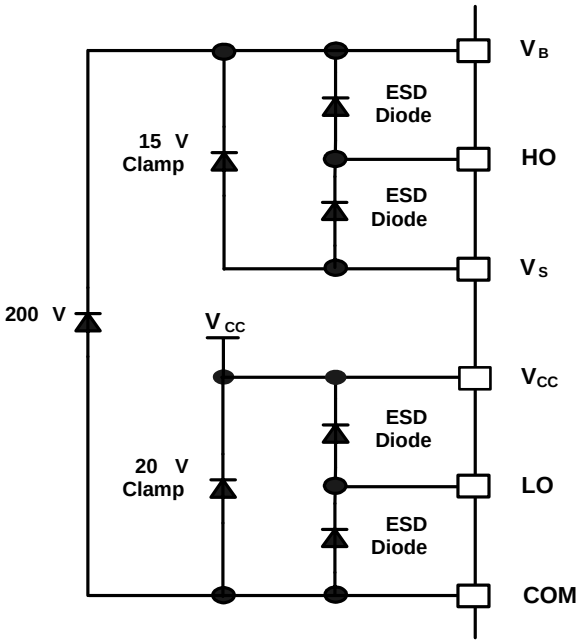
Functional Block Diagram

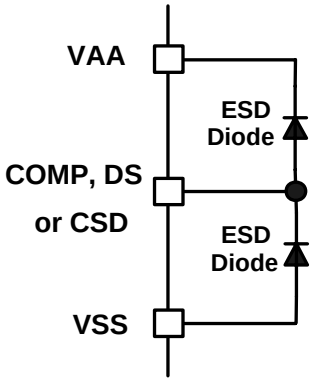


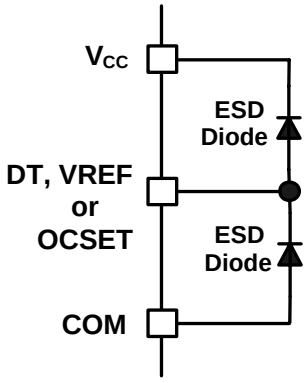
⊠ : HIGH VOLTAGE LEVEL SHIFTER

Input/Output Pin Equivalent Circuit Diagrams





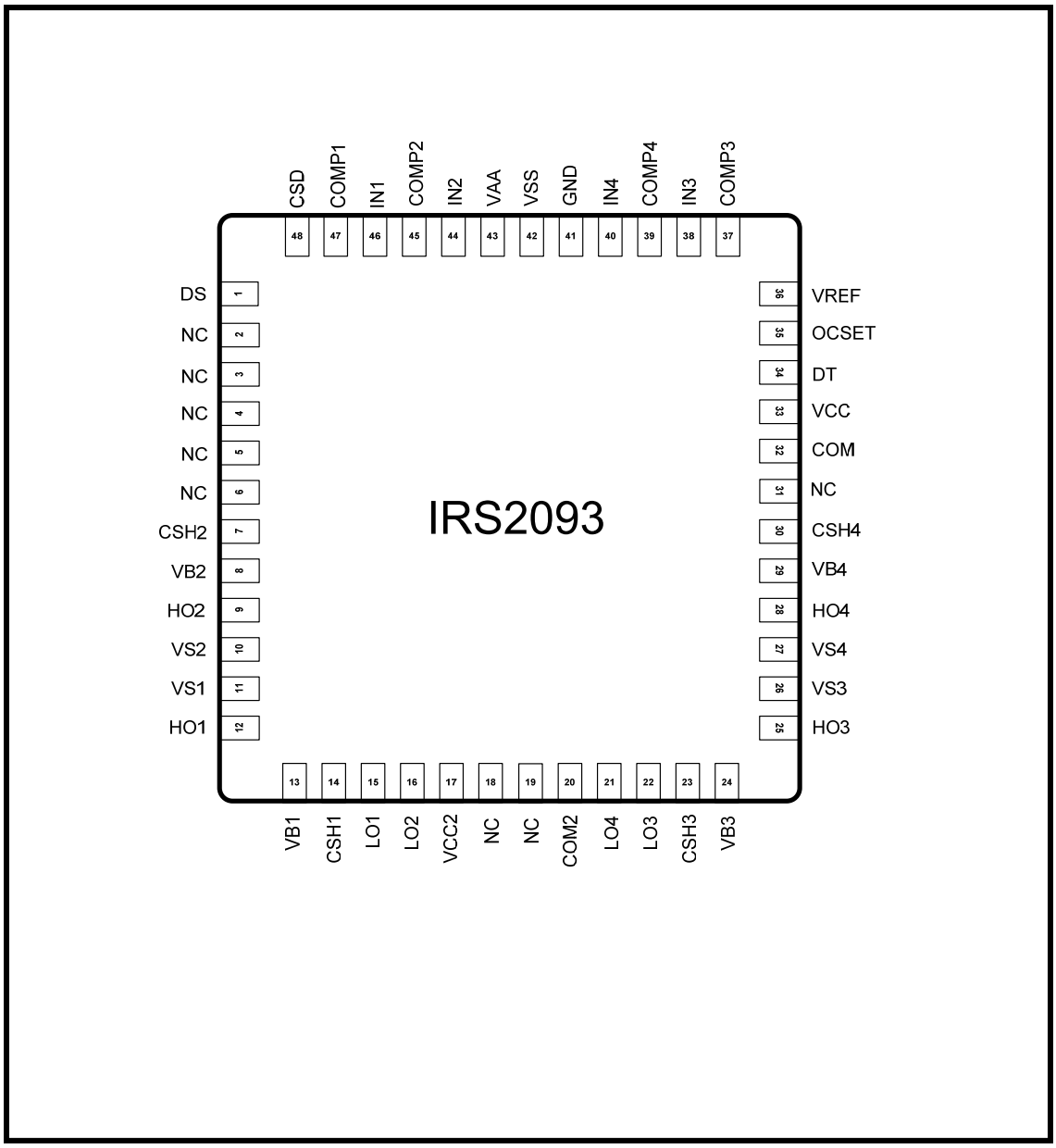




Lead Definitions

Pin #	IN/OUT	Symbol	Description
1	IN	DS	Delay select input, referenced to VSS/VAA. H: with temp/co comp delay
2-6	-	NC	
7	IN	CSH2	CH2 High side over current sensing input, referenced to VS2
8	IN	VB2	CH2 High side floating supply
9	OUT	HO2	CH2 High side output
10	IN	VS2	CH2 High side floating supply return
11	IN	VS1	CH1 High side floating supply return
12		HO1	CH1 High side output
13	IN	VB1	CH1 High side floating supply
14	IN	CSH1	CH1 High side over current sensing input, referenced to VS1
15	OUT	LO1	CH1 Low side output
16	OUT	LO2	CH2 Low side output
17	IN	VCC2	Low side gate drive supply
18-19	-	NC	
20	IN	COM2	Low side gate drive supply return
21	OUT	LO4	CH4 Low side output
22	OUT	LO3	CH3 Low side output
23	IN	CSH3	CH3 High side over current sensing input, referenced to VS3
24	IN	VB3	CH3 High side floating supply
25	OUT	HO3	CH3 High side output
26	IN	VS3	CH3 High side floating supply return
27	IN	VS4	CH4 High side floating supply return
28	OUT	HO4	CH4 High side output
29	IN	VB4	CH4 High side floating supply
30	IN	CSH4	CH4 High side over current sensing input, referenced to VS4
31	-	NC	
32	IN	COM	Low side supply return
33	IN	VCC	Low side logic supply
34	IN	DT	Input for programmable dead-time, referenced to COM
35	IN	OCSET	Low side over current threshold setting, referenced to COM
36	OUT	VREF	5V reference output for setting OCSET
37	OUT	COMP3	CH3 Phase compensation input, comparator input
38	IN	IN3	CH3 Analog inverting input
39	OUT	COMP4	CH4 Phase compensation input, comparator input
40	IN	IN4	CH4 Analog inverting input
41	IN	GND	Floating input supply return
42	IN	VSS	Floating input negative supply
43	IN	VAA	Floating input positive supply
44	IN	IN2	CH2 Analog inverting input
45	OUT	COMP2	CH2 Phase compensation input, comparator input
46	IN	IN1	CH1 Analog inverting input
47	OUT	COMP1	CH1 Phase compensation input, comparator input
48	IN/OUT	CSD	Shutdown timing capacitor, referenced to VSS

Lead Assignments



Application Information and Additional Details

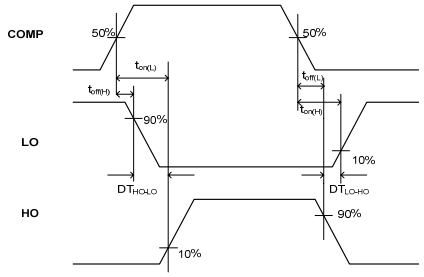


Figure 1 Switching Time Waveform Definitions

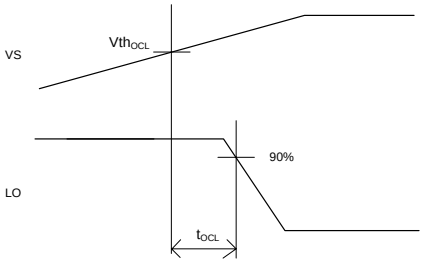


Figure 3 V_S > Vth_{OCL} to Shutdown Waveform

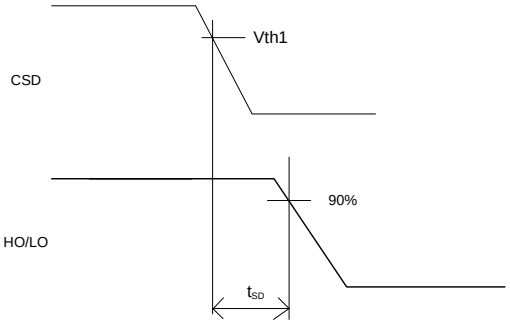


Figure 2 CSD to Shutdown Waveform Definitions

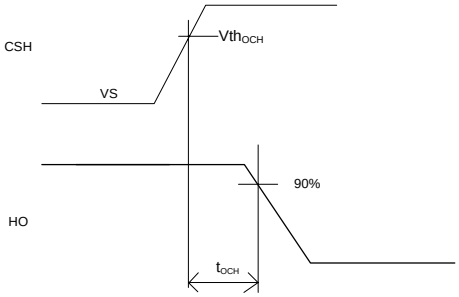
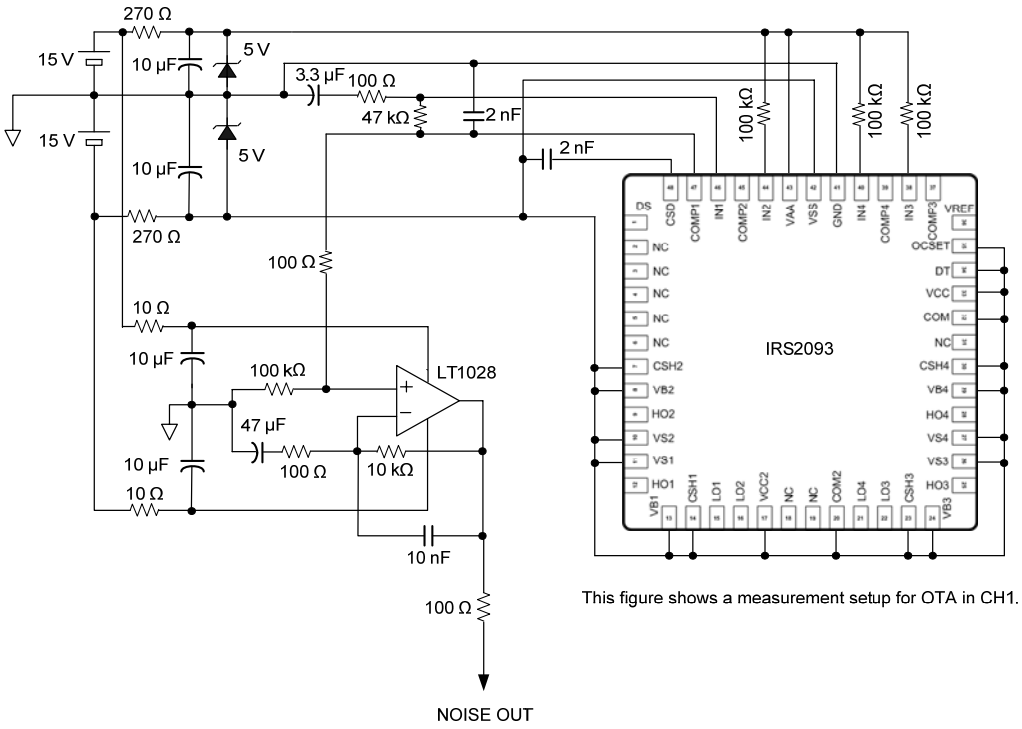


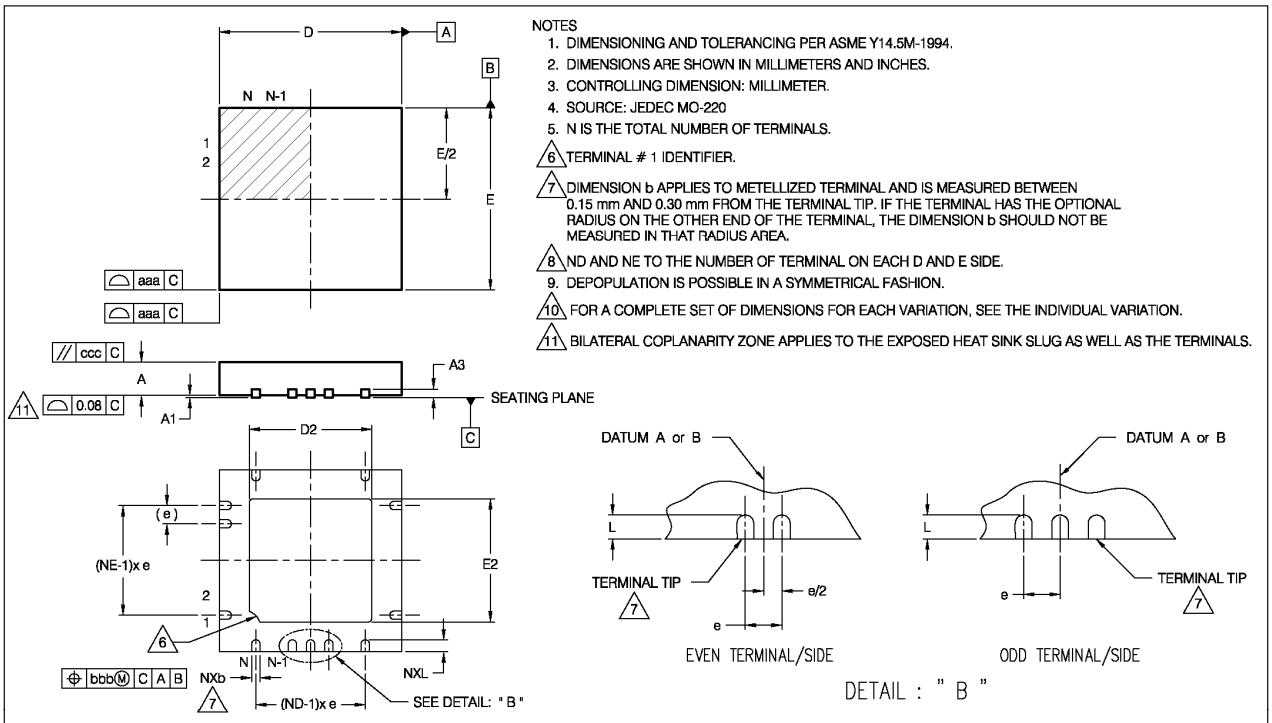
Figure 4 V_{CSH} > Vth_{OCH} to Shutdown Waveform



This figure shows a measurement setup for OTA in CH1.

Figure 5: OTA input noise voltage mesurent circuit

Package Details: MLPQ 7X7



NOTES
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. SOURCE: JEDEC MO-220
5. N IS THE TOTAL NUMBER OF TERMINALS.
6. TERMINAL # 1 IDENTIFIER.
7. DIMENSION b APPLIES TO METELLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
8. ND AND NE TO THE NUMBER OF TERMINAL ON EACH D AND E SIDE.
9. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
10. FOR A COMPLETE SET OF DIMENSIONS FOR EACH VARIATION, SEE THE INDIVIDUAL VARIATION.
11. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

VER.	ESCN NUMBER	BY	DATE	APPROVAL INITIALS
7	REVISED PER ESCN 0421-06	GCR	8/7/06	
8	REVISED PER ESCN 37678	GCR	12/6/06	
9	REVISED PER ESCN 37834	GCR	1/8/07	
10	REVISED PER ESCN 38363	GCR	2/5/07	
11	REVISED PER ESCN 45228	GCR	2/2/09	
12	REVISED PER ESCN 45324	GCR	2/19/09	A. C.

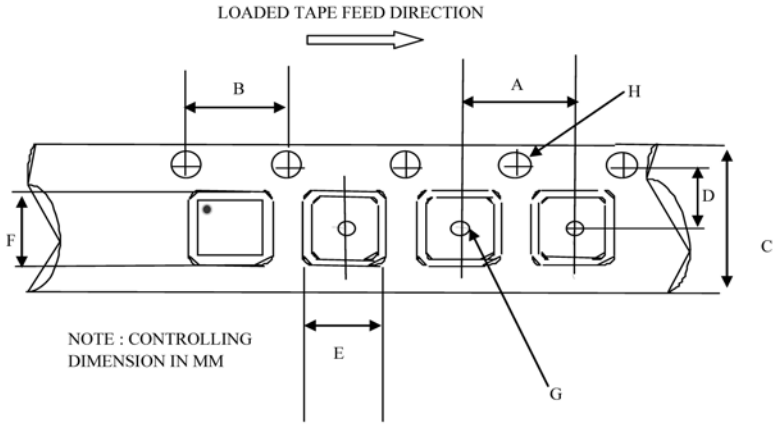
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE: IN INCHES
TOLERANCES ARE:
DECIMALS
.X = +/-
.XX = +/-
.XXX = +/-
.XXXX = +/-
.XXXXX = +/-
ANGLES
∠ = +/- .5°

QFN (MLPQ, MLF) PACKAGE OUTLINE

DRAWN BY G. C. RAMOS 5/4/04	INTERNATIONAL RECTIFIER	
APPROVED BY A. CALICDAN	EL SEGUNDO, CALIFORNIA	
SIGNATURE & DATE A. Calicdan 2/19/09	CAD GENERATED	
DO NOT SCALE DRAWING / SCALE ENLGMT	SHEET 1/3 / DRAWING NO. 01-3086	VER. 12

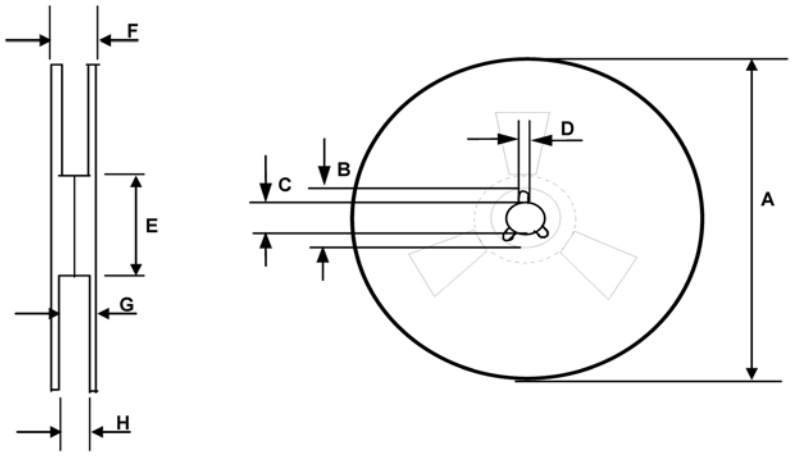
SYMBOL	VKKD-4NJ1					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	.032	.035	.039
A1	0.00	0.02	0.05	.000	.0008	.0019
A3	0.20 REF			.008 REF		
b	0.18	0.25	0.30	.0071	.0098	.0118
D2	5.40	5.55	5.65	.213	.219	.222
D	7.00 BSC			.276 BSC		
E	7.00 BSC			.276 BSC		
E2	5.40	5.55	5.65	.213	.219	.222
L	0.30	0.40	0.50	.012	.016	.020
e	0.50 PITCH			.020 PITCH		
N	48			48		
ND	12			12		
NE	12			12		
aaa	0.15			.0059		
bbb	0.10			.0039		
ccc	0.10			.0039		
ddd	0.05			.0019		

Tape and Reel Details: MLPQ 7X7



CARRIER TAPE DIMENSION FOR 48MLPQ7X7

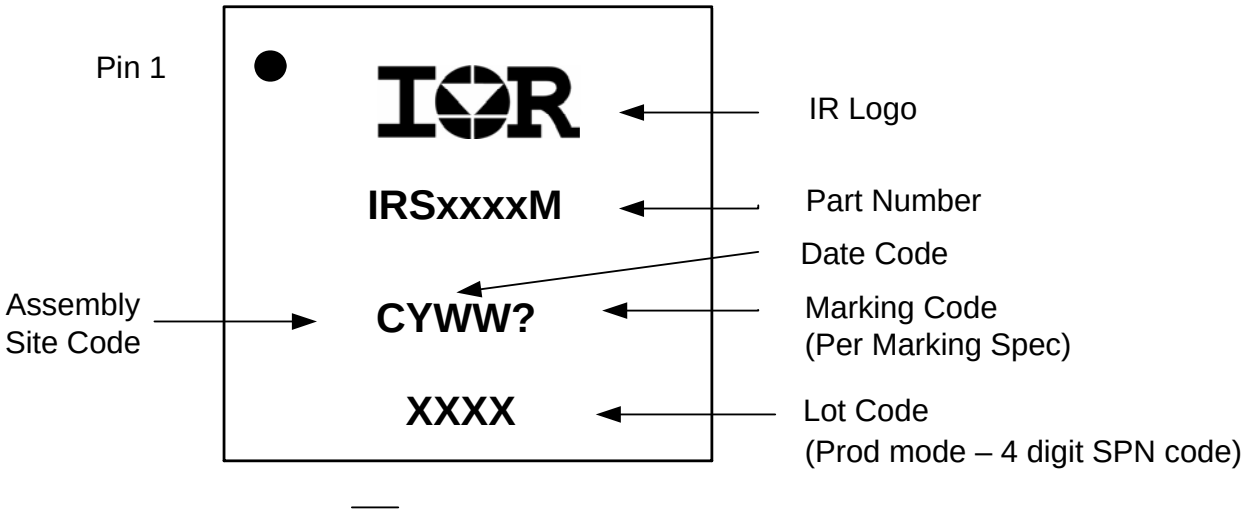
Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.474	0.476
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	7.15	7.35	0.281	0.289
F	7.15	7.35	0.281	0.289
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 48MLPQ7X7

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.4	n/a	0.881
G	18.5	21.1	0.728	0.83
H	16.4	18.4	0.645	0.724

Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2093M	MLPQ 48 7x7	Tube / Bulk	52	IRS2093MPBF
		Tape and Reel	3000	IRS2093MTRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

WORLD HEADQUARTERS:
233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105

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