THE DATASHEET OF

IRU1030CDTR

International
IOR Rectifier

Data Sheet No. PD94124

IRU1030

3A LOW DROPOUT POSITIVE ADJUSTABLE REGULATOR

FEATURES

- Guaranteed < 1.3V Dropout at Full Load Current
- Fast Transient Response
- 1% Voltage Reference Initial Accuracy
- Output Current Limiting
- Built-In Thermal Shutdown

APPLICATIONS

- Low Voltage Processor Applications such as: P54C™, P55C™, Cyrix M2™, POWER PC™, AMD
- GTL+ Termination PENTIUM PRO™, KLAMATH™
- Low Voltage Memory Termination Applications
- Standard 3.3V Chip Set and Logic Applications

DESCRIPTION

The IRU1030 is a low dropout three-terminal adjustable regulator with minimum of 3A output current capability. This product is specifically designed to provide well regulated supply for low voltage IC applications such as Pentium™ P54C™, P55C™ as well as GTL+ termination for Pentium Pro™ and Klamath™ processor applications. The IRU1030 is also well suited for other processors such as Cyrix™, AMD and Power PC™ applications. The IRU1030 is guaranteed to have <1.3V dropout at full load current making it ideal to provide well regulated outputs of 2.5V to 3.3V with 4.75V to 7V input supply.

TYPICAL APPLICATION

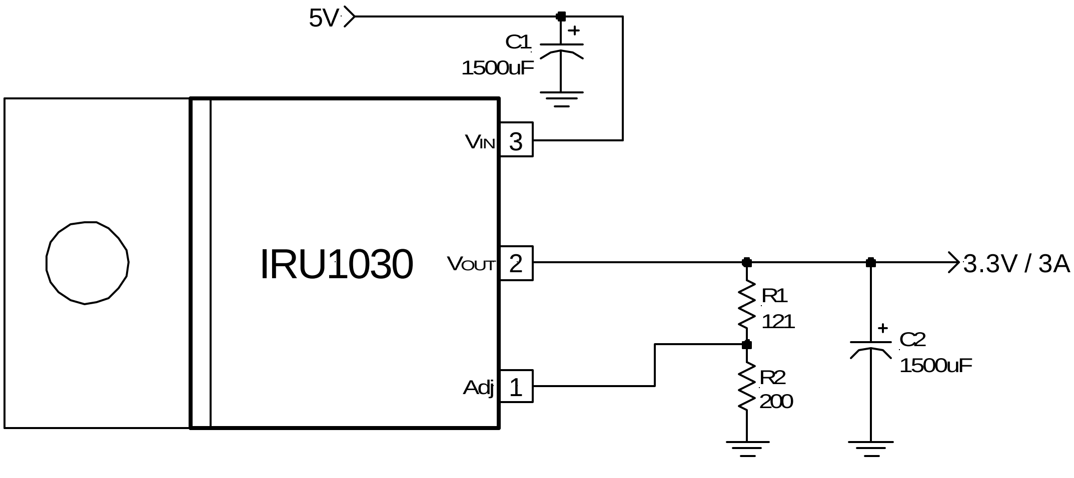


Figure 1 - Typical Application of IRU1030 in a 5V to 3.3V regulator.

Notes: Pentium P54C, P55C, Klamath, Pentium Pro, VRE are trademarks of Intel Corp.Cyrix M2 is trademark of Cyrix Corp. Power PC is trademark of IBM Corp.

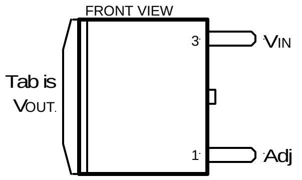
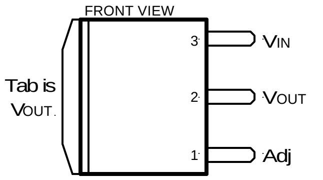
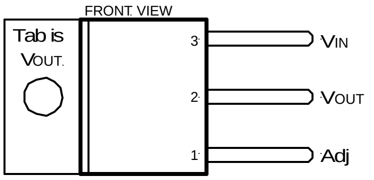
PACKAGE ORDER INFORMATION

T_J (°C)	2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	3-PIN PLASTIC TO-220 (T)
0 To 150	IRU1030CD	IRU1030CM	IRU1030CT

ABSOLUTE MAXIMUM RATINGS

Input Voltage (V_{IN})	7V
Power Dissipation	Internally Limited
Storage Temperature Range	-65°C To 150°C
Operating Junction Temperature Range	0°C To 150°C

PACKAGE INFORMATION

2-PIN PLASTIC TO-252 (D-Pak)	3-PIN PLASTIC TO-263 (M)	3-PIN PLASTIC TO-220 (T)
		
θ_{JA}=70°C/W for 0.5" Square pad	θ_{JA}=35°C/W for 1" Square pad	θ_{JT}=2.7°C/W θ_{JA}=60°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over $C_{IN}=1\mu F$, $C_{OUT}=10\mu F$, and T_J=0 to 150°C. Typical values refer to T_J=25°C.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	Io=10mA, T_J=25°C, (V_{IN}-Vo)=1.5V	1.238	1.250	1.262	V
		Io=10mA, (V_{IN}-Vo)=1.5V	1.225	1.250	1.275	
Line Regulation		Io=10mA, 1.3V<(V_{IN}-Vo)<7V			0.2	%
Load Regulation (Note 1)		V_{IN}=3.3V, V_{ADJ}=0, 10mA<Io<3A			0.4	%
Dropout Voltage (Note 2)	ΔV_O	Note 2, Io=3A		1.1	1.3	V
Current Limit		V_{IN}=3.3V, ΔVo=100mV	3.1			A
Minimum Load Current (Note 3)		V_{IN}=3.3V, V_{ADJ}=0V		5	10	mA
Thermal Regulation		30ms Pulse, V_{IN}-Vo=3V, Io=3A		0.01	0.02	%/W
Ripple Rejection		f=120Hz, Co=25μF Tantalum, Io=1.5A, V_{IN}-Vo=3V	60	70		dB
Adjust Pin Current	I_{ADJ}	Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C, Io=10mA, V_{IN}-Vo=1.5V		55	120	μA
Adjust Pin Current Change		Io=10mA, V_{IN}-Vo=1.5V, T_J=25°C		0.2	5	μA
Temperature Stability		V_{IN}=3.3V, V_{ADJ}=0V, Io=10mA		0.5		%
Long Term Stability		T_J=125°C, 1000Hrs		0.3	1	%
RMS Output Noise		T_J=25°C, 10Hz<f<10KHz		0.003		%V_O

Note 1: Low duty cycle pulse testing with Kelvin connections is required in order to maintain accurate data.

Note 2: Dropout voltage is defined as the minimum differential voltage between V_{IN} and V_{OUT} required to maintain regulation at V_{OUT}. It is measured when the output voltage drops 1% below its nominal value.

Note 3: Minimum load current is defined as the minimum current required at the output in order for the output voltage to maintain regulation. Typically the resistor dividers are selected such that this current is automatically maintained.

PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	Adj	A resistor divider from V_{OUT} to Adj pin to ground sets the output voltage.
2	V_{OUT}	The output of the regulator. A minimum of 10µF capacitor must be connected from this pin to ground to insure stability.
3	V_{IN}	The input pin of the regulator. Typically a large storage capacitor is connected from this pin to ground to insure that the input voltage does not sag below the minimum drop out voltage during the load transient response. This pin must always be 1.3V higher than V_{OUT} in order for the device to regulate properly.

BLOCK DIAGRAM

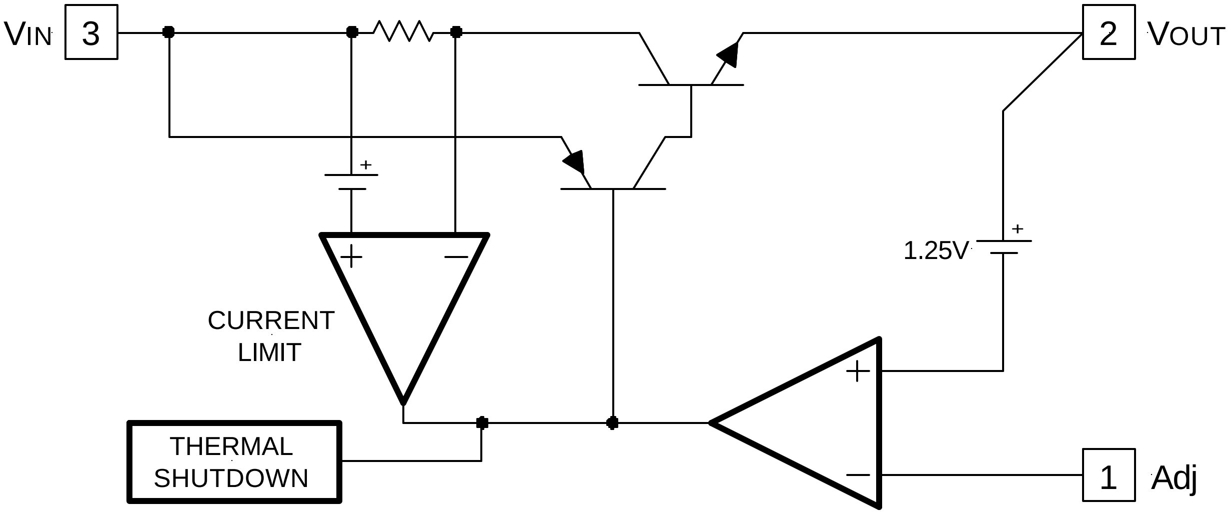


Figure 2 - Simplified block diagram of the IRU1030.

APPLICATION INFORMATION

Introduction

The IRU1030 adjustable Low Dropout (LDO) regulator is a three-terminal device which can easily be programmed with the addition of two external resistors to any voltages within the range of 1.25 to 5.5V. This regulator unlike the first generation of the three-terminal regulators such as LM117 that required 3V differential between the input and the regulated output, only needs 1.3V differential to maintain output regulation. This is a key requirement for today's microprocessors that need typically 3.3V supply and are often generated from the 5V supply. Another major requirement of these microprocessors such as the Intel P54C™ is the need to switch the load current from zero to several amps in tens of nanoseconds at the processor pins, which translates to an approximately 300 to 500ns current step at the regulator. In addition, the output voltage tolerances are also extremely tight and they include the transient response as part of the specification. For example Intel VRE™ specification calls for a total of ±100mV including initial tolerance, load regulation and 0 to 4.6A load step.

The IRU1030 is specifically designed to meet the fast current transient needs as well as providing an accurate initial voltage, reducing the overall system cost with the need for fewer output capacitors.

Output Voltage Setting

The IRU1030 can be programmed to any voltages in the range of 1.25V to 5.5V with the addition of R1 and R2 external resistors according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1+\frac{R2}{R1}\right) + I_{ADJ} \times R2$$

Where:
V_{REF} = 1.25V Typically
I_{ADJ} = 50µA Typically
R1 and R2 as shown in Figure 3:

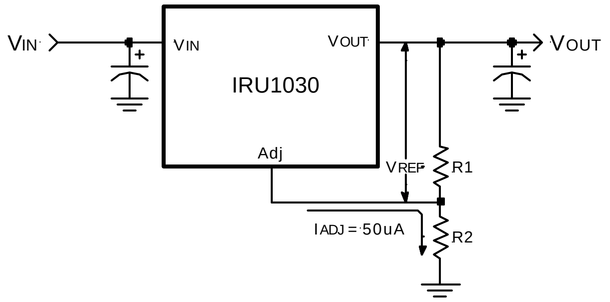


Figure 3 - Typical application of the IRU1030 for programming the output voltage.

The IRU1030 keeps a constant 1.25V between the output pin and the adjust pin. By placing a resistor R1 across these two pins a constant current flows through R1, adding to the I_{ADJ} current and into the R2 resistor producing a voltage equal to the $(1.25/R1) \times R2 + I_{ADJ} \times R2$ which will be added to the 1.25V to set the output voltage. This is summarized in the above equation. Since the minimum load current requirement of the IRU1030 is 10mA, R1 is typically selected to be 121Ω resistor so that it automatically satisfies the minimum current requirement. Notice that since I_{ADJ} is typically in the range of 50µA it only adds a small error to the output voltage and should only be considered when a very precise output voltage setting is required. For example, in a typical 3.3V application where R1=121Ω and R2=200Ω the error due to I_{ADJ} is only 0.3% of the nominal set point.

Load Regulation

Since the IRU1030 is only a three-terminal device, it is not possible to provide true remote sensing of the output voltage at the load. Figure 4 shows that the best load regulation is achieved when the bottom side of R2 is connected to the load and the top side of R1 resistor is connected directly to the case or the V_{OUT} pin of the regulator and not to the load. In fact, if R1 is connected to the load side, the effective resistance between the regulator and the load is gained up by the factor of (1+R2/R1), or the effective resistance will be $R_{P(eff)} = R_P \times (1+R2/R1)$. It is important to note that for high current applications, this can represent a significant percentage of the overall load regulation and one must keep the path from the regulator to the load as short as possible to minimize this effect.

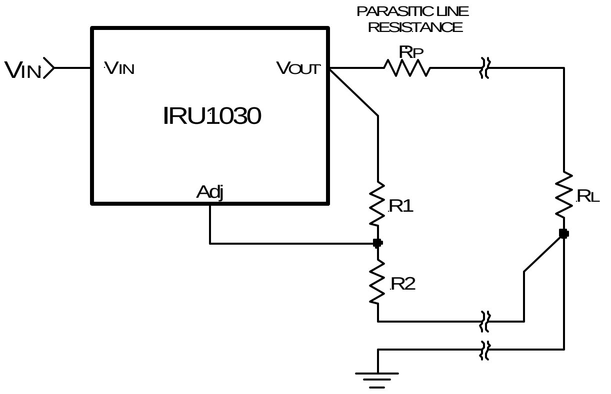


Figure 4 - Schematic showing connection for best load regulation.

Stability

The IRU1030 requires the use of an output capacitor as part of the frequency compensation in order to make the regulator stable. Typical designs for microprocessor applications use standard electrolytic capacitors with a typical ESR in the range of 50 to 100mΩ and an output capacitance of 500 to 1000µF. Fortunately as the capacitance increases, the ESR decreases resulting in a fixed RC time constant. The IRU1030 takes advantage of this phenomena in making the overall regulator loop stable. For most applications a minimum of 100µF aluminum electrolytic capacitor such as Sanyo MVGX series, Panasonic FA series as well as the Nichicon PL series insures both stability and good transient response.

Thermal Design

The IRU1030 incorporates an internal thermal shutdown that protects the device when the junction temperature exceeds the maximum allowable junction temperature. Although this device can operate with junction temperatures in the range of 150°C, it is recommended that the selected heat sink be chosen such that during maximum continuous load operation the junction temperature is kept below this number. The example below shows the steps in selecting the proper regulator heat sink for the GTL+ terminator using a separate regulator for each end.

Assuming the following specifications:

$V_{IN} = 3.3V$
$V_{OUT} = 1.5V$
$I_{OUT(MAX)} = 2.7A$
$T_A = 35°C$

The steps for selecting a proper heat sink to keep the junction temperature below 135°C is given as:

1) Calculate the maximum power dissipation using:

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT})$$

$$P_D = 2.7 \times (3.3 - 1.5) = 4.86W$$

2) Select a package from the regulator data sheet and record its junction to case (or tab) thermal resistance.

Selecting TO-220 package gives us:

$\theta_{JC} = 2.7°C/W$

3) Assuming that the heat sink is black anodized, calculate the maximum heat sink temperature allowed:

Assume, $\theta_{CS}=0.05°C/W$ (heat-sink-to-case thermal resistance for black anodized)

$$T_S = T_J - P_D \times (\theta_{JC} + \theta_{CS})$$

$$T_S = 135 - 4.86 \times (2.7 + 0.05) = 121.7°C$$

4) With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance (θ_{SA}) is calculated by first calculating the temperature rise above the ambient as follows:

$$\Delta T = T_S - T_A = 121.7 - 35 = 86.7°C$$

ΔT=Temperature Rise Above Ambient

$$\theta_{SA} = \frac{\Delta T}{P_D} = \frac{86.7}{4.86} = 17.8°C/W$$

5) Next, a heat sink with lower θ_{SA} than the one calculated in step 4 must be selected. One way to do this is to simply look at the graphs of the "Heat Sink Temp Rise Above the Ambient" vs. the "Power Dissipation" and select a heat sink that results in lower temperature rise than the one calculated in the previous step. The following heat sinks from AAVID and Thermalloy meet this criteria.

	Air Flow (LFM)			
	0	**100**	**200**	**300**
Thermalloy	6109PB	6110PB	7141	7178
AAVID	575002	507302	576802B	577102

Note: For further information regarding the above companies and their latest product offerings and application support contact your local representative or the numbers listed below:

AAVID................PH# (603) 528 3400
Thermalloy..........PH# (214) 243-4321

Designing for Microprocessor Applications

As it was mentioned before the IRU1030 is designed specifically to provide power for the new generation of the low voltage processors requiring voltages in the range of 2.5V to 3.6V generated by stepping down the 5V supply. These processors demand a fast regulator that supports their large load current changes. The worst case current step seen by the regulator is anywhere in the range of 1 to 7A with the slew rate of 300 to 500ns which could happen when the processor transitions from "Stop Clock" mode to the "Full Active" mode. The load current step at the processor is actually much faster, in the order of 15 to 20ns, however the decoupling capacitors placed in the cavity of the processor socket handle this transition until the regulator responds to the load current levels. Because of this requirement the selection of high frequency low ESR and low ESL output capacitors is imperative in the design of these regulator circuits.

Figure 5 shows the effects of a fast transient on the output voltage of the regulator. As shown in this figure, the ESR of the output capacitor produces an instantaneous drop equal to the ($\Delta V_{ESR}=ESR \times \Delta I$) and the ESL effect will be equal to the rate of change of the output current times the inductance of the capacitor. ($\Delta V_{ESL} = L \times \Delta I/\Delta t$). The output capacitance effect is a droop in the output voltage proportional to the time it takes for the regulator to respond to the change in the current, ($\Delta V_C=\Delta t \times \Delta I/C$) where Δt is the response time of the regulator.

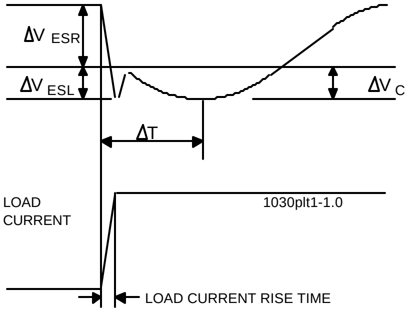


Figure 5 - Typical regulator response to the fast load current step.

An example of a regulator design to meet the Intel Pentium Pro GTL+ specification is given below.

Assume the specification for the processor as shown in Table 1:

Type of Processor	V_{OUT} Nominal	I_{MAX}	Max Allowed Output Tolerance
Pentium Pro	1.50 V	2.7 A	±150 mV

Table 1 - GTL+ Specification for Pentium Pro

The first step is to select the voltage step allowed in the output due to the output capacitor's ESR:

1) Assuming the regulator's initial accuracy plus the resistor divider tolerance is ≈ ±30mV (±2% of 1.5V nominal), then the total step allowed for the ESR and the ESL, is –120 mV.

Assuming that the ESL drop is –10mV, the remaining ESR step will be –110mV. Therefore the output capacitor ESR must be:

$$ESR \leq \frac{110}{2.7} = 40m\Omega$$

The Sanyo MVGX series is a good choice to achieve both price and performance goals. The 6MV1500GX, 1500μF, 6.3V has an ESR of less than 36mΩ typ. Selecting a single capacitor achieves our design goal.

The next step is to calculate the drop due to the capacitance discharge and make sure that this drop in voltage is less than the selected ESL drop in the previous step.

2) With the output capacitance being 1500μF:

$$\Delta Vc = \frac{\Delta t \times \Delta I}{C} = \frac{2 \times 2.7}{1500} = 3.6mV$$

Where:
Δt = 2μs is the regulator response time

To set the output DC voltage, we need to select R1 and R2:

3) Assuming R1 = 121Ω, 0.5%:

$$R2 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R1 = \left(\frac{1.5}{1.25} - 1\right) \times 121 = 24.2\Omega$$

Select R2 = 24.3Ω, 0.5%

Selecting both R1 and R2 resistors to be 0.5% tolerance, results in the least amount of error introduced by the resistor dividers leaving ≈ ±1.3% error budget for the IRU1030 reference which is within the initial accuracy of the device.

Finally, the input capacitor is selected as follows:

4) Assuming that the input voltage can drop 150mV before the main power supply responds, and that the main power supply response time is ≈ 50μs, then the minimum input capacitance for a 2.7A load step is given by:

$$C_{IN} = \frac{2.7 \times 50}{0.15} = 900\mu F$$

The ESR should be less than:

$$ESR = \frac{(V_{IN} - V_{OUT} - \Delta V - V_{DROP})}{\Delta I}$$

Where:
V_{DROP} **L** Input voltage drop allowed in step 4
ΔV **L** Maximum regulator dropout voltage
ΔI **L** Load current step

$$ESR = \frac{(3.3 - 1.5 - 1.2 - 0.15)}{2.7} = 0.16\Omega$$

Selecting a single 1500μF the same type as the output capacitors exceeds our requirements. However, the same input capacitor can also support the second regulator for the other end of termination.

Figure 6 shows the completed schematic for our example.

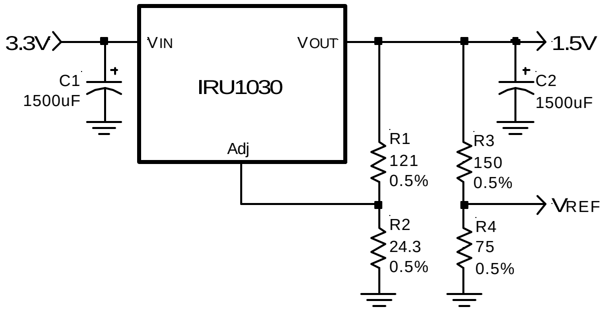


Figure 6 - Final schematic for half of the GTL+ termination regulator.

Layout Consideration

The output capacitors must be located as close to the V_{OUT} terminal of the device as possible. It is recommended to use a section of a layer of the PC board as a plane to connect the V_{OUT} pin to the output capacitors to prevent any high frequency oscillation that may result due to excessive trace inductance.

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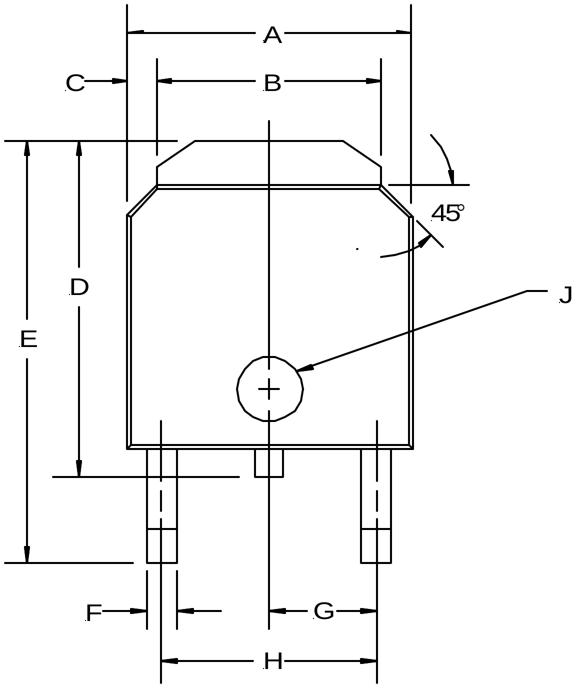
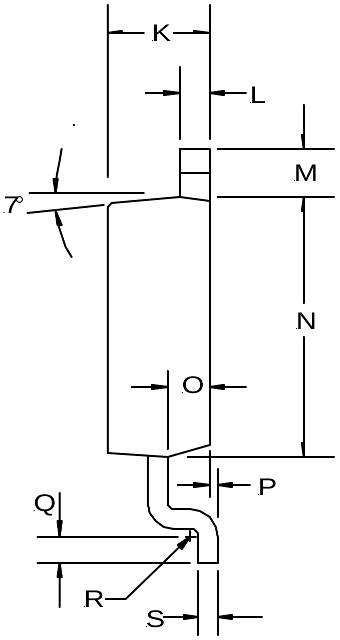
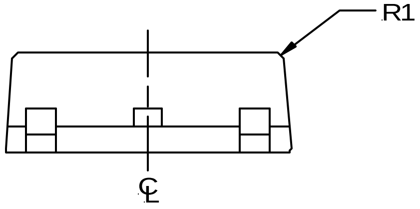
Data and specifications subject to change without notice. 02/01

(D) TO-252 Package
2-Pin



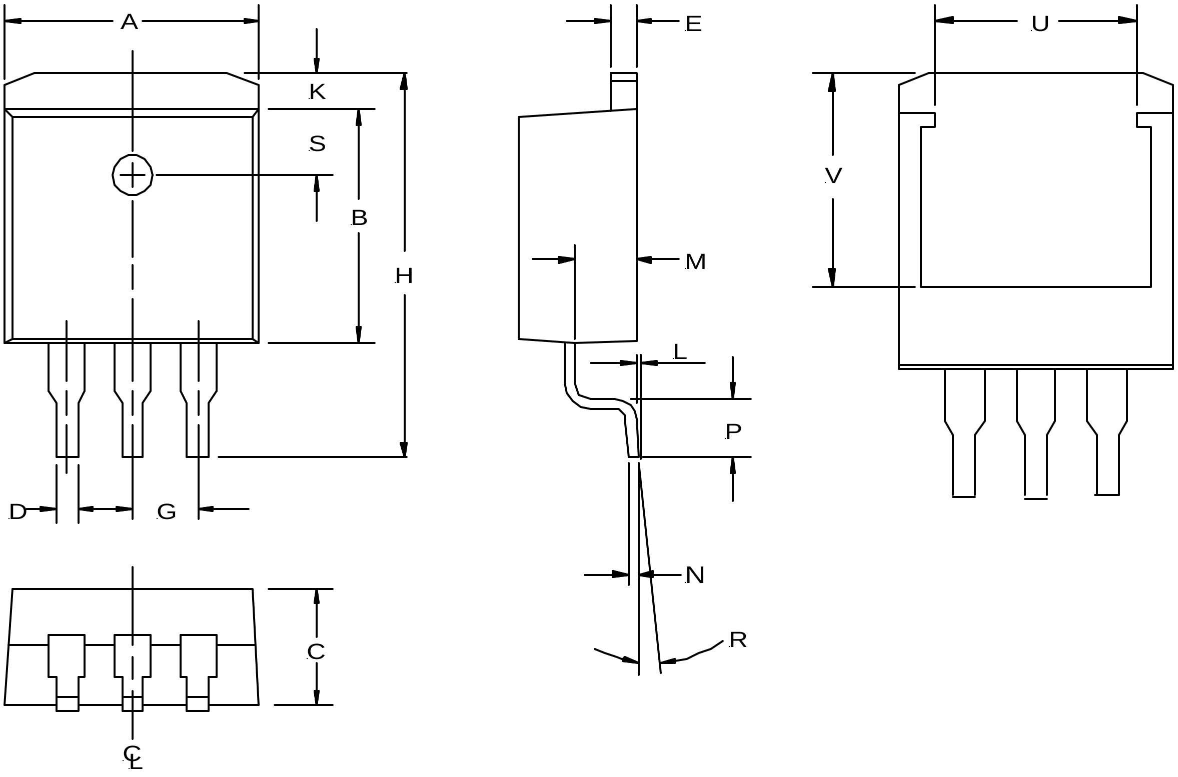




SYMBOL	MIN	MAX
A	6.477	6.731
B	5.004	5.207
C	0.686	0.838
D	7.417	8.179
E	9.703	10.084
F	0.635	0.889
G	2.286 BSC	
H	4.521	4.623
J	∅1.52	∅1.62
K	2.184	2.388
L	0.762	0.864
M	1.016	1.118
N	5.969	6.223
O	1.016	1.118
P	0	0.102
Q	0.534	0.686
R	R0.31 TYP	
R1	R0.51 TYP	
S	0.428	0.588

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

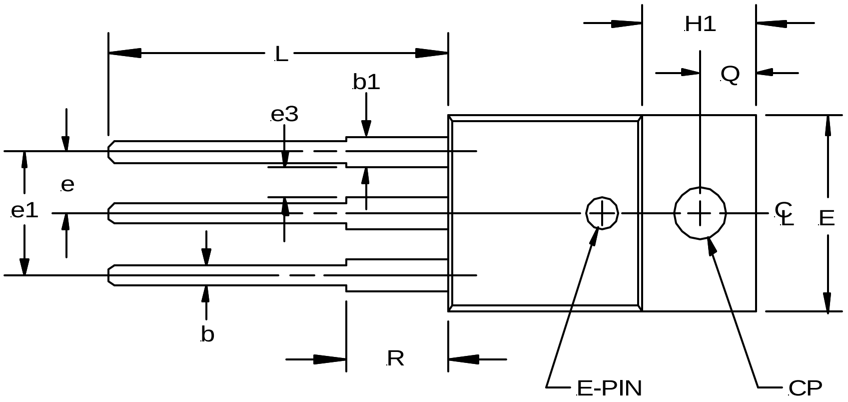
(M) TO-263 Package
3-Pin

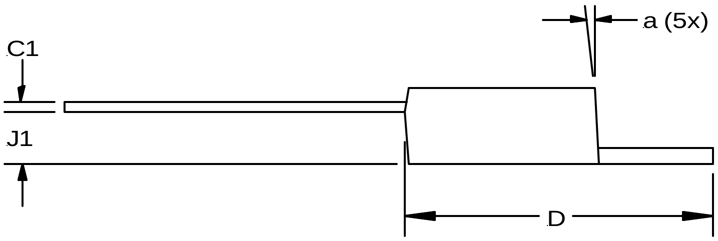


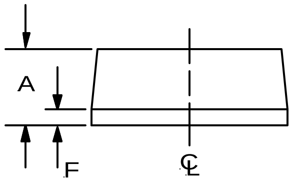
SYMBOL	MIN	MAX
A	10.05	10.312
B	8.28	8.763
C	4.31	4.572
D	0.66	0.91
E	1.14	1.40
G	2.54 REF	
H	14.73	15.75
K	1.40	1.68
L	0.00	0.254
M	2.49	2.74
N	0.33	0.58
P	2.286	2.794
R	0°	8°
S	2.41	2.67
U	6.50 REF	
V	7.75 REF	

NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

(T) TO-220 Package
3-Pin





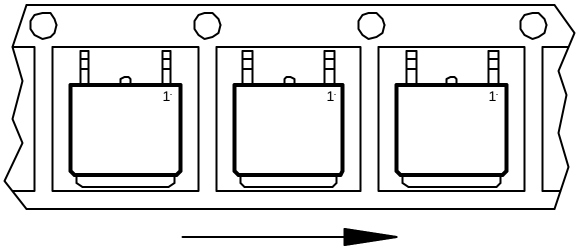


SYMBOL	MIN	MAX
A	4.06	4.83
a	3°	7.5°
b	0.63	1.02
b1	1.14	1.52
C1	0.38	0.56
CP	3.71D	3.96D
D	14.22	15.062
E	9.78	10.54
e	2.29	2.79
e1	4.83	5.33
e3	1.14	1.40
F	1.14	1.40
H1	5.94	6.55
J1	2.29	2.92
L	13.716	14.22
Q	2.62	2.87
R	5.588	6.17

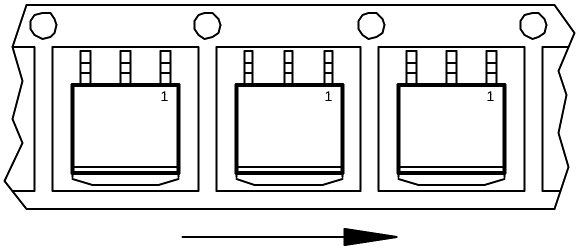
NOTE: ALL MEASUREMENTS
ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
D	TO-252, (D-Pak)	2	75	2500	Fig A
M	TO-263	3	50	750	Fig B
T	TO-220	3	50	---	---



Feed Direction
Figure A



Feed Direction
FigureB

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