THE DATASHEET OF

ISL6412IRZ-TK

ISL6412

Triple Output, Low-Noise LDO Regulator with Integrated Reset Circuit

FN9067
Rev 1.00
Mar 20, 2007

The ISL6412 is an ultra low noise triple output LDO regulator with microprocessor reset circuit and is optimized for powering wireless chip sets. The IC accepts an input voltage range of 3.0V to 3.6V and provides three regulated output voltages: 1.8V (LDO1), 2.8V (LDO2), and another ultra-clean 2.8V (LDO3). On chip logic provides sequencing between LDO1 and LDO2 for the BBP/MAC and the I/O supply voltage outputs. LDO3 features ultra low noise that does not typically exceed 30µV RMS to aid VCO stability. High integration and the thin Quad Flat No-lead (QFN) package makes the ISL6412 an ideal choice to power many of today's small form factor industry standard wireless cards such as PCMCIA, mini-PCI and Cardbus-32.

The ISL6412 uses an internal PMOS transistor as the pass device. The ISL6412 also integrates a reset function, which eliminates the need for the additional reset IC required in WLAN applications. The IC asserts a $\overline{\text{RESET}}$ signal whenever the VIN supply voltage drops below a preset threshold, keeping it asserted for a time set by a capacitor to GND after VIN has risen above the reset threshold. FAULT1 indicates the loss of regulation on LDO1.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6412IR	ISL6412IR	-40 to +85	16 Ld 4x4 QFN	L16.4x4
ISL6412IR-TK	ISL6412IR	-40 to +85	16 Ld 4x4 QFN	L16.4x4
ISL6412IR-T5K	ISL6412IR	-40 to +85	16 Ld 4x4 QFN	L16.4x4
ISL6412IRZ (Note 2)	6412IRZ	-40 to +85	16 Ld 4x4 QFN (Pb-free)	L16.4x4
ISL6412IRZ-TK (Notes 1, 2)	6412IRZ	-40 to +85	16 Ld 4x4 QFN (Pb-free)	L16.4x4

NOTES:

1. Tape and Reel available. Add "-T" suffix for Tape and Reel Packing Option
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

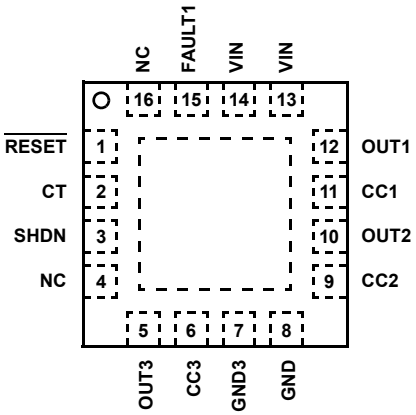
- Small DC/DC Converter Size
  - Three LDOs and Reset Circuitry in a Low-Profile 4x4mm QFN Package
- High Output Current
  - LDO1, 1.8V. 330mA
  - LDO2, 2.8V. 225mA
  - LDO3, 2.8V. 125mA
- Ultra-Low Dropout Voltage
  - LDO2, 2.8V. . . . . 125mV (typ.) at 225mA
  - LDO3, 2.8V. . . . . 100mV (typ.) at 125mA
- Ultra-Low Output Voltage Noise
  - <30µV_{RMS} (typ.) for LDO3 (VCO Supply)
- Stable with Small Ceramic Output Capacitors
- Extensive Protection and Monitoring Features
  - Over current protection
  - Short circuit protection
  - Thermal shutdown
  - FAULT indicator
- Logic-Controlled Shutdown Pin
- Integrated Microprocessor Reset Circuit
  - Programmable Reset Delay
- Proven Reference Design for a Total WLAN System Solution
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - Near Chip-Scale Package Footprint Improves PCB Efficiency and Is Thinner in Profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

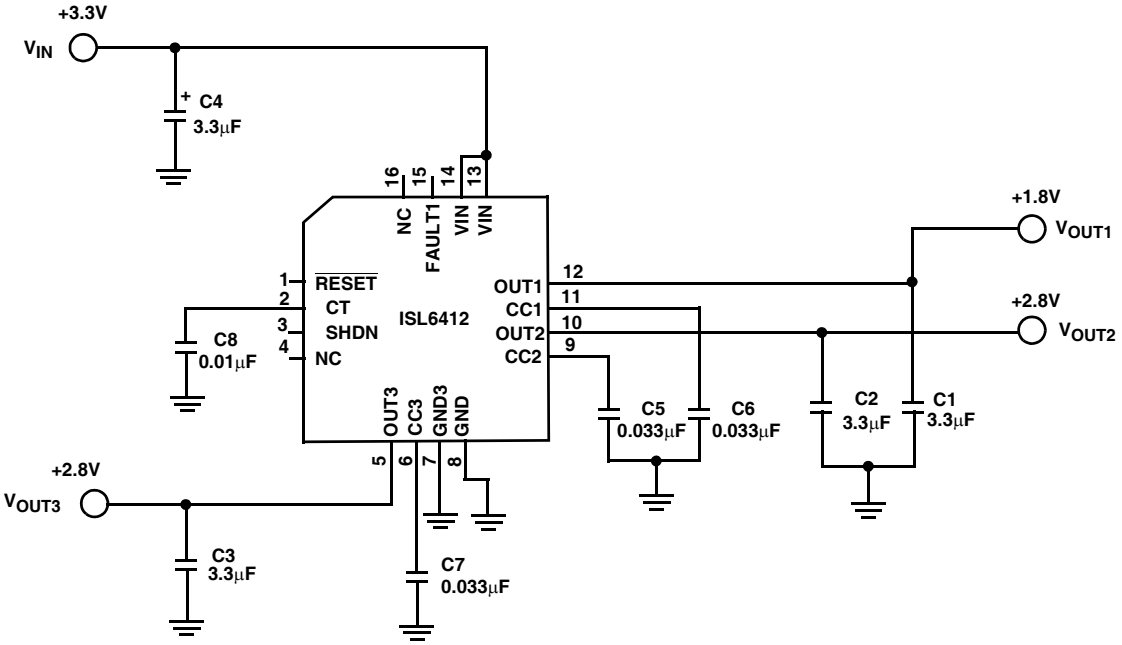
- PRISM® 3 Chipsets – ISL37106P
- WLAN Cards
  - PCMCIA, Cardbus32, MiniPCI Cards
  - Compact Flash Cards
- Liberty Chipset
- Hand-Held Instruments

Pinout

ISL6412 (16 LD QFN)
TOP VIEW



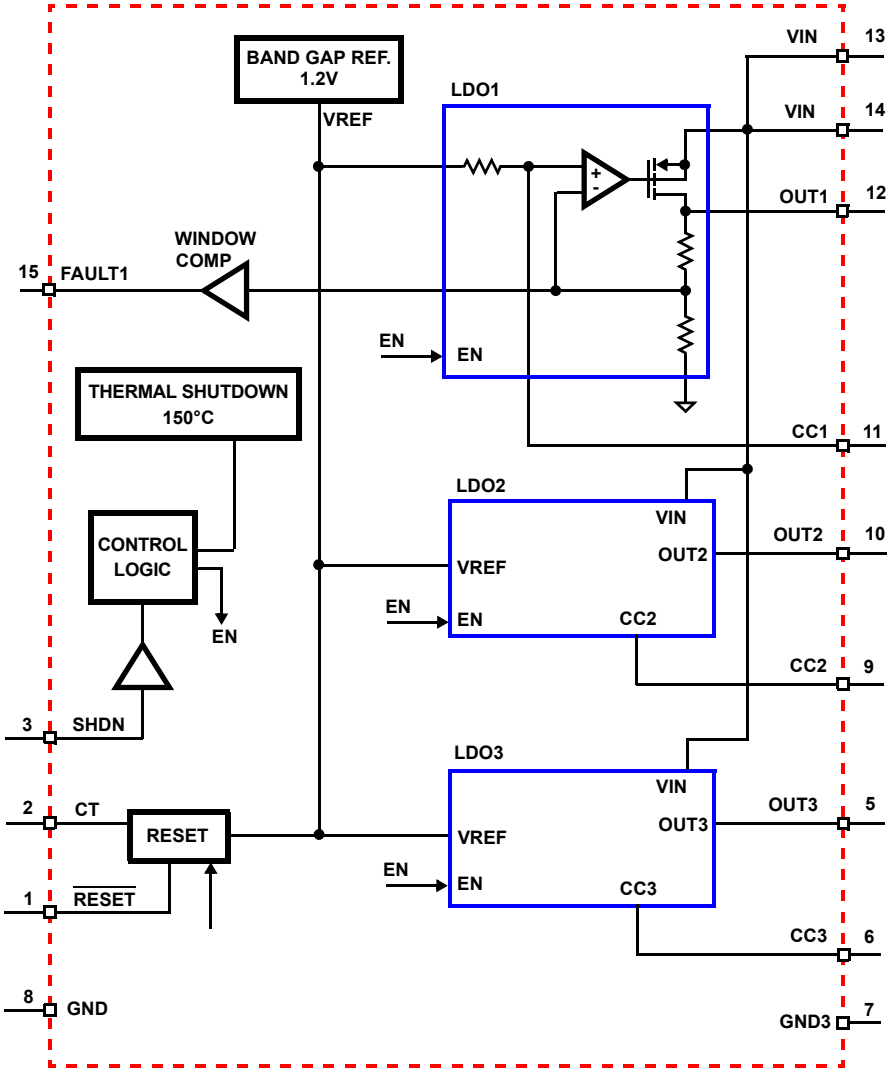
Typical Application Schematic



Typical Bill Of Materials

REFERENCE DESIGNATOR	VALUE	PACKAGE	MANUFACTURER	MANUFACTURER'S PART NUMBER
C1, C2, C3, C4	3.3µF, X7R	1206	TDK	C3216X7R1A106M
C5, C6, C7	0.033µF, X7R	0603	TDK/ANY	C1608X7R1A333K
C8	0.01µF, X7R	0603	TDK/ANY	C1608X7R1A103K
U1	ISL6412IR	QFN16	Intersil	ISL6412IR

Functional Block Diagram



Absolute Maximum Ratings

V_{IN}, SHDN to GND/GND3 . . . . . 7.0V
SET, CC, FAULT to GND/GND3 . . . . . -0.3V to 7.0V
Output Current (Continuous)
LDO1 . . . . . 330mA
LDO2 . . . . . 225mA
LDO3 . . . . . 125mA
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 3, 4)	46	9

Maximum Junction Temperature (Plastic Package) -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
Operating Temperature Range . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{IN} = +3.3V, Compensation Capacitor = 33nF, T_A = +25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL SPECIFICATIONS					
V_{IN} Voltage Range		3.0	3.3	3.6	V
Operating Supply Current	I_{OUT} = 0mA	-	830	1125	µA
Shutdown Supply Current	SHDN = GND	-	5	10	µA
SHDN Input Threshold	V_{IH}, V_{IN} = 3V to 3.6V	2.0	-	-	V
	V_{IL}, V_{IN} = 3V to 3.6V	-	-	0.4	V
Thermal Shutdown Temperature (Note 7)		145	150	160	°C
Thermal Shutdown Hysteresis (Note 7)		-	20	-	°C
Start-up Time (Note 7)	C_{OUT} = 10µF, V_{OUT} = 90% of final value	-	120	-	µs
Input Undervoltage Lockout	Rising 75mV Hysteresis	2.4	2.45	2.6	V
LDO1 SPECIFICATIONS					
Output Voltage (V_{OUT1})		-	1.8	-	V
Output Voltage Initial Accuracy	I_{OUT} = 10mA, T_A = -40°C to 85°C	-2.0	-	2.0	%
Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15	0.0	0.15	%/V
Load Regulation	I_{OUT} = 10mA to 330mA	-1.5	-	1.5	%
Maximum Output Current (I_{OUT1}) (Note 7)		330	-	-	mA
Output Current Limit (Note 7)		500	600	1105	mA
Output Voltage Noise (Note 7)	10Hz < f < 100kHz, C_{OUT} = 4.7µF, I_{OUT} = 50mA	-	115	-	μV_{RMS}
LDO2 SPECIFICATIONS					
Output Voltage (V_{OUT2})		-	2.8	-	V
Output Voltage Accuracy	I_{OUT} = 10mA, T_A = -40°C to 85°C	-2.0	-	2.0	%
Maximum Output Current (I_{OUT2}) (Note 7)	V_{IN} = 3.6V	225	-	-	mA
Output Current Limit (Note 7)		330	-	900	mA
Dropout Voltage (Notes 5, 7)	I_{OUT} = 225mA	-	125	160	mV
Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15	0.0	0.15	%/V
Load Regulation	I_{OUT} = 10mA to 225mA	-	0.2	1.0	%

Electrical Specifications V_{IN} = +3.3V, Compensation Capacitor = 33nF, T_A = +25°C, unless otherwise noted. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Noise (Note 7)	10Hz < f < 100kHz, I_{OUT} = 10mA				
	C_{OUT} = 2.2µF	-	65	-	μV_{RMS}
	C_{OUT} = 10µF	-	60	-	μV_{RMS}
LDO3 SPECIFICATIONS					
Output Voltage (V_{OUT3})		-	2.8	-	V
Output Voltage Accuracy	I_{OUT} = 10mA, T_A = -40°C to +85°C	-2.0	-	2.0	%
Maximum Output Current (I_{OUT3}) (Note 7)	V_{IN} = 3.6V	225	-	-	mA
Output Current Limit (Note 7)		300	450	840	mA
Dropout Voltage (Notes 5, 7)	I_{OUT} = 125mA	-	100	160	mV
Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15	0.0	0.15	%/V
Load Regulation	I_{OUT} = 10mA to 125mA	-	0.2	1.0	%
Output Voltage Noise (Note 7)	10Hz < f < 100kHz, I_{OUT} = 10mA				
	C_{OUT} = 2.2µF	-	30	-	μV_{RMS}
	C_{OUT} = 10µF	-	20	-	μV_{RMS}
RESET BLOCK SPECIFICATIONS					
Reset Threshold		2.564	2.630	2.66	V
Reset Threshold Hysteresis (Note 7)		6.3	-	-	mV
V_{IN} to Reset Delay	VCC = V_{TH} to V_{TH} - 100mV	-	20	-	µs
$\overline{\text{RESET}}$ Active Timeout Period (Notes 6, 7)	CT = 0.01µF	50	-	-	ms
FAULT1					
Rising Threshold	% of V_{OUT}	+5.5	+8.0	+10.5	%
Falling Threshold	% of V_{OUT}	-10.5	-8.0	-5.5	%

NOTES:

5. The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 50mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 0.5V.
6. The $\overline{\text{RESET}}$ time is linear with CT at a slope of ~5ms/nF. Thus, at 10nF (0.01µF) the $\overline{\text{RESET}}$ time is 50ms.
7. Guaranteed by design, not production tested.

Typical Performance Curves

The test conditions for the Typical Operating Performance are: V_{IN} = 3.3V, T_A = +25°C, Unless Otherwise Noted

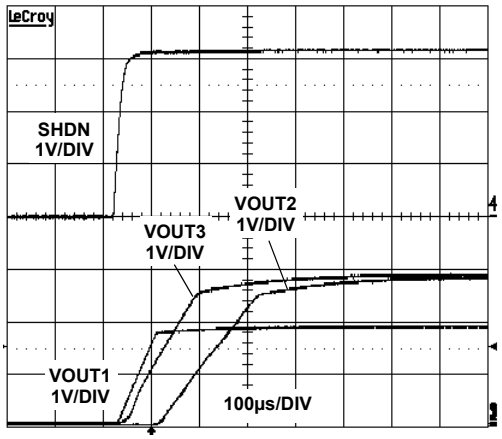


FIGURE 1. START-UP SEQUENCE

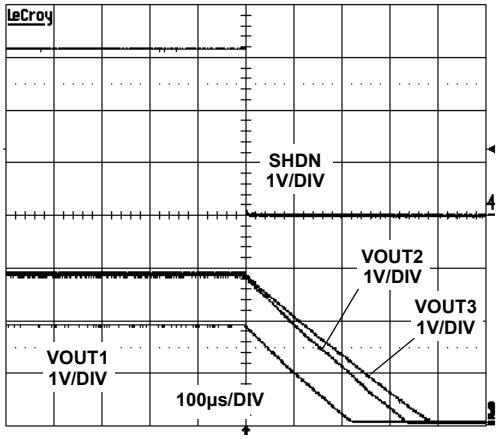


FIGURE 2. SHUTDOWN SEQUENCE

Typical Performance Curves

The test conditions for the Typical Operating Performance are: V_{IN} = 3.3V, T_A = +25°C, Unless Otherwise Noted **(Continued)**

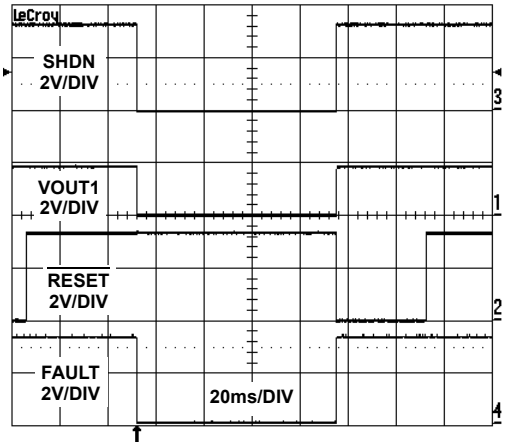


FIGURE 3. SHUTDOWN, FAULT, and $\overline{\text{RESET}}$ OPERATION

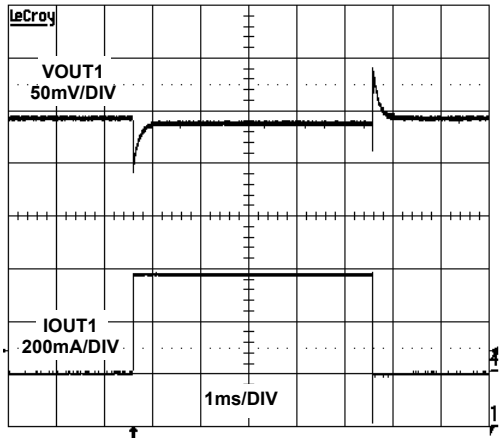


FIGURE 4. LDO1 TRANSIENT RESPONSE (10mA to 330mA)

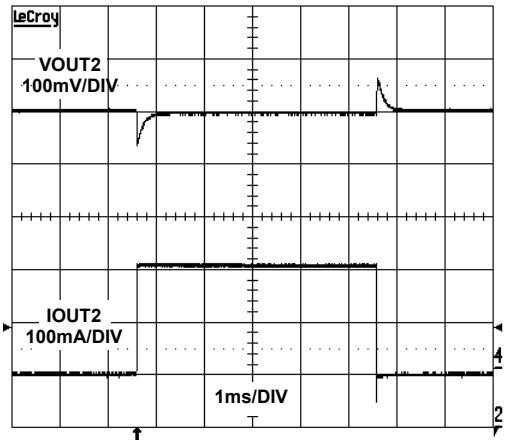


FIGURE 5. LDO2 TRANSIENT RESPONSE (10mA to 200mA)

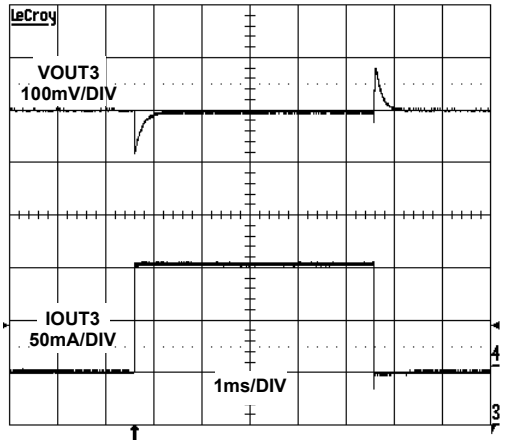


FIGURE 6. LDO3 TRANSIENT RESPONSE (10mA to 100mA)

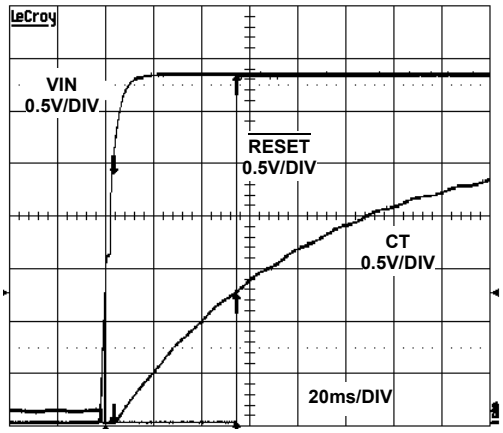


FIGURE 7. RESET DELAY DURING START-UP (CT = 0.01µF)

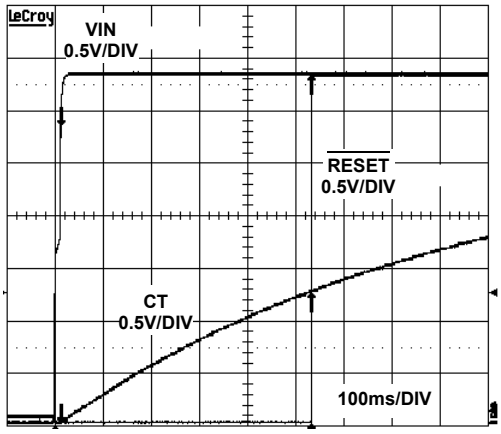


FIGURE 8. RESET DELAY DURING START-UP (CT = 0.1µF)

Typical Performance Curves

The test conditions for the Typical Operating Performance are: V_{IN} = 3.3V, T_A = +25°C, Unless Otherwise Noted **(Continued)**

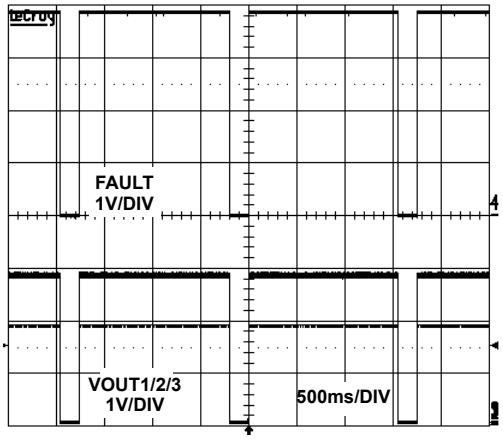


FIGURE 9. THERMAL SHUTDOWN OPERATION

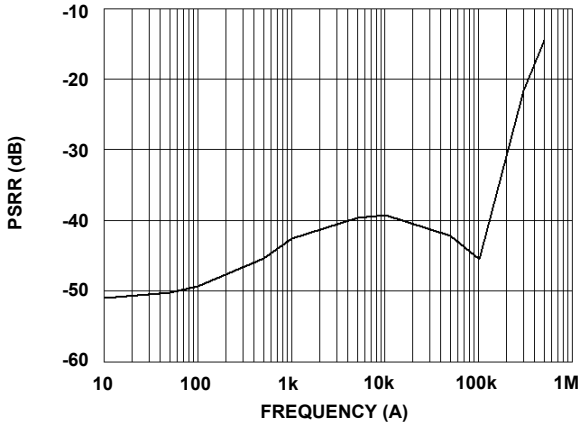


FIGURE 10. LDO1 POWER SUPPLY REJECTION (IOUT1 = 100mA, COUT = 10µF MLCC)

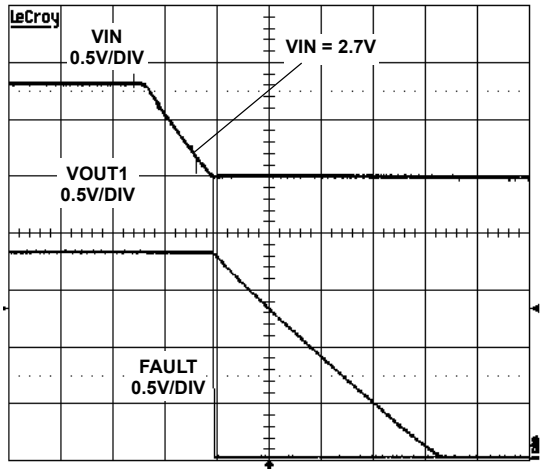


FIGURE 11. VOUT1 REGULATION DOWN TO VIN = 2.7V; FAULT MONITORS VOUT1 ONLY

Pin Descriptions

OUT1 - This pin is the output for LDO1. Bypass with a minimum of 2.2µF, low ESR capacitor to GND for stable operation.

V_{IN} - Supply input pins. Connect to input power source. Bypass with a minimum 2.2µF capacitor to GND. Both V_{IN} pins must be tied together on the PC board, close to the IC.

GND - Ground for LDO1 and LDO2.

CC1 - Compensation Capacitor for LDO1. Connect a 0.033µF capacitor from CC1 to GND.

SHDN - Shutdown input for all LDOs. Connect to V_{IN} for normal operation. Drive this pin LOW to turn off all LDOs.

OUT2 - This pin is the output for LDO2. Bypass with a minimum of 2.2µF, low ESR capacitor to GND for stable operation.

CT - Timing pin for the RESET circuit pulse width.

CC2 - Compensation capacitor for LDO2. Connect a 0.033µF capacitor from CC2 to GND.

OUT3 - This pin is output for LDO3. Bypass with a minimum of 2.2µF, low ESR capacitor to GND3 for stable operation.

GND3 - Ground pin for LDO3.

CC3 - Compensation capacitor for LDO3. Connect a 0.033µF capacitor from CC3 to GND3.

FAULT1 - This is the power good indicator for LDO1. When the 1.8V output is out of regulation this pin goes LOW. This

pin also goes LOW during thermal shutdown or an overcurrent event on LDO1. Connect this pin to GND, if unused.

$\overline{\text{RESET}}$ - This pin is the active-LOW output of the push-pull output stage of the integrated reset supervisory circuit. The reset circuit monitors V_{IN} and asserts a $\overline{\text{RESET}}$ output at this pin, if V_{IN} falls below the RESET threshold. The $\overline{\text{RESET}}$ output remains LOW, while the V_{IN} pin voltage is below the reset threshold, and for at least 25ms, after V_{IN} rises above the RESET threshold.

Functional Description

The ISL6412 is a 3-in-1 multi-output, low dropout, regulator designed for wireless chipset power applications. It supplies three fixed output voltages 1.8V, 2.8V and 2.8V. Each LDO consists of a 1.2V reference, error amplifier, MOSFET driver, P-Channel pass transistor, dual-mode comparator and internal feedback voltage divider.

The 1.2V band gap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference to the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-Channel pass transistor. If the feedback voltage is lower then the reference voltage, the pass transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher then the reference voltage, the pass transistor gate is driven higher, allowing less current to pass to the output. The output voltage is fed back through an internal resistor divider connected to OUT1/OUT2/OUT3 pins.

Additional blocks include an output overcurrent protection, thermal sensor, fault detector, $\overline{\text{RESET}}$ function and shutdown logic.

Internal P-Channel Pass Transistors

The ISL6412 features a typical 0.5Ω $r_{DS(ON)}$ P-channel MOSFET pass transistors. This provides several advantages over similar designs using PNP bipolar pass transistors. The P-Channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste considerable current in dropout when the pass transistor saturates. They also use high base drive currents under large loads. The ISL6412 does not suffer from these problems.

Integrated Reset for MAC/Baseband Processors

The ISL6412 includes a microprocessor supervisory block. This block eliminates the extra reset IC and external components needed in wireless chipset applications. This block performs a single function; it asserts a $\overline{\text{RESET}}$ signal whenever the V_{IN} supply voltage decreases below a preset threshold, keeping it asserted for a programmable time (set by external capacitor CT) after the V_{IN} pin voltage has risen above the reset threshold. The reset threshold for the ISL6412 is 2.63V typical.

The voltage at the CT pin is compared to the 1.2V bandgap voltage. The charging of the CT capacitor behaves like an RC network and the $\overline{\text{RESET}}$ delay can be approximated by:

$$Td = -R*C*\ln(1-1.2V/VIN)$$

Where C is the capacitor at CT, and R is 11.1MΩ for VIN = 3.3V. With no capacitor on the CT pin the $\overline{\text{RESET}}$ delay will be close to zero. Figure 12 shows the $\overline{\text{RESET}}$ delay vs CT capacitance.

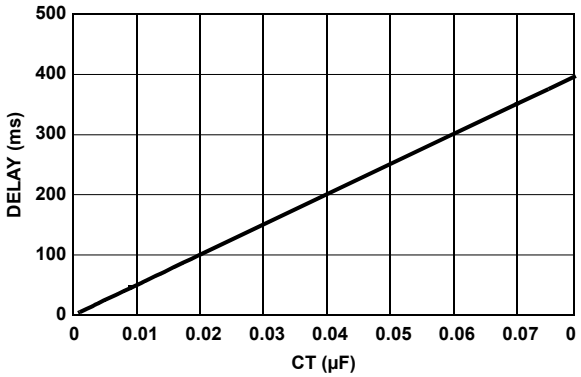


FIGURE 12. RESET DELAY vs CT CAPACITANCE

Output Voltages

The ISL6412 provides fixed output voltages for use in Wireless Chipset applications. Internal trimmed resistor networks set the typical output voltages as shown here:

V_{OUT1} = 1.8V; V_{OUT2} = 2.8V; V_{OUT3} = 2.8V.

Shutdown

Pulling the SHDN pin LOW puts the complete chip into shutdown mode, and supply current drops to 5µA typical. This input has an internal pull-up resistor, so that in normal operation the outputs are always enabled; external pull-up resistors are not required.

Current Limit

The ISL6412 monitors and controls the pass transistor's gate voltage to limit the output current. The current limit for LDO1 is 500mA, LDO2 is 330mA and LDO3 is 300mA. The output can be shorted to ground without damaging the part due to the current limit and thermal protection features.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the ISL6412. When the junction temperature (T_J) exceeds +150°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The pass transistor turns on again after the IC's junction temperature typically cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions. Thermal overload protection protects the ISL6412 against fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

Operating Region and Power Dissipation

The maximum power dissipation of ISL6412 depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipated in the device is:

PT = P1 + P2 + P3, where

$P1 = I_{OUT1} (V_{IN} – V_{OUT1})$

$P2 = I_{OUT2} (V_{IN} – V_{OUT2})$

$P3 = I_{OUT3} (V_{IN}- V_{OUT3})$

The maximum power dissipation is:

$Pmax = (Tjmax – T_A)/\theta JA$

Where Tjmax = +150°C, T_A = ambient temperature, and θJA is the thermal resistance from the junction to the surrounding environment.

The ISL6412 package features an exposed thermal pad on its underside. This pad lowers the thermal resistance of the package by providing a direct heat conduction path from the die to the PC board. Additionally, the ISL6412's ground (GND/GND3) performs the dual function of providing an electrical connection to system ground and channeling heat away. Connect the exposed backside pad and GND to the system ground using a large pad or ground plane, or through multiple vias to the ground plane layer.

Integrator Circuitry

The ISL6412 uses an external 33nF compensation capacitor for minimizing load and line regulation errors and for lowering output noise. When the output voltage shifts due to varying load current or input voltage, the integrator capacitor voltage is raised or lowered to compensate for the systematic offset at the error amplifier. Compensation is limited to ±5% to minimize transient overshoot when the device goes out of dropout, current limit, or thermal shutdown.

FAULT Functionality

TABLE 1.

EVENT	FAULT1
Below UVLO threshold	L
V_{OUT1} = 1.8V ±8% typ V_{OUT2}/V_{OUT3} not in regulation	H
V_{OUT1} not in regulation V_{OUT2} and V_{OUT3} are in regulation	L
Thermal Shutdown	L
Normal Shutdown with SHDN pin	L
Overcurrent only on LDO1	L
Overcurrent only on LDO2/LDO3	H

Applications Information

Capacitor Selection and Regulator Stability

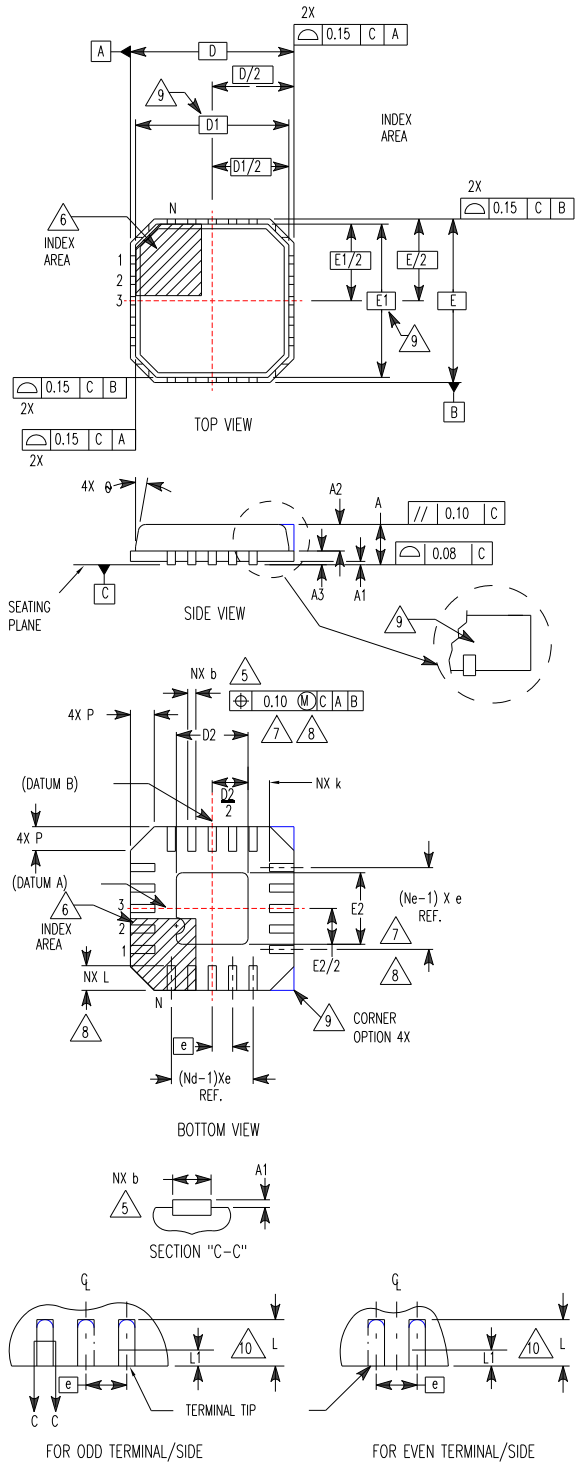
Capacitors are required at the ISL6412's input and output for stable operation over the entire load range and the full temperature range. Use >1µF capacitor at the input of ISL6412. The input capacitor lowers the source impedance of the input supply. Larger capacitor values and lower ESR provides better PSRR and line transient response. The input capacitor must be located at a distance of not more then 0.5 inches from the VIN pins of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used as an input capacitor.

The output capacitor must meet the requirements of minimum amount of capacitance and ESR for all three LDO's. The ISL6412 is specifically designed to work with small ceramic output capacitors. The output capacitor's ESR affects stability and output noise. Use an output capacitor with an ESR of 50mΩ or less to insure stability and optimum transient response. For stable operation, a ceramic capacitor, with a minimum value of 3.3µF, is recommended for V_{OUT1} for 300mA output current, and 2.2µF is recommended for V_{OUT2} and V_{OUT3} each at 200mA load current. There is no upper limit to the output capacitor value. Larger capacitor can reduce noise and improve load transient response, stability and PSRR. Higher value of output capacitor (10µF) is recommended for LDO3 when used to power VCO circuitry in wireless chipsets. The output capacitor should be located very close to VOUT pins to minimize impact of PC board inductances and the other end of the capacitor should be returned to a clean analog ground.

Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. Because the ISL6412 uses a P-channel MOSFET pass transistor, its dropout voltage is a function of $r_{DS(ON)}$ (typically 0.5) multiplied by the load current.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View ISL6412IRZ-TK on WIN SOURCE
- Intersil Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management