THE DATASHEET OF

ISL6566CR-T

ISL6566

Three-Phase Buck PWM Controller with Integrated MOSFET Drivers for VRM9, VRM10, and AMD Hammer Applications

FN9178
Rev 4.00
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The ISL6566 three-phase PWM control IC provides a precision voltage regulation system for advanced microprocessors. The integration of power MOSFET drivers into the controller IC marks a departure from the separate PWM controller and driver configuration of previous multi-phase product families. By reducing the number of external parts, this integration is optimized for a cost and space saving power management solution.

Outstanding features of this controller IC include programmable VID codes compatible with Intel VRM9, VRM10, as well as AMD Hammer microprocessors. A unity gain, differential amplifier is provided for remote voltage sensing, compensating for any potential difference between remote and local grounds. The output voltage can also be positively or negatively offset through the use of a single external resistor.

A unique feature of the ISL6566 is the combined use of both DCR and $r_{DS(ON)}$ current sensing. Load line voltage positioning (droop) and overcurrent protection are accomplished through continuous inductor DCR current sensing, while $r_{DS(ON)}$ current sensing is used for accurate channel-current balance. Using both methods of current sampling utilizes the best advantages of each technique.

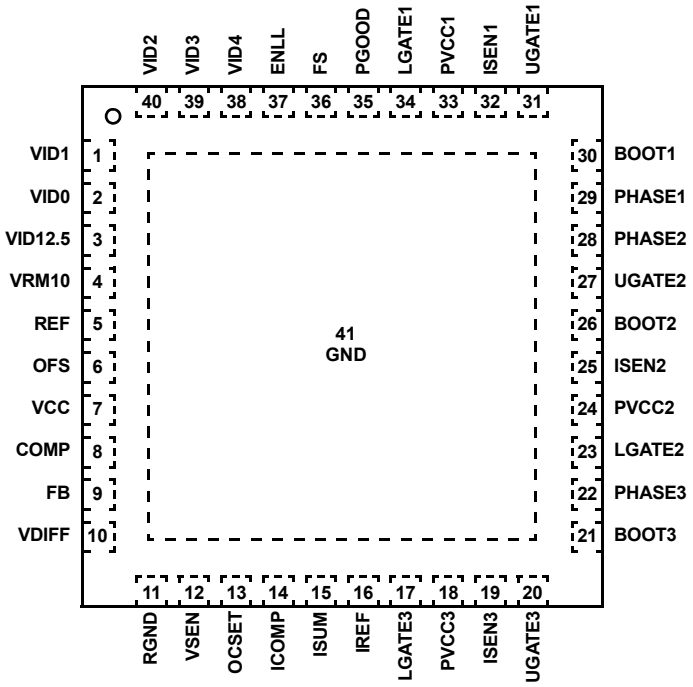
Protection features of this controller IC include a set of sophisticated overvoltage, undervoltage, and overcurrent protection. Overvoltage results in the converter turning the lower MOSFETs ON to clamp the rising output voltage and protect the microprocessor. The overcurrent protection level is set through a single external resistor. Furthermore, the ISL6566 includes protection against an open circuit on the remote sensing inputs. Combined, these features provide advanced protection for the microprocessor and power system.

Features

- Integrated Multi-Phase Power Conversion
  - 1, 2, or 3-Phase Operation
- Precision Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.5% System Accuracy Over Temperature
  - Adjustable Reference-Voltage Offset
- Precision Channel Current Sharing
  - Uses Loss-Less $r_{DS(ON)}$ Current Sampling
- Accurate Load Line Programming
  - Uses Loss-Less Inductor DCR Current Sampling
- Variable Gate Drive Bias: 5V to 12V
- Microprocessor Voltage Identification Inputs
  - Up to a 6-Bit DAC
  - Selectable between Intel's VRM9, VRM10, or AMD Hammer DAC Codes
  - Dynamic VID Technology
- Overcurrent Protection
- Multi-tiered Overvoltage Protection
- Digital Soft-Start
- Selectable Operation Frequency up to 1.5MHz Per Phase
- Pb-Free Plus Anneal Available (RoHS Compliant)

Pinout

ISL6566 (QFN)
TOP VIEW

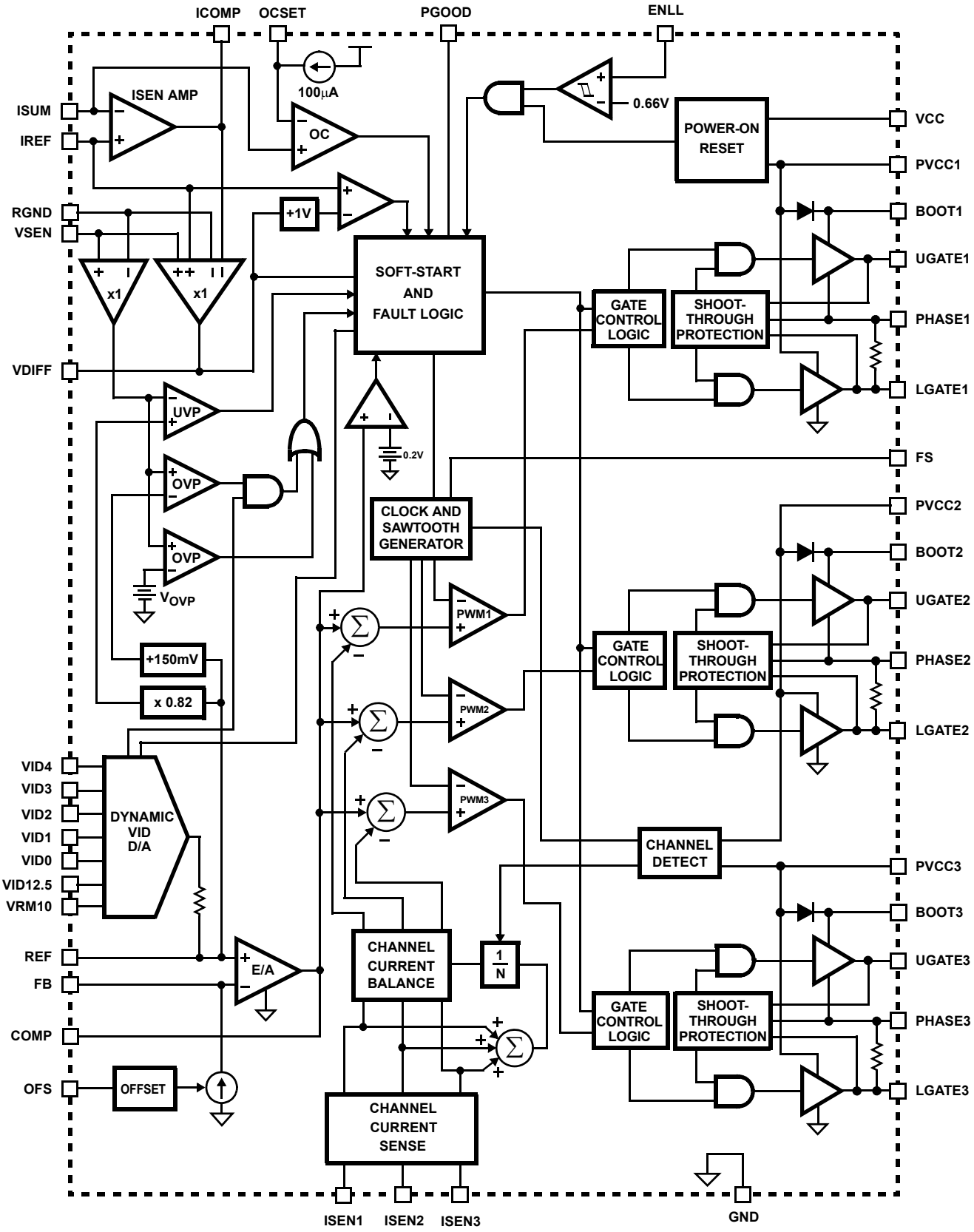


Ordering Information

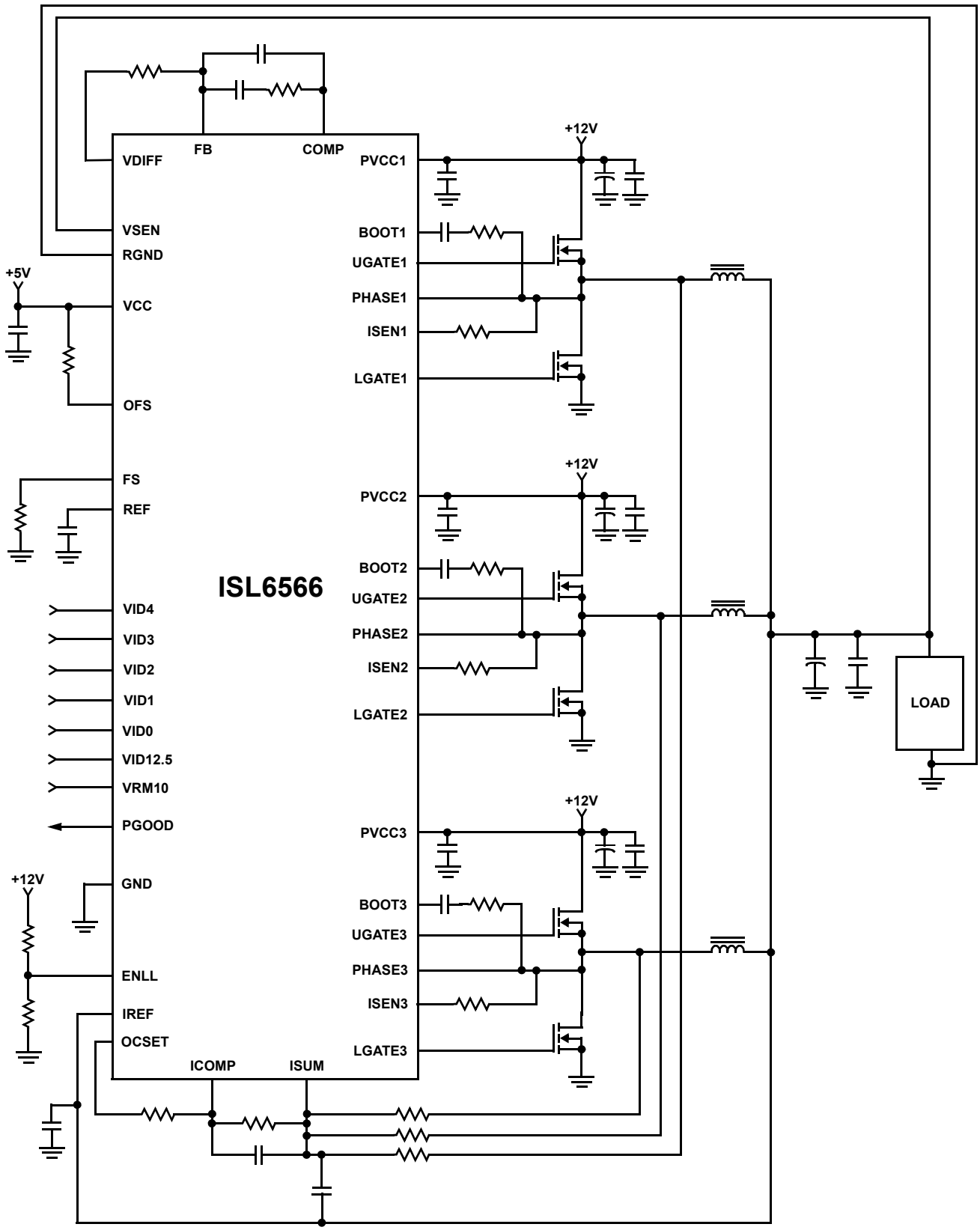
PART NUMBER	PART MARKING	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6566CRR5184	ISL6566CR	0 to 70	40 Ld 6x6 QFN	L40.6x6
ISL6566CR-TR5184	ISL6566CR	0 to 70	40 Ld 6x6 QFN Tape and Reel	L40.6x6
ISL6566CRZR5184 (Note)	ISL6566CRZ	0 to 70	40 Ld 6x6 QFN (Pb-free)	L40.6x6
ISL6566CRZ-TR5184 (Note)	ISL6566CRZ	0 to 70	40 Ld 6x6 QFN (Pb-free) Tape and Reel	L40.6x6
ISL6566CRZAR5184 (Note)	ISL6566CRZ	0 to 70	40 Ld 6x6 QFN (Pb-free)	L40.6x6
ISL6566CRZA-TR5184 (Note)	ISL6566CRZ	0 to 70	40 Ld 6x6 QFN (Pb-free) Tape and Reel	L40.6x6
ISL6566IR	ISL6566IR	-40 to 85	40 Ld 6x6 QFN	L40.6x6
ISL6566IR-T	ISL6566IR	-40 to 85	40 Ld 6x6 QFN Tape and Reel	L40.6x6
ISL6566IRZ (Note)	ISL6566IRZ	-40 to 85	40 Ld 6x6 QFN (Pb-free)	L40.6x6
ISL6566IRZ-T (Note)	ISL6566IRZ	-40 to 85	40 Ld 6x6 QFN (Pb-free) Tape and Reel	L40.6x6
ISL6566IRZA (Note)	ISL6566IRZ	-40 to 85	40 Ld 6x6 QFN (Pb-free)	L40.6x6
ISL6566IRZA-T (Note)	ISL6566IRZ	-40 to 85	40 Ld 6x6 QFN (Pb-free)	L40.6x6

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

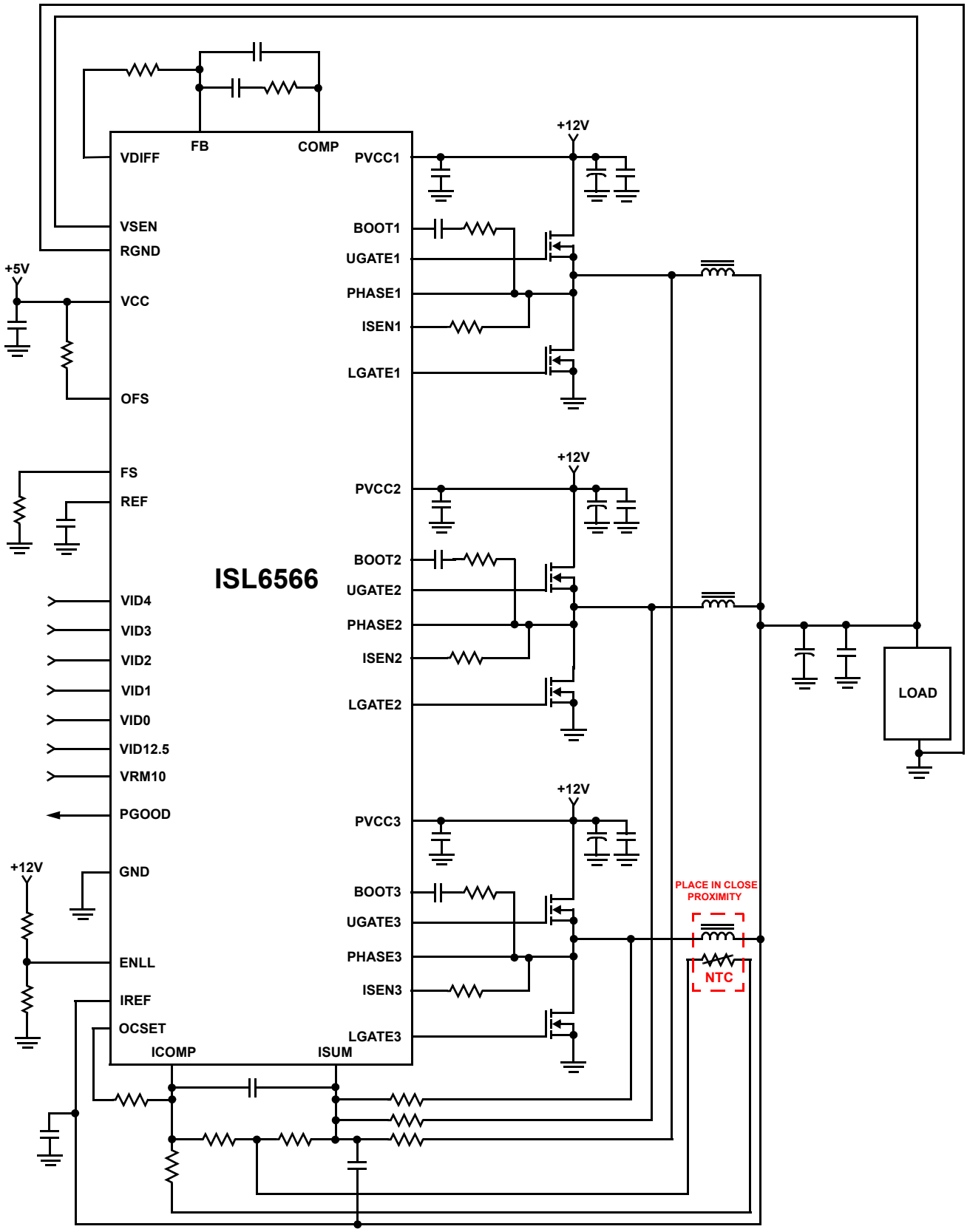
Block Diagram



Typical Application - ISL6566



Typical Application - ISL6566 with NTC Thermal Compensation



Absolute Maximum Ratings

Supply Voltage, VCC . . . . . -0.3V to +6V
Supply Voltage, PVCC . . . . . -0.3V to +15V
Absolute Boot Voltage, V_{BOOT} . . . . . GND - 0.3V to GND + 36V
Phase Voltage, V_{PHASE} . . . . . GND - 0.3V to 15V (PVCC = 12)
GND - 8V (<400ns, 20µJ) to 24V (<200ns, $V_{BOOT-PHASE}$ = 12V)
Upper Gate Voltage, V_{UGATE} . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
Lower Gate Voltage, V_{LGATE}. . . . . GND - 0.3V to PVCC + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to PVCC+ 0.3V
Input, Output, or I/O Voltage . . . . . GND - 0.3V to VCC + 0.3V
ESD Classification . . . . . Class I JEDEC STD

Recommended Operating Conditions

VCC Supply Voltage . . . . . +5V ±5%
PVCC Supply Voltage . . . . . +5V to 12V ±5%
Ambient Temperature (ISL6566CR, ISL6566CRZ) . . . . 0°C to 70°C
Ambient Temperature (ISL6566IR, ISL6566IRZ) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	32	3.5

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLY AND INTERNAL OSCILLATOR					
Input Bias Supply Current	I_{VCC}; ENLL = high	-	15	20	mA
Gate Drive Bias Current	I_{PVCC}; ENLL = high	-	0.8	-	mA
VCC POR (Power-On Reset) Threshold	VCC Rising	4.25	4.38	4.50	V
	VCC Falling	3.75	3.88	4.00	V
PVCC POR (Power-On Reset) Threshold	PVCC Rising	4.25	4.38	4.50	V
	PVCC Falling	3.60	3.88	4.00	V
Oscillator Ramp Amplitude (Note 3)	V_{PP}	-	1.50	-	V
Maximum Duty Cycle (Note 3)		-	66.6	-	%
Oscillator Frequency, F_{SW}	R_T = 100kΩ (± 0.1%)	225	250	275	kHz
CONTROL THRESHOLDS					
ENLL Rising Threshold		-	0.66	-	V
ENLL Hysteresis		-	100	-	mV
COMP Shutdown Threshold	COMP Falling	0.2	0.3	0.4	V
REFERENCE AND DAC					
System Accuracy (VID = 1.0V - 1.850V)		-0.5	-	0.5	%
System Accuracy (VID = 0.8V - 1.0V)		-0.8	-	0.8	%
DAC Input Low Voltage (VR9, VR10)		-	-	0.4	V
DAC Input High Voltage (VR9, VR10)		0.8	-	-	V
DAC Input Low Voltage (AMD)		-	-	0.6	V
DAC Input High Voltage (AMD)		1.0	-	-	V
OFS Sink Current Accuracy (Negative Offset)	R_{OFS} = 30kΩ from OFS to VCC	47.5	50.0	52.5	µA
OFS Source Current Accuracy (Positive Offset)	R_{OFS} = 10kΩ from OFS to GND	47.5	50.0	52.5	µA

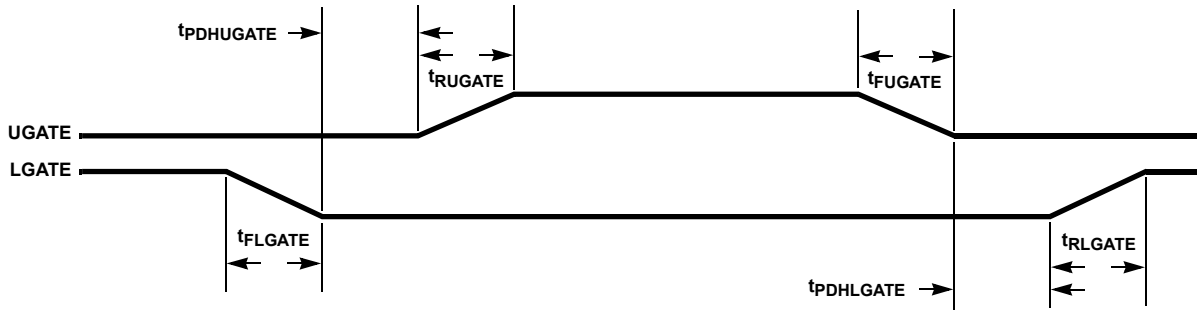
Electrical Specifications Recommended Operating Conditions, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER					
DC Gain (Note 3)	R_L = 10K to ground	-	96	-	dB
Gain-Bandwidth Product (Note 3)	C_L = 100pF, R_L = 10K to ground	-	20	-	MHz
Slew Rate (Note 3)	C_L = 100pF, Load = ±400µA	-	8	-	V/µs
Maximum Output Voltage	Load = 1mA	3.90	4.20	-	V
Minimum Output Voltage	Load = -1mA	-	0.85	1.0	V
OVERCURRENT PROTECTION					
OCSET trip current		93	100	107	µA
OCSET Accuracy	OCSET and ISUM Difference	-5	0	5	mV
ICOMP Offset		-5	0	5	mV
PROTECTION					
Undervoltage Threshold	VSEN falling	80	82	84	%VID
Undervoltage Hysteresis	VSEN Rising	-	3	-	%VID
Overvoltage Threshold while IC Disabled	V_{OVP}, VRM9.0 Configuration	1.92	1.97	2.02	V
	V_{OVP}, Hammer and VRM10.0 Configurations	1.62	1.67	1.72	V
Overvoltage Threshold	VSEN Rising	VID + 125mV	VID + 150mV	VID + 175mV	V
Overvoltage Hysteresis	VSEN Falling	-	50	-	mV
Open Sense-Line Protection Threshold	IREF Rising and Falling	VDIFF + 0.9V	VDIFF + 1V	VDIFF + 1.1V	V
SWITCHING TIME (Note 3)					
UGATE Rise Time	t_{RUGATE}; V_{PVCC} = 12V, 3nF Load, 10% to 90%	-	26	-	ns
LGATE Rise Time	t_{RLGATE}; V_{PVCC} = 12V, 3nF Load, 10% to 90%	-	18	-	ns
UGATE Fall Time	t_{FUGATE}; V_{PVCC} = 12V, 3nF Load, 90% to 10%	-	18	-	ns
LGATE Fall Time	t_{FLGATE}; V_{PVCC} = 12V, 3nF Load, 90% to 10%	-	12	-	ns
UGATE Turn-On Non-overlap	$t_{PDHUGATE}$; V_{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
LGATE Turn-On Non-overlap	$t_{PDHLGATE}$; V_{PVCC} = 12V, 3nF Load, Adaptive	-	10	-	ns
GATE DRIVE RESISTANCE (Note 3)					
Upper Drive Source Resistance	V_{PVCC} = 12V, 15mA Source Current	1.25	2.0	3.0	Ω
Upper Drive Sink Resistance	V_{PVCC} = 12V, 15mA Sink Current	0.9	1.65	3.0	Ω
Lower Drive Source Resistance	V_{PVCC} = 12V, 15mA Source Current	0.85	1.25	2.2	Ω
Lower Drive Sink Resistance	V_{PVCC} = 12V, 15mA Sink Current	0.60	0.80	1.35	Ω
OVER TEMPERATURE SHUTDOWN					
Thermal Shutdown Setpoint (Note 3)		-	160	-	°C
Thermal Recovery Setpoint (Note 3)		-	100	-	°C

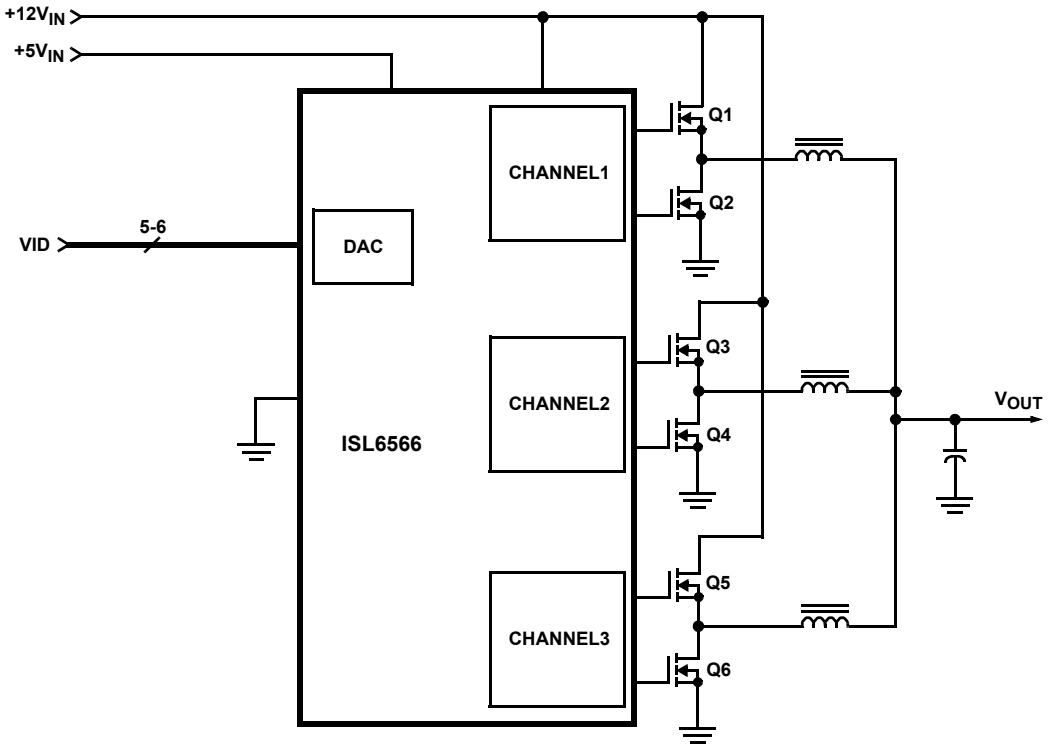
NOTE:

3. Parameter magnitude guaranteed by design. Not 100% tested.

Timing Diagram



Simplified Power System Diagram



Functional Pin Description

VCC

VCC is the bias supply for the ICs small-signal circuitry. Connect this pin to a +5V supply and locally decouple using a quality 1.0µF ceramic capacitor.

PVCC1, PVCC2, PVCC3

These pins are the power supply pins for the corresponding channel MOSFET drive, and can be connected to any voltage from +5V to +12V, depending on the desired MOSFET gate drive level.

The number of active channels is determined by the state of PVCC2 and PVCC3. Leave PVCC3 unconnected or grounded for 2-phase operation. For 1-phase operation leave both PVCC3 and PVCC2 unconnected or grounded.

GND

GND is the bias and reference ground for the IC.

ENLL

This pin is a threshold-sensitive (approximately 0.66V) enable input for the controller. Held low, this pin disables controller operation. Pulled high, the pin enables the controller for operation. ENLL has a internal 1.0µA pull-up to 5V.

FS

A resistor, placed from FS to ground, will set the switching frequency. Refer to Equation 34 for proper resistor calculation.

VID4, VID3, VID2, VID1, VID0, and VID12.5

These are the inputs for the internal DAC that provides the reference voltage for output regulation. These pins respond to TTL logic thresholds. The ISL6566 decodes the VID inputs to establish the output voltage; see VID Tables for correspondence between DAC codes and output voltage settings. These pins are internally pulled high, to approximately 1.2V, by 40µA (typically) internal current sources; the internal pull-up current decreases to 0 as the VID voltage approaches the internal pull-up voltage. All VID pins are compatible with external pull-up voltages not exceeding the IC's bias voltage (VCC).

VRM10

This pin selects VRM10.0 DAC compliance when pulled high or open. If VRM10 is grounded, VID12.5 selects the compliance standard for the internal DAC: pulled to ground, it encodes the DAC with AMD Hammer VID codes, while left open or pulled high, it encodes the DAC with Intel VRM9.0 codes.

VSEN and RGND

VSEN and RGND are inputs to the precision differential remote-sense amplifier and should be connected to the sense pins of the remote load.

ICOMP, ISUM, and IREF

ISUM, IREF, and ICOMP are the DCR current sense amplifier's negative input, positive input, and output respectively. For accurate DCR current sensing, connect a resistor from each channel's phase node to ISUM and connect IREF to the summing point of the output inductors, roughly Vout. A parallel R-C feedback circuit connected between ISUM and ICOMP will then create a voltage from IREF to ICOMP proportional to the voltage drop across the inductor DCR. This voltage is referred to as the droop voltage and is added to the differential remote-sense amplifier output.

Note: An optional 0.01µF ceramic capacitor can be placed from the IREF pin to the ISUM pin, or from the IREF pin to GND to help reduce any noise affects that may occur due to layout.

VDIFF

VDIFF is the output of the differential remote-sense amplifier. The voltage on this pin is equal to the difference between VSEN and RGND added to the difference between IREF and ICOMP. VDIFF therefore represents the output voltage plus the droop voltage.

FB and COMP

These pins are the internal error amplifier inverting input and output respectively. FB, VDIFF, and COMP are tied together through external R-C networks to compensate the regulator.

REF

The REF input pin is the positive input of the error amplifier. It is internally connected to the DAC output through a 1kΩ resistor. A capacitor is used between the REF pin and ground to smooth the voltage transition during Dynamic VID operations.

OFS

The OFS pin provides a means to program a dc current for generating an offset voltage across the resistor between FB and VDIFF. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unconnected.

OCSET

This is the overcurrent set pin. Placing a resistor from OCSET to ICOMP allows a 100µA current to flow out this pin, producing a voltage reference. Internal circuitry compares the voltage at OCSET to the voltage at ISUM, and if ISUM ever exceeds OCSET, the overcurrent protection activates.

ISEN1, ISEN2 and ISEN3

These pins are used for balancing the channel currents by sensing the current through each channel's lower MOSFET when it is conducting. Connect a resistor between the ISEN1, ISEN2, and ISEN3 pins and their respective phase node. This resistor sets a current proportional to the current in the lower MOSFET during its conduction interval.

UGATE1, UGATE2, and UGATE3

Connect these pins to the corresponding upper MOSFET gates. These pins are used to control the upper MOSFETs and are monitored for shoot-through prevention purposes. Maximum individual channel duty cycle is limited to 66%.

BOOT1, BOOT2, and BOOT3

These pins provide the bias voltage for the corresponding upper MOSFET drives. Connect these pins to appropriately-chosen external bootstrap capacitors. Internal bootstrap diodes connected to the PVCC pins provide the necessary bootstrap charge.

PHASE1, PHASE2, and PHASE3

Connect these pins to the sources of the corresponding upper MOSFETs. These pins are the return path for the upper MOSFET drives.

LGATE1, LGATE2, and LGATE3

These pins are used to control the lower MOSFETs. Connect these pins to the corresponding lower MOSFETs' gates.

PGOOD

During normal operation PGOOD indicates whether the output voltage is within specified overvoltage and undervoltage limits. If the output voltage exceeds these limits or a reset event occurs (such as an overcurrent event), PGOOD is pulled low. PGOOD is always low prior to the end of soft-start.

Operation

Multi-Phase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multi-phase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter that is both cost-effective and thermally viable have forced a change to the cost-saving approach of multi-phase. The ISL6566 controller helps simplify implementation by integrating vital functions and requiring minimal external components. The block diagram on page 3 provides a top level view of multi-phase power conversion using the ISL6566 controller.

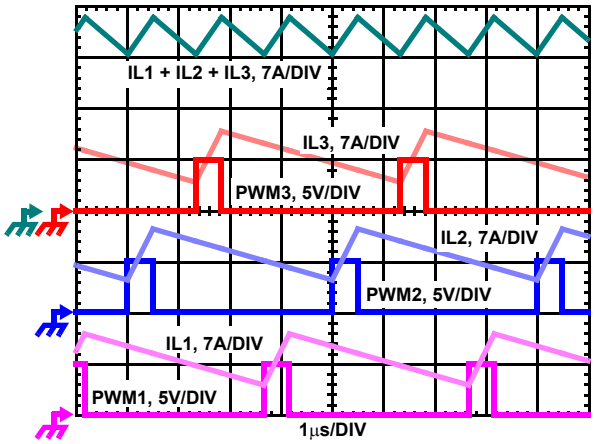


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the dc components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine the equation representing an individual channel peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{L f_S V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N V_{OUT})V_{OUT}}{L f_S V_{IN}} \quad \text{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 1.5V to a 36A load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

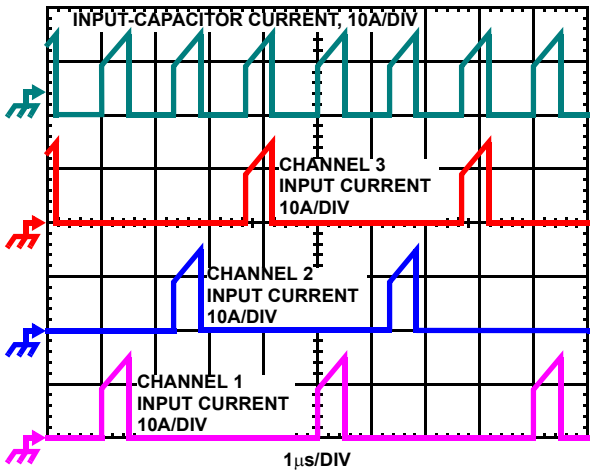


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Figures 22 and 23 in the section entitled *Input Capacitor Selection* can be used to determine the input-capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution.

PWM Operation

The timing of each converter leg is set by the number of active channels. The default channel setting for the ISL6566 is three. One switching cycle is defined as the time between the internal PWM1 pulse termination signals. The pulse termination signal is the internally generated clock signal that triggers the falling edge of PWM1. The cycle time of the pulse termination signal is the inverse of the switching frequency set by the resistor between the FS pin and ground. Each cycle begins when the clock signal commands PWM1 to go low. The PWM1 transition signals the internal channel-1 MOSFET driver to turn off the channel-1 upper MOSFET and turn on the channel-1 synchronous MOSFET. In the default channel configuration, the PWM2 pulse terminates 1/3 of a cycle after the PWM1 pulse. The PWM3 pulse terminates 1/3 of a cycle after PWM2.

If PVCC3 is left open or connected to ground, two channel operation is selected and the PWM2 pulse terminates 1/2 of a cycle after the PWM1 pulse terminates. If both PVCC3 and PVCC2 are left open or connected to ground, single channel operation is selected.

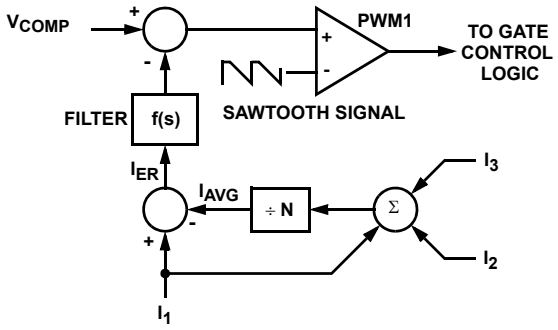
Once a PWM pulse transitions low, it is held low for a minimum of 1/3 cycle. This forced off time is required to ensure an accurate current sample. Current sensing is described in the next section. After the forced off time expires, the PWM output is enabled. The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, minus the current correction signal relative to the sawtooth ramp as illustrated in Figure 3. When the modified V_{COMP} voltage crosses the sawtooth ramp, the PWM output transitions high. The internal MOSFET driver detects the change in state of the PWM signal and turns off the synchronous MOSFET and turns on the upper MOSFET. The PWM signal will remain high until the pulse termination signal marks the beginning of the next cycle by triggering the PWM signal low.

Channel-Current Balance

One important benefit of multi-phase operation is the thermal advantage gained by distributing the dissipated heat over multiple devices and greater area. By doing this the designer avoids the complexity of driving parallel MOSFETs and the expense of using expensive heat sinks and exotic magnetic materials.

In order to realize the thermal advantage, it is important that each channel in a multi-phase converter be controlled to carry about the same amount of current at any load level. To achieve this, the currents through each channel must be sampled every switching cycle. The sampled currents, I_n, from each active channel are summed together and divided by the number of active channels. The resulting cycle average current, I_{AVG}, provides a measure of the total load-current demand on the converter during each switching cycle. Channel-current balance is achieved by comparing the sampled current of each channel to the cycle average current, and making the proper adjustment to each channel pulse width based on the error. Intersil's patented current-balance method is illustrated in Figure 3, with error correction for channel 1 represented. In the figure, the cycle average current, I_{AVG}, is compared with the channel 1 sample, I_1, to create an error signal I_{ER}.

The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.



NOTE: Channel 2 and 3 are optional.

FIGURE 3. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Current Sampling

In order to realize proper current-balance, the currents in each channel must be sampled every switching cycle. This sampling occurs during the forced off-time, following a PWM transition low. During this time the current-sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. This sensed current, I_{SEN}, is simply a scaled version of the inductor current. The sample window opens exactly 1/6 of the switching period, t_{SW}, after the PWM transitions low. The sample window then stays open the rest of the switching cycle until PWM transitions high again, as illustrated in Figure 4.

The sampled current, at the end of the t_{SAMPLE}, is proportional to the inductor current and is held until the next switching period sample. The sampled current is used only for channel-current balance.

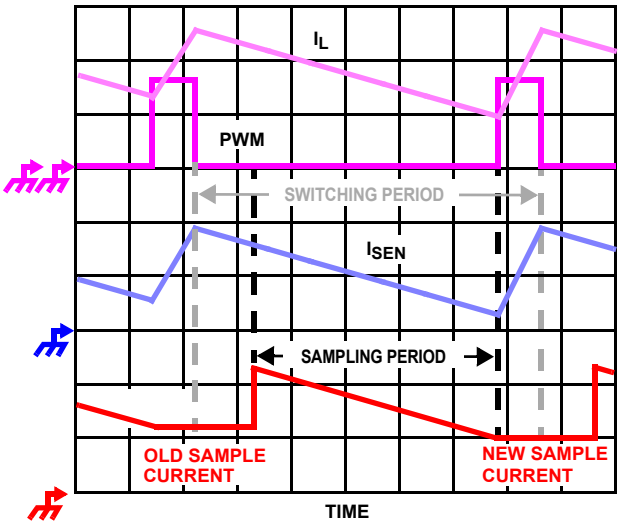


FIGURE 4. SAMPLE AND HOLD TIMING

The ISL6566 supports MOSFET $r_{DS(ON)}$ current sensing to sample each channel's current for channel-current balance. The internal circuitry, shown in Figure 5 represents channel n of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on the status of the PVCC3 and PVCC2 pins, as described in the *PWM Operation* section.

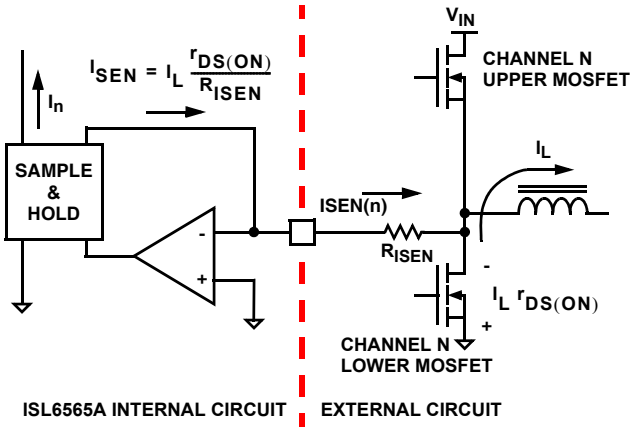


FIGURE 5. ISL6566 INTERNAL AND EXTERNAL CURRENT-SENSING CIRCUITRY FOR CURRENT BALANCE

The ISL6566 senses the channel load current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$, as shown in Figure 5. A ground-referenced operational amplifier, internal to the ISL6566, is connected to the PHASE node through a resistor, R_{ISEN}. The voltage across R_{ISEN} is equivalent to the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET while it is conducting. The resulting current into the ISEN pin is proportional to the channel current, I_L. The ISEN current is sampled and held as described in the *Current Sampling* section. From Figure 5, the following equation for I_n is derived where I_L is the channel current.

$$I_n = I_L \frac{r_{DS(ON)}}{R_{ISEN}} \quad \text{(EQ. 3)}$$

Output Voltage Setting

The ISL6566 uses a digital to analog converter (DAC) to generate a reference voltage based on the logic signals at the VID pins. The DAC decodes the 5 or 6-bit logic signals into one of the discrete voltages shown in Tables 2, 3, and 4. Each VID pin is pulled up to an internal 1.2V voltage by a weak current source (40µA current), which decreases to 0 as the voltage at the VID pin varies from 0 to the internal 1.2V pull-up voltage. External pull-up resistors or active-high output stages can augment the pull-up current sources, up to a voltage of 5V.

The ISL6566 accommodates three different DAC ranges: Intel VRM9.0, AMD Hammer, or Intel VRM10.0. The state of the VRM10 and VID12.5 pins decide which DAC version is active. Refer to Table 1 for a description of how to select the desired DAC version.

TABLE 1. ISL6566 DAC SELECT TABLE

DAC VERSION	VRM10 PIN	VID12.5 PIN
VRM10.0	high	-
VRM9.0	low	high
AMD HAMMER	low	low

TABLE 2. AMD HAMMER VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	0.800
1	1	1	0	1	0.825
1	1	1	0	0	0.850
1	1	0	1	1	0.875
1	1	0	1	0	0.900
1	1	0	0	1	0.925
1	1	0	0	0	0.950
1	0	1	1	1	0.975
1	0	1	1	0	1.000
1	0	1	0	1	1.025
1	0	1	0	0	1.050
1	0	0	1	1	1.075
1	0	0	1	0	1.100
1	0	0	0	1	1.125
1	0	0	0	0	1.150
0	1	1	1	1	1.175
0	1	1	1	0	1.200
0	1	1	0	1	1.225
0	1	1	0	0	1.250
0	1	0	1	1	1.275
0	1	0	1	0	1.300

TABLE 2. AMD HAMMER VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
0	1	0	0	1	1.325
0	1	0	0	0	1.350
0	0	1	1	1	1.375
0	0	1	1	0	1.400
0	0	1	0	1	1.425
0	0	1	0	0	1.450
0	0	0	1	1	1.475
0	0	0	1	0	1.500
0	0	0	0	1	1.525
0	0	0	0	0	1.550

TABLE 3. VRM9 VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725

TABLE 3. VRM9 VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VDAC
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

TABLE 4. VRM10 VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
1	1	1	1	1	1	Off
1	1	1	1	1	0	Off
0	1	0	1	0	0	0.8375
0	1	0	0	1	1	0.8500
0	1	0	0	1	0	0.8625
0	1	0	0	0	1	0.8750
0	1	0	0	0	0	0.8875
0	0	1	1	1	1	0.9000
0	0	1	1	1	0	0.9125
0	0	1	1	0	1	0.9250
0	0	1	1	0	0	0.9375
0	0	1	0	1	1	0.9500
0	0	1	0	1	0	0.9625
0	0	1	0	0	1	0.9750
0	0	1	0	0	0	0.9875
0	0	0	1	1	1	1.0000
0	0	0	1	1	0	1.0125
0	0	0	1	0	1	1.0250
0	0	0	1	0	0	1.0375
0	0	0	0	1	1	1.0500
0	0	0	0	1	0	1.0625
0	0	0	0	0	1	1.0750
0	0	0	0	0	0	1.0875
1	1	1	1	0	1	1.1000
1	1	1	1	0	0	1.1125
1	1	1	0	1	1	1.1250
1	1	1	0	1	0	1.1375
1	1	1	0	0	1	1.1500
1	1	1	0	0	0	1.1625
1	1	0	1	1	1	1.1750
1	1	0	1	1	0	1.1875
1	1	0	1	0	1	1.2000

TABLE 4. VRM10 VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
1	1	0	1	0	0	1.2125
1	1	0	0	1	1	1.2250
1	1	0	0	1	0	1.2375
1	1	0	0	0	1	1.2500
1	1	0	0	0	0	1.2625
1	0	1	1	1	1	1.2750
1	0	1	1	1	0	1.2875
1	0	1	1	0	1	1.300
1	0	1	1	0	0	1.3125
1	0	1	0	1	1	1.3250
1	0	1	0	1	0	1.3375
1	0	1	0	0	1	1.3500
1	0	1	0	0	0	1.3625
1	0	0	1	1	1	1.3750
1	0	0	1	1	0	1.3875
1	0	0	1	0	1	1.4000
1	0	0	1	0	0	1.4125
1	0	0	0	1	1	1.4250
1	0	0	0	1	0	1.4375
1	0	0	0	0	1	1.4500
1	0	0	0	0	0	1.4625
0	1	1	1	1	1	1.4750
0	1	1	1	1	0	1.4875
0	1	1	1	0	1	1.5000
0	1	1	1	0	0	1.5125
0	1	1	0	1	1	1.5250
0	1	1	0	1	0	1.5375
0	1	1	0	0	1	1.5500
0	1	1	0	0	0	1.5625
0	1	0	1	1	1	1.5750
0	1	0	1	1	0	1.5875
0	1	0	1	0	1	1.6000

Voltage Regulation

In order to regulate the output voltage to a specified level, the ISL6566 uses the integrating compensation network shown in Figure 6. This compensation network insures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6566 to include the combined tolerances of each of these elements.

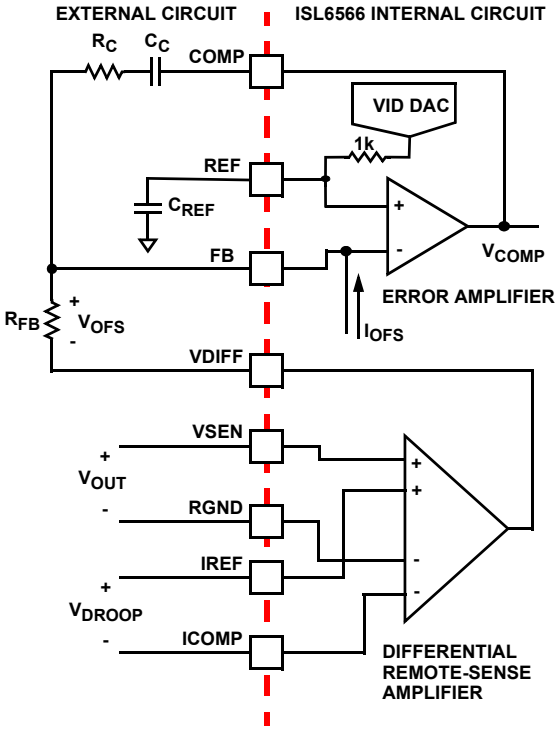


FIGURE 6. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

The ISL6566 incorporates an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the controller ground reference point, resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The droop voltage, V_{DROOP}, also feeds into the remote-sense amplifier. The remote-sense output, V_{DIFF}, is therefore equal to the sum of the output voltage, V_{OUT}, and the droop voltage. V_{DIFF} is connected to the inverting input of the error amplifier through an external resistor.

The output of the error amplifier, V_{COMP}, is compared to the sawtooth waveform to generate the PWM signals. The PWM signals control the timing of the Internal MOSFET drivers and regulate the converter output so that the voltage at FB is equal to the voltage at REF. This will regulate the output voltage to be equal to Equation 4. The internal and external circuitry that controls voltage regulation is illustrated in Figure 6.

$$V_{OUT} = V_{REF} - V_{OFS} - V_{DROOP} \quad \text{(EQ. 4)}$$

Load-Line (Droop) Regulation

Some microprocessor manufacturers require a precisely-controlled output impedance. This dependence of output voltage on load current is often termed “droop” or “load line” regulation.

As shown in Figure 6, a voltage, V_{DROOP}, proportional to the total current in all active channels, I_{OUT}, feeds into the differential remote-sense amplifier. The resulting voltage at the output of the remote-sense amplifier is the sum of the output voltage and the droop voltage. As Equation 4 shows, feeding this voltage into the compensation network causes the regulator to adjust the output voltage so that it's equal to the reference voltage minus the droop voltage.

The droop voltage, V_{DROOP}, is created by sensing the current through the output inductors. This is accomplished by using a continuous DCR current sensing method.

Inductor windings have a characteristic distributed resistance or DCR (Direct Current Resistance). For simplicity, the inductor DCR is considered as a separate lumped quantity, as shown in Figure 7. The channel current, I_L, flowing through the inductor, passes through the DCR. Equation 5 shows the s-domain equivalent voltage, V_L, across the inductor.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 5)}$$

The inductor DCR is important because the voltage dropped across it is proportional to the channel current. By using a simple R-C network and a current sense amplifier, as shown in Figure 7, the voltage drop across all of the inductors DCRs can be extracted. The output of the current sense amplifier, V_{DROOP}, can be shown to be proportional to the channel currents I_{L1}, I_{L2}, and I_{L3}, shown in Equation 6.

$$V_{DROOP}(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{(s \cdot R_{COMP} \cdot C_{COMP} + 1)} \cdot \frac{R_{COMP}}{R_S} \cdot (I_{L1} + I_{L2} + I_{L3}) \cdot DCR \quad \text{(EQ. 6)}$$

If the R-C network components are selected such that the R-C time constant matches the inductor L/DCR time constant, then V_{DROOP} is equal to the sum of the voltage drops across the individual DCRs, multiplied by a gain. As Equation 7 shows, V_{DROOP} is therefore proportional to the total output current, I_{OUT}.

$$V_{DROOP} = \frac{R_{COMP}}{R_S} \cdot I_{OUT} \cdot DCR \quad \text{(EQ. 7)}$$

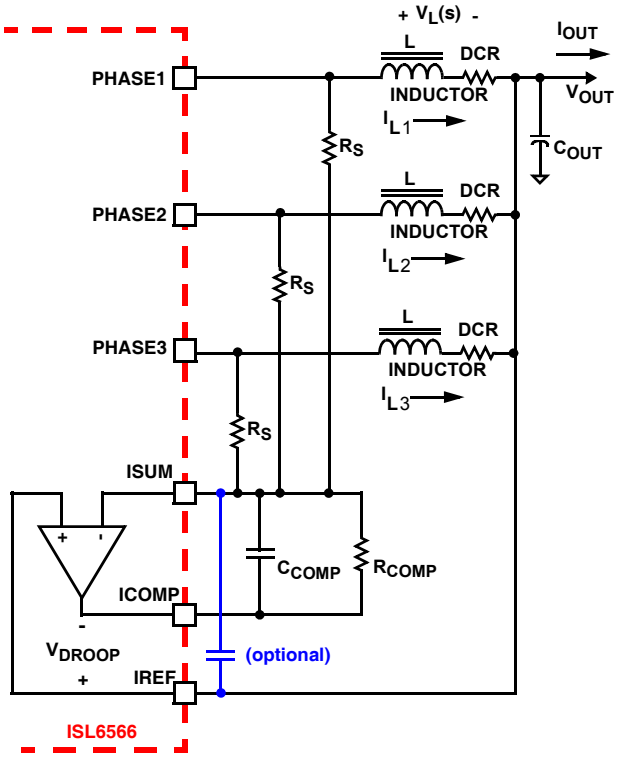


FIGURE 7. DCR SENSING CONFIGURATION

By simply adjusting the value of R_S, the load line can be set to any level, giving the converter the right amount of droop at all load currents. It may also be necessary to compensate for any changes in DCR due to temperature. These changes cause the load line to be skewed, and cause the R-C time constant to not match the L/DCR time constant. If this becomes a problem a simple negative temperature coefficient resistor network can be used in the place of R_{COMP} to compensate for the rise in DCR due to temperature.

Note: An optional 10nF ceramic capacitor from the ISUM pin to the IREF pin is recommended to help reduce any noise affects on the current sense amplifier due to layout.

Output-Voltage Offset Programming

The ISL6566 allows the designer to accurately adjust the offset voltage by connecting a resistor, R_{OFS}, from the OFS pin to VCC or GND. When R_{OFS} is connected between OFS and VCC, the voltage across it is regulated to 1.5V. This causes a proportional current (I_{OFS}) to flow into the OFS pin and out of the FB pin. If R_{OFS} is connected to ground, the voltage across it is regulated to 0.5V, and I_{OFS} flows into the FB pin and out of the OFS pin. The offset current flowing through the resistor between VDIFF and FB will generate the desired offset voltage which is equal to the product (I_{OFS} x R_{FB}). These functions are shown in Figures 8 and 9.

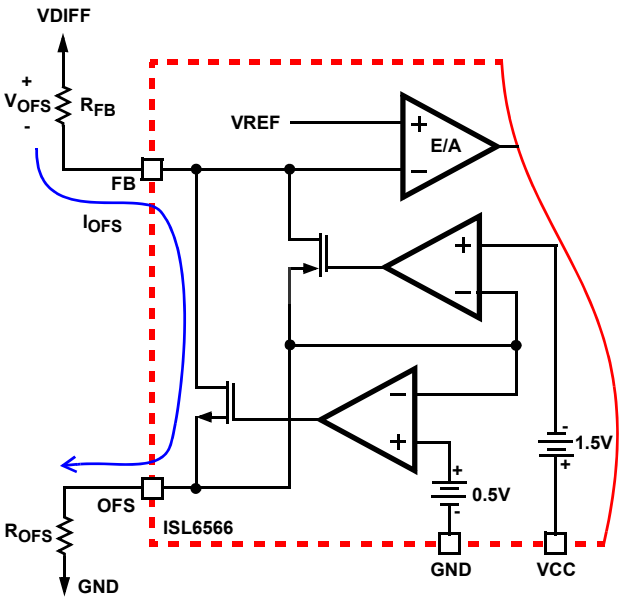


FIGURE 8. POSITIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

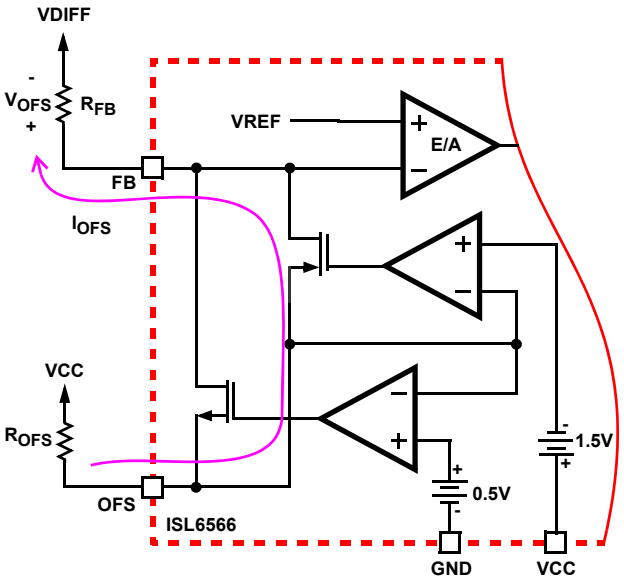


FIGURE 9. NEGATIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

Once the desired output offset voltage has been determined, use the following formulas to set R_{OFS}:

For Positive Offset (connect R_{OFS} to GND):

$$R_{OFS} = \frac{0.5 \times R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 8)}$$

For Negative Offset (connect R_{OFS} to VCC):

$$R_{OFS} = \frac{1.5 \times R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 9)}$$

Dynamic VID

Modern microprocessors need to make changes to their core voltage as part of normal operation. They direct the core-voltage regulator to do this by making changes to the VID inputs. The core-voltage regulator is required to monitor the DAC inputs and respond to on-the-fly VID changes in a controlled manner, supervising a safe output voltage transition without discontinuity or disruption.

The DAC mode the ISL6566 is operating in determines how the controller responds to a dynamic VID change. When in VRM10 mode the ISL6566 checks the VID inputs six times every switching cycle. If a new code is established and it stays the same for 3 consecutive readings, the ISL6566 recognizes the change and increments the reference. Specific to VRM10, the processor controls the VID transitions and is responsible for incrementing or decrementing one VID step at a time. In VRM10 setting, the ISL6566 will immediately change the reference to the new requested value as soon as the request is validated; in cases where the reference step is too large, the sudden change can trigger overcurrent or overvoltage events.

In order to ensure the smooth transition of output voltage during a VRM10 VID change, a VID step change smoothing network is required for an ISL6566 based voltage regulator. This network is composed of a 1kΩ internal resistor between the output of DAC and the capacitor C_{REF}, between the REF pin and ground. The selection of C_{REF} is based on the time duration for 1 bit VID change and the allowable delay time.

Assuming the microprocessor controls the VID change at 1 bit every T_{VID}, the relationship between C_{REF} and T_{VID} is given by Equation 10.

$$C_{REF} = 0.004 \times T_{VID} \quad \text{(EQ. 10)}$$

As an example, for a VID step change rate of 5µs per bit, the value of C_{REF} is 22nF based on Equation 10.

When running in VRM9 or AMD Hammer operation, the ISL6566 responds slightly different to a dynamic VID change than when in VRM10 mode. In these modes the VID code can be changed by more than a 1-bit step at a time. Once the controller receives the new VID code it waits half of a phase cycle and then begins slewing the DAC 12.5mV every phase cycle, until the VID and DAC are equal. Thus, the total time required for a VID change, t_{DVID}, is dependent on the switching frequency (f_S), the size of the change (ΔV_{VID}), and the time required to register the VID change. The one-cycle addition in the t_{DVID} equation is due to the possibility that the VID code change may occur up to one full switching cycle before being recognized. The approximate time required for a ISL6566-based converter in AMD Hammer configuration running at f_S = 335kHz to make a 1.1V to 1.5V reference voltage change is about 100µs, as calculated using the following equation.

$$t_{DVID} = \frac{1}{f_S}\left(\frac{\Delta V_{VID}}{0.0125} + 1.5\right) \quad \text{(EQ. 11)}$$

Advanced Adaptive Zero Shoot-Through Deadtime Control (Patent Pending)

The integrated drivers incorporate a unique adaptive deadtime control technique to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower MOSFET body-diode conduction, and to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

During turn-off of the lower MOSFET, the PHASE voltage is monitored until it reaches a -0.3V/+0.8V trip point for a forward/reverse current, at which time the UGATE is released to rise. An auto-zero comparator is used to correct the $r_{DS(ON)}$ drop in the phase voltage preventing false detection of the -0.3V phase level during $r_{DS(ON}$ conduction period. In the case of zero current, the UGATE is released after 35ns delay of the LGATE dropping below 0.5V. During the phase detection, the disturbance of LGATE falling transition on the PHASE node is blanked out to prevent falsely tripping. Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn on.

Internal Bootstrap Device

All three integrated drivers feature an internal bootstrap schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the PHASE node. This reduces voltage stress on the boot to phase pins.

The bootstrap capacitor must have a maximum voltage rating above PVCC + 5V and its capacitance value can be chosen from the following equation:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \quad \text{(EQ. 12)}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet PVCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

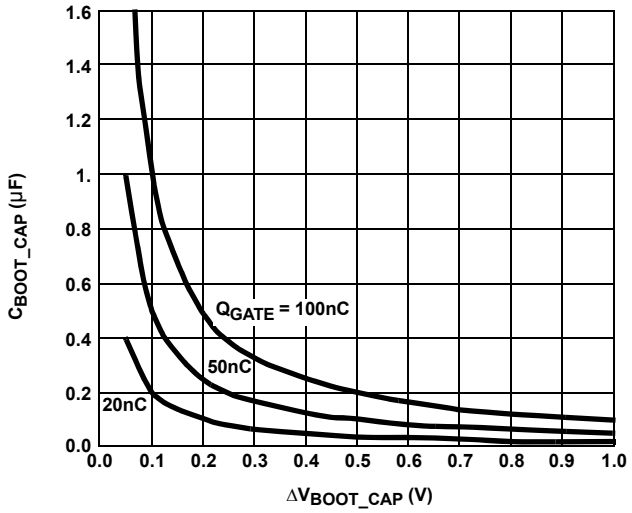


FIGURE 10. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Gate Drive Voltage Versatility

The ISL6566 provides the user flexibility in choosing the gate drive voltage for efficiency optimization. The controller ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

Initialization

Prior to initialization, proper conditions must exist on the ENLL, VCC, PVCC and the VID pins. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, the controller asserts PGOOD.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state. This forces the drivers to short gate-to-source of the upper and lower MOSFET's to assure the MOSFETs remain off. The following input conditions must be met before the ISL6566 is released from this shutdown mode.

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6566 is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6566 will not inadvertently turn off unless the bias voltage drops substantially (see *Electrical Specifications*).

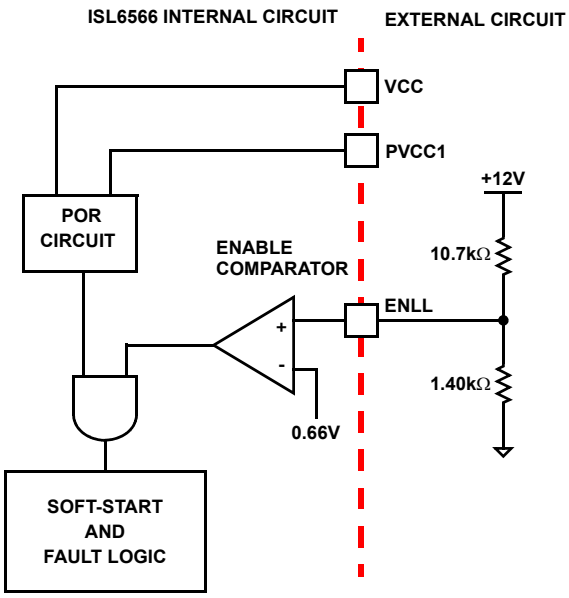


FIGURE 11. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (ENLL) FUNCTION

2. The voltage on ENLL must be above 0.66V. The ENLL input allows for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6566 in shutdown until the voltage at ENLL rises above 0.66V. The enable comparator has 60mV of hysteresis to prevent bounce.
3. The driver bias voltage applied at the PVCC pins must reach the internal power-on reset (POR) rising threshold. In order for the ISL6566 to begin operation, PVCC1 is the only pin that is required to have a voltage applied that exceeds POR. However, for 2 or 3-phase operation PVCC2 and PVCC3 must also exceed the POR threshold. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6566 will not inadvertently turn off unless the PVCC bias voltage drops substantially (see *Electrical Specifications*).
4. The VID code must not be 111111 or 111110 in VRM10 mode or 11111 in AMD Hammer or VRM9 modes. These codes signal the controller that no load is present. The controller will enter shut-down mode after receiving either of these codes and will execute soft-start upon receiving any other code. These codes can be used to enable or disable the controller but it is not recommended. After receiving one of these codes, the controller executes a 2-cycle delay before changing the overvoltage trip level to the shut-down level and disabling PWM. Overvoltage shutdown cannot be reset using one of these codes.

When each of these conditions is true, the controller immediately begins the soft-start sequence.

SOFT-START

The soft-start function allows the converter to bring up the output voltage in a controlled fashion, resulting in a linear ramp-up. Following a delay of 16 PHASE clock cycles between enabling the chip and the start of the ramp, the output voltage progresses at a fixed rate of 12.5mV per each 16 PHASE clock cycles.

Thus, the soft-start period (not including the 16 PHASE clock cycle delay) up to a given voltage, V_{DAC}, can be approximated by the following equation

$$T_{SS} = \frac{V_{DAC} \cdot 1280}{f_S} \quad \text{(EQ. 13)}$$

where V_{DAC} is the DAC-set VID voltage, and f_S is the switching frequency.

The ISL6566 also has the ability to start up into a pre-charged output, without causing any unnecessary disturbance. The FB pin is monitored during soft-start, and should it be higher than the equivalent internal ramping reference voltage, the output drives hold both MOSFETs off. Once the internal ramping reference exceeds the FB pin potential, the output drives are enabled, allowing the output to ramp from the pre-charged level to the final level dictated by the DAC setting. Should the output be pre-charged to a level exceeding the DAC setting, the output drives are enabled at the end of the soft-start period, leading to an abrupt correction in the output voltage down to the DAC-set level.

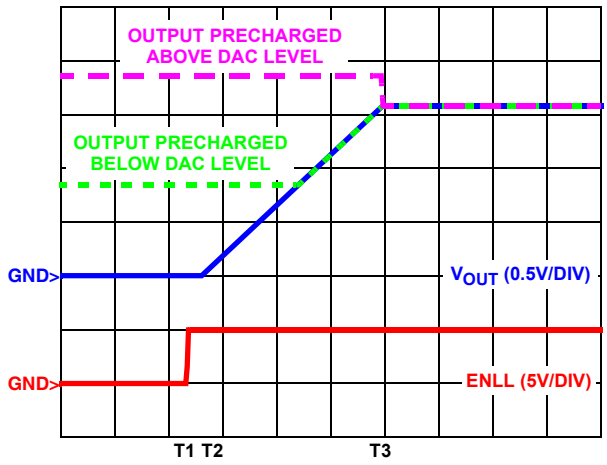


FIGURE 12. SOFT-START WAVEFORMS FOR ISL6566-BASED MULTI-PHASE CONVERTER

Fault Monitoring and Protection

The ISL6566 actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indicator is provided for linking to external system monitors. The schematic in Figure 13 outlines the interaction between the fault monitors and the power good signal.

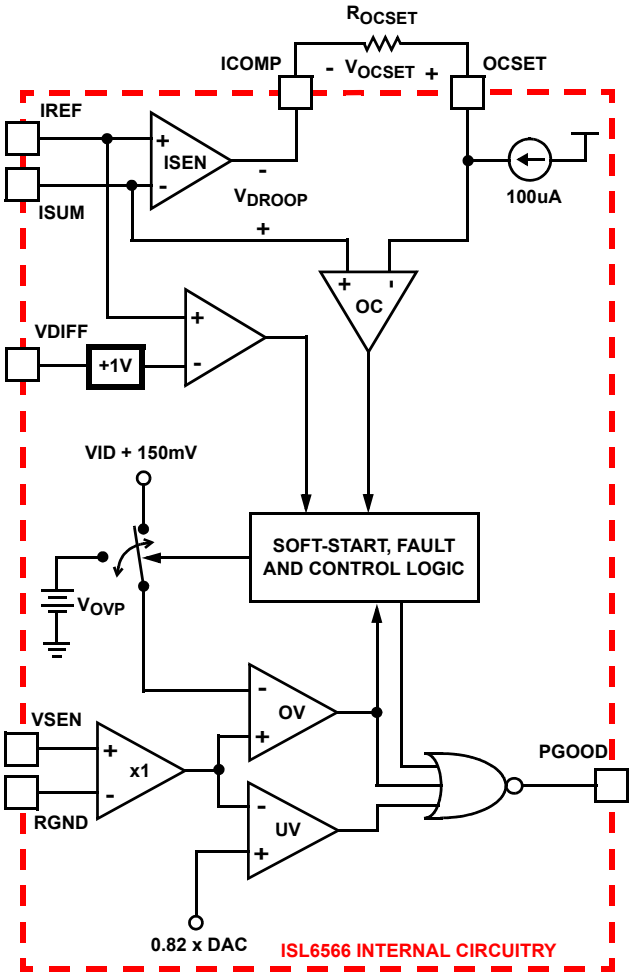


FIGURE 13. POWER GOOD AND PROTECTION CIRCUITRY

Power Good Signal

The power good pin (PGOOD) is an open-drain logic output that transitions high when the converter is operating after soft-start. PGOOD pulls low during shutdown and releases high after a successful soft-start. PGOOD transitions low when an undervoltage, overvoltage, or overcurrent condition is detected or when the controller is disabled by a reset from ENLL, POR, or one of the no-CPU VID codes. If after an undervoltage or overvoltage event occurs the output returns to within under and overvoltage limits, PGOOD will return high.

Undervoltage Detection

The undervoltage threshold is set at 82% of the VID code. When the output voltage (VSEN-RGND) is below the undervoltage threshold, PGOOD gets pulled low. No other action is taken by the controller. PGOOD will return high if the output voltage rises above 85% of the VID code.

Overvoltage Protection

The ISL6566 constantly monitors the difference between the VSEN and RGND voltages to detect if an overvoltage event occurs. During soft-start, while the DAC is ramping up, the overvoltage trip level is the higher of DAC plus 150mV or a fixed voltage, V_{OVP}. The fixed voltage, V_{OVP}, is 1.67V when running in AMD Hammer, or VRM10 modes, and 1.97V for VRM9 mode. Upon successful soft-start, the overvoltage trip level is only DAC plus 150mV. OVP releases 50mV below its trip point if it was “DAC plus 150mV” that tripped it, and releases 100mV below its trip point if it was the fixed voltage, V_{OVP}, that tripped it. Actions are taken by the ISL6566 to protect the microprocessor load when an overvoltage condition occurs, until the output voltage falls back within set limits.

At the inception of an overvoltage event, all LGATE signals are commanded high, and the PGOOD signal is driven low. This causes the controller to turn on the lower MOSFETs and pull the output voltage below a level that might cause damage to the load. The LGATE outputs remain high until VDIFF falls to within the overvoltage limits explained above. The ISL6566 will continue to protect the load in this fashion as long as the overvoltage condition recurs.

Once an overvoltage condition ends the ISL6566 continues normal operation and PGOOD returns high.

Pre-POR Overvoltage Protection

Prior to PVCC and VCC exceeding their POR levels, the ISL6566 is designed to protect the load from any overvoltage events that may occur. This is accomplished by means of an internal 10kΩ resistor tied from PHASE to LGATE, which turns on the lower MOSFET to control the output voltage until the overvoltage event ceases or the input power supply cuts off. For complete protection, the low side MOSFET should have a gate threshold well below the maximum voltage rating of the load/microprocessor.

In the event that during normal operation the PVCC or VCC voltage falls back below the POR threshold, the pre-POR overvoltage protection circuitry reactivates to protect from any more pre-POR overvoltage events.

Open Sense Line Protection

In the case that either of the remote sense lines, VSEN or GND, become open, the ISL6566 is designed to detect this and shut down the controller. This event is detected by monitoring the voltage on the IREF pin, which is a local version of V_{OUT} sensed at the outputs of the inductors.

If VSEN or RGND become opened, VDIFF falls, causing the duty cycle to increase and the output voltage on IREF to increase. If the voltage on IREF exceeds “VDIFF+1V”, the controller will shut down. Once the voltage on IREF falls below “VDIFF+1V”, the ISL6566 will restart at the beginning of soft-start.

Overcurrent Protection

The ISL6566 detects overcurrent events by comparing the droop voltage, V_{DROOP}, to the OCSET voltage, V_{OCSET}, as shown in Figure 13. The droop voltage, set by the external current sensing circuitry, is proportional to the output current as shown in Equation 7. A constant 100µA flows through R_{OCSET}, creating the OCSET voltage. When the droop voltage exceeds the OCSET voltage, the overcurrent protection circuitry activates. Since the droop voltage is proportional to the output current, the overcurrent trip level, I_{MAX}, can be set by selecting the proper value for R_{OCSET}, as shown in Equation 14.

$$R_{OCSET} = \frac{I_{MAX} \cdot R_{COMP} \cdot DCR}{100\mu \cdot R_S} \quad \text{(EQ. 14)}$$

Once the output current exceeds the overcurrent trip level, V_{DROOP} will exceed V_{OCSET}, and a comparator will trigger the converter to begin overcurrent protection procedures. At the beginning of overcurrent shutdown, the controller turns off both upper and lower MOSFETs. The system remains in this state for a period of 4096 switching cycles. If the controller is still enabled at the end of this wait period, it will attempt a soft-start (as shown in Figure 14). If the fault remains, the trip-retry cycles will continue indefinitely until either the controller is disabled or the fault is cleared. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard.

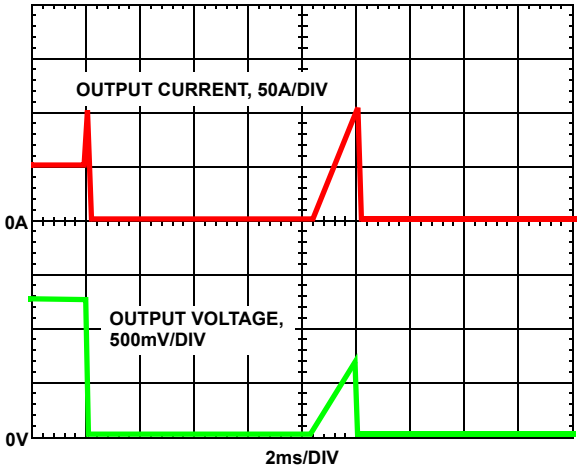


FIGURE 14. OVERCURRENT BEHAVIOR IN HICCUP MODE F_{SW} = 500kHz

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multi-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

Power Stages

The first step in designing a multi-phase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board, whether through-hole components are permitted, the total board space available for power-supply circuitry, and the maximum amount of load current. Generally speaking, the most economical solutions are those in which each phase handles between 25 and 30A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

MOSFETS

The choice of MOSFETs depends on the current each MOSFET will be required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for power loss in the lower MOSFET is simple, since virtually all of the loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 15, I_M is the maximum continuous output current, I_{PP} is the peak-to-peak inductor current (see Equation 1), and d is the duty cycle (V_{OUT}/V_{IN}).

$$P_{LOW,1} = r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 (1-d) + \frac{I_{L,PP}^2(1-d)}{12}\right] \quad \text{(EQ. 15)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$, the switching frequency, f_S, and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)} f_S \left[\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right) t_{d1} + \left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right) t_{d2}\right] \quad \text{(EQ. 16)}$$

The total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$ and $P_{LOW,2}$.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times, the lower-MOSFET body-diode reverse-recovery charge, Q_{rr}, and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 17, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN}\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right)\left(\frac{t_1}{2}\right)f_S \quad \text{(EQ. 17)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 18, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN}\left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right)\left(\frac{t_2}{2}\right)f_S \quad \text{(EQ. 18)}$$

A third component involves the lower MOSFET reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET body diode can recover all of Q_{rr}, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is $P_{UP,3}$.

$$P_{UP,3} = V_{IN}Q_{rr}f_S \quad \text{(EQ. 19)}$$

Finally, the resistive part of the upper MOSFET is given in Equation 20 as $P_{UP,4}$.

$$P_{UP,4} \approx r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 d + \frac{I_{PP}^2}{12}\right] \quad \text{(EQ. 20)}$$

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 17, 18, 19 and 20. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

Package Power Dissipation

When choosing MOSFETs it is important to consider the amount of power being dissipated in the integrated drivers located in the controller. Since there are a total of three drivers in the controller package, the total power dissipated by all three drivers must be less than the maximum allowable power dissipation for the QFN package.

Calculating the power dissipation in the drivers for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the 6x6 QFN package is approximately 4W at room temperature. See *Layout Considerations* paragraph for thermal transfer improvement suggestions.

When designing the ISL6566 into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses, P_{Qg_TOT}, due to the gate charge of MOSFETs and the integrated driver's internal circuitry and their corresponding average driver current can be estimated with Equations 21 and 22, respectively.

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \bullet VCC \quad \text{(EQ. 21)}$$

$$P_{Qg\_Q1} = \frac{3}{2} \bullet Q_{G1} \bullet PVCC \bullet F_{SW} \bullet N_{Q1} \bullet N_{PHASE}$$

$$P_{Qg\_Q2} = Q_{G2} \bullet PVCC \bullet F_{SW} \bullet N_{Q2} \bullet N_{PHASE}$$

$$I_{DR} = \left(\frac{3}{2} \bullet Q_{G1} \bullet N_{Q1} + Q_{G2} \bullet N_{Q2}\right) \bullet N_{PHASE} \bullet F_{SW} + I_Q \quad \text{(EQ. 22)}$$

In Equations 21 and 22, P_{Qg_Q1} is the total upper gate drive power loss and P_{Qg_Q2} is the total lower gate drive power loss; the gate charge (Q_{G1} and Q_{G2}) is defined at the particular gate to source drive voltage PVCC in the corresponding MOSFET data sheet; I_Q is the driver total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are the number of upper and lower MOSFETs per phase, respectively; N_{PHASE} is the number of active phases. The I_Q*VCC product is the quiescent power of the controller without capacitive load and is typically 75mW at 300kHz.

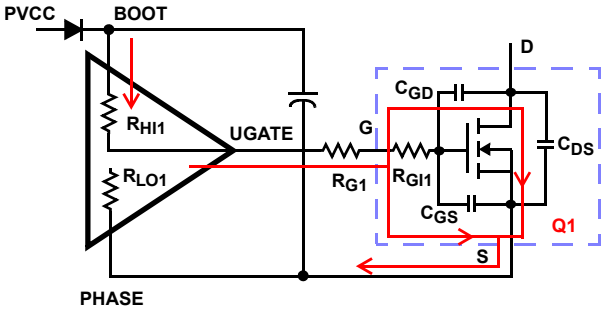


FIGURE 15. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

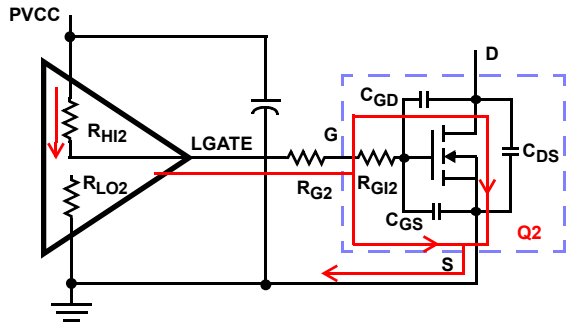


FIGURE 16. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

The total gate drive power losses are dissipated among the resistive components along the transition path and in the bootstrap diode. The portion of the total power dissipated in the controller itself is the power dissipated in the upper drive path resistance, P_{DR_UP}, the lower drive path resistance, P_{DR_UP}, and in the boot strap diode, P_{BOOT}. The rest of the power will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of the MOSFETs. Figures 15 and 16 show the typical upper and lower gate drives turn-on transition path. The total power dissipation in the controller itself, P_{DR}, can be roughly estimated as:

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + P_{BOOT} + (I_Q \bullet VCC) \quad \text{(EQ. 23)}$$

$$P_{BOOT} = \frac{P_{Qg\_Q1}}{3}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg\_Q1}}{3}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

Current Balancing Component Selection

The ISL6566 senses the channel load current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$, as shown in Figure 17. The ISEN pins are denoted ISEN1, ISEN2, and ISEN3. The resistors connected between these pins and the respective phase nodes determine the gains in the channel-current balance loop.

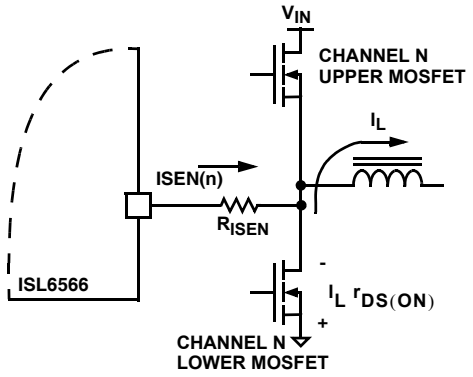


FIGURE 17. ISL6566 INTERNAL AND EXTERNAL CURRENT-SENSING CIRCUITRY

Select values for these resistors based on the room temperature $r_{DS(ON)}$ of the lower MOSFETs; the full-load operating current, I_{FL}; and the number of phases, N using Equation 24.

$$R_{ISEN} = \frac{r_{DS(ON)}}{50 \times 10^{-6}} \frac{I_{FL}}{N} \quad \text{(EQ. 24)}$$

In certain circumstances, it may be necessary to adjust the value of one or more ISEN resistors. When the components of one or more channels are inhibited from effectively dissipating their heat so that the affected channels run hotter than desired, choose new, smaller values of R_{ISEN} for the affected phases (see the section entitled *Channel-Current Balance*). Choose $R_{ISEN,2}$ in proportion to the desired decrease in temperature rise in order to cause proportionally less current to flow in the hotter phase.

$$R_{ISEN,2} = R_{ISEN} \frac{\Delta T_2}{\Delta T_1} \quad \text{(EQ. 25)}$$

In Equation 25, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. While a single adjustment according to Equation 25 is usually sufficient, it may occasionally be necessary to adjust R_{ISEN} two or more times to achieve optimal thermal balance between all channels.

Load Line Regulation Component Selection (DCR Current Sensing)

For accurate load line regulation, the ISL6566 senses the total output current by detecting the voltage across the output inductor DCR of each channel (As described in the *Load Line Regulation* section). As Figure 18 illustrates, an R-C network is required to accurately sense the inductor DCR voltage and convert this information into a “droop” voltage, which is proportional to the total output current.

Choosing the components for this current sense network is a two step process. First, R_{COMP} and C_{COMP} must be chosen so that the time constant of this R_{COMP}-C_{COMP} network matches the time constant of the inductor L/DCR.

Then the resistor R_S must be chosen to set the current sense network gain, obtaining the desired full load droop voltage. Follow the steps below to choose the component values for this R-C network.

1. Choose an arbitrary value for C_{COMP}. The recommended value is 0.01µF.
2. Plug the inductor L and DCR component values, and the values for C_{COMP} chosen in steps 1, into Equation 26 to calculate the value for R_{COMP}.

$$R_{COMP} = \frac{L}{DCR \cdot C_{COMP}} \quad \text{(EQ. 26)}$$

3. Use the new value for R_{COMP} obtained from Equation 26, as well as the desired full load current, I_{FL}, full load droop voltage, V_{DROOP}, and inductor DCR in Equation 27 to calculate the value for R_S.

$$R_S = \frac{I_{FL}}{V_{DROOP}} \cdot R_{COMP} \cdot DCR \quad \text{(EQ. 27)}$$

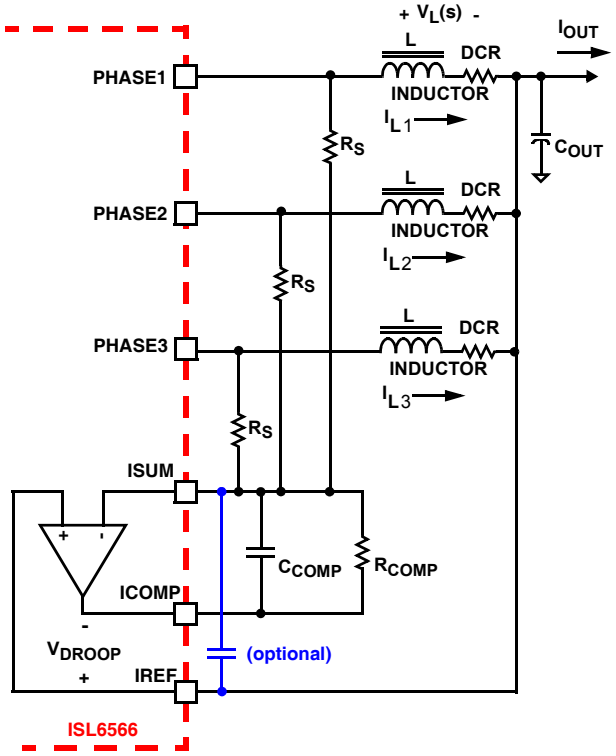


FIGURE 18. DCR SENSING CONFIGURATION

Due to errors in the inductance or DCR it may be necessary to adjust the value of R_{COMP} to match the time constants correctly. The effects of time constant mismatch can be seen in the form of droop overshoot or undershoot during the initial load transient spike, as shown in Figure 19. Follow the steps below to ensure the R-C and inductor L/DCR time constants are matched accurately.

1. Capture a transient event with the oscilloscope set to about L/DCR/2 (sec/div). For example, with L = 1µH and DCR = 1mΩ, set the oscilloscope to 500µs/div.
2. Record ΔV1 and ΔV2 as shown in Figure 19.
3. Select a new value, $R_{COMP,2}$, for the time constant resistor based on the original value, $R_{COMP,1}$, using the following equation.

$$R_{COMP,2} = R_{COMP,1} \cdot \frac{\Delta V_1}{\Delta V_2} \quad \text{(EQ. 28)}$$

4. Replace R_{COMP} with the new value and check to see that the error is corrected. Repeat the procedure if necessary.

After choosing a new value for R_{COMP}, it will most likely be necessary to adjust the value of R_S to obtain the desired full load droop voltage. Use Equation 27 to obtain the new value for R_S.

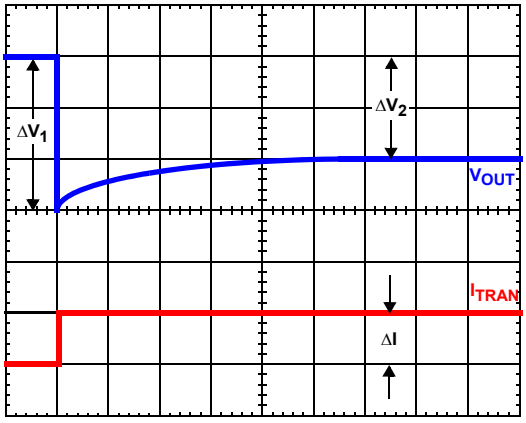


FIGURE 19. TIME CONSTANT MISMATCH BEHAVIOR

Compensation

The two opposing goals of compensating the voltage regulator are stability and speed.

The load-line regulated converter behaves in a similar manner to a peak current mode controller because the two poles at the output filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C.

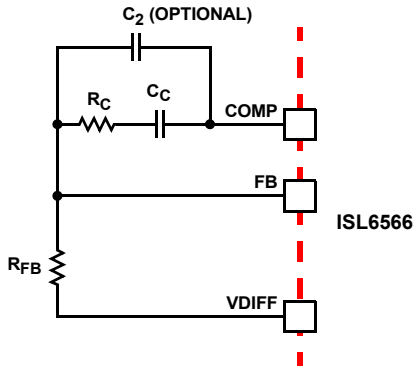


FIGURE 20. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL6566 CIRCUIT

Since the system poles and zero are affected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated.

Fortunately, there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator, by compensating the L-C poles and the ESR zero of the voltage mode approximation, yields a solution that is always stable with very close to ideal transient performance.

Select a target bandwidth for the compensated system, f_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of f_0 to the L-C pole frequency and the ESR zero frequency. For each of the following three, there is a separate set of equations for the compensation components.

Case 1: $\frac{1}{2\pi\sqrt{LC}} > f_0$

$$R_C = R_{FB}\frac{2\pi f_0 V_{pp}\sqrt{LC}}{0.66V_{IN}}$$

$$C_C = \frac{0.66V_{IN}}{2\pi V_{PP}R_{FB}f_0}$$

Case 2: $\frac{1}{2\pi\sqrt{LC}} \le f_0 < \frac{1}{2\pi C(ESR)}$

$$R_C = R_{FB}\frac{V_{PP}(2\pi)^2 f_0^2 LC}{0.66\,V_{IN}} \qquad \text{(EQ. 29)}$$

$$C_C = \frac{0.66V_{IN}}{(2\pi)^2 f_0^2 V_{PP}R_{FB}\sqrt{LC}}$$

Case 3: $f_0 > \frac{1}{2\pi C(ESR)}$

$$R_C = R_{FB}\frac{2\pi f_0 V_{pp}L}{0.66\,V_{IN}(ESR)}$$

$$C_C = \frac{0.66V_{IN}(ESR)\sqrt{C}}{2\pi V_{PP}R_{FB}f_0\sqrt{L}}$$

In Equations 29, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent series resistance of the bulk output filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in the *Electrical Specifications*.

Once selected, the compensation values in Equations 29 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_C. Slowly increase the value of R_C while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_C will not need adjustment. Keep the value of C_C from Equations 29 unless some performance issue is noted.

The optional capacitor C_2, is sometimes needed to bypass noise away from the PWM comparator (see Figure 20). Keep a position available for C_2, and be prepared to install a high-frequency capacitor of between 22pF and 150pF in case any leading edge jitter problem is noted.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter limits the system transient response. The output capacitors must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI, the load-current slew rate, di/dt, and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \qquad \text{(EQ. 30)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor ac ripple current (see *Interleaving* and Equation 2), a voltage develops across the bulk capacitor ESR equal to $I_{C,PP}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance.

$$L \ge (ESR)\frac{\left(V_{IN} - NV_{OUT}\right)V_{OUT}}{f_S V_{IN} V_{PP(MAX)}} \qquad \text{(EQ. 31)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 32 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 33 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2 \cdot N \cdot C \cdot V_O}{(\Delta I)^2}\left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \quad \text{(EQ. 32)}$$

$$L \leq \frac{(1.25) \cdot N \cdot C}{(\Delta I)^2}\left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right]\left(V_{IN} - V_O\right) \quad \text{(EQ. 33)}$$

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper MOSFET loss calculation. These effects are outlined in *MOSFETs*, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in *Output Filter Design*. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Switching frequency is determined by the selection of the frequency-setting resistor, R_T. Figure 21 and Equation 34 are provided to assist in selecting the correct value for R_T.

$$R_T = 10^{[10.61 - 1.035\log(f_S)]} \quad \text{(EQ. 34)}$$

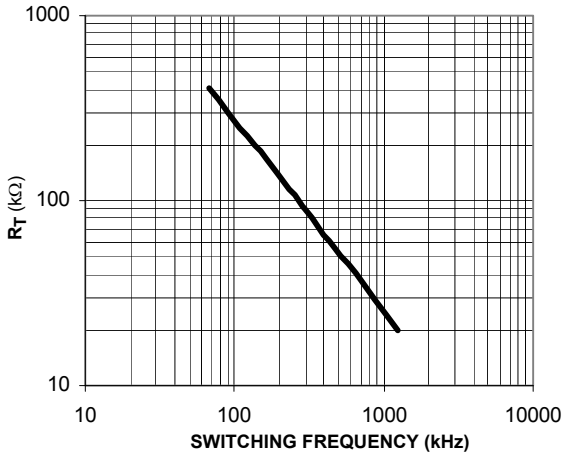


FIGURE 21. R_T vs SWITCHING FREQUENCY

Input Capacitor Selection

The input capacitors are responsible for sourcing the ac component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the ac component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

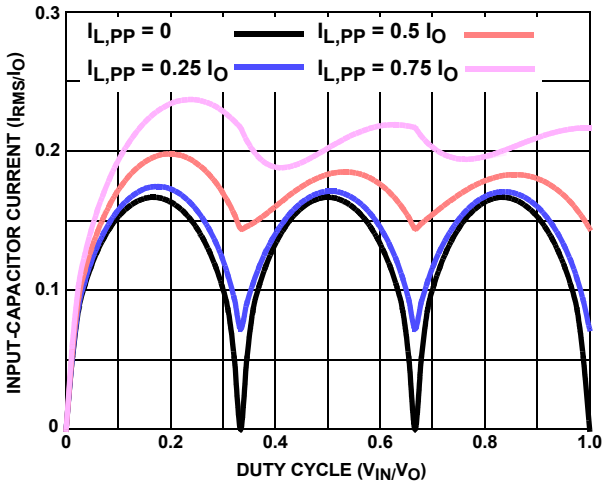


FIGURE 22. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

For a three-phase design, use Figure 22 to determine the input-capacitor RMS current requirement set by the duty cycle, maximum sustained output current (I_O), and the ratio of the peak-to-peak inductor current ($I_{L,PP}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage. Figures 23 and 24 provide the same input RMS current information for two-phase and single-phase designs respectively. Use the same approach for selecting the bulk capacitor type and number.

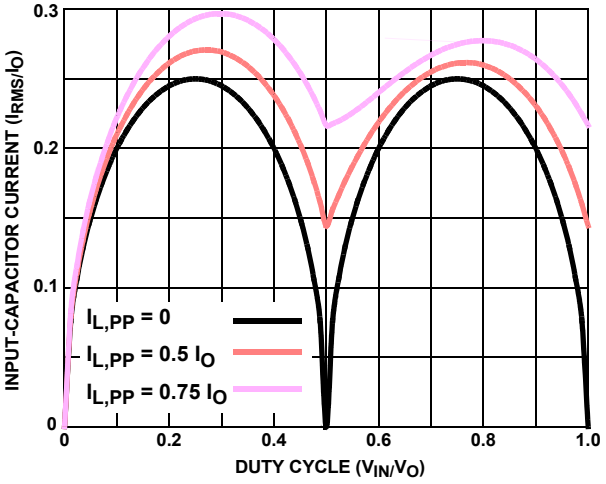


FIGURE 23. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 2-PHASE CONVERTER

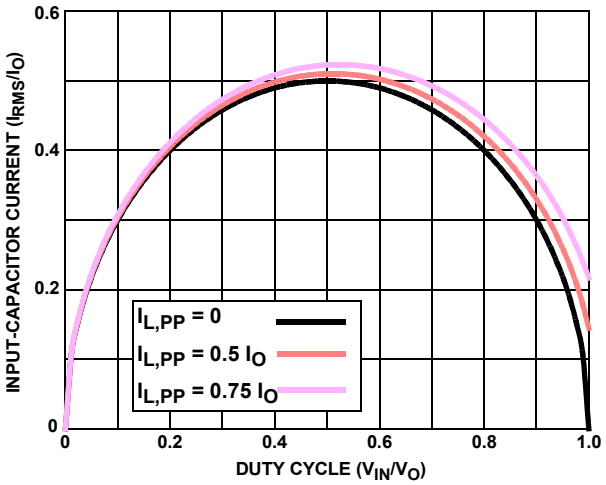


FIGURE 24. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR SINGLE-PHASE CONVERTER

Low capacitance, high-frequency ceramic capacitors are needed in addition to the input bulk capacitors to suppress leading and falling edge voltage spikes. The spikes result from the high current slew rate produced by the upper MOSFET turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitics and maximize suppression.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component selection, layout, and placement minimizes these voltage spikes. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET was carrying channel current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using a ISL6566 controller. The power components are the most critical because they switch large amounts of energy. Next are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first, which include the MOSFETs, input and output capacitors, and the inductors. It is important to have a symmetrical layout for each power train, preferably with the controller located equidistant from each. Symmetrical layout allows heat to be dissipated equally across all three power trains. Equidistant placement of the controller to the three power trains also helps keep the gate drive traces equally short, resulting in equal trace impedances and similar drive capability of all sets of MOSFETs.

When placing the MOSFETs try to keep the source of the upper FETs and the drain of the lower FETs as close as thermally possible. Input Bulk capacitors should be placed close to the drain of the upper FETs and the source of the lower FETs. Locate the output inductors and output capacitors between the MOSFETs and the load. The high-frequency input and output decoupling capacitors (ceramic) should be placed as close as practicable to the decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND next or on the capacitor solder pad.

The critical small components include the bypass capacitors for VCC and PVCC, and many of the components surrounding the controller including the feedback network and current sense components. Locate the VCC/PVCC bypass capacitors as close to the ISL6566 as possible. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up. It is also important to place the current sense components close to their respective pins on the ISL6566, including R_{ISEN}, R_S, R_{COMP}, and C_{COMP}.

A multi-layer printed circuit board is recommended. Figure 25 shows the connections of the critical components for the converter. Note that capacitors C_{xxIN} and C_{xxOUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually the one underneath the component side of the board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to output inductors short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring.

Routing UGATE, LGATE, and PHASE traces

Great attention should be paid to routing the UGATE, LGATE, and PHASE traces since they drive the power train MOSFETs using short, high current pulses. It is important to size them as large and as short as possible to reduce their overall impedance and inductance. They should be sized to carry at least one ampere of current (0.02” to 0.05”). Going between layers with vias should also be avoided, but if so, use two vias for interconnection when possible.

Extra care should be given to the LGATE traces in particular since keeping their impedance and inductance low helps to significantly reduce the possibility of shoot-through. It is also important to route each channels UGATE and PHASE traces in as close proximity as possible to reduce their inductances.

Thermal Management

For maximum thermal performance in high current, high switching frequency applications, connecting the thermal GND pad of the ISL6566 to the ground plane with multiple vias is recommended. This heat spreading allows the part to achieve its full thermal potential. It is also recommended that the controller be placed in a direct path of airflow if possible to help thermally manage the part.

Suppressing MOSFET Gate Leakage

With VCC at ground potential, UGATE is high impedance. In this state, any stray leakage has the potential to deliver charge to the gate of the upper MOSFET. If UGATE receives sufficient charge to bias the device on, a low impedance path will be connected between the upper MOSFET drain and PHASE. If this occurs and the input power supply is present and active, the system could see potentially damaging current. Worst-case leakage currents are on the order of pico-amps; therefore, a 10kΩ resistor, connected from UGATE to PHASE, is more than sufficient to bleed off any stray leakage current. This resistor will not affect the normal performance of the driver or reduce its efficiency.

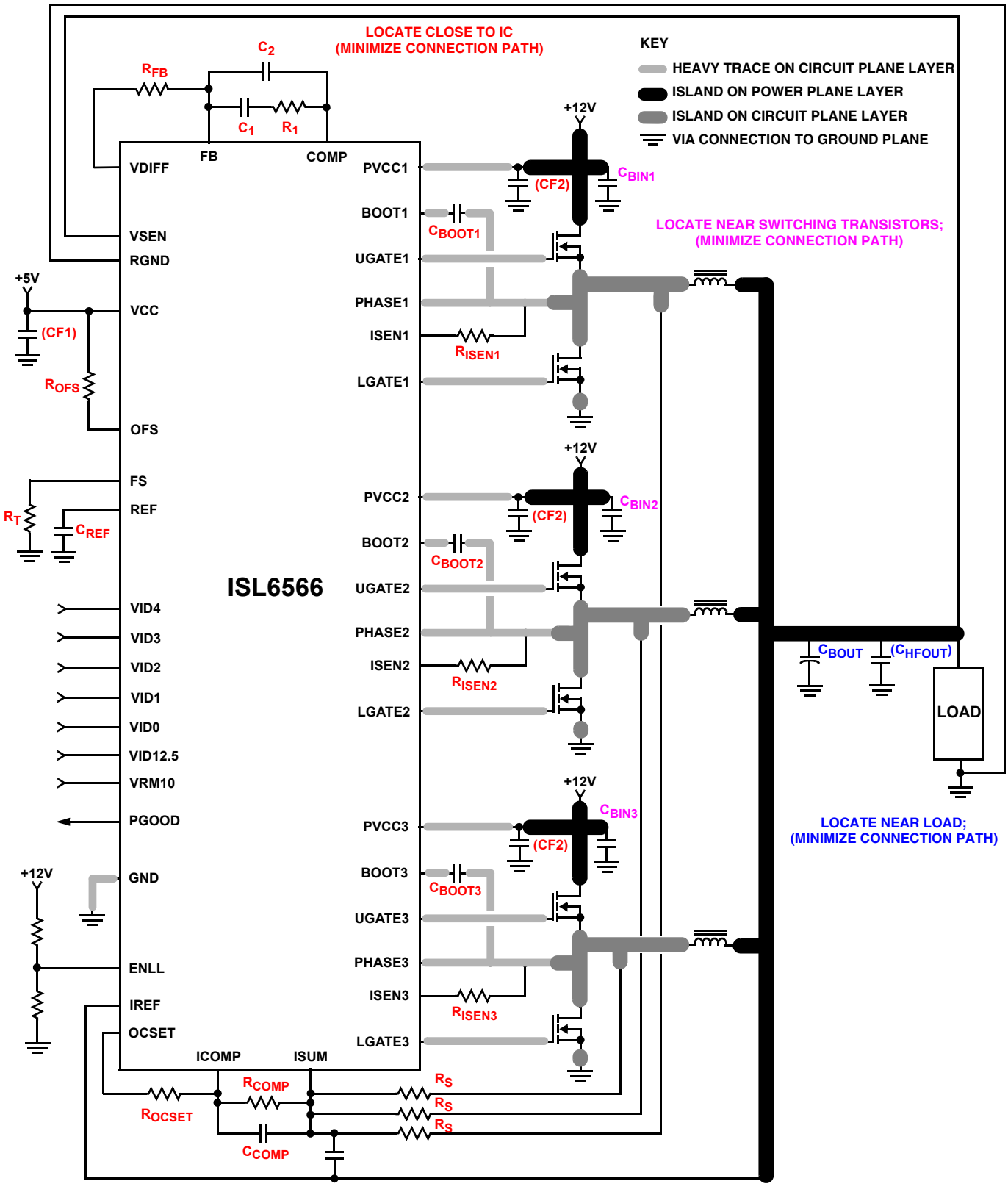
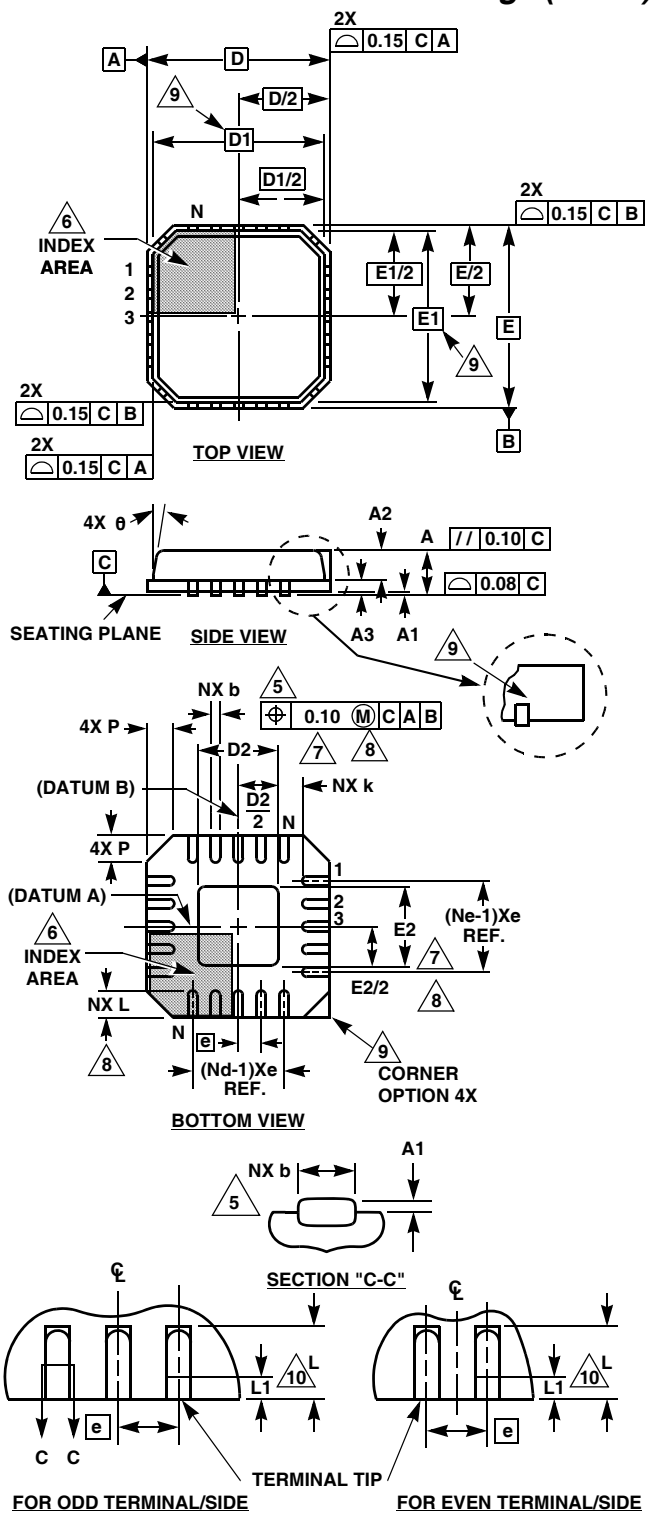


FIGURE 25. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L40.6x6

40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VJJD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		6.00 BSC		-
D1		5.75 BSC		9
D2	3.95	4.10	4.25	7, 8
E		6.00 BSC		-
E1		5.75 BSC		9
E2	3.95	4.10	4.25	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		40		2
Nd		10		3
Ne		10		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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