THE DATASHEET OF

ISL97519IUZ

DATASHEET

ISL97519

1% Output Accuracy 600kHz/1.2MHz PWM Step-Up Regulator

FN6454
Rev 4.00
February 16, 2012

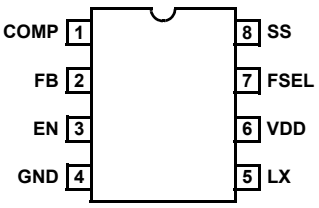
The ISL97519 is a high frequency, high efficiency step-up voltage regulator operated at constant frequency PWM mode. With an internal 2.0A, 200mΩ MOSFET, it can deliver up to 1A output current at over 90% efficiency. The selectable 600kHz and 1.2MHz allows smaller inductors and faster transient response. An external compensation pin gives the user greater flexibility in setting frequency compensation allowing the use of low ESR ceramic output capacitors.

When shut down, it draws <1µA of current and can operate down to 2.3V input supply. These features, along with 1.2MHz switching frequency, make it an ideal device for portable equipment and TFT-LCD displays.

The ISL97519 is available in an 8 Ld MSOP package with a maximum height of 1.1mm. The device is specified for operation over the full -40°C to +105°C temperature range.

Pin Configuration

ISL97519
(8 LD MSOP)
TOP VIEW



Features

- 1% Output Accuracy
- >90% Efficiency
- 2.0A, 200mΩ Power MOSFET
- 2.3V to 5.5V Input
- 1.1*VIN to 25V Output
- 600kHz/1.2MHz Switching Frequency Selection
- Adjustable Soft-Start
- Internal Thermal Protection
- 1.1mm Max Height 8 Ld MSOP Package
- Pb-Free (RoHS compliant)
- Halogen Free

Applications

- TFT-LCD displays
- DSL modems
- PCMCIA cards
- Digital cameras
- GSM/CDMA phones
- Portable equipment
- Handheld devices

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL97519IUZ	7519Z	8 Ld MSOP	M8.118A
ISL97519IUZ-T	7519Z	8 Ld MSOP	M8.118A
ISL97519IUZ-TK	7519Z	8 Ld MSOP	M8.118A

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL97519. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (T_A = +25°C)

LX to GND 27V
V_{DD} to GND 6.5V
COMP, FB, EN, SS, FSEL to GND . . . . . -0.3V to (V_{DD} + 0.3V)

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
8 Lead MSOP	160

Storage Temperature . . . . . -65°C to +150°C
Operating Ambient Temperature . . . . . -40°C to +105°C
Operating Junction Temperature . . . . . +135°C
Power Dissipation . . . . . See Curves
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

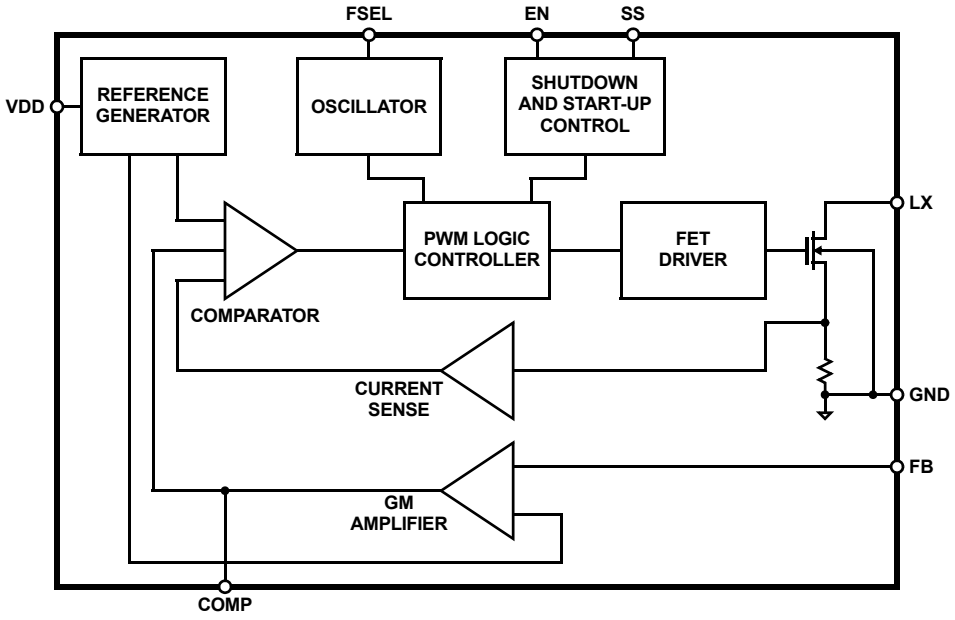
V_{IN} = 3.3V, V_{OUT} = 12V, I_{OUT} = 0mA, FSEL = GND, T_A = -40°C to +105°C Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
I_{Q1}	Quiescent Current - Shutdown	EN = 0V		1	**5**	µA
I_{Q2}	Quiescent Current - Not Switching	EN = V_{DD}, FB = 1.3V		0.7		mA
I_{Q3}	Quiescent Current - Switching	EN = V_{DD}, FB = 1.0V		3	**4**	mA
V_{FB}	Feedback Voltage	T_A = -40°C to +85°C	1.281	1.294	1.307	V
		T_A = -40°C to +105°C	**1.276**	1.294	**1.307**	V
I_{B-FB}	Feedback Input Bias Current			0.01	**0.5**	µA
V_{DD}	Input Voltage Range		**2.3**		**5.5**	V
D_{MAX} - 600kHz	Maximum Duty Cycle	FSEL = 0V	**85**	92		%
D_{MAX} - 1.2MHz	Maximum Duty Cycle	FSEL = V_{DD}	**85**	90		%
I_{LIM}	Current Limit - Max Peak Input Current		**1.5**	2.0		A
I_{EN}	Shutdown Input Bias Current	EN = 0V		0.01	**0.5**	µA
$r_{DS(ON)}$	Switch ON-Resistance	V_{DD} = 2.7V, I_{LX} = 1A		0.2		Ω
$I_{LX-LEAK}$	Switch Leakage Current	VSW = 27V		0.01	**3**	µA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	3V < V_{IN} < 5.5V, V_{OUT} = 12V		0.2		%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	V_{IN} = 3.3V, V_{OUT} = 12V, I_O = 30mA to 200mA		0.3		%
f_{OSC1}	Switching Frequency Accuracy	FSEL = 0V	**500**	620	**740**	kHz
f_{OSC2}	Switching Frequency Accuracy	FSEL = V_{DD}	**1000**	1250	**1500**	kHz
V_{IL}	EN, FSEL Input Low Level				**0.5**	V
V_{IH}	EN, FSEL Input High Level		**1.5**			V
G_M	Error Amp Tranconductance	ΔI = 5µA	**70**	130	**150**	1µ/Ω
V_{DD-ON}	V_{DD} UVLO On Threshold		**2.1**	2.2	**2.3**	V
HYS	V_{DD} UVLO Hysteresis			100		mV
I_{SS}	Soft-Start Charge Current		**4**	6	**8**	µA
OTP	Over-Temperature Protection			150		°C

NOTE:

5. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

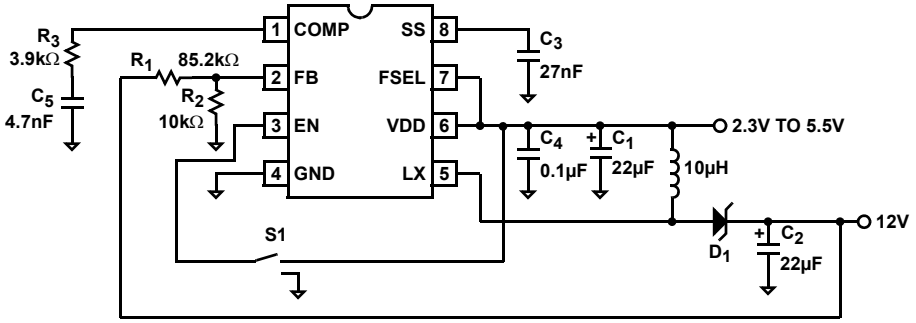
Block Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	COMP	Compensation pin. Output of the internal error amplifier. Capacitor and resistor from COMP pin to ground.
2	FB	Voltage feedback pin. Internal reference is 1.294V nominal. Connect a resistor divider from V_{OUT}. $V_{OUT} = 1.294V (1 + R_1/R_2)$. See “Typical Application Circuit”.
3	EN	Shut-down control pin. Pull EN low to turn off the device.
4	GND	Analog and power ground.
5	LX	Power switch pin. Connected to the drain of the internal power MOSFET.
6	VDD	Analog power supply input pin.
7	FSEL	Frequency select pin. When FSEL is set low, switching frequency is set to 620kHz. When connected to high or V_{DD}, switching frequency is set to 1.25MHz.
8	SS	Soft-start control pin. Connect a capacitor to control the converter start-up.

Typical Application Circuit



Typical Performance Curves

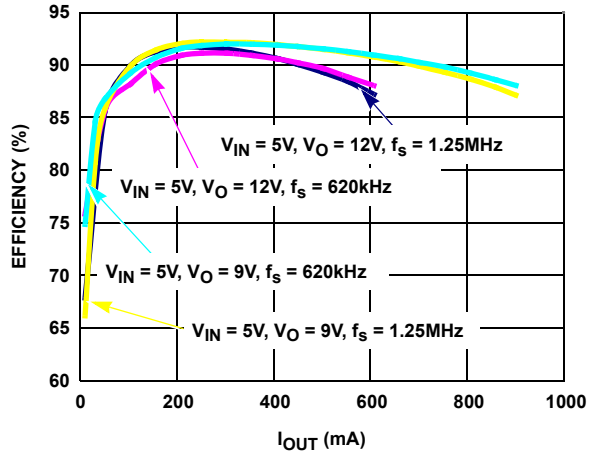


FIGURE 1. BOOST EFFICIENCY vs I_{OUT}

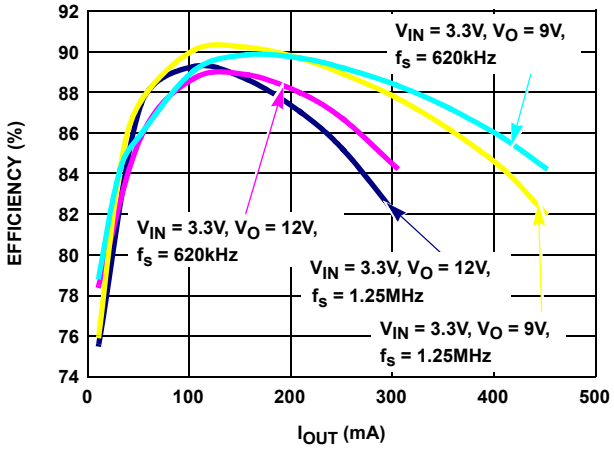


FIGURE 2. BOOST EFFICIENCY vs I_{OUT}

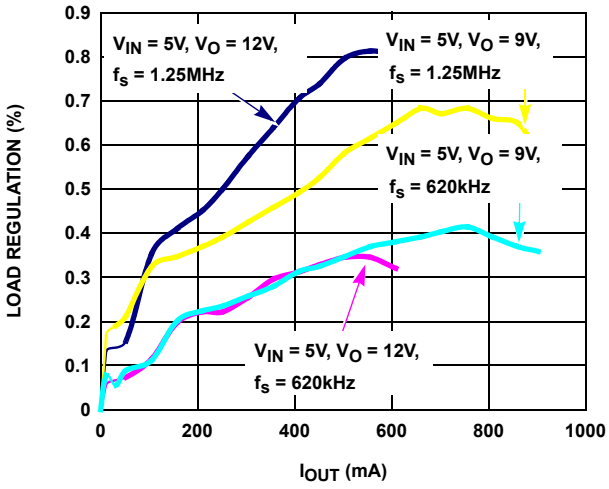


FIGURE 3. LOAD REGULATION vs I_{OUT}

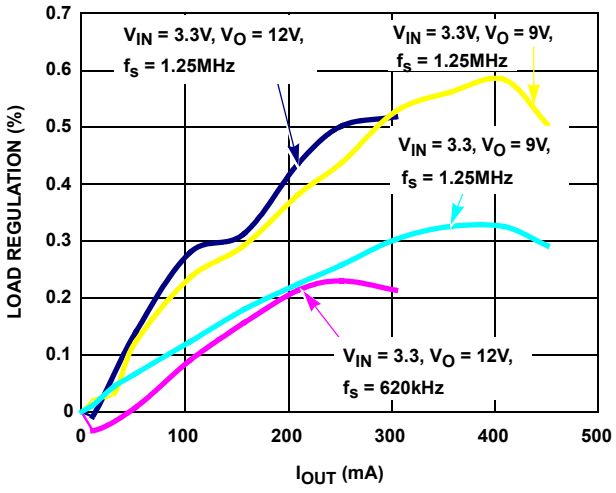


FIGURE 4. LOAD REGULATION vs I_{OUT}

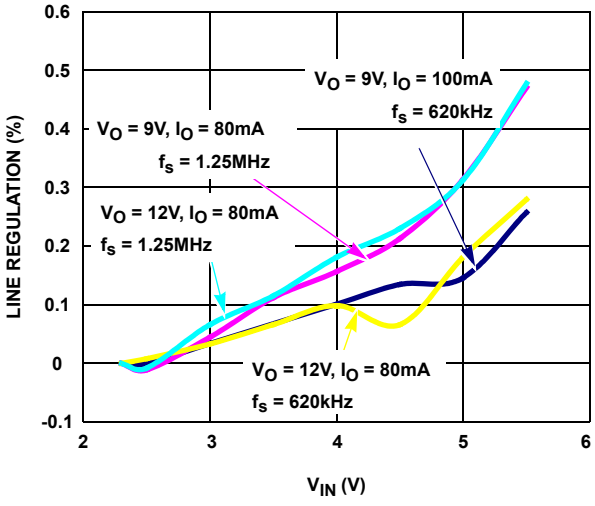


FIGURE 5. LINE REGULATION vs V_{IN}

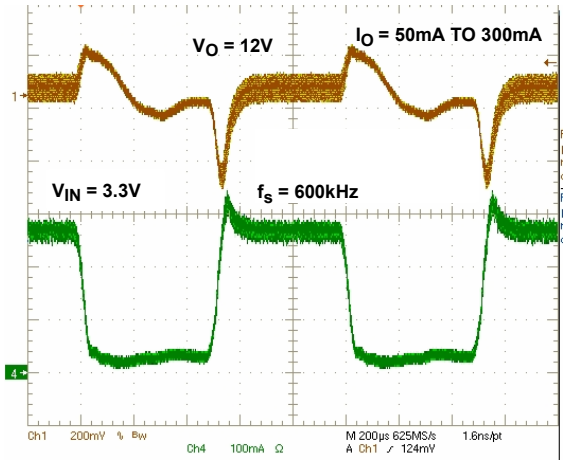


FIGURE 6. TRANSIENT RESPONSE

Typical Performance Curves (Continued)

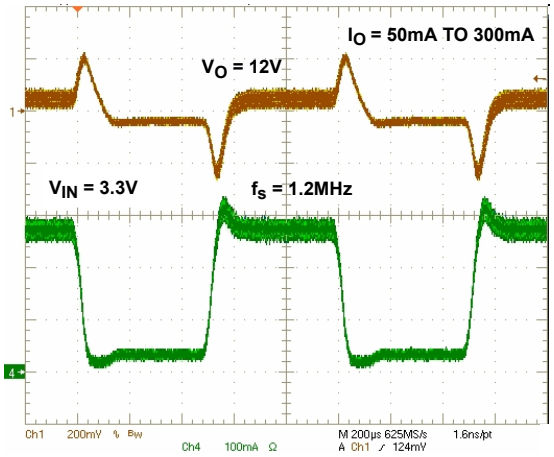


FIGURE 7. TRANSIENT RESPONSE

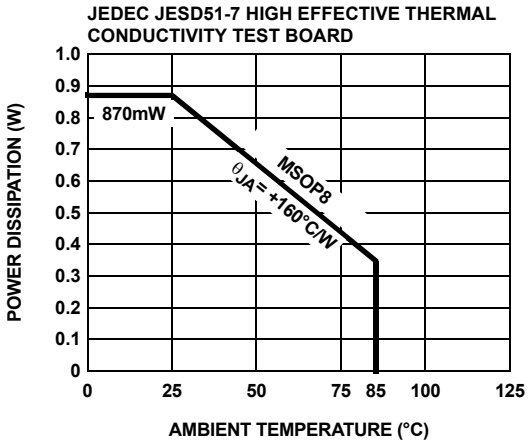


FIGURE 8. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

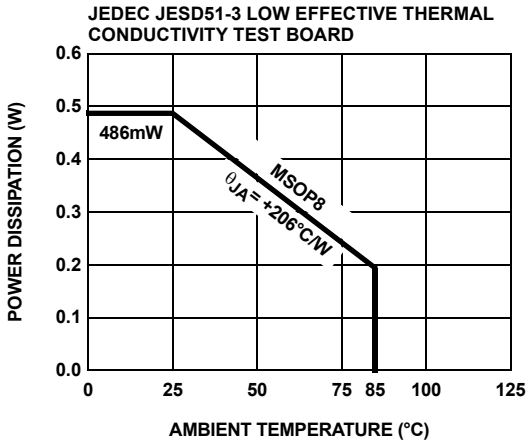


FIGURE 9. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

The ISL97519 is a high frequency, high efficiency boost regulator operated at constant frequency PWM mode. The boost converter stores energy from an input voltage source and delivers it to a higher output voltage. The input voltage range is 2.3V to 5.5V and the output voltage range is 5V to 25V. The switching frequency is selectable between 600kHz and 1.2MHz allowing smaller inductors and faster transient response. An external compensation pin gives the user greater flexibility in setting output transient response and tighter load regulation. The converter soft-start characteristic can also be controlled by the external C_{SS} capacitor. The EN pin allows the user to completely shut-down the device.

Boost Converter Operations

Figure 10 shows a boost converter with all the key components. In steady-state operating and continuous conduction mode where the inductor current is continuous, the boost converter operates in two cycles. During the first cycle, as shown in Figure 11, the internal power FET turns on and the Schottky diode is reverse biased and cuts off the current flow to the output. The output current is supplied from the output capacitor. The voltage across the inductor is V_{IN} and the inductor current ramps up in a rate of V_{IN}/L, L is the inductance. The inductance is magnetized and energy is stored in the inductor. The change in inductor current is shown in Equation 1:

$$\Delta I_{L1} = \Delta t1 \times \frac{V_{IN}}{L}$$

$$\Delta t1 = \frac{D}{f_{SW}}$$

D = Duty Cycle

$$\Delta V_O = \frac{I_{OUT}}{C_{OUT}} \times \Delta t_1 \quad \text{(EQ. 1)}$$

During the second cycle, the power FET turns off and the Schottky diode is forward biased, (see Figure 12). The energy stored in the inductor is pumped to the output supplying output current and charging the output capacitor. The Schottky diode side of the inductor is clamped to a Schottky diode above the output voltage. So the voltage drop across the inductor is V_{IN} - V_{OUT}. The change in inductor current during the second cycle is shown in Equation 2:

$$\Delta I_L = \Delta t2 \times \frac{V_{IN} - V_{OUT}}{L}$$

$$\Delta t2 = \frac{1 - D}{f_{SW}} \quad \text{(EQ. 2)}$$

For stable operation, the same amount of energy stored in the inductor must be taken out. The change in inductor current during the two cycles must be the same.

$$\Delta I1 + \Delta I2 = 0$$

$$\frac{D}{f_{SW}} \times \frac{V_{IN}}{L} + \frac{1 - D}{f_{SW}} \times \frac{V_{IN} - V_{OUT}}{L} = 0$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D} \quad \text{(EQ. 3)}$$

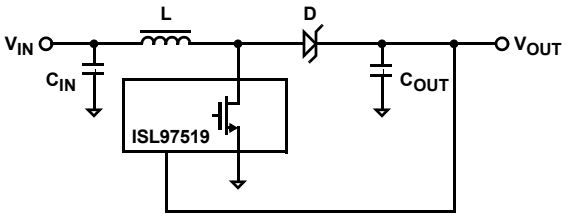


FIGURE 10. BOOST CONVERTER

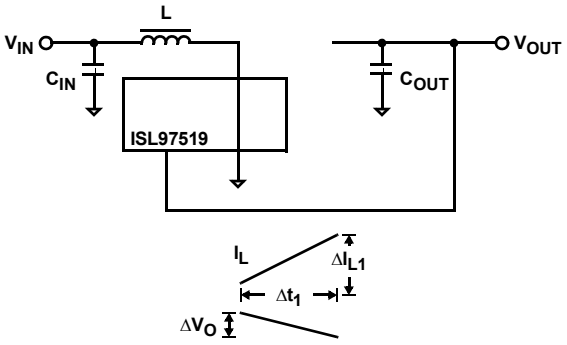


FIGURE 11. BOOST CONVERTER - CYCLE 1, POWER SWITCH CLOSED

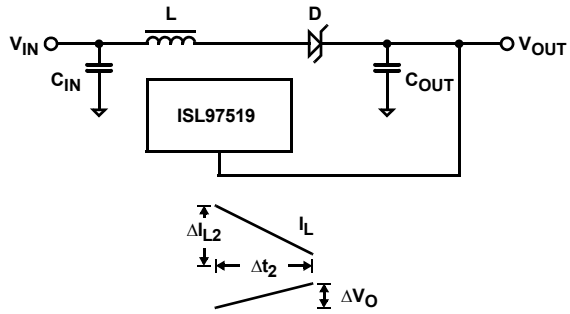


FIGURE 12. BOOST CONVERTER - CYCLE 2, POWER SWITCH OPEN

Output Voltage

An external feedback resistor divider is required to divide the output voltage down to the nominal 1.294V reference voltage. The current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network less than 100k is recommended. The boost converter output voltage is determined by the relationship in Equation 4:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 4)}$$

The nominal VFB voltage is 1.294V.

Inductor Selection

The inductor selection determines the output ripple voltage, transient response, output current capability, and efficiency. Its selection depends on the input voltage, output voltage, switching frequency, and maximum output current. For most applications, the inductance should be in the range of 2µH to 33µH. The inductor maximum DC current specification must be greater than the peak inductor current required by the regulator. The peak inductor current can be calculated using Equation 5:

$$I_{L(PEAK)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN}} + 1/2 \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{L \times V_{OUT} \times FREQ} \quad \text{(EQ. 5)}$$

Output Capacitor

Low ESR capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors (X5R and X7R) are preferred for the output capacitors because of their lower ESR and small packages. Tantalum capacitors with higher ESR can also be used. The output ripple can be calculated in Equation 6:

$$\Delta V_O = \frac{I_{OUT} \times D}{f_{SW} \times C_O} + I_{OUT} \times ESR \quad \text{(EQ. 6)}$$

For noise sensitive applications, a 0.1µF placed in parallel with the larger output capacitor is recommended to reduce the switching noise coupled from the LX switching node.

Schottky Diode

In selecting the Schottky diode, the reverse break down voltage, forward current and forward voltage drop must be considered for optimum converter performance. The diode must be rated to handle 2.0A, the current limit of the ISL97519. The breakdown voltage must exceed the maximum output voltage. Low forward voltage drop, low leakage current, and fast reverse recovery will help the converter to achieve the maximum efficiency.

Input Capacitor

The value of the input capacitor depends upon the input and output voltages, the maximum output current, the inductor value and the noise allowed to put back on the input line. For most applications, a minimum 10µF is required. For applications that run close to the maximum output current limit, an input capacitor in the range of 22µF to 47µF is recommended.

The ISL97519 is powered from the VIN. A High frequency 0.1µF bypass cap is recommended to be close to the VIN pin to reduce supply line noise and ensure stable operation.

Loop Compensation

The ISL97519 incorporates a transconductance amplifier in its feedback path to allow the user some adjustment on the transient response and better regulation. The ISL97519 uses current mode control architecture, which has a fast current sense loop and a slow voltage feedback loop. The fast current feedback loop does not require any compensation. The slow voltage loop must be compensated for stable operation. The compensation network is a series RC network from COMP pin to ground. The resistor sets the high frequency integrator gain for fast transient response and the capacitor sets the integrator zero to ensure loop stability. For most applications, the compensation resistor is in the range of 2k to 7.5k and the compensation capacitor is in the range of 3nF to 10nF.

Soft-Start

The soft-start is provided by an internal 6µA current source, which charges the external C_{SS}; the peak MOSFET current is limited by the voltage on the capacitor. This in turn controls the rising rate of the output voltage. The regulator goes through the start-up sequence as well, after the EN pin is pulled to HI.

Frequency Selection

The ISL97519 switching frequency can be user selected to operate at either constant 620kHz or 1.25MHz. Connecting FSEL pin to ground sets the PWM switching frequency to 620kHz. When connecting FSEL high or VDD, the switching frequency is set to 1.25MHz.

Shut-down Control

When the EN pin is pulled down, the ISL97519 is shut down reducing the supply current to <1µA.

Maximum Output Current

The MOSFET current limit is nominally 2.0A and guaranteed 1.7A. This restricts the maximum output current, I_{OMAX}, based on Equation 7:

$$I_L = I_{L\text{-}AVG} + (1/2 \times \Delta I_L) \quad \text{(EQ. 7)}$$

where:

I_L = MOSFET current limit

$I_{L\text{-}AVG}$ = average inductor current

ΔI_L = inductor ripple current

$$\Delta I_L = \frac{V_{IN} \times [(V_O + V_{DIODE}) - V_{IN}]}{L \times (V_O + V_{DIODE}) \times f_S} \quad \text{(EQ. 8)}$$

V_{DIODE} = Schottky diode forward voltage, typically, 0.6V

f_S = switching frequency, 600kHz or 1.2MHz

$$I_{L\text{-}AVG} = \frac{I_{OUT}}{1 - D} \quad \text{(EQ. 9)}$$

D = MOSFET turn-on ratio:

$$D = 1 - \frac{V_{IN}}{V_{OUT} + V_{DIODE}} \quad \text{(EQ. 10)}$$

Table 1 gives typical maximum I_{OUT} values for 1.2MHz switching frequency and 10µH inductor.

TABLE 1. MAXIMUM I_{OUT} VALUES

V_{IN} (V)	V_{OUT} (V)	I_{OMAX} (mA)
2.5	5	870
2.5	9	500
2.5	12	380
3.3	5	1150
3.3	9	655
3.3	12	500
5	9	990
5	12	750

Cascaded MOSFET Application

An 25V N-Channel MOSFET is integrated in the boost regulator. For the applications where the output voltage is greater than 25V, an external cascaded MOSFET is needed, as shown in Figure 13. The voltage rating of the external MOSFET should be greater than A_{VDD}.

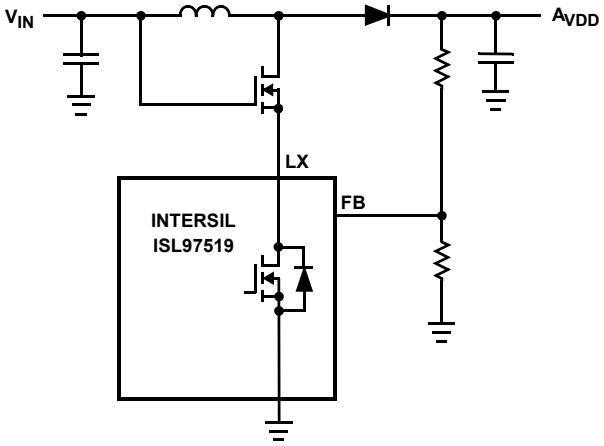


FIGURE 13. CASCADED MOSFET TOPOLOGY FOR HIGH OUTPUT VOLTAGE APPLICATIONS

DC Path Block Application

Note that there is a DC path in the boost converter from the input to the output through the inductor and diode, hence the input voltage will be seen at output with a forward voltage drop of diode before the part is enabled. If this voltage is not desired, the following circuit can be inserted between input and inductor to disconnect the DC path when the part is disabled.

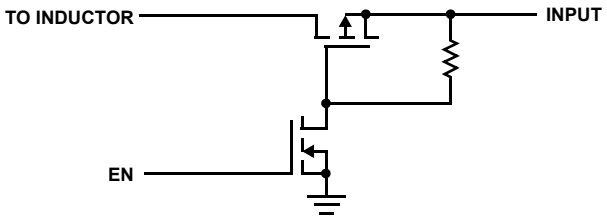
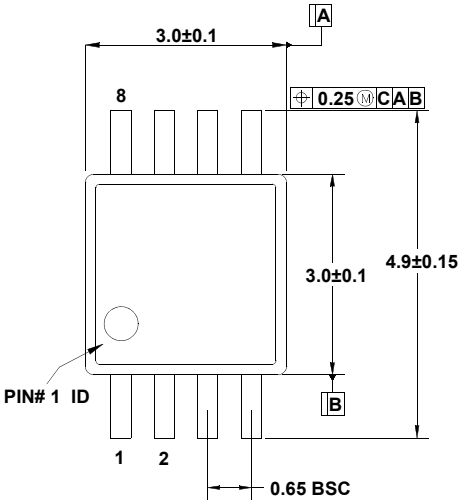


FIGURE 14. CIRCUIT TO DISCONNECT THE DC PATH OF BOOST CONVERTER

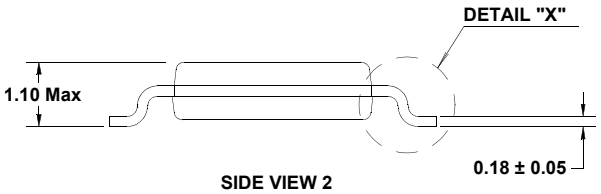
Package Outline Drawing

M8.118A

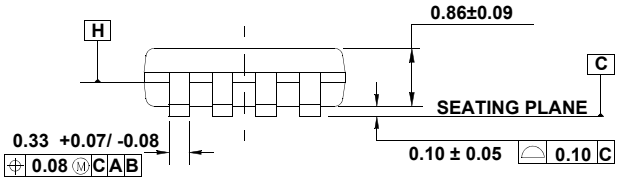
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)
Rev 0, 9/09



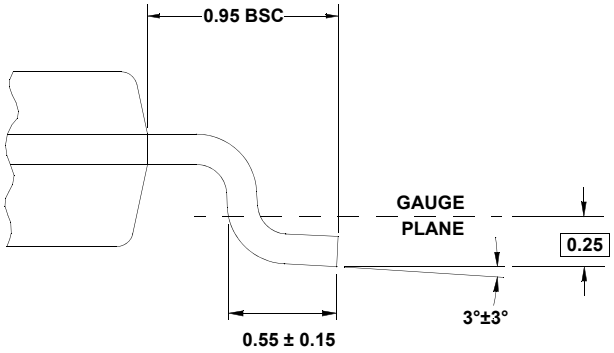
TOP VIEW



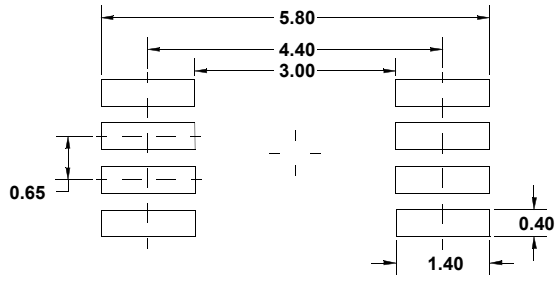
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP 8L.

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- Shortage Management
- Alternative Solution
- Excess Inventory Management