



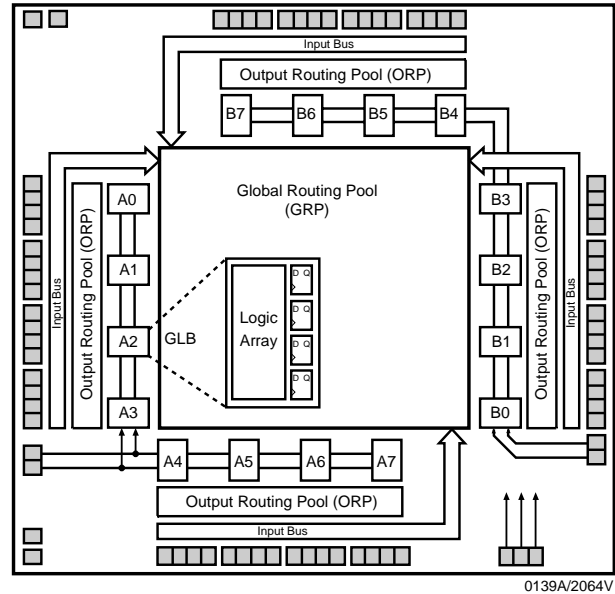
**THE DATASHEET OF  
ISPLSI2064VE-100LT44**





## Features Functional Block Diagram

- **SuperFAST HIGH DENSITY PROGRAMMABLE LOGIC**
  - 2000 PLD Gates
  - 64 and 32 I/O Pin Versions, Four Dedicated Inputs
  - 64 Registers
  - High Speed Global Interconnect
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - 100% Functional, JEDEC and Pinout Compatible with ispLSI 2064V Devices
- **3.3V LOW VOLTAGE 2064 ARCHITECTURE**
  - Interfaces with Standard 5V TTL Devices
- **HIGH-PERFORMANCE E<sup>2</sup>CMOS<sup>®</sup> TECHNOLOGY**
  - $f_{max} = 280\text{MHz}$  Maximum Operating Frequency
  - $t_{pd} = 3.5\text{ns}$  Propagation Delay
  - Electrically Erasable and Reprogrammable
  - Non-Volatile
  - 100% Tested at Time of Manufacture
  - Unused Product Term Shutdown Saves Power
- **IN-SYSTEM PROGRAMMABLE**
  - 3.3V In-System Programmability (ISP<sup>™</sup>) Using Boundary Scan Test Access Port (TAP)
  - Open-Drain Output Option for Flexible Bus Interface Capability, Allowing Easy Implementation of Wired-OR or Bus Arbitration Logic
  - Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
  - Reprogram Soldered Devices for Faster Prototyping
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE**
- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAs**
  - Enhanced Pin Locking Capability
  - Three Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Programmable Output Slew Rate Control
  - Flexible Pin Placement
  - Optimized Global Routing Pool Provides Global Interconnectivity
- **LEAD-FREE PACKAGE OPTIONS**



## Description

The ispLSI 2064VE is a High Density Programmable Logic Device available in 64 and 32 I/O-pin versions. The device contains 64 Registers, four Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2064VE features in-system programmability through the Boundary Scan Test Access Port (TAP) and is 100% IEEE 1149.1 Boundary Scan Testable. The ispLSI 2064VE offers non-volatile reprogrammability of the logic, as well as the interconnect, to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2064VE device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1...B7 (see Figure 1). There are a total of 16 GLBs in the ispLSI 2064VE device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

Copyright © 2004 Lattice Semiconductor Corp. All brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



**Absolute Maximum Ratings <sup>1</sup>**

Supply Voltage  $V_{CC}$ ..... -0.5 to +5.4V  
 Input Voltage Applied ..... -0.5 to +5.6V  
 Off-State Output Voltage Applied ..... -0.5 to +5.6V  
 Storage Temperature ..... -65 to 150°C  
 Case Temp. with Power Applied ..... -55 to 125°C  
 Max. Junction Temp. ( $T_J$ ) with Power Applied ..... 150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

**DC Recommended Operating Condition**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	
$V_{CC}$	Supply Voltage	Commercial $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	3.0	3.6	V
		Industrial $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.0	3.6	V
$V_{IL}$	Input Low Voltage	$V_{SS} - 0.5$	0.8	V	
$V_{IH}$	Input High Voltage	2.0	5.25	V	

Table 2-0005/2064VE

**Capacitance ( $T_A=25^\circ\text{C}$ ,  $f=1.0\text{ MHz}$ )**

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
$C_1$	Dedicated Input Capacitance	8	pf	$V_{CC} = 3.3\text{V}$ , $V_{IN} = 0.0\text{V}$
$C_2$	I/O Capacitance	6	pf	$V_{CC} = 3.3\text{V}$ , $V_{I/O} = 0.0\text{V}$
$C_3$	Clock and Global Output Enable Capacitance	10	pf	$V_{CC} = 3.3\text{V}$ , $V_Y = 0.0\text{V}$

Table 2-0006/2064VE

**Erase Reprogram Specifications**

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/2064VE

**Switching Test Conditions**

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 1.5 ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

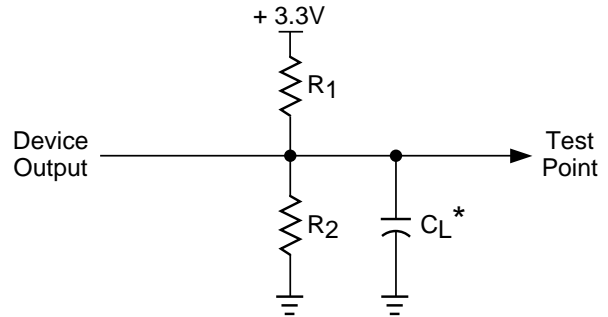
Table 2-0003/2064VE

**Output Load Conditions (see Figure 2)**

TEST CONDITION		R1	R2	CL
A		316Ω	348Ω	35pF
B	Active High	∞	348Ω	35pF
	Active Low	316Ω	348Ω	35pF
C	Active High to Z at $V_{OH}-0.5V$	∞	348Ω	5pF
	Active Low to Z at $V_{OL}+0.5V$	316Ω	348Ω	5pF

Table 2-0004/2064V

**Figure 2. Test Load**



\*CL includes Test Fixture and Probe Capacitance.

0213A/2064V

**DC Electrical Characteristics**

**Over Recommended Operating Conditions**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. <sup>3</sup>	MAX.	UNITS
<b>V<sub>OL</sub></b>	Output Low Voltage	$I_{OL} = 8 \text{ mA}$	–	–	0.4	V
<b>V<sub>OH</sub></b>	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4	–	–	V
<b>I<sub>IL</sub></b>	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (\text{Max.})$	–	–	-10	μA
<b>I<sub>IH</sub></b>	Input or I/O High Leakage Current	$(V_{CC} - 0.2)V \leq V_{IN} \leq V_{CC}$	–	–	10	μA
		$V_{CC} \leq V_{IN} \leq 5.25V$	–	–	10	μA
<b>I<sub>IL-isp</sub></b>	BSCAN Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$	–	–	-150	μA
<b>I<sub>IL-PU</sub></b>	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	–	–	-150	μA
<b>I<sub>OS</sub><sup>1</sup></b>	Output Short Circuit Current	$V_{CC} = 3.3V, V_{OUT} = 0.5V$	–	–	-100	mA
<b>I<sub>CC</sub><sup>2,4</sup></b>	Operating Power Supply Current	$V_{IL} = 0.0V, V_{IH} = 3.0V$ $f_{CLOCK} = 1 \text{ MHz}$	–	90	–	mA

Table 2-0007/2064VE

- One output at a time for a maximum duration of one second.  $V_{OUT} = 0.5V$  was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
- Measured using four 16-bit counters.
- Typical values are at  $V_{CC} = 3.3V$  and  $T_A = 25^\circ C$ .
- Maximum  $I_{CC}$  varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum  $I_{CC}$ .

## External Timing Parameters

### Over Recommended Operating Conditions

PARAMETER	TEST COND. <sup>3</sup>	#	DESCRIPTION <sup>1</sup>	-280		-200		UNITS
				MIN.	MAX.	MIN.	MAX.	
t <sub>pd1</sub>	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	3.5	–	4.5	ns
t <sub>pd2</sub>	A	2	Data Propagation Delay	–	5.5	–	7.0	ns
f <sub>max</sub>	A	3	Clock Frequency with Internal Feedback <sup>2</sup>	280	–	200	–	MHz
f <sub>max</sub> (Ext.)	–	4	Clock Frequency with External Feedback ( $\frac{1}{t_{su2} + t_{co1}}$ )	182	–	133	–	MHz
f <sub>max</sub> (Tog.)	–	5	Clock Frequency, Max. Toggle	300	–	200	–	MHz
t <sub>su1</sub>	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	2.3	–	3.0	–	ns
t <sub>co1</sub>	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	2.5	–	3.5	ns
t <sub>h1</sub>	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t <sub>su2</sub>	–	9	GLB Reg. Setup Time before Clock	3.0	–	4.0	–	ns
t <sub>co2</sub>	A	10	GLB Reg. Clock to Output Delay	–	3.3	–	4.5	ns
t <sub>h2</sub>	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t <sub>r1</sub>	A	12	Ext. Reset Pin to Output Delay, ORP Bypass	–	5.5	–	6.0	ns
t <sub>rw1</sub>	–	13	Ext. Reset Pulse Duration	3.5	–	4.0	–	ns
t <sub>ptoen</sub>	B	14	Input to Output Enable	–	6.0	–	8.0	ns
t <sub>ptoedis</sub>	C	15	Input to Output Disable	–	6.0	–	8.0	ns
t <sub>goeen</sub>	B	16	Global OE Output Enable	–	3.5	–	5.0	ns
t <sub>goedis</sub>	C	17	Global OE Output Disable	–	3.5	–	5.0	ns
t <sub>wh</sub>	–	18	External Synchronous Clock Pulse Duration, High	1.6	–	2.5	–	ns
t <sub>wl</sub>	–	19	External Synchronous Clock Pulse Duration, Low	1.6	–	2.5	–	ns

Table 2-0030A/2064VE v.0.0

1. Unless noted otherwise, all parameters use a GRP load of four, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

**External Timing Parameters**

**Over Recommended Operating Conditions**

PARAMETER	TEST COND. <sup>3</sup>	#	DESCRIPTION <sup>1</sup>	-135		-100		UNITS
				MIN.	MAX.	MIN.	MAX.	
t <sub>pd1</sub>	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10.0	ns
t <sub>pd2</sub>	A	2	Data Propagation Delay	–	10.0	–	13.0	ns
f <sub>max</sub>	A	3	Clock Frequency with Internal Feedback <sup>2</sup>	135	–	100	–	MHz
f <sub>max</sub> (Ext.)	–	4	Clock Frequency with External Feedback ( $\frac{1}{t_{su2} + t_{co1}}$ )	100	–	77	–	MHz
f <sub>max</sub> (Tog.)	–	5	Clock Frequency, Max. Toggle	143	–	100	–	MHz
t <sub>su1</sub>	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.0	–	6.5	–	ns
t <sub>co1</sub>	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.0	–	5.0	ns
t <sub>h1</sub>	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t <sub>su2</sub>	–	9	GLB Reg. Setup Time before Clock	6.0	–	8.0	–	ns
t <sub>co2</sub>	A	10	GLB Reg. Clock to Output Delay	–	5.0	–	6.0	ns
t <sub>h2</sub>	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t <sub>r1</sub>	A	12	Ext. Reset Pin to Output Delay, ORP Bypass	–	9.0	–	12.5	ns
t <sub>rw1</sub>	–	13	Ext. Reset Pulse Duration	5.0	–	6.5	–	ns
t <sub>ptoen</sub>	B	14	Input to Output Enable	–	12.0	–	15.0	ns
t <sub>ptoedis</sub>	C	15	Input to Output Disable	–	12.0	–	15.0	ns
t <sub>goeen</sub>	B	16	Global OE Output Enable	–	7.0	–	9.0	ns
t <sub>goedis</sub>	C	17	Global OE Output Disable	–	7.0	–	9.0	ns
t <sub>wh</sub>	–	18	External Synchronous Clock Pulse Duration, High	3.5	–	5.0	–	ns
t <sub>wl</sub>	–	19	External Synchronous Clock Pulse Duration, Low	3.5	–	5.0	–	ns

1. Unless noted otherwise, all parameters use a GRP load of four, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

Table 2-0030B/2064VE v.0.0

## Internal Timing Parameters<sup>1</sup>

### Over Recommended Operating Conditions

PARAMETER	# <sup>2</sup>	DESCRIPTION	-280		-200		UNITS
			MIN.	MAX.	MIN.	MAX.	
<b>Inputs</b>							
<b>t<sub>io</sub></b>	20	Input Buffer Delay	–	0.4	–	0.5	ns
<b>t<sub>din</sub></b>	21	Dedicated Input Delay	–	0.8	–	1.1	ns
<b>GRP</b>							
<b>t<sub>grp</sub></b>	22	GRP Delay	–	0.4	–	0.6	ns
<b>GLB</b>							
<b>t<sub>4ptbpc</sub></b>	23	4 Product Term Bypass Path Delay (Combinatorial)	–	1.1	–	1.4	ns
<b>t<sub>4ptbpr</sub></b>	24	4 Product Term Bypass Path Delay (Registered)	–	1.6	–	1.9	ns
<b>t<sub>1ptxor</sub></b>	25	1 Product Term/XOR Path Delay	–	2.3	–	2.9	ns
<b>t<sub>20ptxor</sub></b>	26	20 Product Term/XOR Path Delay	–	2.3	–	2.9	ns
<b>t<sub>xoradj</sub></b>	27	XOR Adjacent Path Delay <sup>3</sup>	–	2.3	–	2.9	ns
<b>t<sub>gbp</sub></b>	28	GLB Register Bypass Delay	–	0.0	–	0.0	ns
<b>t<sub>gsu</sub></b>	29	GLB Register Setup Time before Clock	0.6	–	1.2	–	ns
<b>t<sub>gh</sub></b>	30	GLB Register Hold Time after Clock	1.7	–	1.8	–	ns
<b>t<sub>gco</sub></b>	31	GLB Register Clock to Output Delay	–	0.2	–	0.3	ns
<b>t<sub>gro</sub></b>	32	GLB Register Reset to Output Delay	–	0.4	–	0.4	ns
<b>t<sub>ptre</sub></b>	33	GLB Product Term Reset to Register Delay	–	4.1	–	4.3	ns
<b>t<sub>ptoe</sub></b>	34	GLB Product Term Output Enable to I/O Cell Delay	–	2.9	–	3.9	ns
<b>t<sub>ptck</sub></b>	35	GLB Product Term Clock Delay	0.8	2.9	1.0	4.0	ns
<b>ORP</b>							
<b>t<sub>orp</sub></b>	36	ORP Delay	–	1.2	–	1.5	ns
<b>t<sub>orpbp</sub></b>	37	ORP Bypass Delay	–	0.4	–	0.5	ns
<b>Outputs</b>							
<b>t<sub>ob</sub></b>	38	Output Buffer Delay	–	1.2	–	1.5	ns
<b>t<sub>sl</sub></b>	39	Output Slew Limited Delay Adder	–	1.8	–	2.0	ns
<b>t<sub>oen</sub></b>	40	I/O Cell OE to Output Enabled	–	2.3	–	3.0	ns
<b>t<sub>odis</sub></b>	41	I/O Cell OE to Output Disabled	–	2.3	–	3.0	ns
<b>t<sub>goe</sub></b>	42	Global Output Enable	–	1.2	–	2.0	ns
<b>Clocks</b>							
<b>t<sub>gy0</sub></b>	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	0.7	0.7	1.2	1.2	ns
<b>t<sub>gy1/2</sub></b>	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	0.9	0.9	1.4	1.4	ns
<b>Global Reset</b>							
<b>t<sub>gr</sub></b>	45	Global Reset to GLB	–	3.5	–	3.6	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036A/2064VE v.0.0

**Internal Timing Parameters<sup>1</sup>**

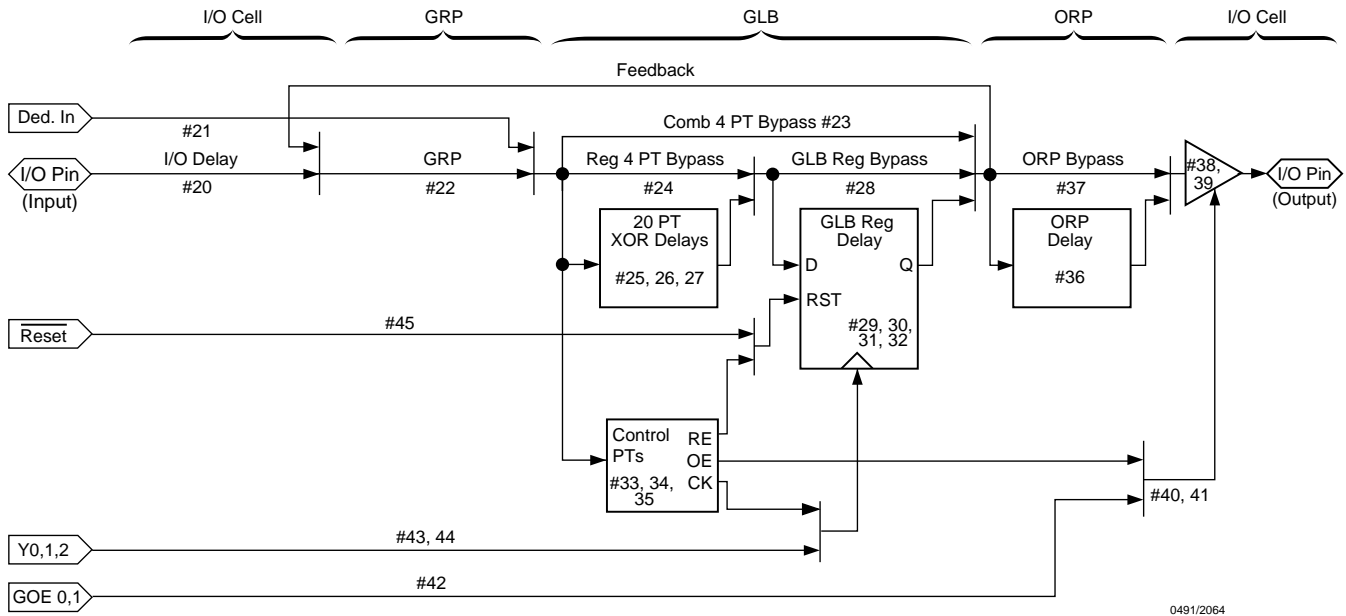
**Over Recommended Operating Conditions**

PARAMETER	# <sup>2</sup>	DESCRIPTION	-135		-100		UNITS
			MIN.	MAX.	MIN.	MAX.	
<b>Inputs</b>							
t <sub>io</sub>	20	Input Buffer Delay	–	0.5	–	0.7	ns
t <sub>din</sub>	21	Dedicated Input Delay	–	1.7	–	2.5	ns
<b>GRP</b>							
t <sub>grp</sub>	22	GRP Delay	–	1.2	–	1.8	ns
<b>GLB</b>							
t <sub>4ptbpc</sub>	23	4 Product Term Bypass Path Delay (Combinatorial)	–	3.7	–	5.2	ns
t <sub>4ptbpr</sub>	24	4 Product Term Bypass Path Delay (Registered)	–	3.7	–	4.7	ns
t <sub>1ptxor</sub>	25	1 Product Term/XOR Path Delay	–	4.7	–	6.2	ns
t <sub>20ptxor</sub>	26	20 Product Term/XOR Path Delay	–	4.7	–	6.2	ns
t <sub>xoradj</sub>	27	XOR Adjacent Path Delay <sup>3</sup>	–	4.7	–	6.2	ns
t <sub>gbp</sub>	28	GLB Register Bypass Delay	–	0.5	–	1.0	ns
t <sub>gsu</sub>	29	GLB Register Setup Time before Clock	1.2	–	1.7	–	ns
t <sub>gh</sub>	30	GLB Register Hold Time after Clock	3.8	–	4.8	–	ns
t <sub>gco</sub>	31	GLB Register Clock to Output Delay	–	0.3	–	0.3	ns
t <sub>gro</sub>	32	GLB Register Reset to Output Delay	–	1.1	–	3.1	ns
t <sub>ptre</sub>	33	GLB Product Term Reset to Register Delay	–	6.1	–	7.1	ns
t <sub>ptoe</sub>	34	GLB Product Term Output Enable to I/O Cell Delay	–	6.9	–	9.1	ns
t <sub>ptck</sub>	35	GLB Product Term Clock Delay	1.6	5.0	2.6	5.6	ns
<b>ORP</b>							
t <sub>orp</sub>	36	ORP Delay	–	1.5	–	1.7	ns
t <sub>orpbp</sub>	37	ORP Bypass Delay	–	0.5	–	0.7	ns
<b>Outputs</b>							
t <sub>ob</sub>	38	Output Buffer Delay	–	1.6	–	1.6	ns
t <sub>sl</sub>	39	Output Slew Limited Delay Adder	–	2.0	–	2.0	ns
t <sub>oen</sub>	40	I/O Cell OE to Output Enabled	–	3.4	–	3.4	ns
t <sub>odis</sub>	41	I/O Cell OE to Output Disabled	–	3.4	–	3.4	ns
t <sub>goe</sub>	42	Global Output Enable	–	3.6	–	5.6	ns
<b>Clocks</b>							
t <sub>gy0</sub>	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	1.6	1.6	2.4	2.4	ns
t <sub>gy1/2</sub>	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	1.8	1.8	2.6	2.6	ns
<b>Global Reset</b>							
t <sub>gr</sub>	45	Global Reset to GLB	–	5.8	–	7.1	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036B/2064VE v.0.0

**ispLSI 2064VE Timing Model**



0491/2064

**Derivations of tsu, th and tco from the Product Term Clock**

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg su} - \text{Clock (min)} \\
 &= (t_{io} + t_{grp} + t_{20ptxor}) + (t_{gsu}) - (t_{io} + t_{grp} + t_{ptck(min)}) \\
 &= (\#20 + \#22 + \#26) + (\#29) - (\#20 + \#22 + \#35) \\
 2.1\text{ns} &= (0.4 + 0.4 + 2.3) + (0.6) - (0.4 + 0.4 + 0.8) \\
 \\
 t_h &= \text{Clock (max)} + \text{Reg h} - \text{Logic} \\
 &= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gh}) - (t_{io} + t_{grp} + t_{20ptxor}) \\
 &= (\#20 + \#22 + \#35) + (\#30) - (\#20 + \#22 + \#26) \\
 2.3\text{ns} &= (0.4 + 0.4 + 2.9) + (1.7) - (0.4 + 0.4 + 2.3) \\
 \\
 t_{co} &= \text{Clock (max)} + \text{Reg co} + \text{Output} \\
 &= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#22 + \#35) + (\#31) + (\#36 + \#38) \\
 6.3\text{ns} &= (0.4 + 0.4 + 2.9) + (0.2) + (1.2 + 1.2)
 \end{aligned}$$

Note: Calculations are based on timing specifications for the ispLSI 2064VE-280L.

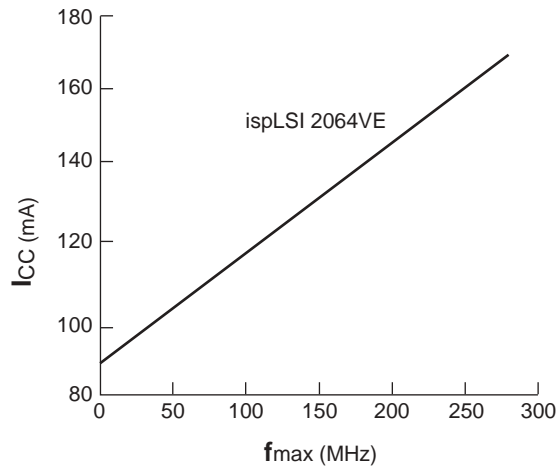
Table 2-0042/2064VE

**Power Consumption**

Power consumption in the ispLSI 2064VE device depends on two primary factors: the speed at which the device is operating and the number of Product Terms

used. Figure 3 shows the relationship between power and operating speed.

**Figure 3. Typical Device Power Consumption vs fmax**



Notes: Configuration of four 16-bit counters  
Typical current at 3.3V, 25° C

ICC can be estimated for the ispLSI 2064VE using the following equation:

$$I_{CC}(mA) = 8 + (\# \text{ of PTs} * 0.67) + (\# \text{ of Nets} * F_{max} * 0.0045)$$

Where:

- # of PTs = Number of Product Terms used in design
- # of nets = Number of Signals used in device
- Max freq = Highest Clock Frequency to the device (in MHz)

The ICC estimate is based on typical conditions (VCC = 3.3V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127/2064VE

### 64-I/O Signal Descriptions

Signal Name	Description
RESET	Active Low (0) Reset pin resets all the registers in the device.
GOE 0, GOE1	Global Output Enable input pins.
Y0, Y1, Y2	Dedicated Clock Input – These clock inputs are connected to one of the clock inputs of all the GLBs in the device.
BSCAN	Input – Dedicated in-system programming Boundary Scan enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.
TDI/IN 0	Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a serial data input pin to load programming data into the device. (2) When BSCAN is high, it functions as a dedicated input pin.
TCK/IN 3	Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a clock pin for the Boundary Scan state machine. (2) When BSCAN is high, it functions as a dedicated input pin.
TMS/IN 1	Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a mode control pin for the Boundary Scan state machine. (2) When BSCAN is high, it functions as a dedicated input pin.
TDO/IN 2	Output/Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as an output pin to read serial shift register data. (2) When BSCAN is high, it functions as a dedicated input pin.
GND	Ground (GND)
VCC	Vcc
NC <sup>1</sup>	No Connect
I/O	Input/Output Pins – These are the general purpose I/O pins used by the logic array.

1. NC pins are not to be connected to any active signals, VCC or GND.

### 32-I/O Signal Descriptions

Signal Name	Description
GOE 0/IN 3	This pin performs one of two functions. It can be programmed to function as a Global Output Enable pin or a Dedicated Input pin.
GOE 1/Y0	This pin performs one of two functions. (1) It can be programmed to function as a Global Output Enable or a Dedicated Clock input. (2) This clock input is connected to one of the clock inputs of all GLBs on the device.
RESET/Y1	This pin performs two functions: (1) Active Low (0) Reset pin which resets all of the registers in the device. (2) When active low (0), it functions as a dedicated clock input.
BSCAN	Input – Dedicated in-system programming Boundary Scan Enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.
TDI/IN 0	Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a serial data input pin to load programming data into the device. (2) When BSCAN is high, it functions as a dedicated input pin.
TMS/IN 2	Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a mode control pin for the Boundary Scan state machine. (2) When BSCAN is high, it functions as a dedicated input pin.
TDO/IN 1	Output/Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as an output pin to read serial shift register data. (2) When BSCAN is high, it functions as a dedicated input pin.
TCK/Y2	Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a clock pin for the Boundary Scan state machine. (2) When BSCAN is high, it functions as a dedicated clock input.
GND	Ground (GND)
VCC	Vcc
NC <sup>1</sup>	No Connect
I/O	Input/Output pins – These are the general purpose I/O pins used by the logic array.

1. NC pins are not to be connected to any active signals, VCC or GND.

## 64-I/O Signal Locations

Signal	100-Ball caBGA	100-Pin TQFP
RESET	D2	11
GOE 0, GOE 1	F9, E1	62, 13
Y0, Y1, Y2	E3, F6, F8	10, 65, 60
BSCAN	E5	15
TDI/IN 0	F2	16
TCK/IN 3	G10	59
TMS/IN 1	J5	37
TDO/IN 2	B6	87
GND	B7, F1, G9, K6	14, 39, 61, 86
VCC	A5, E2, F10, J4	12, 36, 63, 89
NC <sup>1</sup>	A6, A8, C3, C4, D1, D6, D8, E7, E9, E10, F4, G3, G5, H7, H8, K3, K5	4, 9, 21, 25, 31, 38, 44, 50, 54, 64, 66, 71, 75, 81, 88, 94, 100

1. NC pins are not to be connected to any active signals, VCC or GND.

## 32-I/O Signal Locations

Signal	44-Pin TQFP	44-Pin PLCC
GOE 0/ IN 3	40	2
GOE 1/Y0	5	11
RESET/Y1	29	35
BSCAN	7	13
TDI/IN 0	8	14
TMS/IN 2	30	36
TDO/IN 1	18	24
TCK/Y2	27	33
GND	17, 39	1, 23
VCC	6, 28	12, 34
NC <sup>1</sup>	—	—

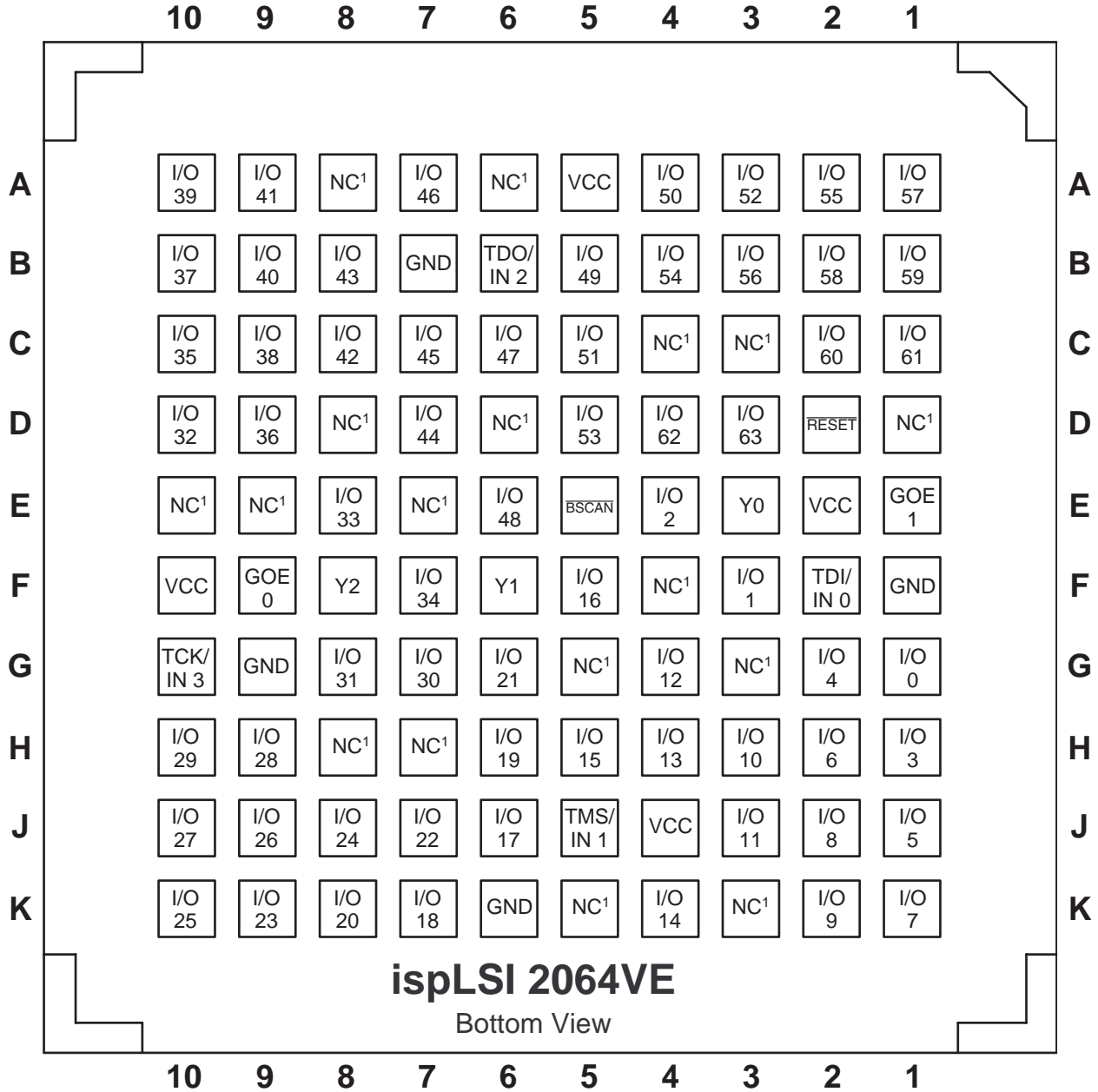
1. NC pins are not to be connected to any active signals, VCC or GND.

## I/O Locations

Signal	100 caBGA	100 TQFP	44 TQFP	44 PLCC
I/O 0	G1	17	9	15
I/O 1	F3	18	10	16
I/O 2	E4	19	11	17
I/O 3	H1	20	12	18
I/O 4	G2	22	13	19
I/O 5	J1	23	14	20
I/O 6	H2	24	15	21
I/O 7	K1	26	16	22
I/O 8	J2	27	19	25
I/O 9	K2	28	20	26
I/O 10	H3	29	21	27
I/O 11	J3	30	22	28
I/O 12	G4	32	23	29
I/O 13	H4	33	24	30
I/O 14	K4	34	25	31
I/O 15	H5	35	26	32
I/O 16	F5	40	31	37
I/O 17	J6	41	32	38
I/O 18	K7	42	33	39
I/O 19	H6	43	34	40
I/O 20	K8	45	35	41
I/O 21	G6	46	36	42
I/O 22	J7	47	37	43
I/O 23	K9	48	38	44
I/O 24	J8	49	41	3
I/O 25	K10	51	42	4
I/O 26	J9	52	43	5
I/O 27	J10	53	44	6
I/O 28	H9	55	1	7
I/O 29	H10	56	2	8
I/O 30	G7	57	3	9
I/O 31	G8	58	4	10
I/O 32	D10	67	—	—
I/O 33	E8	68	—	—
I/O 34	F7	69	—	—
I/O 35	C10	70	—	—
I/O 36	D9	72	—	—
I/O 37	B10	73	—	—
I/O 38	C9	74	—	—
I/O 39	A10	76	—	—
I/O 40	B9	77	—	—
I/O 41	A9	78	—	—
I/O 42	C8	79	—	—
I/O 43	B8	80	—	—
I/O 44	D7	82	—	—
I/O 45	C7	83	—	—
I/O 46	A7	84	—	—
I/O 47	C6	85	—	—
I/O 48	E6	90	—	—
I/O 49	B5	91	—	—
I/O 50	A4	92	—	—
I/O 51	C5	93	—	—
I/O 52	A3	95	—	—
I/O 53	D5	96	—	—
I/O 54	B4	97	—	—
I/O 55	A2	98	—	—
I/O 56	B3	99	—	—
I/O 57	A1	1	—	—
I/O 58	B2	2	—	—
I/O 59	B1	3	—	—
I/O 60	C2	5	—	—
I/O 61	C1	6	—	—
I/O 62	D4	7	—	—
I/O 63	D3	8	—	—

**Signal Configuration**

ispLSI 2064VE 100-Ball caBGA Signal Diagram (0.8mm Ball Pitch/10.0 x 10.0mm Body Size)



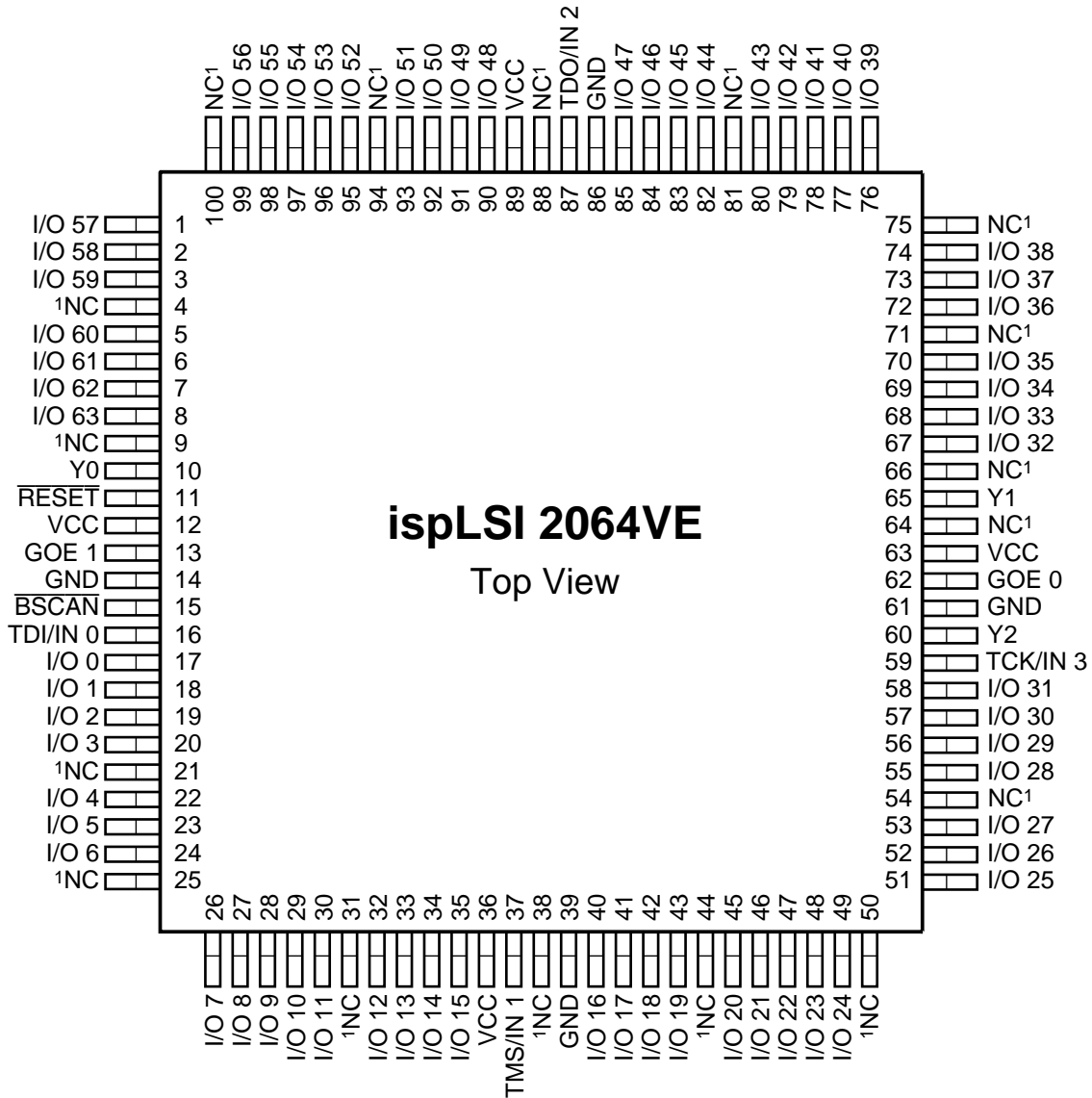
100-BGA/2064VE

<sup>1</sup>NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

**Pin Configuration**

ispLSI 2064VE 100-Pin TQFP Pinout Diagram (0.5mm Lead Pitch/14.0 x 14.0mm Body Size)

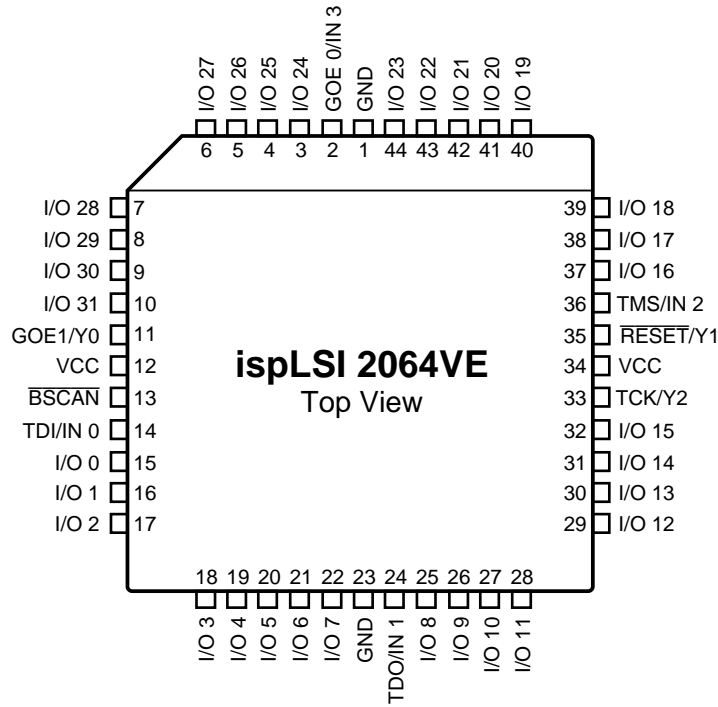


100 TQFP/2064VE

1. NC pins are not to be connected to any active signals, VCC or GND.

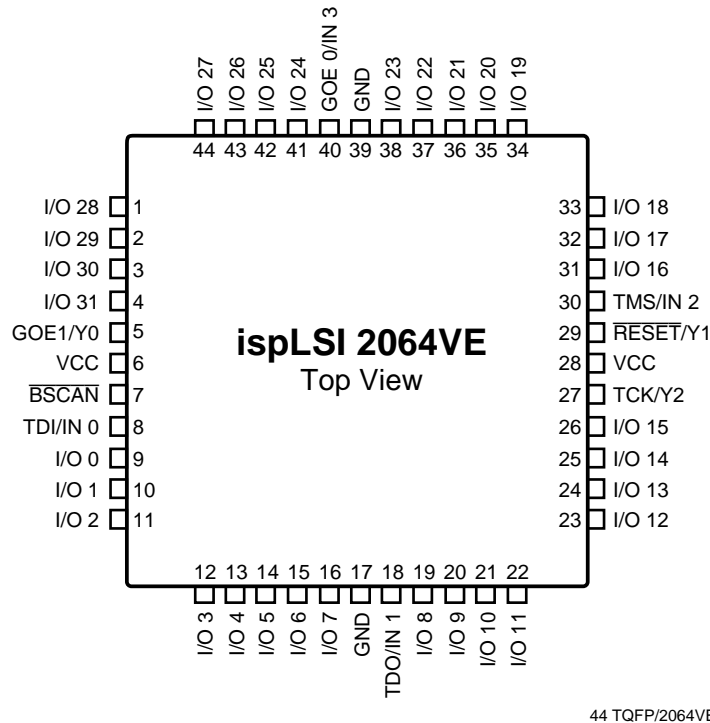
**Pin Configuration**

ispLSI 2064VE 44-Pin PLCC Pinout Diagram (0.05in Lead Pitch/0.65 x 0.65in Body Size)

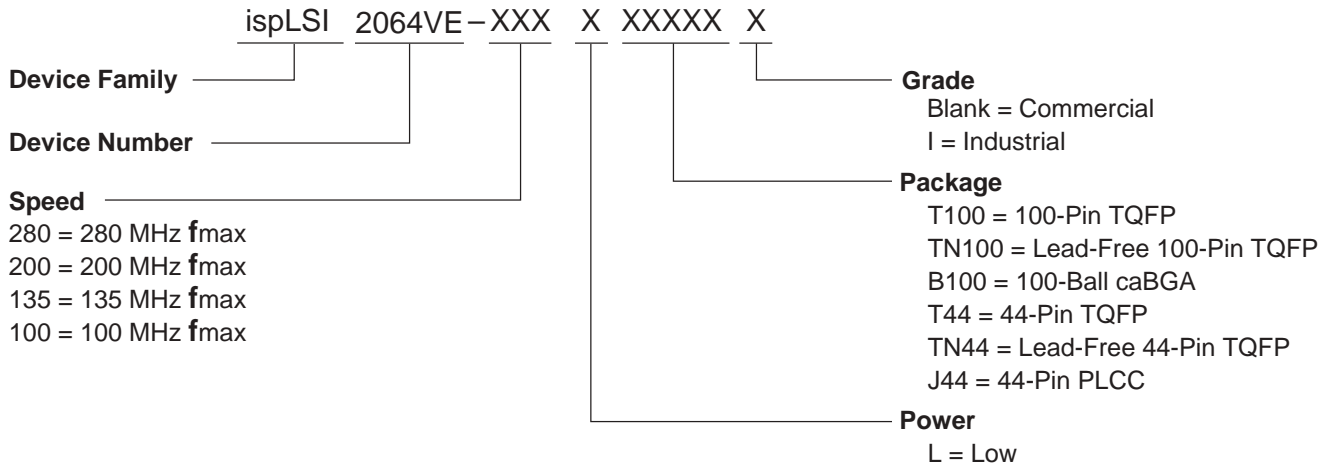


**Pin Configuration**

ispLSI 2064VE 44-Pin TQFP Pinout Diagram (0.8mm Lead Pitch/10.0 x 10.0mm Body Size)



## Part Number Description



## ispLSI 2064VE Ordering Information

### Conventional Packaging

#### COMMERCIAL

FAMILY	$f_{max}$ (MHz)	$t_{pd}$ (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	280	3.5	64	ispLSI 2064VE-280LT100	100-Pin TQFP
	280	3.5	64	ispLSI 2064VE-280LB100	100-Ball caBGA
	280	3.5	32	ispLSI 2064VE-280LT44	44-Pin TQFP
	200	4.5	64	ispLSI 2064VE-200LT100	100-Pin TQFP
	200	4.5	64	ispLSI 2064VE-200LB100	100-Ball caBGA
	200	4.5	32	ispLSI 2064VE-200LJ44	44-Pin PLCC
	200	4.5	32	ispLSI 2064VE-200LT44	44-Pin TQFP
	135	7.5	64	ispLSI 2064VE-135LT100	100-Pin TQFP
	135	7.5	64	ispLSI 2064VE-135LB100	100-Ball caBGA
	135	7.5	32	ispLSI 2064VE-135LJ44	44-Pin PLCC
	135	7.5	32	ispLSI 2064VE-135LT44	44-Pin TQFP
	100	10	64	ispLSI 2064VE-100LT100	100-Pin TQFP
	100	10	64	ispLSI 2064VE-100LB100	100-Ball caBGA
	100	10	32	ispLSI 2064VE-100LJ44	44-Pin PLCC
100	10	32	ispLSI 2064VE-100LT44	44-Pin TQFP	

Table 2-0041A/2064VE

#### INDUSTRIAL

FAMILY	$f_{max}$ (MHz)	$t_{pd}$ (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	135	7.5	64	ispLSI 2064VE-135LT100I	100-Pin TQFP
	135	7.5	32	ispLSI 2064VE-135LT44I	44-Pin TQFP

Table 2-0041B/2064VE

**ispLSI 2064VE Ordering Information (Cont.)**
**Lead-Free Packaging**
**COMMERCIAL**


FAMILY	fmax (MHz)	tpd (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	280	3.5	64	ispLSI 2064VE-280LTN100	Lead-Free 100-Pin TQFP
	280	3.5	32	ispLSI 2064VE-280LTN44	Lead-Free 44-Pin TQFP
	200	4.5	64	ispLSI 2064VE-200LTN100	Lead-Free 100-Pin TQFP
	200	4.5	32	ispLSI 2064VE-200LTN44	Lead-Free 44-Pin TQFP
	135	7.5	64	ispLSI 2064VE-135LTN100	Lead-Free 100-Pin TQFP
	135	7.5	32	ispLSI 2064VE-135LTN44	Lead-Free 44-Pin TQFP
	100	10	64	ispLSI 2064VE-100LTN100	Lead-Free 100-Pin TQFP
	100	10	32	ispLSI 2064VE-100LTN44	Lead-Free 44-Pin TQFP

**INDUSTRIAL**

FAMILY	fmax (MHz)	tpd (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	135	7.5	64	ispLSI 2064VE-135LTN100I	Lead-Free 100-Pin TQFP
	135	7.5	32	ispLSI 2064VE-135LTN44I	Lead-Free 44-Pin TQFP

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View ISPLSI2064VE-100LT44 on WIN SOURCE](#)
-  [Lattice Semiconductor Corporation](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management