SILICON LABS

SiBG301 Wireless SoC Family Data Sheet

KEY FEATURES

- Optimized for LED lighting applications
- 32-bit ARM M33® core with 150 MHz maximum operating frequency
- Up to 4 MB of flash and 512 KB of RAM
- High-performance radio with up to +10 dBm output power
- Secure Vault™ High
- LED pre-driver
- PIXELRZ interface
- Enhanced PWM

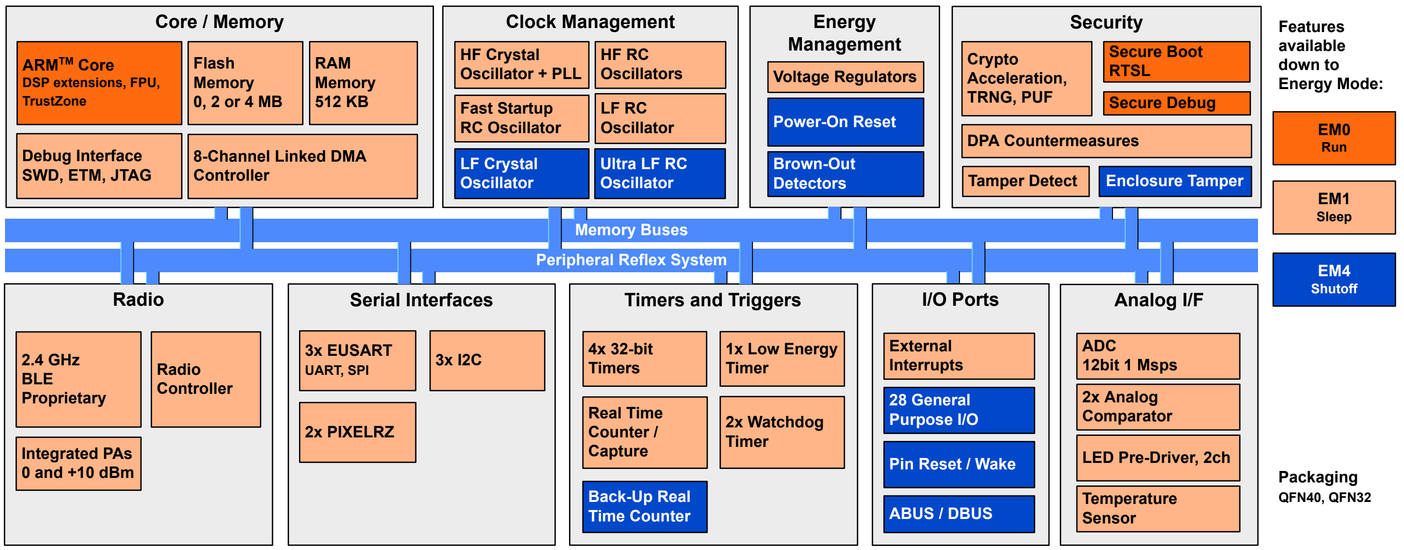
The SiBG301 SoC family of wireless SoCs supports Bluetooth, Bluetooth mesh, and Proprietary 2.4 GHz applications.

The SiBG301 is the next generation Series 3 platform that further extends our leadership in ultra-low power IoT SoCs and modules by enabling the security, compute, RF performance, power efficiency, and low cost required to tap into emerging IoT markets. The multi-core device has an ARM Cortex®-M33 running up to 150 MHz and dedicated cores for the radio and security engine. Our Secure Vault™ High is PSA level 4 certified and helps to protect both the data and the device, while up to 4 MB flash and 512 KB RAM allow for more demanding applications while leaving room for future growth.

Optimized for LED lighting applications, SiBG301 devices integrate key features including an enhanced PWM for improved LED dimming and control, a PIXELRZ single wire communication interface for LED controller ICs, and an LED pre-driver on select devices, eliminating the need for an LED driver, reducing the BOM, and lowering product cost.

Target applications include the following:

- Smart Lighting - LED Bulbs, LED Fixtures, Luminaires
- Smart Home - Smart Plugs, Switches
- Building Automation - Smart Plugs, Switches



1. Feature List

The SiBG301 highlighted features are listed below.

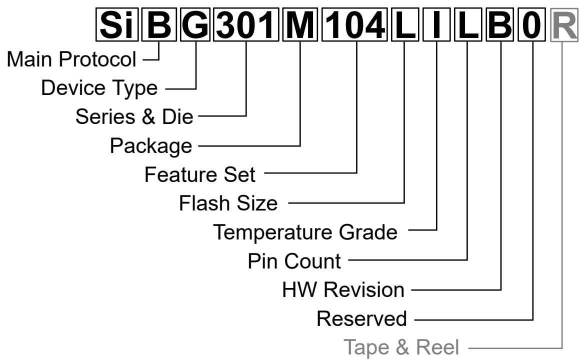
- **Compute**
  - High-performance 32-bit 150 MHz ARM Cortex-M33® Core with DSP instruction and floating-point unit for efficient signal processing
  - Up to 4 MB co-packaged flash program memory or external QSPI memory interface with run-time authentication and encryption
  - Up to 512 KB RAM data memory
- **Radio**
  - 2.4 GHz radio operation
  - -106.8 dBm sensitivity @ 125 kbps GFSK
  - -98.6 dBm sensitivity @ 1 Mbps GFSK
  - -95.7 dBm sensitivity @ 2 Mbps GFSK
  - TX power up to 10 dBm
- **Protocol Support**
  - Bluetooth Low Energy
  - Bluetooth Mesh
  - Proprietary 2.4 GHz
  - Multiprotocol (Bluetooth + Proprietary)
- **Supported Modulation Formats**
  - 2 (G)FSK with fully configurable shaping
  - OQPSK DSSS
  - (G)MSK
- **Secure Vault™ High**
  - Hardware Cryptographic Acceleration for AES128/192/256, SHA-1, SHA-2/256/384/512, ECDSA+ECDH(P-192, P-256), Ed25519 and Curve25519, J-PAKE, PBKDF2, SPAKE2+
  - True Random Number Generator (TRNG)
  - ARM® TrustZone®
  - Secure Boot (Root of Trust Secure Loader)
  - Secure Debug Lock/Unlock
  - DPA Countermeasures
  - Secure Key Management with PUF
  - Anti-Tamper
  - Secure Attestation
  - DFA Detection
  - Authenticated XiP (AXiP)
- **Low-Power Peripherals**
  - 12-bit, 1 Msps Analog to Digital Converter (ADC)
  - 2 × Analog Comparator (ACMP)
  - Up to 28 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller (LDMA)
  - 16 Channel Peripheral Reflex System (PRS)
  - 2 × 7-channel, 32-bit Timer/Counter with Compare, Capture, and Enhanced PWM capabilities
  - 2 × 3-channel, 32-bit Timer/Counter with Compare, Capture, and Enhanced PWM capabilities
  - 2 × 32-bit Real Time Counter (SYSRTC/BURTC)
  - 24-bit Low Energy Timer for waveform generation (LETIMER)
  - 16-bit Pulse Counter with asynchronous operation (PCNT)
  - 2 × Watchdog Timer (WDOG)
  - 3 × Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART) supporting UART/SPI/DALI/IrDA/SmartCard
  - 3 × I^2C interface with SMBus support
  - High-Frequency Crystal Oscillator (HFXO)
  - High-Frequency RC Oscillator (HFRCO)
  - Low-Frequency 32.768 kHz RC Oscillator (LFRCO)
  - Low-Frequency 32.768 kHz Crystal Oscillator (LFXO)
  - 2-channel LED Pre-driver (LEDDRV)
  - 2 × Serial Pixel Interface (PIXELRZ)
  - Die temperature sensor
- **Low Power Consumption**
  - 7.8 mA RX current (1 Mbps 2GFSK, EM1 @ 38.4 MHz)
  - 11.1 mA TX current @ 0 dBm output power (EM1 @ 38.4 MHz)
  - 28.2 mA TX current @ 10 dBm output power (EM1 @ 38.4 MHz)
  - 47 μA/MHz in Active Mode EM0 at 150 MHz
- **Operating Conditions**
  - 1.8 to 3.63 V single power supply
  - -40 to 125 °C
- **Packages**
  - **QFN32** 4 × 4 × 0.85 mm
  - **QFN40** 5 × 5 × 0.85 mm

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Flash (KB)	RAM (KB)	GPIO	Package / Pinout	Temp Range
SiBG301M114KIHB0	Bluetooth LE	2048	512	17	QFN32 with LED Pre-Drive	-40 to 125 °C
SiBG301M114KGHB0	Bluetooth LE	2048	512	17	QFN32 with LED Pre-Drive	-40 to 85 °C
SiBG301M104XILB0	Bluetooth LE	External	512	22	QFN40 with External Flash	-40 to 125 °C
SiBG301M104LILB0	Bluetooth LE	4096	512	28	QFN40 Max GPIO	-40 to 125 °C
SiBG301M104LIHB0	Bluetooth LE	4096	512	20	QFN32 Max GPIO	-40 to 125 °C
SiBG301M104LGLB0	Bluetooth LE	4096	512	28	QFN40 Max GPIO	-40 to 85 °C
SiBG301M104LGHB0	Bluetooth LE	4096	512	20	QFN32 Max GPIO	-40 to 85 °C

Note:
- 192 KB of flash is reserved for Secure Engine firmware.
- If AXiP feature is used, 11.1% of code space (4 KB of every 36 KB) is reserved for runtime authentication.



Field	Options
Main Protocol	• **M**: 802.15.4, Zigbee, Thread
Device Type	• **G**: System-On-Chip

Series & Die [s1][s2][d1]	• s1, s2
	  • **30**: Series 30
	• d1
	  • **1**: Die Code 1

Package	• **M**: QFN

Feature Set [f1][f2][f3]	• f1
	  • **1**: Reserved
	• f2
	  • **0**: No LED Pre-Driver
	  • **1**: LED Pre-Driver Available
	• f3
	  • **3**: 384 KB RAM
	  • **4**: 512 KB RAM

Flash Size	• **X**: No Flash • **K**: 2 MB Co-Packaged Flash • **L**: 4 MB Co-Packaged Flash
Temperature Grade	• **G**: -40 to +85 °C • **I**: -40 to +125 °C
Pin Count	• **H**: 32 pins • **L**: 40 pins
Hardware Revision	• **B**: Revision B
Reserved	• **0**: Reserved
Tape & Reel	• **R**: Tape & Reel (optional)

Figure 2.1. Ordering Code Key

Table of Contents

3. System Overview

3.1 Introduction

The SiBG301 family of devices combines a powerful MCU core with a high-performance radio transceiver and Secure Vault™ hardware. The devices are well suited for secure connected IoT multiprotocol devices requiring high performance and large memory footprints. This section gives a short introduction to the radio and MCU system. More detailed functional descriptions can be found in the product reference manual.

A block diagram of the SiBG301 family is shown in the figure below. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult 2. Ordering Information.

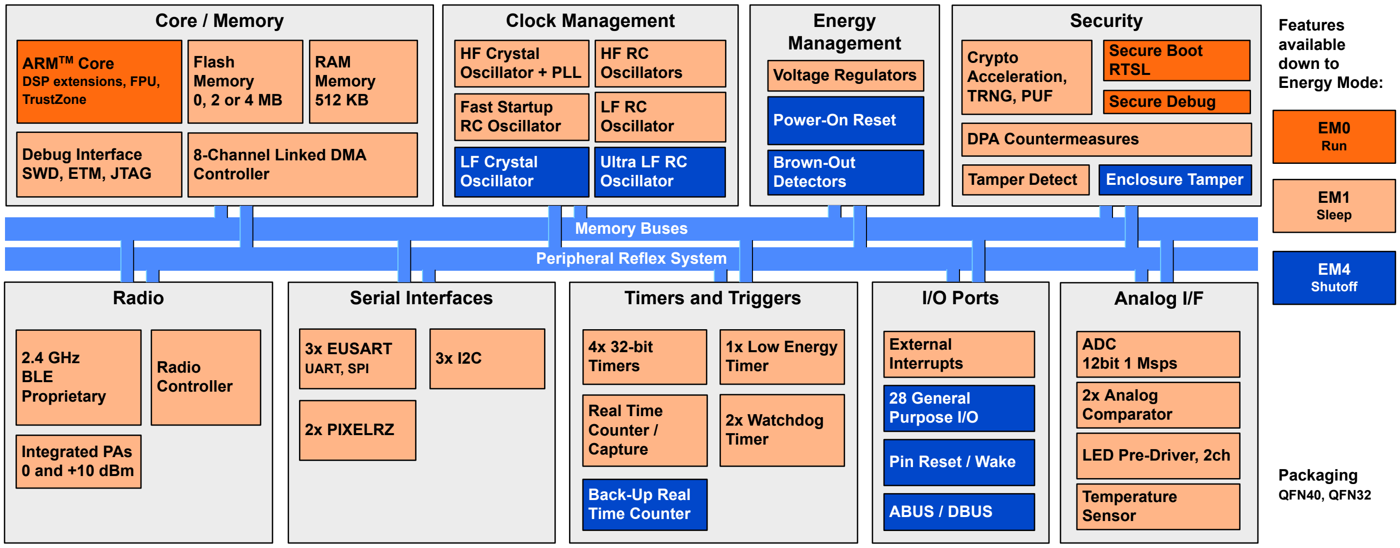


Figure 3.1. SiBG301 Block Diagram

3.2 Processor Core and Memory

The host processor is an ARM Cortex-M33® integrating the following features in the system:

- ARM RISC processor
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 4096 KB co-packaged flash program memory
- Two-level cache:
  - 16 KB L1 cache
  - 64 KB L2 cache
- Up to 512 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.2.1 External Memory Interface (EXTMEM)

The SiBG301 interfaces to 1.8 V external flash memory through a high-speed quad SPI interface (QSPI) with dedicated encryption, decryption, and authentication hardware. An L2CACHE holds cached read data for efficient access. Devices are available with or without co-packaged flash memory. An integrated LDO powers the flash at 1.8 V, removing the need for a second external supply in 3.3 V applications. The dedicated flash PLL (FLPLL) is used to optimize QSPI interface timing.

Flash memory contents are managed by the SE and the external memory hardware to provide robust security for program memory. The user can partition the flash memory into code and non-volatile data storage segments according to the needs of the application. Devices reserve 192 KB of the attached flash to store the upgradeable portion of SE firmware.

Code partitions can be stored using three different methods: unencrypted, encrypted, or authenticated and encrypted. When storing a code partition as authenticated, a portion of the flash memory is reserved to store authentication data (4 KB of authentication data for every 32 KB of code). The memory interface hardware manages addressing, decryption, and authentication.

The interface hardware supports eXecute-in-Place (XiP) for all code regions. Encrypted eXecute-in-Place (EXiP) decrypts the read data and does not incur any additional performance impact compared to XiP of unencrypted code. Authenticated eXecute-in-Place (AXiP) authenticates and decrypts the read data, while incurring only a small performance impact due to reading the additional authentication data.

3.2.2 Linked Direct Memory Access Controller (LDMA)

The LDMA controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.2.3 Memory Map

The accessible address space for the host processor is shown in Table 3.1 Host Core Address Map on page 11. Each region is aliased to both a secure and a non-secure address range to enable TrustZone functionality.

Table 3.1. Host Core Address Map

Non-Secure Address Range	Secure Address Range	Region
0x00800000 - 0x0087FFFFF	0x10800000 - 0x1087FFFFF	DMEM (CODE Bus)[1, 2]
0x01000000 - 0x04FFFFFF	0x11000000 - 0x14FFFFFF	EXTMEM (CODE Bus)[1, 3]
0x0FE00000 - 0x0FE0BFFF	0x1FE00000 - 0x1FE0BFFF[4]	DEVINFO[4]
0x20000000 - 0x2007FFFF	0x30000000 - 0x3007FFFF	DMEM (SYSTEM Bus)[2]
0x40000000 - 0x403FFFFF	0x50000000 - 0x503FFFFF	APBLF Peripherals
0x40800000 - 0x40BFFFFF	0x50800000 - 0x50BFFFFF	APBHF Peripherals
0x41000000 - 0x413FFFFF	0x51000000 - 0x513FFFFF	APBUHF Peripherals
0x41C00000 - 0x41FFFFFF	0x51C00000 - 0x51FFFFFF	KSU
0x42800000 - 0x42BFFFFF	0x52800000 - 0x52BFFFFF	SEMAILBOX
0x61000000 - 0x67FFFFFF	0x71000000 - 0x77FFFFFF	EXTMEM (SYSTEM Bus)[3]
0xA0000000 - 0xA03FFFFF	0xB0000000 - 0xxB03FFFFF	LPW0 Radio
0xA3000000 - 0xA307FFFF	0xB3000000 - 0xB307FFFF	APBSYSMB Peripherals

Note:
1. DMEM and EXTMEM have separate aliased regions on the CODE and SYSTEM buses. Addresses 0x00000000 to 0x1FFFFFFF are accessed using the CODE bus, and addresses 0x20000000 and above are accessed using the SYSTEM bus. All regions are cachable by default, but can be declared non-cacheable using the MPU.
2. DMEM CODE regions allow for optimized instruction execution from DMEM, while the host data interface targets the DMEM SYSTEM region for stack and variable storage.
3. Flash memory partitions designated as code space should target the CODE region. Flash memory partitions designated as non-volatile data storage may target the EXTMEM SYSTEM data region.
4. The DEVINFO region is always non-secure access in both aliased locations.

3.3 Radio

The SiBG301 wireless SoC family features a highly configurable radio transceiver supporting Bluetooth Low Energy, Bluetooth Mesh, and proprietary 2.4 GHz wireless protocols.

3.3.1 Antenna Interface

The 2.4 GHz antenna interface consists of a single-ended pin (RF2G4_IO). The external components for the antenna interface in typical applications are shown in the RF Matching Networks section.

3.3.2 Fractional-N Frequency Synthesizer

The SiBG301 contains a high-performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency for the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance, frequency resolution better than 100 Hz, and low energy consumption. The synthesizer's fast frequency settling allows for very short receiver and transmitter wake up times to reduce system energy consumption.

3.3.3 Receiver Architecture

The SiBG301 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high-quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, level-based proximity detection, and RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame, and the dynamic RSSI measurement can be monitored throughout reception.

3.3.4 Transmitter Architecture

The SiBG301 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or LBT algorithms can be automatically timed by the SiBG301. These algorithms are typically defined by regulatory standards to improve interoperability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.3.5 Packet and State Trace

The SiBG301 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data, and state information
- Data observability on a single-pin UART data output or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data, and state / meta information in a single serial data stream

3.3.6 Data Buffering

The SiBG301 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 to 4096 bytes. Each buffer can be used for RX, TX, or both. The buffer data is located in RAM, enabling zero-copy operations.

3.3.7 Radio Controller (RAC)

The RAC controls the top level state of the radio subsystem in the SiBG301. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter, and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.3.8 RF Signal Identifier

When an IoT radio is placed next to a high duty-cycle co-located Wi-Fi radio transmission, IoT radios are blocked from receiving weak signals. The RF Signal Identifier feature available on SiBG301 devices enables the IoT radio to detect partial 802.15.4 or BLE/BT Mesh packets. When a partial packet is detected, the IoT radio can communicate this information to the corresponding Wi-Fi device (through serial interface or GPIO asserts), which can consequently halt transmission while the IoT radio waits for a packet retry to be received. This helps provide a higher success rate of receiving packets from other devices on the network when co-located with an interfering Wi-Fi radio.

3.4 Energy Management Unit (EMU)

The EMU manages transitions of energy modes, controls integrated regulators and individual peripheral power domains, and handles reset sequencing for the device. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.4.1 Energy Modes

The SiBG301 supports three main energy modes. Within each mode there are other options such as clock and peripheral power gating that can reduce the energy consumption of the device according to the application's needs.

- EM0 is the active mode of the system. The host processor is powered up and capable of code executing code. All peripherals and oscillator sources are available in EM0.
- EM1 is the sleep mode for the system. The host processor is inactive and not executing code, but can be activated very quickly upon detection of a system event. All peripherals are available in EM1.
- EM4 is a deep power down mode. Most of the device is powered off in EM4, and waking from this mode is similar to a device reset. A small number of low-energy peripherals can remain active and GPIO state retention is supported in EM4.

3.4.2 Power Domains

The SiXG301 device family has three primary power domains (PD0, PD1, and PDHV). Each power domain may be subdivided into smaller subdomains (for example, PD0A, PD0B, and so on). Power domains are managed automatically by the EMU.

The lowest-energy power domain is the "high-voltage" power domain (PDHV), which supports extremely low-energy infrastructure and peripherals. Circuits powered from PDHV are always on and available in all energy modes down to EM4.

Devices also support the active power domain (PD1) and a low-energy power domain (PD0). PD1 and PD0 power most of the device circuitry, including the CPU core and all peripherals not on PDHV. PD1 and PD0 are always powered on in EM0 and EM1. PD1 and PD0 are always shut down in EM4.

Table 3.2 PDHV Peripheral Power Subdomain on page 13 shows the peripherals on the PDHV domain. Any peripheral not listed is on PD1 or PD0.

Table 3.2. PDHV Peripheral Power Subdomain

Always On in EM4
PDHV
LFRCO (Non-precision mode)
LFXO
BURTC
ULFRCO
ETAMPDET
BURAM

3.5 Clock Management Unit (CMU)

The CMU controls oscillators and clocks in the SiBG301. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.1 Internal and External Oscillators

The SiBG301 includes a number of oscillator options for clocking different portions of the system.

- HFXO is a high-frequency crystal oscillator with integrated load capacitors, tunable in small steps. It provides a precise timing reference for the MCU and RF synthesizer. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.
- HFRCO0 / HFRCODPLL is an integrated high-frequency RC oscillator operating up to 100 MHz. HFRCO0 employs fast startup at minimal energy consumption combined with a wide frequency range and good open-loop accuracy. For higher precision, the DPLL function can be used to generate frequencies from 16 to 100 MHz using HFXO or LFXO as a reference.
- SOCPLL is a high-frequency PLL supporting the maximum operating frequency of the MCU core.
- FLPLL is a high-frequency PLL which provides a high speed clock to the QSPI memory interface.
- HFRCO1 / HFRCOEM23 is a second high-frequency RC oscillator available as a peripheral timing resource with good accuracy. It supports fast startup and operates in energy modes other than EM4 to enable duty-cycled operation of peripherals like the ADC. It can be calibrated against other clock sources in the device to increase accuracy.
- FSRCO is an integrated fast startup RC oscillator that runs at a nominal 20 MHz and consumes very little energy. It is used primarily for system housekeeping tasks, but is also available as a peripheral timing reference when high accuracy is not needed.
- LFXO is a 32.768 kHz crystal oscillator providing an accurate timing reference for low power operation.
- LFRCO is an integrated low frequency 32.768 kHz RC oscillator for low power operation. A precision mode is available to improve the oscillator frequency tolerance, eliminating the need for a low-frequency crystal in some applications.
- ULFRCO is an integrated ultra-low frequency 1 kHz RC oscillator. It is used by the system to perform periodic housekeeping tasks and is available as a peripheral timing reference for certain low-energy peripherals.

3.6 General Purpose Input/Output (GPIO)

SiBG301 has up to 28 GPIO pins. Each GPIO pin can be individually configured as digital output or input, or connected to analog signals. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for these pins.

Peripheral connections to GPIO have either a direct connection to a specific pin or they can be muxed to a variety of pins using the digital bus (DBUS) and analog bus (ABUS) muxes. Direct connections are detailed in the Alternate Function Table. Muxable digital and analog connections are detailed in the DBUS Routing Table and the ABUS Routing Table, respectively.

Certain GPIOs can also act as an external wake source from EM4. These pins will include an alternate function named GPIO.EM4WU in the Alternate Function Table section.

3.7 Timers and Triggers

3.7.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 32-bit counter with up to 7 compare/capture channels. Each channel is configurable in one of three modes:

- In capture mode, the counter state is stored in a buffer at a selected input event.
- In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value.
- In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers.

Complementary outputs with dead-time insertion are available on select output channels.

See 3.11 Configuration Summary for information on the feature set of each timer.

3.7.2 Low Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is clocked from low-frequency clock sources and has two compare output channels. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the PRS and can be configured to start counting on compare matches from other peripherals such as the RTCs.

3.7.3 Pulse Counter (PCNT)

The PCNT peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from several of the internal oscillators.

3.7.4 System Real Time Clock with Capture (SYSRTC)

The SYSRTC is a 32-bit counter that provides accurate timekeeping in all energy modes other than EM4. The SYSRTC can be clocked by any of the on-board, low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

3.7.5 Back-Up Real Time Counter (BURTC)

The BURTC is a 32-bit counter that provides timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board, low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

3.7.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the PRS.

3.7.7 Peripheral Reflex System (PRS)

The PRS provides several channels of hardware interconnect logic that can be configured to communicate between different peripheral modules. The PRS saves power and reduces latency for critical timing functions by allowing peripherals to interact autonomously with each other without software intervention. At the basic level, PRS routes a signal from one peripheral (a producer) to another peripheral (a consumer), allowing the consumer to quickly perform actions in response to the producer event. Edge triggers and simple glue logic operations (AND, OR, NOT) can be applied to one or more PRS channels.

3.8 Communications and other Digital Peripherals

3.8.1 Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)

The EUSART supports full duplex asynchronous UART communication with hardware flow control, RS-485, and IrDA support. The EUSART also supports high-speed SPI. In EM0 and EM1, the EUSART provides a high-speed, buffered communication interface.

3.8.2 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode, fast-mode, and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low energy modes.

3.8.3 Serial Pixel Interface (PIXELRZ)

The PIXELRZ interface is a single-wire asynchronous communications interface for individually addressable LED light controllers using an RZ bit stream. High and low times for all symbols are programmable, allowing PIXELRZ to communicate with a wide variety of LED controller chips. The LDMA interface and flexible options allow PIXELRZ to autonomously send full frames to 512 pixels without processor intervention.

3.8.4 Symmetric Cryptographic Accelerator (SYMCRYPTO)

The SYMCRYPTO hardware is an autonomous hardware accelerator that can be used directly by the host processor. SYMCRYPTO includes Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys for public key operations and hashes.

Supported block cipher modes of operation for AES include:
- Electronic Code Book (ECB)
- Counter Mode (CTR)
- Cipher Block Chaining (CBC)
- Cipher Feedback (CFB)
- Galois Counter Mode (GCM)
- Counter with CBC-MAC (CCM)
- Cipher Block Chaining Message Authentication Code (CBC-MAC)
- Galois Message Authentication Code (GMAC)

Supported hashes include SHA-1 and SHA-2/256/384/512.

Note: AES_ECB, AES_CBC, AES_CBCMAC, and SHA-1 are provided for legacy compatibility and are not recommended for cryptographic purposes without thoroughly understanding their potential security weaknesses.

3.9 Analog Peripherals

3.9.1 Analog to Digital Converter (ADC)

The ADC is a 12-bit, 1 Msps Successive Approximation Register (SAR) converter. The channel scan hardware and FIFO with DMA support allow for a mix of single-ended and differential inputs to be converted back-to-back without processor intervention. An integrated hardware accumulator can collect multiple samples and simplify averaging operations to reduce system-level noise. Reference options include an internal calibrated reference, external pin, and the supply voltage.

3.9.2 Analog Comparator (ACMP)

The ACMP is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The trade off between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 LED Pre-Driver (LEDDRV)

The LEDDRV block is designed to provide a power-efficient solution in single-color and tunable white LED bulb applications. It integrates a charge pump and two channels of gate drivers to directly drive power MOSFET gates and replace dedicated driver chips to control a warm white and cool white LED string. The LEDDRV peripheral monitors the AC mains supply to allow for in-system calibration. Current monitoring and over-current protection are provided for both channels, as well as drain voltage sensing to optimize the output timing. The processor interfaces to the block using two PWM channels generated from TIMER blocks to control dimming and mixing between the two channels.

3.9.4 Temperature Sensor

An accurate temperature sensor provides readings once every 250 ms. On-demand outputs with hardware averaging are also supported. Output compare circuitry allows the temperature sensor to interrupt the processor when above or below the configurable set points.

3.10 Secure Vault

A dedicated hardware secure engine containing its own CPU enables the Secure Vault functions. It isolates cryptographic functions and data from the host Cortex-M33 core and provides several additional security features. The SiBG301 family includes the Secure Vault features summarized in the following table.

Table 3.3. Secure Vault Features

Feature	Details
Authenticated Execute-in-Place (AXiP)	Yes
Encrypted Execute-in-Place (EXiP)	Yes
True Random Number Generator (TRNG)	Yes
Secure Boot with Root of Trust and Secure Loader (RTSL)	Yes, when using AXiP
Secure Debug with Lock/Unlock	Yes
DPA and DFA Countermeasures	Yes
Anti-Tamper	Yes
Secure Attestation	Yes
Secure Key Management	Yes
Symmetric Encryption	• AES 128 / 192 / 256 bit • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, GMAC, and OFB
Public Key Encryption - ECDSA / ECDH / EdDSA	• p192 and p256 • Curve25519 (ECDH) • Ed25519 (EdDSA)
Key Derivation	• ECJ-PAKE p192 and p256 • PBKDF2 • HKDF
Hashes	• SHA-1 • SHA-2/256/384/512 • AES-MMO

3.10.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins with an immutable memory (ROM).

It prevents malware injection and rollback, ensures that only authentic firmware is executed, and protects Over-The-Air (OTA) updates.

3.10.2 Cryptographic Accelerator

The Cryptographic Accelerator in Secure Vault is an autonomous hardware accelerator with DPA countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, and Elliptic Curve Cryptography (ECC) to support public key operations, and hashes.

Supported block cipher modes of operation for AES include:
- Electronic Code Book (ECB)
- Counter Mode (CTR)
- Cipher Block Chaining (CBC)
- Cipher Feedback (CFB)
- Galois Counter Mode (GCM)
- Counter with CBC-MAC (CCM)
- Cipher Block Chaining Message Authentication Code (CBC-MAC)
- Galois Message Authentication Code (GMAC)
- Output Feedback (OFB)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192 and P-256 for ECDH (Elliptic Curve Diffie-Hellman) key derivation, and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations. The non-NIST Curve25519 for ECDH and Ed25519 for EdDSA (Edwards-curve Digital Signature Algorithm) sign and verify operations are also supported.

Secure Vault also supports ECJ-PAKE (Elliptic Curve variant of Password Authenticated Key Exchange by Juggling), and PBKDF2 (Password-Based Key Derivation Function 2).

Supported hashes include SHA-1, SHA-2/256/384/512, and HMAC-AES-MMO.

This implementation provides a fast and energy-efficient solution to state of the art cryptographic needs.

3.10.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes startup health tests for the entropy source as required by NIST SP800-90B and AIS-31, as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.10.4 Secure Debug with Lock/Unlock

For security reasons, it is critical for a product to have its debug interface locked before being released in the field.

Secure Vault also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

For more information about this feature, see AN1190: Series 2 Secure Debug.

3.10.5 Differential Power Analysis (DPA) Countermeasures

The AES and ECC accelerators have DPA countermeasure support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

3.10.6 Differential Fault Analysis (DFA) Countermeasures

The SE AES engine includes DFA countermeasures to detect and protect against fault injection attacks.

3.10.7 Secure Key Management with PUF

Key material in Secure Vault High products is protected by "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of protecting a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33, which includes off-chip storage as well. The symmetric key used for this wrapping and unwrapping must be highly secure because it can expose all other key materials in the system. The Secure Vault Key Management system uses a Physically Unclonable Function (PUF) to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

3.10.8 Key Slot Unit (KSU)

The KSU is a hardware block that allows the system to use securely stored keys in the high performance host AES and SHA engines without exposing them. The KSU also separates the process of key unwrapping from key usage, allowing faster access to keys. Either the host or radio processor can request a specific key to be unwrapped by the SE and stored in a certain key slot. The processor can then tell encryption hardware to use the key in that slot to perform an operation. The key material itself is protected and never accessible to the processor.

3.10.9 Anti-Tamper

Secure Vault High devices provide internal tamper protection which monitors parameters such as voltage, temperature, and electromagnetic pulses as well as detecting tampering of the security sub-system itself. Additionally, eight external configurable tamper pins support external tamper sources, such as enclosure tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all protected key materials un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

For more information about this feature, see AN1247: Anti-Tamper Protection Configuration and Use.

3.10.10 External Tamper Detection (ETAMPDET)

The ETAMPDET module enables detection of external tampering, such as unauthorized enclosure opening. ETAMPDET operates in all energy modes down to EM4. Up to two signals can be generated and monitored to identify external tamper events. When a tamper event occurs, an interrupt is generated to allow software to take system-appropriate actions. The tamper block within the SE can be configured to respond autonomously to an ETAMPDET event.

3.10.11 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory. This key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate, which is signed into a Silicon Labs CA chain and then programmed back into the chip into immutable OTP memory.

The secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

For more information about this feature, see AN1268: Authenticating Silicon Labs Devices Using Device Certificates.

3.11 Configuration Summary

The features of the SiBG301 are a subset of the feature set described in the device reference manual. The following table describes device-specific implementation of the features. Remaining modules support full configuration.

Table 3.4. Configuration Summary

Module	Configuration
TIMER0	32-bit, 3-channels + 3 DTI channels
TIMER1	32-bit, 3-channels + 3 DTI channels
TIMER2	32-bit, 7-channels + 3 DTI channels
TIMER3	32-bit, 7-channels + 3 DTI channels
EUSART0	HF clock: Full high-speed operation, all modes LF clock: UART operation, 9600 Baud
EUSART1	HF clock: Full high-speed operation, all modes
EUSART2	HF clock: Full high-speed operation, all modes

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and all supplies at 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific, external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Power Supply Pin Dependencies

Due to on-chip circuitry (e.g., diodes), some power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various supply pins are defined below. Exceeding the following constraints can result in damage to the device and/or increased current draw.

- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD
- DVDD ≥ FVDD
  - DVDD must meet the minimum and maximum input supply requirements of the flash regulator when used to power FVDD.
  - In applications where FVDD is powered from an external supply, it is recommended to tie FVDD and DVDD together.
- IOVDD can be powered independently from any other supply.
  - IOVDD must meet the minimum and maximum input supply requirements of the LEDDRV charge pump when used to power LEDVDD.
- AVDD can be powered independent from any other supply.

4.2 Absolute Maximum Ratings

Stresses greater than those listed in the following table may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage on DVDD, AVDD, IOVDD, RFVDD, PAVDD, or VREGVDD supply pins	V_{DDMAX}		-0.3	—	3.8	V
Voltage on FVDD pin	$V_{FVDDMAX}$		-0.3	—	2.05	V
Voltage on DECOUPLE pin	$V_{DECOUPLEMAX}$		-0.3	—	0.99	V
Storage temperature range	T_{STG}		-50	—	150	°C
Junction temperature	T_{JMAX}	-G grade	—	—	105	°C
		-I grade	—	—	125	°C
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1	V / µs
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.05	V
DC voltage on any GPIO pin	V_{GPIO}		-0.3	—	V_{IOVDD} + 0.3	V
DC voltage on quad spi interface pins	V_{QSPI}		-0.3	—	V_{FVDD} + 0.3	V
DC voltage on RESETn pin[1]	V_{RESETn}		-0.3	—	3.63	V
Input RF level on pin RF2G4_IO	$P_{RFMAX2G4}$		—	—	+10	dBm
Absolute voltage on RF pin RF2G4_IO	V_{MAX2G4}		-0.3	—	V_{PAVDD}	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per GPIO pin	I_{IOMAX}	Sink	—	—	20	mA
		Source	—	—	20	mA
Current for all GPIO pins	$I_{IOALLMAX}$	Sink	—	—	160	mA
		Source	—	—	160	mA

Note:

1. The RESETn pin has a pull-up device to the DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD.

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-G temperature grade [1]	-40	—	85	°C
		-I temperature grade [1]	-40	—	125	°C
DVDD supply voltage	V_{DVDD}		1.8	—	3.63	V
AVDD supply voltage	V_{AVDD}		1.8	—	3.63	V
IOVDD operating supply voltage	V_{IOVDD}		1.8	—	3.63	V
RFVDD operating supply voltage	V_{RFVDD}		1.8	—	3.63	V
PAVDD operating supply voltage	V_{PAVDD}		1.8	—	3.63	V
DECOUPLE output capacitor[2]	$C_{DECOUPLE}$		—	1	—	µF
Core clock (SYSCLK) frequency	f_{SYSCLK}		2	—	150	MHz
HCLK frequency	f_{HCLK}		2	—	150	MHz
PCLK frequency	f_{PCLK}		2	—	75	MHz
LSPCLK frequency	f_{LSPCLK}		1	—	37.5	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$		—	—	100	MHz
EM01 Group C clock frequency	$f_{EM01GRPCCLK}$		—	—	100	MHz
EM01 Group D clock frequency	$f_{EM01GRPDCLK}$		—	—	100	MHz
TRACECLKIN frequency	$f_{TRACECLKIN}$		—	—	100	MHz
TRACECLK frequency	$f_{TRACECLK}$		—	—	50	MHz
HCLKLPW frequency	$f_{HCLKLPW}$		1	—	40	MHz
External Clock Input	f_{CLKIN}		2	—	38	MHz
Exported Clock Output	f_{EXPCLK}		—	—	50	MHz

Note:

1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. $T_A = T_{JMAX} - (THETA_{JA} \times PowerDissipation)$. Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and $THETA_{JA}$.
2. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.

4.4 Thermal Characteristics

Table 4.3. Thermal Characteristics

Package	Board	Parameter	Symbol	Test Condition	Value	Unit
40QFN (5x5mm), co-packaged flash	JEDEC - High Thermal Cond. (2s2p)[1]	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	26.4	°C/W
		Thermal Resistance, Junction to Board	Θ_{JB}		4.3	°C/W
		Thermal Resistance, Junction to Top Center	Ψ_{JT}		0.6	°C/W
		Thermal Resistance, Junction to Board	Ψ_{JB}		20.2	°C/W
40QFN (5x5mm), external flash	JEDEC - High Thermal Cond. (2s2p)[2]	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	25.4	°C/W
		Thermal Resistance, Junction to Board	Θ_{JB}		4.8	°C/W
		Thermal Resistance, Junction to Top Center	Ψ_{JT}		0.35	°C/W
		Thermal Resistance, Junction to Board	Ψ_{JB}		4.2	°C/W
32QFN (4x4mm), co-packaged flash	JEDEC - High Thermal Cond. (2s2p)[3]	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	41.3	°C/W
		Thermal Resistance, Junction to Board	Θ_{JB}		4.8	°C/W
		Thermal Resistance, Junction to Top Center	Ψ_{JT}		1.0	°C/W
		Thermal Resistance, Junction to Board	Ψ_{JB}		19.8	°C/W

Note:

1. Based on 4-layer PCB with dimension 3 x 4.5", PCB thickness of 1.6 mm, per JEDEC. PCB Center Land with 16 via to top internal plane of PCB.
2. Based on 4-layer PCB with dimension 3 x 4.5", PCB thickness of 1.6 mm, per JEDEC. PCB Center Land with 9 via to top internal plane of PCB.
3. Based on 4-layer PCB with dimension 3 x 4.5", PCB thickness of 1.6 mm, per JEDEC. PCB Center Land with 4 via to top internal plane of PCB.

4.5 Current Consumption

4.5.1 MCU Current Consumption at 3.0 V Supply (QSPI at 20 MHz)

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- QSPI is clocked at 20 MHz from FSRCO
- Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.4. MCU Current Consumption at 3.0 V Supply (QSPI at 20 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode, execution from cache, peripherals disabled	I_{EM0_CACHE}	150 MHz SOCPLL, referenced to HFXO with 38.4 MHz crystal, running CoreMark	—	62	—	µA/MHz
		150 MHz SOCPLL, referenced to HFXO with 38.4 MHz crystal, running while loop	—	47	—	µA/MHz
		145 MHz SOCPLL in open-loop mode, running CoreMark	—	61	—	µA/MHz
		145 MHz SOCPLL in open-loop mode, running while loop	—	46	—	µA/MHz
		100 MHz HFRCO, running CoreMark	—	62	—	µA/MHz
		100 MHz HFRCO, running while loop	—	46	TBD	µA/MHz
		38.4 MHz HFXO, running CoreMark	—	93	—	µA/MHz
		38.4 MHz HFXO, running while loop	—	76	—	µA/MHz
		38 MHz HFRCO, running while loop	—	67	—	µA/MHz
Current consumption in EM1 mode, peripherals disabled	I_{EM1}	150 MHz SOCPLL, referenced to HFXO with 38.4 MHz crystal	—	33	—	µA/MHz
		145 MHz SOCPLL in open-loop mode	—	31	—	µA/MHz
		100 MHz HFRCO	—	31	TBD	µA/MHz
		38.4 MHz HFXO	—	61	—	µA/MHz
		38 MHz HFRCO	—	53	—	µA/MHz
Current consumption in EM1 mode with HCLK divided by 16, peripherals disabled	I_{EM1_DIV16}	38.4 MHz HFXO, HCLK = 2.4 MHz	—	1843	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.26	TBD	µA
		With BURTC running from 32.768 kHz LF oscillator	—	0.75	—	µA

4.5.2 MCU Current Consumption at 3.0 V Supply (QSPI at 104 MHz)

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- QSPI is clocked at 104 MHz from FLPLL

Table 4.5. MCU Current Consumption at 3.0 V Supply (QSPI at 104 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode, execution from cache, peripherals disabled	I_{EM0_CACHE}	150 MHz SOCPLL, referenced to HFXO with 38.4 MHz crystal, running CoreMark	—	72	—	µA/MHz
		150 MHz SOCPLL, referenced to HFXO with 38.4 MHz crystal, running while loop	—	57	—	µA/MHz
		145 MHz SOCPLL in open-loop mode, running CoreMark	—	71	—	µA/MHz
		145 MHz SOCPLL in open-loop mode, running while loop	—	56	—	µA/MHz
		100 MHz HFRCO, running CoreMark	—	82	—	µA/MHz
		100 MHz HFRCO, running while loop	—	66	—	µA/MHz
		38.4 MHz HFXO, running CoreMark	—	133	—	µA/MHz
		38.4 MHz HFXO, running while loop	—	117	—	µA/MHz
		38 MHz HFRCO, running while loop	—	120	—	µA/MHz
Current consumption in EM1 mode, peripherals disabled	I_{EM1}	150 MHz SOCPLL, referenced to HFXO with 38.4 MHz crystal	—	43	—	µA/MHz
		145 MHz SOCPLL in open-loop mode	—	42	—	µA/MHz
		100 MHz HFRCO	—	51	—	µA/MHz
		38.4 MHz HFXO	—	102	—	µA/MHz
		38 MHz HFRCO	—	106	—	µA/MHz
Current consumption in EM1 mode with HCLK divided by 16, peripherals disabled	I_{EM1_DIV16}	38.4 MHz HFXO, HCLK = 2.4 MHz	—	3406	—	µA

4.5.3 MCU Current Consumption at 3.0 V Supply (QSPI at 133 MHz)

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- QSPI is clocked at 133 MHz from FLPLL
- Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.6. MCU Current Consumption at 3.0 V Supply (QSPI at 133 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode, execution from cache, peripherals disabled	I_{EM0_CACHE}	150 MHz SOCPLL, referenced to HFXO with 38.4 MHz crystal, running CoreMark	—	71	—	µA/MHz
		150 MHz SOCPLL, referenced to HFXO with 38.4 MHz crystal, running while loop	—	58	—	µA/MHz
		145 MHz SOCPLL in open-loop mode, running CoreMark	—	70	—	µA/MHz
		145 MHz SOCPLL in open-loop mode, running while loop	—	57	—	µA/MHz
		100 MHz HFRCO, running CoreMark	—	81	—	µA/MHz
		100 MHz HFRCO, running while loop	—	67	—	µA/MHz
		38.4 MHz HFXO, running CoreMark	—	133	—	µA/MHz
		38.4 MHz HFXO, running while loop	—	119	—	µA/MHz
		38 MHz HFRCO, running while loop	—	123	—	µA/MHz
Current consumption in EM1 mode, peripherals disabled	I_{EM1}	150 MHz SOCPLL, referenced to HFXO with 38.4 MHz crystal	—	42	—	µA/MHz
		145 MHz SOCPLL in open-loop mode	—	42	—	µA/MHz
		100 MHz HFRCO	—	51	—	µA/MHz
		38.4 MHz HFXO	—	103	—	µA/MHz
		38 MHz HFRCO	—	107	—	µA/MHz
Current consumption in EM1 mode with HCLK divided by 16, peripherals disabled	I_{EM1_DIV16}	38.4 MHz HFXO, HCLK = 2.4 MHz	—	3458	—	µA

4.5.4 Radio Operational Supply Current at 3.0 V Supply (QSPI at 20 MHz)

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz, SYSCLK = 38.4 MHz.
- QSPI is clocked at 20 MHz from FSRCO

Table 4.7. Radio Operational Supply Current at 3.0 V Supply (QSPI at 20 MHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 2.4 MHz	—	7.7	—	mA
		500 kbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 2.4 MHz	—	8.3	—	mA
		1 Mbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 2.4 MHz	—	7.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 2.4 MHz	—	8.1	—	mA
		125 kbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 38.4 MHz	—	8.4	—	mA
		500 kbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 38.4 MHz	—	9.0	—	mA
		1 Mbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 38.4 MHz	—	7.8	—	mA
		2 Mbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 38.4 MHz	—	8.8	—	mA
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 2.4 MHz	—	7.8	—	mA
		500 kbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 2.4 MHz	—	7.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 2.4 MHz	—	7.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 2.4 MHz	—	8.1	—	mA
		125 kbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 38.4 MHz	—	8.4	—	mA
		500 kbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 38.4 MHz	—	8.4	—	mA
		1 Mbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 38.4 MHz	—	7.8	—	mA
		2 Mbit/s, 2GFSK, f = 2.44 GHz, EM1, HCLK = 38.4 MHz	—	8.8	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode	I_{TX}	f = 2.44 GHz, CW, 0 dBm PA, $P_{OUT<}$ = 0 dBm, EM1, HCLK = 38.4 MHz	—	11.1	—	mA
		f = 2.44 GHz, CW, 10 dBm PA, $P_{OUT<}$ = 0 dBm, EM1, HCLK = 38.4 MHz	—	14.4	—	mA
		f = 2.44 GHz, CW, 10 dBm PA, $P_{OUT<}$ = 10 dBm, EM1, HCLK = 38.4 MHz	—	28.2	—	mA

4.6 Flash Interface and Support

4.6.1 Flash regulator (FLREG)

Table 4.8. Flash regulator (FLREG)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash regulator input supply range	V_{DVDD_REG}	Flash regulator supplied from DVDD	1.92	—	3.6	V
Flash regulator output voltage	V_{FVDD_OUT}	On-chip flash regulator used, output voltage when enabled. $I_{OUT} \leq$ 40 mA.	1.7	1.81	1.87	V
Flash regulator output load current	I_{OUT}		—	—	40	mA
Flash regulator quiescent current	I_{FLREG}		—	12.6	—	μA
Flash regulator startup time	t_{FLREG_START}		—	268	TBD	μs
FVDD external supply range	V_{FVDD_IN}	On-chip flash regulator not used, flash and QSPI interface powered from external supply connected to FVDD pin	1.8	—	1.98	V
FVDD bypass capacitor	C_{FVDD}		0.7	1.0	6.1	μF
FVDD BOD threshold	V_{FVDD_BOD}	Supply rising, FLREG enabled, FLREG.OVROVERRIDEEN = 0, FLREG.OVRENLP = 0	—	—	1.75	V
		Supply falling, FLREG enabled, FLREG.OVROVERRIDEEN = 0, FLREG.OVRENLP = 0	1.65	—	—	V
		Supply rising, FLREG disabled, FLREG.OVROVERRIDEEN = 1, FLREG.OVRENLP = 1	—	—	1.71	V
		Supply falling, FLREG disabled, FLREG.OVROVERRIDEEN = 1, FLREG.OVRENLP = 1	1.65	—	—	V
FVDD BOD response time	$t_{RESP\_FVDDBOD}$	Supply falling at 100 mV/μs slew rate[1]	—	0.93	—	μs
FVDD BOD hysteresis	$V_{HYST\_FVDDBOD}$		—	12	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.6.2 Flash PLL (FLPLL)

Table 4.9. Flash PLL (FLPLL)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference clock frequency	f_{REF}		38	—	40	MHz
Startup time	$t_{STARTUP}$	Cold start to lock	—	13.8	—	µs
Frequency output step size	f_{STEP}		—	f_{REF} / 2048	—	kHz
PLL output clock frequency	f_{FLPLL}		240	—	440	MHz
Supply current	I_{FLPLL}	f_{FLPLL} = 440 MHz	—	665	—	µA
		f_{FLPLL} = 240 MHz	—	528	—	µA

4.6.3 Co-Packaged Flash (I temperature grade)

Table 4.10. Co-Packaged Flash (I temperature grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Program time[1]	t_{PROG}	Page program (1-256 bytes)	—	1.25	3	ms
Erase time	t_{ERASE}	Sector Erase (4 KB)	—	30	250	ms
		Region Erase (32 KB)	—	150	1250	ms
		Full Erase (4 MB)	—	20.4	25.2	s
Read time[1]	t_{READ}	Direct data read, plaintext region	—	—	0.985	µs
		Direct data read, encrypted region	—	—	TBD	µs
		Direct data read, encrypted and authenticated region	—	—	TBD	µs
Cache miss latency[1]	t_{MISS}	Line fetched from plaintext region	—	—	0.985	µs
		Line fetched from encrypted region	—	—	TBD	µs
		Line fetched from encrypted and authenticated region	—	—	TBD	µs
Program current[1]	I_{PROG}		—	10	20	mA
Erase current	I_{ERASE}	Block Erase	—	10	20	mA
		Full Erase	—	10	20	mA
Read current[1]	I_{READ}		—	11	18	mA

Note:

1. QSPI clocked at 104 MHz using FLPLL

4.6.4 Co-Packaged Flash (G temperature grade)

Table 4.11. Co-Packaged Flash (G temperature grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Program time[1]	t_{PROG}	Page program (1-256 bytes)	—	0.25	TBD	ms
Erase time	t_{ERASE}	Sector Erase (4 KB)	—	25	TBD	ms
		Region Erase (32 KB)	—	60	TBD	ms
		Full Erase (4 MB)	—	15.7	TBD	s
Read time[1]	t_{READ}	Direct data read, plaintext region	—	—	TBD	µs
		Direct data read, encrypted region	—	—	TBD	µs
		Direct data read, encrypted and authenticated region	—	—	TBD	µs
Cache miss latency[1]	t_{MISS}	Line fetched from plaintext region	—	—	TBD	µs
		Line fetched from encrypted region	—	—	TBD	µs
		Line fetched from encrypted and authenticated region	—	—	TBD	µs
Program current[1]	I_{PROG}		—	8	TBD	mA
Erase current	I_{ERASE}	Block Erase	—	8	TBD	mA
		Full Erase	—	8	TBD	mA
Read current[1]	I_{READ}		—	6.5	TBD	mA

Note:

1. QSPI clocked at 133 MHz using FLPLL

4.6.5 QSPI I/O Interface

Table 4.12. QSPI I/O Interface

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply range	V_{FLVDD}		1.7	—	1.98	V
Input low voltage	V_{IL}		—	—	0.3 * FLVDD	V
Input high voltage	V_{IH}		0.7 * FLVDD	—	—	V
Output low voltage	V_{OL}	IOL = 100 µA	—	—	0.2	V
Output high voltage	V_{OH}	IOH = -100 µA	FLVDD - 0.2	—	—	V
Input leakage current on I/O	I_{LEAK_IO}	Input logic high	—	0.8	TBD	µA
		Input logic low	—	-1	TBD	µA
Pin capacitance	C_{PIN}		—	6	—	pF
Load capacitance	C_{LOAD}		—	—	20	pF
Driver output impedance	Z_{OUT}	TXDRV = 0	—	24	—	Ω
		TXDRV = 1	—	36	—	Ω
		TXDRV = 2	—	61	—	Ω
		TXDRV = 3	—	111	—	Ω
Rise time	T_{RISE}	10% to 90%, C_{LOAD} = 20 pF, TXDRV = 0	0.568	0.712	1.046	ns
		10% to 90%, C_{LOAD} = 20 pF, TXDRV = 1	1.089	1.0	1.83	ns
		10% to 90%, C_{LOAD} = 20 pF, TXDRV = 2	2.068	2.36	3.373	ns
		10% to 90%, C_{LOAD} = 20 pF, TXDRV = 3	4.005	4.59	6.416	ns
Fall time	T_{FALL}	90% to 10%, C_{LOAD} = 20 pF, TXDRV = 0	0.542	0.684	1.112	ns
		90% to 10%, C_{LOAD} = 20 pF, TXDRV = 1	1.064	1.03	1.936	ns
		90% to 10%, C_{LOAD} = 20 pF, TXDRV = 2	2.013	2.5	3.53	ns
		90% to 10%, C_{LOAD} = 20 pF, TXDRV = 3	3.862	5.07	6.714	ns

4.6.6 QSPI SDR Mode Timing

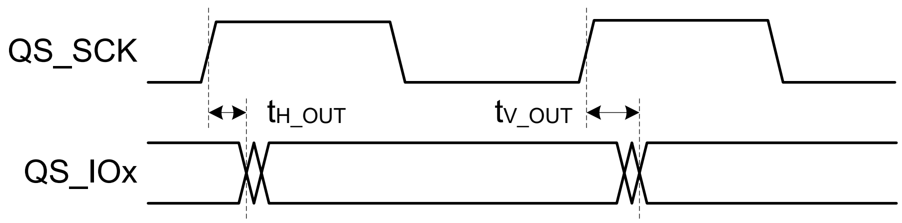


Figure 4.1. SDR Mode Output Timing

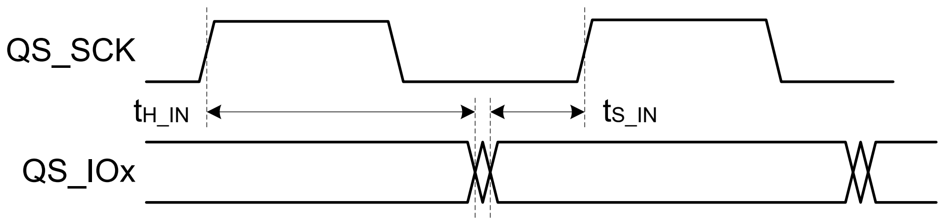


Figure 4.2. SDR Mode Input Timing

4.6.6.1 QSPI SDR Timing

Table 4.13. QSPI SDR Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Serial clock frequency	f_{SCK}	FLPLL used	60	—	133	MHz
		FSRCO used	—	20	—	MHz
Data in setup time	t_{S_IN}		2.6	—	—	ns
Data in hold time	t_{H_IN}		0.5	—	—	ns
Data out valid time	t_{V_OUT}	C_{LOAD} = 15 pF	—	—	1.88	ns
Data out hold time	t_{H_OUT}	C_{LOAD} = 15 pF	0	—	—	ns

4.7 Energy Mode Wake and Entry Timing

Table 4.14. Energy Mode Wake and Entry Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake-up Time from EM1	t_{EM1_WU}	Code execution from cache	—	1.71	—	µs
		Code execution from RAM	—	1.05	—	µs
Wake-up Time from EM4	t_{EM4_WU}	Code execution from flash	—	19.0	—	ms
Entry time to EM1	t_{EM1_ENT}		—	0.8	—	µs
Entry time to EM4	t_{EM4_ENT}		—	378	—	µs

4.8 Boot Timing

Secure boot impacts the recovery time from all sources of device reset. In addition to the root code authentication process, which cannot be disabled or bypassed, the root code can authenticate a bootloader, and the bootloader can authenticate the application. In projects that include only an application and no bootloader, the root code can authenticate the application directly. The duration of each authentication operation depends on two factors: the computation of the associated image hash, which is proportional to the size of the image, and the verification of the image signature, which is independent of image size.

The duration for the root code to authenticate the bootloader will depend on the SE firmware version as well as on the size of the bootloader.

The duration for the bootloader to authenticate the application can depend on the size of the application.

The test conditions for boot timing values assume that the associated bootloader and application code images do not contain a bootloader certificate or an application certificate. Authenticating a bootloader certificate or an application certificate will extend the boot time by an additional 6 to 7 ms.

All specifications are the durations from the termination of reset until the completion of the secure boot process (start of main() function in the application image) under various conditions.

Conditions:

- SE firmware version 3.1.0
- Bootloader size 15.4 KB

Timing is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

Table 4.15. Boot Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Boot time	t_{BOOT}	Secure boot application check disabled, no bootloader	—	45.9	—	ms
		Secure boot application check disabled, second stage bootloader check enabled, 50 KB application size	—	53.5	—	ms
		Secure boot application check enabled, second stage bootloader check enabled, 50 KB application size	—	63.4	—	ms
		Secure boot application check enabled, second stage bootloader check enabled, 150 KB application size	—	69.5	—	ms
		Secure boot application check enabled, second stage bootloader check enabled, 350 KB application size	—	81.6	—	ms
		Secure boot application check enabled, second stage bootloader check enabled, 1024 KB application size	—	131.2	—	ms

4.9 LPW 2.4 GHz RF Transmitter Characteristics

4.9.1 RF Transmitter General Characteristics for 0 dBm in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- P_{out} = 0 dBm, using 0 dBm PA and matching

Table 4.16. RF Transmitter General Characteristics for 0 dBm in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Maximum TX power[1]	$POUT_{MAX}$	0 dBm PA	—	0	—	dBm
Minimum active TX power	$POUT_{MIN}$	0 dBm PA	—	-24.9	—	dBm
Output power variation vs supply voltage variation, frequency = 2440 MHz	$POUT_{VAR\_V}$	0 dBm PA at P_{out} = 0 dBm, with PAVDD voltage swept from 1.8 V to 3.0 V	—	0.1	—	dB
Output power variation vs temperature, frequency = 2440 MHz	$POUT_{VAR\_T}$	0 dBm PA at P_{out} = 0 dBm, (T_A = -40 to 125 °C)	—	1.67	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	0 dBm PA, P_{out} = 0 dBm	—	0.13	—	dB
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-60	—	dBm
		25-1000 MHz, excluding above frequencies. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-42	—	dBm
		1G-25G, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.

4.9.2 RF Transmitter General Characteristics for 10 dBm in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- P_{out} = 10 dBm, using 10 dBm PA and matching

Table 4.17. RF Transmitter General Characteristics for 10 dBm in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Maximum TX power[1]	$POUT_{MAX}$	10 dBm PA	—	10	—	dBm
Minimum active TX power	$POUT_{MIN}$	10 dBm PA	—	-32.1	—	dBm
Output power variation vs supply voltage variation, frequency = 2440 MHz	$POUT_{VAR\_V}$	10 dbm PA at P_{out} = 10 dBm, with PAVDD voltage swept from 1.8 V to 3.0 V	—	0.1	—	dB
Output power variation vs temperature, frequency = 2440 MHz	$POUT_{VAR\_T}$	10 dBm PA at P_{out} = 10 dBm, (T_A = -40 to 125 °C)	—	0.26	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	10 dBm PA, P_{out} = 10 dBm	—	0.16	—	dB
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-60	—	dBm
		25-1000 MHz, excluding above frequencies. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-42	—	dBm
		1G-25G, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.

4.9.3 RF Transmitter Characteristics for 0 dBm Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- P_{out} = 0 dBm, using 0 dBm PA and matching

Table 4.18. RF Transmitter Characteristics for 0 dBm Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power spectral density limit	PSD_{LIMIT}	PSD per FCC Part 15.247, Continuous PN9 sequence, Average method per ANSI C63.10-2020 11.10.3 AVGPSD-1	—	-19.0	—	dBm/3kHz
		PSD per FCC Part 15.247, Continuous PN9 sequence, Peak method per ANSI C63.10-2020 11.10.2 PKPSD	—	-15.5	—	dBm/3kHz
		Per ETSI EN300.328 at 10 dBm/1 MHz	—	1.54	—	dBm
Occupied channel bandwidth	OCP	Per ETSI EN300.328, 99% BW at highest and lowest channels in band	—	1.02	—	MHz
In-band spurious emissions[1]	$SPUR_{INB}$	Inband spurs at ± 2 MHz	—	-51.0	—	dBm
		Inband spurs at ± 3 MHz	—	-56.5	—	dBm
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30 - 88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-58	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-40	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-16	—	dBm

Note:

1. With allowed exceptions.

4.9.4 RF Transmitter Characteristics for 10 dBm Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- P_{out} = 10 dBm, using 10 dBm PA and matching

Table 4.19. RF Transmitter Characteristics for 10 dBm Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power spectral density limit	PSD_{LIMIT}	PSD per FCC Part 15.247, Continuous PN9 sequence, Average method per ANSI C63.10-2020 11.10.3 AVGPSD-1	—	-9.3	—	dBm/3kHz
		PSD per FCC Part 15.247, Continuous PN9 sequence, Peak method per ANSI C63.10-2020 11.10.2 PKPSD	—	-6.0	—	dBm/3kHz
		Per ETSI EN300.328 at 10 dBm/1 MHz	—	9.9	—	dBm
Occupied channel bandwidth	OCP	Per ETSI EN300.328, 99% BW at highest and lowest channels in band	—	1.03	—	MHz
In-band spurious emissions[1]	$SPUR_{INB}$	Inband spurs at ± 2 MHz	—	-41.3	—	dBm
		Inband spurs at ± 3 MHz	—	-47.4	—	dBm
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30 - 88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-58	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-40	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-16	—	dBm

Note:

1. With allowed exceptions.

4.9.5 RF Transmitter Characteristics for 0 dBm Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- P_{out} = 0 dBm, using 0 dBm PA and matching

Table 4.20. RF Transmitter Characteristics for 0 dBm Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power spectral density limit	PSD_{LIMIT}	PSD per FCC Part 15.247, Continuous PN9 sequence, Average method per ANSI C63.10-2020 11.10.3 AVGPSD-1	—	-22.6	—	dBm/3kHz
		PSD per FCC Part 15.247, Continuous PN9 sequence, Peak method per ANSI C63.10-2020 11.10.2 PKPSD	—	-20.8	—	dBm/3kHz
		Per ETSI EN300.328 at 10 dBm/1 MHz	—	0.51	—	dBm
Occupied channel bandwidth	OCP	Per ETSI EN300.328, 99% BW at highest and lowest channels in band	—	2.08	—	MHz
In-band spurious emissions[1]	$SPUR_{INB}$	Inband spurs at ± 4 MHz	—	-53.2	—	dBm
		Inband spurs at ± 6 MHz	—	-58.3	—	dBm
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30 - 88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-58	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-40	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-16	—	dBm

Note:

1. With allowed exceptions.

4.9.6 RF Transmitter Characteristics for 10 dBm Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- P_{out} = 10 dBm, using 10 dBm PA and matching

Table 4.21. RF Transmitter Characteristics for 10 dBm Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power spectral density limit	PSD_{LIMIT}	PSD per FCC Part 15.247, Continuous PN9 sequence, Average method per ANSI C63.10-2020 11.10.3 AVGPSD-1	—	-13.0	—	dBm/3kHz
		PSD per FCC Part 15.247, Continuous PN9 sequence, Peak method per ANSI C63.10-2020 11.10.2 PKPSD	—	-11.3	—	dBm/3kHz
		Per ETSI EN300.328 at 10 dBm/1 MHz	—	9.9	—	dBm
Occupied channel bandwidth	OCP	Per ETSI EN300.328, 99% BW at highest and lowest channels in band	—	2.08	—	MHz
In-band spurious emissions[1]	$SPUR_{INB}$	Inband spurs at ± 4 MHz	—	-43.9	—	dBm
		Inband spurs at ± 6 MHz	—	-49.4	—	dBm
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30 - 88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-58	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-40	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-16	—	dBm

Note:

1. With allowed exceptions.

4.9.7 RF Transmitter Characteristics for 0 dBm Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- P_{out} = 0 dBm, using 0 dBm PA and matching

Table 4.22. RF Transmitter Characteristics for 0 dBm Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power spectral density limit	PSD_{LIMIT}	PSD per FCC Part 15.247, Continuous PN9 sequence, Average method per ANSI C63.10-2020 11.10.3 AVGPSD-1	—	-4.6	—	dBm/ 3kHz
		PSD per FCC Part 15.247, Continuous PN9 sequence, Peak method per ANSI C63.10-2020 11.10.2 PKPSD	—	-4.0	—	dBm/ 3kHz
		Per ETSI EN300.328 at 10 dBm/1 MHz	—	1.48	—	dBm
Occupied channel bandwidth	OCP	Per ETSI EN300.328, 99% BW at highest and lowest channels in band	—	1.02	—	MHz
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30 - 88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-58	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-40	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-16	—	dBm

4.9.8 RF Transmitter Characteristics for 10 dBm Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- P_{out} = 10 dBm, using 10 dBm PA and matching

Table 4.23. RF Transmitter Characteristics for 10 dBm Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power spectral density limit	PSD_{LIMIT}	PSD per FCC Part 15.247, Continuous PN9 sequence, Average method per ANSI C63.10-2020 11.10.3 AVGPSD-1	—	4.9	—	dBm/ 3kHz
		PSD per FCC Part 15.247, Continuous PN9 sequence, Peak method per ANSI C63.10-2020 11.10.2 PKPSD	—	5.7	—	dBm/ 3kHz
		Per ETSI EN300.328 at 10 dBm/1 MHz	—	9.9	—	dBm
Occupied channel bandwidth	OCP	Per ETSI EN300.328, 99% BW at highest and lowest channels in band	—	1.02	—	MHz
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30 - 88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-58	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-40	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-16	—	dBm

4.9.9 RF Transmitter Characteristics for 0 dBm Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- P_{out} = 0 dBm, using 0 dBm PA and matching

Table 4.24. RF Transmitter Characteristics for 0 dBm Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power spectral density limit	PSD_{LIMIT}	PSD per FCC Part 15.247, Continuous PN9 sequence, Average method per ANSI C63.10-2020 11.10.3 AVGPSD-1	—	-19.0	—	dBm/3kHz
		PSD per FCC Part 15.247, Continuous PN9 sequence, Peak method per ANSI C63.10-2020 11.10.2 PKPSD	—	-15.5	—	dBm/3kHz
		Per ETSI EN300.328 at 10 dBm/1 MHz	—	1.54	—	dBm
Occupied channel bandwidth	OCP	Per ETSI EN300.328, 99% BW at highest and lowest channels in band	—	1.03	—	MHz
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30 - 88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-58	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-40	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-16	—	dBm

4.9.10 RF Transmitter Characteristics for 10 dBm Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- P_{out} = 10 dBm, using 10 dBm PA and matching

Table 4.25. RF Transmitter Characteristics for 10 dBm Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power spectral density limit	PSD_{LIMIT}	PSD per FCC Part 15.247, Continuous PN9 sequence, Average method per ANSI C63.10-2020 11.10.3 AVGPSD-1	—	-9.2	—	dBm/ 3kHz
		PSD per FCC Part 15.247, Continuous PN9 sequence, Peak method per ANSI C63.10-2020 11.10.2 PKPSD	—	-5.9	—	dBm/ 3kHz
		Per ETSI EN300.328 at 10 dBm/1 MHz	—	9.9	—	dBm
Occupied channel bandwidth	OCP	Per ETSI EN300.328, 99% BW at highest and lowest channels in band	—	1.03	—	MHz
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NR}$	Continuous transmission of modulated carrier. P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30 - 88 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission modulated carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band, per ETSI EN300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-694 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-58	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 694-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-40	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-16	—	dBm

4.10 LPW 2.4 GHz RF Receiver Characteristics

4.10.1 RF Receiver General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz

Table 4.26. RF Receiver General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission per ETSI EN300	$SPUR_{RX\_ETSI}$	30 MHz to 1 GHz, per ETSI EN300.328	—	-63	—	dBm
		1 GHz to 12.75 GHz, per ETSI EN300.328	—	-53	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, conducted measurement	—	-55	—	dBm
		Above 960 MHz, conducted measurement.	—	-47	—	dBm
2GFSK Sensitivity	$SENS_{2GFSK}$	2 Mbps 2GFSK signal, 1% PER	—	-93.0	—	dBm
		250 kbps 2GFSK signal, 0.1% BER	—	-103.8	—	dBm

4.10.2 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- Packet length is 37 bytes

Table 4.27. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	RX_{SAT}	Signal is reference signal	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload, BER = 0.1% (PER = 30.8%)	—	-98.6	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017% (PER = 30.2%)	—	-97.1	—	dBm
		With non-ideal signals, 37 byte payload, BER = 0.1% (PER = 30.8%)	—	-98.3	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 2]	—	6.5	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 2 3 4]	—	-7.1	—	dB
		Interferer is reference signal at -1 MHz offset[1 2 3 4]	—	-7.6	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 2 3 4]	—	-43.2	—	dB
		Interferer is reference signal at -2 MHz offset[1 2 3 4]	—	-45.5	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 2 3 4]	—	-48.8	—	dB
		Interferer is reference signal at -3 MHz offset[1 2 3 4]	—	-49.5	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency[1 4]	—	-7.1	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz[1 4]	—	-43.2	—	dB
		Interferer is reference signal at image frequency -1 MHz[1 4]	—	6.5	—	dB
Intermodulation performance	IM	n = 3	—	-17.8	—	dBm
RSSI resolution	$RSSI_{RES}$	Between SENS and +5 dBm	—	0.25	—	dB
RSSI accuracy	$RSSI_{ACC}$	Between SENS and +5 dBm, with coverage factor K=2 (95%)	—	+/-4	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. 0.1% Bit Error Rate, 37-byte payload 2. Desired signal -67 dBm 3. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz 4. With allowed exceptions.						

4.10.3 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- Packet length is 37 bytes

Table 4.28. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	RX_{SAT}	Signal is reference signal	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload, BER = 0.1% (PER = 30.8%)	—	-95.7	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017% (PER = 30.2%)	—	-94.2	—	dBm
		With non-ideal signals, 37 byte payload, BER = 0.1% (PER = 30.8%)	—	-95.4	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 2]	—	6.5	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset[1 2 3 4]	—	-6.5	—	dB
		Interferer is reference signal at -2 MHz offset[1 2 3 4]	—	-8.1	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset[1 2 3 4]	—	-44.1	—	dB
		Interferer is reference signal at -4 MHz offset[1 2 3 4]	—	-46.4	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset[1 2 3 4]	—	-47.9	—	dB
		Interferer is reference signal at -6 MHz offset[1 2 3 4]	—	-49.3	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency[1 4]	—	-6.5	—	dB
Selectivity to image frequency ± 2 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz[1 4]	—	-44.1	—	dB
		Interferer is reference signal at image frequency -2 MHz[1 4]	—	6.5	—	dB
Intermodulation performance	IM	n = 3	—	-17.9	—	dBm
RSSI resolution	$RSSI_{RES}$	Between SENS and +5 dBm	—	0.25	—	dB
RSSI accuracy	$RSSI_{ACC}$	Between SENS and +5 dBm, with coverage factor K=2 (95%)	—	+/-4	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. 0.1% Bit Error Rate, 37-byte payload
2. Desired signal -67 dBm
3. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz
4. With allowed exceptions.

4.10.4 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- Packet length is 37 bytes

Table 4.29. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	RX_{SAT}	Signal is reference signal	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload, BER = 0.1% (PER = 30.8%)	—	-106.8	—	dBm
		With non-ideal signals, 37 byte payload, BER = 0.1% (PER = 30.8%)	—	-106.4	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 2]	—	0.2	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 2 3 4]	—	-13.1	—	dB
		Interferer is reference signal at -1 MHz offset[1 2 3 4]	—	-13.7	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 2 3 4]	—	-52.7	—	dB
		Interferer is reference signal at -2 MHz offset[1 2 3 4]	—	-54.5	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 2 3 4]	—	-53.9	—	dB
		Interferer is reference signal at -3 MHz offset[1 2 3 4]	—	-57.7	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency[1 4]	—	-53.9	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz[1 4]	—	-58.0	—	dB
		Interferer is reference signal at image frequency -1 MHz[1 4]	—	-52.7	—	dB
RSSI resolution	$RSSI_{RES}$	Between SENS and +5 dBm	—	0.25	—	dB
RSSI accuracy	$RSSI_{ACC}$	Between SENS and +5 dBm, with coverage factor K=2 (95%)	—	+/-4	—	dB

Note:

1. 0.1% Bit Error Rate, 37-byte payload
2. Desired signal -79 dBm
3. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz
4. With allowed exceptions.

4.10.5 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are:

- T_A = 25 °C
- AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V
- Crystal frequency = 38.4 MHz
- RF center frequency = 2.44 GHz
- Packet length is 37 bytes

Table 4.30. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	RX_{SAT}	Signal is reference signal	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload, BER = 0.1% (PER = 30.8%)	—	-102.5	—	dBm
		With non-ideal signals, 37 byte payload, BER = 0.1% (PER = 30.8%)	—	-101.8	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 2]	—	1.7	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 2 3 4]	—	-8.9	—	dB
		Interferer is reference signal at -1 MHz offset[1 2 3 4]	—	-9.5	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 2 3 4]	—	-48.0	—	dB
		Interferer is reference signal at -2 MHz offset[1 2 3 4]	—	-49.8	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 2 3 4]	—	-50.3	—	dB
		Interferer is reference signal at -3 MHz offset[1 2 3 4]	—	-53.5	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency[1 4]	—	-50.3	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz[1 4]	—	-53.7	—	dB
		Interferer is reference signal at image frequency -1 MHz[1 4]	—	-48.0	—	dB
RSSI resolution	$RSSI_{RES}$	Between SENS and +5 dBm	—	0.25	—	dB
RSSI accuracy	$RSSI_{ACC}$	Between SENS and +5 dBm, with coverage factor K=2 (95%)	—	+/-4	—	dB

Note:

1. 0.1% Bit Error Rate, 37-byte payload
2. Desired signal -72 dBm
3. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz
4. With allowed exceptions.

4.11 Oscillators

4.11.1 High-Frequency Crystal Oscillator (HFXO)

Table 4.31. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency[1 2 3]	F_{HFXO}		38	38.4	40	MHz
Supported crystal maximum equivalent series resistance (ESR)[3]	ESR_{HFXO}		—	40	60	Ω
Supported range of crystal load capacitance[4 3]	C_{L_HFXO}		6	—	10	pF
Supply current	I_{HFXO}		—	383	—	µA
Startup time[5]	$T_{STARTUP}$		—	166	—	µs
On-chip tuning cap step size[6]	SS_{HFXO}		—	0.04	—	pF

Note:

1. The BLE radio requires a crystal with a tolerance of ± 50 ppm over temperature and aging, and supports only certain crystal frequencies. Use a crystal with the recommended frequency and tolerance (refer to AN0016.3 for recommended crystals).
2. The radio requires additional software configuration based on crystal frequency. Refer to the Simplicity Studio component "RAIL Utility, Built-in PHYs Across HFXO Frequencies".
3. RF performance characteristics have been determined using crystals with an ESR of 40 Ω and C_L of 10 pF at the operating frequency designated in the RF performance table.
4. Total load capacitance as seen by the crystal.
5. Startup time does not include time implemented by programmable TIMEOUTSTEADY delay.
6. The tuning step size is the effective step size when incrementing both of the tuning capacitors by one count. The step size for each of the individual tuning capacitors is twice this value.

4.11.2 SOCPLL

Table 4.32. SOCPLL

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input reference frequency	f_{REF}		34	—	44	MHz
Supply current	I_{SOCPLL}	All supplies, PLL active, 150 MHz	—	696	—	µA
		All supplies, Open-loop mode, 145 MHz	—	485	—	µA
Startup time	$t_{STARTUP}$		—	36	—	µs

4.11.3 Low-Frequency Crystal Oscillator (LFXO)

Table 4.33. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	F_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	100	kΩ
Supported range of crystal load capacitance [1]	C_{L_LFXO}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	9	pF
		GAIN = 2	9	—	12	pF
		GAIN = 3 (see note[2])	12	—	18	pF
Crystal shunt capacitance	C_{0_LFXO}		—	—	2	pF
External sine amplitude	A_{EXTSIN}	Peak-to-peak voltage at LFXO_I input in external sine mode	0.2	—	1.0	Vpp
Startup time[3]	$T_{STARTUP}$	C_L = 6 pF, GAIN[4] = 1	—	31.3	—	ms
		C_L = 12.5 pF, GAIN[4] = 3	—	37.5	—	ms
Current consumption[3]	I_{LFXO}	C_L = 6 pF, GAIN[4] = 1, MODE[5] = XTAL	—	101	—	nA
		C_L = 12.5 pF, GAIN[4] = 3, MODE[5] = XTAL	—	141	—	nA
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
On-chip tuning capacitor value at minimum setting[6]	C_{LFXO_MIN}	CAPTUNE[4] = 0	—	7.1	—	pF
On-chip tuning capacitor value at maximum setting[6]	C_{LFXO_MAX}	CAPTUNE[4] = 0x59	—	29	—	pF

Note:

1. Total load capacitance seen by the crystal.
2. Crystals with a load capacitance of greater than 12.5 pF require external load capacitors.
3. Characterized using crystal with ESR ≤ 70 kΩ.
4. In LFXO_CAL Register.
5. In LFXO_CFG Register.
6. Including GPIO parasitic capacitance. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.11.4 High-Frequency RC Oscillator (HFRCO)

Table 4.34. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	f_{HFRCO_ACC}	For production calibrated frequencies	-2.5	—	2.5	%
Nominal calibrated frequency options	f_{CAL}	Using HFRCOEM23DEFAULT value from DEVINFO with HFRCOEM23	—	20	—	MHz
		Using HFRCOCALDEFAULT value from DEVINFO with HFRCODPLL	—	38	—	MHz
		Using HFRCOCALSPEED value from DEVINFO with HFRCODPLL	—	100	—	MHz
Startup time[1]	$t_{STARTUP}$	20 MHz, Settle to ± 0.5%	—	360	—	ns
		38 MHz, Settle to ± 0.5%	—	445	—	ns
		100 MHz, Settle to ± 0.5%	—	460	—	ns
Current consumption on all supplies	I_{HFRCO}	HFRCODPLL, free running	—	3.0	—	µA/MHz
		HFRCODPLL, with DPLL active[2]	—	3.5	—	µA/MHz
		HFRCOEM23	—	1.35	—	µA/MHz
DPLL band frequency limits[3]	f_{BAND_RANGE}	HFRCODPLLBAND1	20	—	24	MHz
		HFRCODPLLBAND2	24	—	30	MHz
		HFRCODPLLBAND3	30	—	36	MHz
		HFRCODPLLBAND4	36	—	42	MHz
		HFRCODPLLBAND5	42	—	50	MHz
		HFRCODPLLBAND6	50	—	60	MHz
		HFRCODPLLBAND7	60	—	70	MHz
		HFRCODPLLBAND8	70	—	80	MHz
		HFRCODPLLBAND9	80	—	90	MHz
		HFRCODPLLBAND10	90	—	100	MHz

Note:

1. Hardware delay ensures settling to within ± 0.5%. Hardware also enforces this delay when changes to the oscillator setup are made.
2. Operating with DPLL adds an additional 26 µA of static current on top of the dynamic current.
3. Limits represent the lowest and highest target frequency for HFRCODPLL operation using the production-calibrated DPLL bands stored at the specified location in DEVINFO.

4.11.5 Fast Startup RC Oscillator (FSRCO)

Table 4.35. Fast Startup RC Oscillator (FSRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSRCO frequency	F_{FSRCO}		18.8	20	21.2	MHz
FSRCO supply current	I_{FSRCO}		—	16.1	—	μA
FSRCO startup time	t_{START}		—	0.06	—	μs

4.11.6 Low-Frequency RC Oscillator (LFRCO)

Table 4.36. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}	Normal mode, across operating temperature range	-3	—	3	%
		Precision mode[1], across operating temperature range[2]	-500	—	500	ppm
Startup time	$t_{STARTUP}$	Normal mode	—	216	—	μs
		Precision mode[1]	—	11.6	—	ms
Current consumption	I_{LFRCO}	Normal mode	—	248	—	nA
		Precision mode[1], T_A = stable at 25 °C [3]	—	571	—	nA

Note:
1. The LFRCO operates in high-precision mode when CFG_HIGHPRECEN is set to 1. High-precision mode is not available in EM4.
2. Includes ± 40 ppm frequency tolerance of the HFXO crystal.
3. Includes periodic re-calibration against HFXO crystal oscillator.

4.11.7 Ultra-Low-Frequency RC Oscillator (ULFRCO)

Table 4.37. Ultra-Low-Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}	1 kHz Nominal	0.9	1	1.1	kHz

4.12 GPIO and RESETn Pins

Table 4.38. GPIO and RESETn Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, low-noise mode disabled, IOVDD = 3.63 V, $T_A = T_{A(max)}$}, pin input voltage at IOVDD (pin sinking current)	—	—	60	nA
		MODEx = DISABLED, low-noise mode disabled, IOVDD = 3.63 V, $T_A = T_{A(max)}$, pin input voltage at VSS (pin sourcing current)	—	—	150	nA
		MODEx = DISABLED, low-noise mode disabled, IOVDD = 1.8 V	—	1	—	nA
		MODEx = DISABLED, low-noise mode disabled, IOVDD = 3.0 V	—	1	—	nA
		MODEx = DISABLED, low-noise mode enabled, IOVDD = 3.63 V, $T_A = T_{A(max)}$}, pin input voltage at IOVDD (pin sinking current)	—	—	50	nA
		MODEx = DISABLED, low-noise mode enabled, IOVDD = 3.63 V, $T_A = T_{A(max)}$, pin input voltage at VSS (pin sourcing current)	—	—	135	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3 * IOVDD	V
		RESETn	—	—	0.3 * DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7 * IOVDD	—	—	V
		RESETn	0.7 * DVDD	—	—	V
Output low voltage	V_{OL}	Sinking 16 mA, IOVDD = 3.0 V	—	—	0.2 * IOVDD	V
		Sinking 8 mA, IOVDD = 1.8 V	—	—	0.4 * IOVDD	V
Output high voltage	V_{OH}	Sourcing 16 mA, IOVDD = 3.0 V	0.8 * IOVDD	—	—	V
		Sourcing 8 mA, IOVDD = 1.8 V	0.6 * IOVDD	—	—	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 3.0 V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	12.7	—	ns
		IOVDD = 1.8 V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	19.6	—	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 3.0 V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	9.3	—	ns
		IOVDD = 1.8 V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	16.2	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Pull up/down resistance[2]	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	30	38.5	50	kΩ
		RESETn pin. Pull-up to DVDD	30	38.5	50	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	33	—	ns
RESETn low time to ensure pin reset	T_{RESET}		100	—	—	ns

Note:

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

4.13 12-Bit SAR ADC

Table 4.39. 12-Bit SAR ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC resolution	Resolution		—	12	—	bits
Sampling rate	f_{SAMPLE}		—	—	1	Msps
Startup time	$t_{STARTUP}$	From shutdown state	—	—	5	μs
		From standby state	—	—	1	μs
Acquisition time	t_{ACQ}	Gain = 0.3125x, 0.5x, or 1x. Any ABUS. Any WARMUPMODE	250	—	—	ns
		Gain = 2x, ABUSA, ABUSB, or ABUSCD. Any WARMUPMODE	350	—	—	ns
		Gain = 4x, ABUSA or ABUSB. Any WARMUPMODE	350	—	—	ns
		Gain = 4x, ABUSCD. WARMUP-MODE = KEEPWARM	350	—	—	ns
		Gain = 4x, ABUSCD. WARMUP-MODE = NORMAL or KEEP-STANDBY	550	—	—	ns
Conversion time, cycles of ADCCLK	t_{CNV}	12-bit output	—	—	13	clocks
Clock frequency for ADC block	f_{CLK_IN}	Before SAR clock prescaler	—	—	44	MHz
SAR clock frequency	f_{CLK_SAR}	To achieve 1 Msps sampling rate	17	20	22	MHz
Input sampling capacitance	C_S	Gain = 0.3125x	—	0.375	—	pF
		Gain = 0.5x	—	0.6	—	pF
		Gain = 1x	—	1.2	—	pF
		Gain = 2x	—	2.4	—	pF
		Gain = 4x	—	4.8	—	pF
Equivalent input resistance [1]	R_{IN}	Differential mode, 1 Msps, Gain = 1x, impedance from AIN+ to AIN- input	—	1000	—	kΩ
		Single-ended mode, 1 Msps, Gain = 1x, impedance from AIN+ input to VSS	—	500	—	kΩ
		With supply selected as input	—	40	—	kΩ
Equivalent input resistance of external reference	R_{VREFP}		—	135	—	kΩ
Input source resistance	R_{SIN}	To achieve performance at 1 Msps	—	—	1	kΩ
External VREF source resist-ance	R_{SVREF}	To achieve performance at 1 Msps	—	—	1	kΩ
Maximum input range	V_{IN_MAX}	Voltage on AIN+ or AIN- input pins	0	—	AVDD	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Full-scale voltage	V_{FS}		—	V_{REF} / Gain	—	V
Input measurement range	V_{IN}	Single-ended conversions, AIN+ input voltage	0	—	V_{FS}	V
		Differential conversions, Difference between AIN+ and AIN- inputs	$-V_{FS}$	—	$+V_{FS}$	V
Reference voltage	V_{REF}	Internal reference (REFSEL = VREFINT)	1.185	1.20	1.215	V
		External VREFP, Buffered Mode (REFSEL = VREFPBUF)	1.14	—	1.26	V
		External VREFP, Direct Mode High Range (REFSEL = VREFPH)	1.25	—	AVDD	V
Signal to noise and distortion ratio [2]	SNDR	Differential conversions, 1 Msps, Gain = 0.3125x, 10 kHz full-scale input, internal reference	—	66.7	—	dB
		Differential conversions, 1 Msps, Gain = 0.5x, 10 kHz full-scale input, internal reference	—	68.5	—	dB
		Differential conversions, 1 Msps, Gain = 1x, 10 kHz full-scale input, internal reference	61.7	67.0	—	dB
		Differential conversions, 1 Msps, Gain = 2x, 10 kHz full-scale input, internal reference	—	64.8	—	dB
		Differential conversions, 1 Msps, Gain = 4x, 10 kHz full-scale input, internal reference	—	60.7	—	dB
		Differential conversions, 1 Msps, Gain = 1x, 10 kHz full-scale input, external 1.2 V reference	—	67.6	—	dB
		Single-ended conversions, 1 Msps, Gain = 0.3125x, 10 kHz full-scale input, internal reference	—	61.0	—	dB
		Single-ended conversions, 1 Msps, Gain = 0.5x, 10 kHz full-scale input, internal reference	—	63.8	—	dB
		Single-ended conversions, 1 Msps, Gain = 1x, 10 kHz full-scale input, internal reference	57.1	62.5	—	dB
		Single-ended conversions, 1 Msps, Gain = 2x, 10 kHz full-scale input, internal reference	—	59.6	—	dB
		Single-ended conversions, 1 Msps, Gain = 4x, 10 kHz full-scale input, internal reference	—	56.3	—	dB
Total harmonic distortion	THD	Differential conversions, 1 Msps, Gain = 1x, 10 kHz full-scale input, internal reference	—	-79.2	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-free dynamic range	SFDR	Differential conversions, 1 Msps, Gain = 1x, 10 kHz full-scale input, internal reference	62	80.3	—	dB
Effective number of bits [2]	ENOB	Differential conversions, 1 Msps, Gain = 0.3125x, 10 kHz full-scale input, internal reference	—	10.8	—	bits
		Differential conversions, 1 Msps, Gain = 0.5x, 10 kHz full-scale input, internal reference	—	11.1	—	bits
		Differential conversions, 1 Msps, Gain = 1x, 10 kHz full-scale input, internal reference	9.9	10.8	—	bits
		Differential conversions, 1 Msps, Gain = 2x, 10 kHz full-scale input, internal reference	—	10.5	—	bits
		Differential conversions, 1 Msps, Gain = 4x, 10 kHz full-scale input, internal reference	—	9.8	—	bits
		Single-ended conversions, 1 Msps, Gain = 0.3125x, 10 kHz full-scale input, internal reference	—	9.8	—	bits
		Single-ended conversions, 1 Msps, Gain = 0.5x, 10 kHz full-scale input, internal reference	—	10.3	—	bits
		Single-ended conversions, 1 Msps, Gain = 1x, 10 kHz full-scale input, internal reference	9.2	10.1	—	bits
		Single-ended conversions, 1 Msps, Gain = 2x, 10 kHz full-scale input, internal reference	—	9.6	—	bits
		Single-ended conversions, 1 Msps, Gain = 4x, 10 kHz full-scale input, internal reference	—	9.0	—	bits
Power supply rejection ratio	PSRR	DC, internal reference	—	60	—	dB
		AC @ 500kHz, internal reference	—	46	—	dB
Common-mode rejection ratio	CMRR	DC	—	80	—	dB
		AC @ 500kHz	—	51	—	dB
Differential nonlinearity	DNL	Differential input, no missing codes	-1	+/-0.31	1	LSB12
Integral nonlinearity	INL	Differential input	-3	+/-0.81	3	LSB12

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset error	E_{OFFSET}	Differential input, Gain = 0.3125, using external VREF, direct mode	-3	—	3	LSB12
		Differential input, Gain = 0.5, using external VREF, direct mode	-3	—	3	LSB12
		Differential input, Gain = 1, using external VREF, direct mode	-3	—	3	LSB12
		Differential input, Gain = 2, using external VREF, direct mode	-3	—	3	LSB12
		Differential input, Gain = 4, using external VREF, direct mode	-3	—	3	LSB12
		Single-ended input, Gain = 0.3125, using external VREF, direct mode	-6	—	6	LSB12
		Single-ended input, Gain = 0.5, using external VREF, direct mode	-6	—	6	LSB12
		Single-ended input, Gain = 1, using external VREF, direct mode	-6	—	6	LSB12
		Single-ended input, Gain = 2, using external VREF, direct mode	-6	—	6	LSB12
		Single-ended input, Gain = 4, using external VREF, direct mode	-6	—	6	LSB12
Gain error	E_{GAIN}	Gain = 0.3125, using external VREF, direct mode	-1.5	0.56	1.5	%
		Gain = 0.5, using external VREF, direct mode	-1	0.51	1	%
		Gain = 1, using external VREF, direct mode	-1	0.38	1	%
		Gain = 2, using external VREF, direct mode	-1	0.26	1	%
		Gain = 4, using external VREF, direct mode	-1	0.14	1	%
Operational supply current (all supplies)	I_{ADC}	1 Msps, continuous operation, internal reference, conversions self-triggered in repeat mode	—	233	—	μA

Note:

1. R_{IN} is dependent on sampling frequency and sampling capacitor value. In differential mode, R_{IN} between the differential inputs is 2 / (f_{SAMPLE} * C_S). In single-ended mode, R_{IN} between the input pin and VSS is 1 / (f_{SAMPLE} * C_S).
2. The relationship between ENOB and SNDR is specified according to the equation: ENOB = (SNDR - 1.76) / 6.02.

4.14 Analog Comparator (ACMP)

Table 4.40. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ACMP supply current (all supplies)	I_{ACMP}	BIAS = 4, HYSTRISE = HYSTFALL = DISABLED	—	6.2	—	µA
		BIAS = 5, HYSTRISE = HYSTFALL = DISABLED	—	12.4	—	µA
		BIAS = 6, HYSTRISE = HYSTFALL = DISABLED	—	32.2	—	µA
		BIAS = 7, HYSTRISE = HYSTFALL = DISABLED	—	60.8	—	µA
ACMP supply current with hysteresis (all supplies)	I_{ACMP_WHYS}	BIAS = 4, HYSTRISE = HYSTFALL != DISABLED	—	6.6	—	µA
		BIAS = 5, HYSTRISE = HYSTFALL != DISABLED	—	13.2	—	µA
		BIAS = 6, HYSTRISE = HYSTFALL != DISABLED	—	34.5	—	µA
		BIAS = 7, HYSTRISE = HYSTFALL != DISABLED	—	65.1	—	µA
Current consumption from VREFDIV in continuous mode (all supplies)	$I_{VREFDIV}$	NEGSEL = VREFDIVAVDD	—	2.5	—	µA
		NEGSEL = VREFDIV1V25	—	3.7	—	µA
		NEGSEL = VREFDIV2V5	—	6.1	—	µA
Current consumption from VREFDIV in sample/hold mode (all supplies)	$I_{VREFDIV\_SH}$	NEGSEL = VREFDIV2V5LP	—	122.4	—	nA
		NEGSEL = VREFDIV1V25LP	—	115.2	—	nA
		NEGSEL = VREFDIVAVDDLP	—	114.4	—	nA
Current consumption from VSENSEDIV in continuous mode (all supplies)	$I_{VSENSEDIV}$	NEGSEL = VSENSE01DIV4	—	1.2	—	µA
Current consumption from VSENSEDIV in sample/hold mode (all supplies)	$I_{VSENSEDIV\_SH}$	NEGSEL = VSENSE01DIV4LP	—	57	—	nA
Hysteresis (BIAS = 4)	V_{HYST_4}	HYSTRISE = HYST10POS[1]	—	10.5	—	mV
		HYSTRISE = HYST20POS[1]	—	21.7	—	mV
		HYSTRISE = HYST30POS[1]	—	34.2	—	mV
		HYSTFALL = HYST10NEG[1]	—	-10.5	—	mV
		HYSTFALL = HYST20NEG[1]	—	-21.7	—	mV
		HYSTFALL = HYST30NEG[1]	—	-34.2	—	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	1.2	1.25	1.3	V
		Internal 2.5 V reference	2.4	2.5	2.6	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input offset voltage	V_{OFFSET}	BIAS = 4, VCMRANGE = FULL, V_{CM} = 50 mV to AVDD - 50 mV	—	-0.97	—	mV
		BIAS = 7, VCMRANGE = FULL, V_{CM} = 50 mV to AVDD - 50 mV	—	-0.98	—	mV
Input range	V_{IN}	Input voltage range	0	—	AVDD	V
Input common mode range	V_{CM}	VCMRANGE = FULL	0	—	AVDD	V
Comparator delay with 100 mV overdrive	T_{DELAY}	BIAS = 4	—	189	—	ns
		BIAS = 5	—	106	—	ns
		BIAS = 6	—	61	—	ns
		BIAS = 7	—	46	—	ns

Note:

1. V_{CM} = 1.25 V

4.15 Temperature Sensor

Table 4.41. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature sensor range[1]	T_{RANGE}		-40	—	125	°C
Temperature sensor resolution	$T_{RESOLUTION}$		—	0.7	—	°C
Measurement noise (RMS)	T_{NOISE}	Single measurement	—	0.67	—	°C
		16-sample average (TEMPAVG-NUM = 0)	—	0.18	—	°C
		64-sample average (TEMPAVG-NUM = 1)	—	0.11	—	°C
Measurement interval	t_{MEAS}		—	250	—	ms

Note:

1. The sensor reports absolute die temperature in Kelvin (K). All specifications are in °C to match the units of the specified product temperature range.

4.16 LED FET Pre-Driver (LEDDRV)

Table 4.42. LED FET Pre-Driver (LEDDRV)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operational input supply voltage range	V_{IOVDD}	Charge pump supplied from IOVDD	2.97	3.3	3.63	V
Nominal charge pump output voltage	V_{LEDVDD}		—	V_{IOVDD} + 2.7	—	V
Charge pump output supply voltage accuracy	ACC_{LEDVDD}	No load	-1.7	0.17	1.5	%
Charge pump output drop	$DROP_{LEDVDD}$	At 1 mA load, relative to no load	—	—	1	%
Charge pump supply capacitor	C_{LEDVDD}		—	0.1	—	µF
Charge pump load current [1]	I_{CPLOAD}		—	—	1	mA
Driver impedance	$R_{LEDGATE}$	Pull-up	—	36	—	Ω
		Pull-Down	—	13	—	Ω
Current loop inductor	L_{DSNS}		—	330	—	µH
Current sense reference voltage nominal	V_{ISNS_REF}		—	300	—	mV
Current sense reference accuracy	ACC_{ISNS_REF}	At nominal V_{ISNS_REF}	-9	—	6	%

Note:

1. The charge pump load current is calculated as C*V*F, depending on the output load capacitance on the drivers, voltage, and switching frequency. At 1 nF loading, 6 V, and 165 kHz, this is approximately 1 mA.

4.17 External Tamper Detection (ETAMPDET) Supply Current

Table 4.43. External Tamper Detection (ETAMPDET) Supply Current

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current consumption	$I_{ETAMPDET}$	One channel, operating from 1 kHz ULFRCO divided down to 100 Hz, with 1 nF load capacitance from GPIO to ground	—	83	—	nA
		One channel, operating from 32.768 kHz LFXO divided down to 100 Hz, with 1 nF load capacitance from GPIO to ground	—	142	—	nA
		One channel, operating from 32.768 kHz LFRCO divided down to 100 Hz, with 1 nF load capacitance from GPIO to ground	—	146	—	nA

4.18 Brown Out Detectors (BOD)

4.18.1 DVDD BOD

BOD thresholds on DVDD in EM0 and EM1 only, unless otherwise noted.

Table 4.44. DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{DVDD_BOD}	Supply rising	—	1.68	1.71	V
		Supply falling	1.62	1.66	—	V
BOD response time	$t_{RESPONSE}$	Supply falling at 100 mV/µs slew rate[1]	—	342	—	ns
BOD hysteresis	$V_{DVDD\_BOD\_HYST}$		—	22	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold) or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.18.2 LE DVDD BOD

BOD thresholds on DVDD pin for low-energy mode EM4, unless otherwise noted.

Table 4.45. LE DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	$V_{DVDD\_LE\_BOD}$	Supply falling	1.45	1.6	1.71	V
BOD response time	$t_{DVDD\_LE\_BOD\_DELAY}$	Supply dropping at 2 mV/µs slew rate[1]	—	41	—	µs
BOD hysteresis	$V_{DVDD\_LE\_BOD\_HYST}$		—	26	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold) or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.18.3 AVDD and IOVDD BODs

BOD thresholds for AVDD BOD and IOVDD BOD. Available in all energy modes.

Table 4.46. AVDD and IOVDD BODs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{BOD}	Supply falling	1.45	1.59	1.71	V
BOD response time	t_{BOD_DELAY}	Supply dropping at 2 mV/µs slew rate[1]	—	34	—	µs
BOD hysteresis	V_{BOD_HYST}		—	23	—	mV

Note:
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold) or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.19 EUSART SPI Main Timing

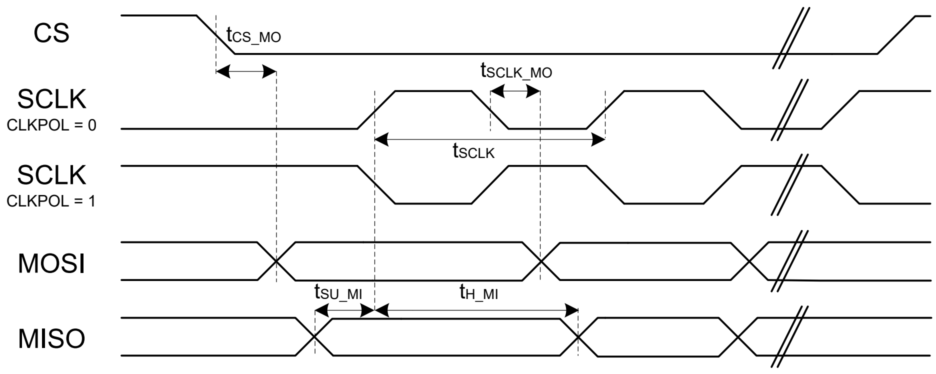


Figure 4.3. SPI Main Timing

4.19.1 EUSART SPI Main Timing

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.47. EUSART SPI Main Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		t_{PCLK}	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-17	—	16	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-7	—	12	ns
MISO setup time[1 2]	t_{SU_MI}		11	—	—	ns
MISO hold time[1 2]	t_{H_MI}		-12	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.20 EUSART SPI Secondary Timing

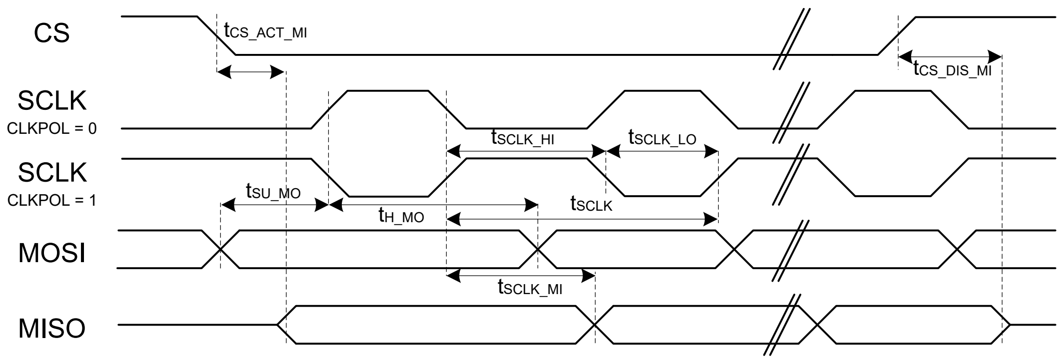


Figure 4.4. SPI Secondary Timing

4.20.1 EUSART SPI Secondary Timing

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.48. EUSART SPI Secondary Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time[1 2]	t_{SCLK_HI}		50	—	—	ns
SCLK low time[1 2]	t_{SCLK_LO}		50	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		6	—	66	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		6	—	50	ns
MOSI setup time[1 2]	t_{SU_MO}		9	—	—	ns
MOSI hold time[1 2]	t_{H_MO}		-38	—	—	ns
SCLK to MISO[1 2]	t_{SCLK_MI}		16	—	60	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).

4.21 I2C Electrical Specifications

4.21.1 I2C Standard-mode (Sm)

CLHR clearred to 0 in the I2Cn_CTRL register.

Table 4.49. I2C Standard-mode (Sm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	µs
Repeated START condition hold time	t_{HD_STA}		4.0	—	—	µs
STOP condition set-up time	t_{SU_STO}		4.0	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.21.2 I2C Fast-mode (Fm)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.50. I2C Fast-mode (Fm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.21.3 I2C Fast-mode Plus (Fm+)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.51. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	μs
SCL clock high time	t_{HIGH}		0.26	—	—	μs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	μs
Repeated START condition hold time	t_{HD_STA}		0.26	—	—	μs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	μs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	μs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.22 Pulse Counter (PCNT)

Table 4.52. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	f_{IN}	Asynchronous single and quadrature modes	—	—	1	MHz
		Sampled modes with debounce filter set to 0	—	—	8	kHz
Setup time in asynchronous external clock mode	$t_{SU\_S1N\_S0N}$	S1N (data) to S0N (clock)	16.5	—	—	ns
Hold time in asynchronous external clock mode	$t_{HD\_S0N\_S1N}$	S0N (clock) to S1N (data)	18.6	—	—	ns

4.23 Symmetric Cryptography Timing

HCLK = 38.4 MHz

Table 4.53. Symmetric Cryptography Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AES-128 timing	t_{AES128}	AES-128 CCM encryption, PT 1 kB	—	133.6	—	µs
		AES-128 CCM encryption, PT 32 kB	—	1480	—	µs
		AES-128 CTR encryption, PT 1 kB	—	80.7	—	µs
		AES-128 CTR encryption, PT 32 kB	—	702.5	—	µs
		AES-128 GCM encryption, PT 1 kB	—	111.7	—	µs
		AES-128 GCM encryption, PT 32 kB	—	733.0	—	µs
AES-256 timing	t_{AES256}	AES-256 CCM encryption, PT 1 kB	—	148.5	—	µs
		AES-256 CCM encryption, PT 32 kB	—	1905	—	µs
		AES-256 CTR encryption, PT 1 kB	—	88.2	—	µs
		AES-256 CTR encryption, PT 32 kB	—	914.8	—	µs
		AES-256 GCM encryption, PT 1 kB	—	118.9	—	µs
		AES-256 GCM encryption, PT 32 kB	—	943.5	—	µs
SHA-256 timing	t_{SHA256}	SHA-256, PT 1 kB	—	96.7	—	µs
		SHA-256, PT 32 kB	—	949.5	—	µs
SHA-512 timing[1]	t_{SHA512}	SHA-512, PT 1 kB	—	89.3	—	µs
		SHA-512, PT 32 kB	—	722.3	—	µs

Note:

1. Option is only available on OPNs with Secure Vault High feature set.

4.24 Symmetric Cryptography Timing at 150 MHz

HCLK = 150 MHz

Table 4.54. Symmetric Cryptography Timing at 150 MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AES-128 timing	t_{AES128}	AES-128 CCM encryption, PT 1 kB	—	62.7	—	µs
		AES-128 CCM encryption, PT 32 kB	—	413.8	—	µs
		AES-128 CTR encryption, PT 1 kB	—	45.5	—	µs
		AES-128 CTR encryption, PT 32 kB	—	201	—	µs
		AES-128 GCM encryption, PT 1 kB	—	58.9	—	µs
		AES-128 GCM encryption, PT 32 kB	—	218.1	—	µs
AES-256 timing	t_{AES256}	AES-256 CCM encryption, PT 1 kB	—	66.5	—	µs
		AES-256 CCM encryption, PT 32 kB	—	524.7	—	µs
		AES-256 CTR encryption, PT 1 kB	—	45.5	—	µs
		AES-256 CTR encryption, PT 32 kB	—	257.3	—	µs
		AES-256 GCM encryption, PT 1 kB	—	58.8	—	µs
		AES-256 GCM encryption, PT 32 kB	—	274.0	—	µs
SHA-256 timing	t_{SHA256}	SHA-256, PT 1 kB	—	46.6	—	µs
		SHA-256, PT 32 kB	—	267.2	—	µs
SHA-512 timing[1]	t_{SHA512}	SHA-512, PT 1 kB	—	45.6	—	µs
		SHA-512, PT 32 kB	—	208.0	—	µs

Note:

1. Option is only available on OPNs with Secure Vault High feature set.

4.25 Crypto Operation Timing for SE Manager API

Values in the following table represent timing from the SE Manager API call to return. The Cortex-M33 HCLK frequency is 38.4 MHz. The timing specifications below are measured at the SE Manager function call API. Each duration in the table contains some portion that is influenced by the SE Manager build compilation and Cortex-M33 operating frequency, and some portion that is influenced by the Hardware Secure Engine's firmware version and its operating speed (typically 80 MHz). The contributions of the Cortex-M33 properties to the overall specification timing are most pronounced for the shorter operations such as AES and hash when operating on small payloads. The overhead of command processing at the mailbox interface can also dominate the timing for shorter operations.

Conditions:

- SE firmware version 3.1.0

Timing is expected to be similar for subsequent SE firmware versions. Refer to the SE firmware release notes for any significant changes.

Table 4.55. Crypto Operation Timing for SE Manager API

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AES-128 timing	t_{AES128}	AES-128 CCM encryption, PT 1 kB	—	749	—	µs
		AES-128 CCM encryption, PT 32 kB	—	3438	—	µs
		AES-128 CTR encryption, PT 1 kB	—	630	—	µs
		AES-128 CTR encryption, PT 32 kB	—	2077	—	µs
		AES-128 GCM encryption, PT 1 kB	—	647	—	µs
		AES-128 GCM encryption, PT 32 kB	—	2086	—	µs
AES-256 timing	t_{AES256}	AES-256 CCM encryption, PT 1 kB	—	790	—	µs
		AES-256 CCM encryption, PT 32 kB	—	4815	—	µs
		AES-256 CTR encryption, PT 1 kB	—	649	—	µs
		AES-256 CTR encryption, PT 32 kB	—	2623	—	µs
		AES-256 GCM encryption, PT 1 kB	—	663	—	µs
		AES-256 GCM encryption, PT 32 kB	—	2630	—	µs
ECC P-256 timing	t_{ECC_P256}	ECC key generation, P-256	—	6.5	—	ms
		ECC signing, P-256	—	6.5	—	ms
		ECC verification, P-256	—	6.0	—	ms
ECC P-25519 timing	t_{ECC_P25519}	ECC key generation, P-25519	—	4.8	—	ms
		ECC signing, P-25519	—	8.3	—	ms
		ECC verification, P-25519	—	6.0	—	ms
ECDH compute secret timing	t_{ECDH}	ECDH compute secret, P-25519	—	4.8	—	ms
		ECDH compute secret, P-256	—	6.3	—	ms
ECJPAKE client timing	$t_{ECJPAKE\_C}$	ECJPAKE client write round one	—	24.6	—	ms
		ECJPAKE client read round one	—	11.8	—	ms
		ECJPAKE client write round two	—	16.3	—	ms
		ECJPAKE client read round two	—	6.5	—	ms
		ECJPAKE client derive secret	—	9.0	—	ms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ECJPAKE server timing	$t_{ECJPAKE\_S}$	ECJPAKE server write round one	—	24.4	—	ms
		ECJPAKE server read round one	—	11.9	—	ms
		ECJPAKE server write round two	—	16.7	—	ms
		ECJPAKE server read round two	—	6.4	—	ms
		ECJPAKE server derive secret	—	8.7	—	ms
SHA-256 timing	t_{SHA256}	SHA-256, PT 1 kB	—	335	—	µs
		SHA-256, PT 32 kB	—	776	—	µs
SHA-512 timing[1]	t_{SHA512}	SHA-512, PT 1 kB	—	335	—	µs
		SHA-512, PT 32 kB	—	655	—	µs

Note:

1. Option is only available on OPNs with Secure Vault High feature set.

4.26 Crypto Operation Average Current for SE Manager API

Values in the following table represent current consumed by the security core during operation, due to the Hardware Secure Engine CPU and its associated crypto accelerators. Current consumed by the Cortex-M33 application CPU is not included. The current measurements below represent the average value of the current for the duration of the crypto operation. Instantaneous peak currents may be higher.

Conditions:

- SE firmware version 3.1.0

Current consumption is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

Table 4.56. Crypto Operation Average Current for SE Manager API

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AES-128 current	I_{AES128}	AES-128 CCM encryption, PT 1 kB	—	2.4	—	mA
		AES-128 CCM encryption, PT 32 kB	—	3.3	—	mA
		AES-128 CTR encryption, PT 1 kB	—	2.2	—	mA
		AES-128 CTR encryption, PT 32 kB	—	3.4	—	mA
		AES-128 GCM encryption, PT 1 kB	—	2.3	—	mA
		AES-128 GCM encryption, PT 32 kB	—	3.6	—	mA
AES-256 current	I_{AES256}	AES-256 CCM encryption, PT 1 kB	—	2.4	—	mA
		AES-256 CCM encryption, PT 32 kB	—	3.3	—	mA
		AES-256 CTR encryption, PT 1 kB	—	2.3	—	mA
		AES-256 CTR encryption, PT 32 kB	—	3.4	—	mA
		AES-256 GCM encryption, PT 1 kB	—	2.3	—	mA
		AES-256 GCM encryption, PT 32 kB	—	3.5	—	mA
ECC P-256 current	$I_{ECCP256}$	ECC key generation, P-256	—	1.7	—	mA
		ECC signing, P-256	—	1.7	—	mA
		ECC verification, P-256	—	1.7	—	mA
ECC P-25519 current	$I_{ECCP25519}$	ECC key generation, P-25519	—	1.7	—	mA
		ECC signing, P-25519	—	1.7	—	mA
		ECC verification, P-25519	—	1.6	—	mA
ECDH compute secret current	I_{ECDH}	ECDH compute secret, P-25519	—	1.6	—	mA
		ECDH compute secret, P-256	—	1.7	—	mA
ECJPAKE client current	$I_{ECJPAKE\_C}$	ECJPAKE client write round one	—	1.7	—	mA
		ECJPAKE client read round one	—	1.7	—	mA
		ECJPAKE client write round two	—	1.7	—	mA
		ECJPAKE client read round two	—	1.7	—	mA
		ECJPAKE client derive secret	—	1.7	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ECJPAKE server current	$I_{ECJPAKE\_S}$	ECJPAKE server write round one	—	1.7	—	mA
		ECJPAKE server read round one	—	1.7	—	mA
		ECJPAKE server write round two	—	1.7	—	mA
		ECJPAKE server read round two	—	1.7	—	mA
		ECJPAKE server derive secret	—	1.7	—	mA
SHA-256 current	I_{SHA256}	SHA-256, PT 1 kB	—	2.1	—	mA
		SHA-256, PT 32 kB	—	2.6	—	mA
SHA-512 current[1]	I_{SHA512}	SHA-512, PT 1 kB	—	2.1	—	mA
		SHA-512, PT 32 kB	—	2.5	—	mA

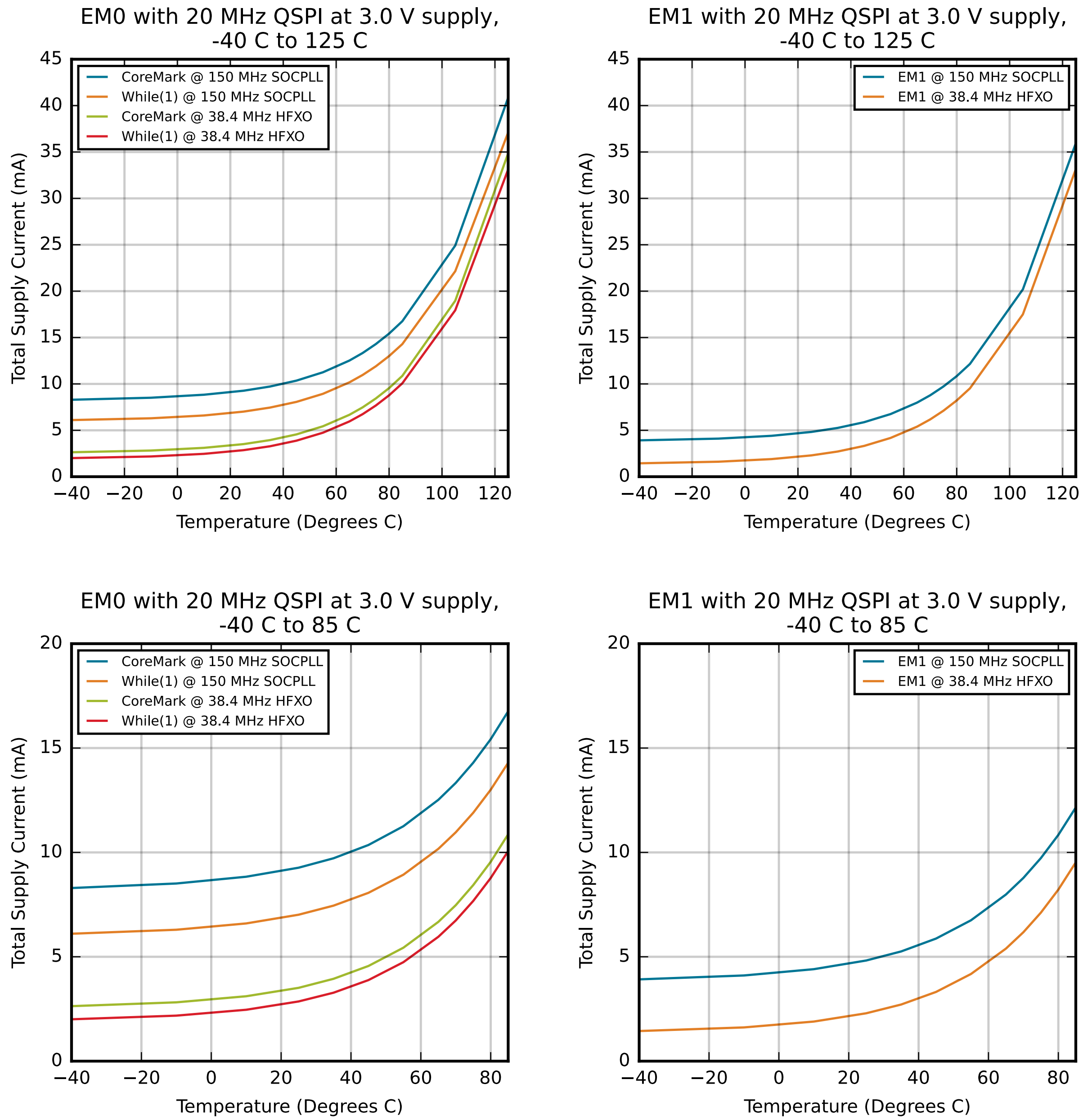
Note:
1. Option is only available on OPNs with Secure Vault High feature set.

4.27 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.27.1 Supply Current

Figure 4.5. EM0 and EM1 Typical Supply Current vs. Temperature with QSPI Clocked at 20 MHz from FSRCO



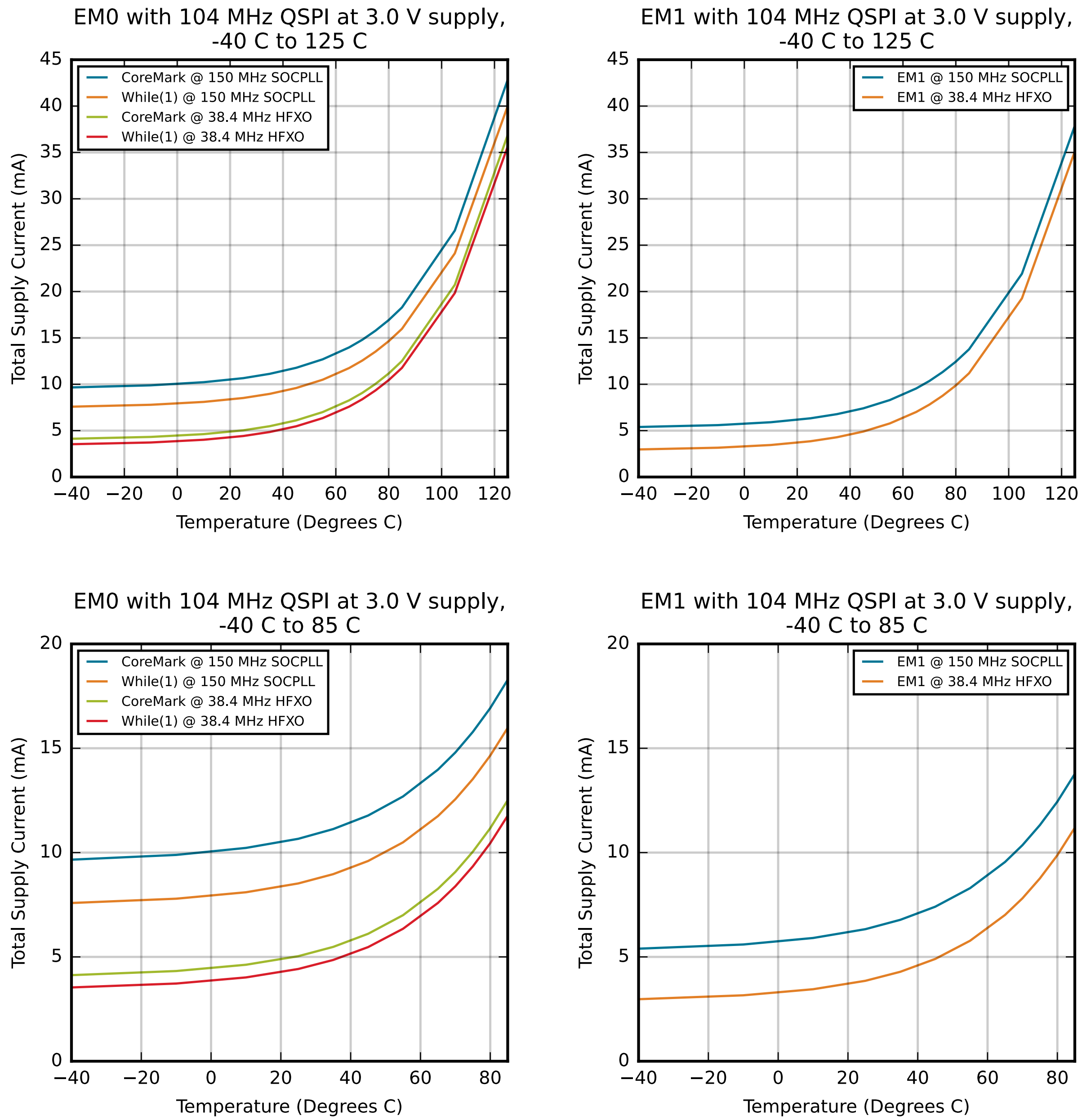


Figure 4.6. EM0 and EM1 Typical Supply Current vs. Temperature with QSPI Clocked at 104 MHz from FLPLL

5. Typical Connections

5.1 Power Supplies

Typical connections for power supplies and external crystals are shown in the following figures.

Note: The supply connections to the device are flexible. Supplies may be connected in configurations not shown, as long as the supply limits described in 4.1 Electrical Characteristics are met.

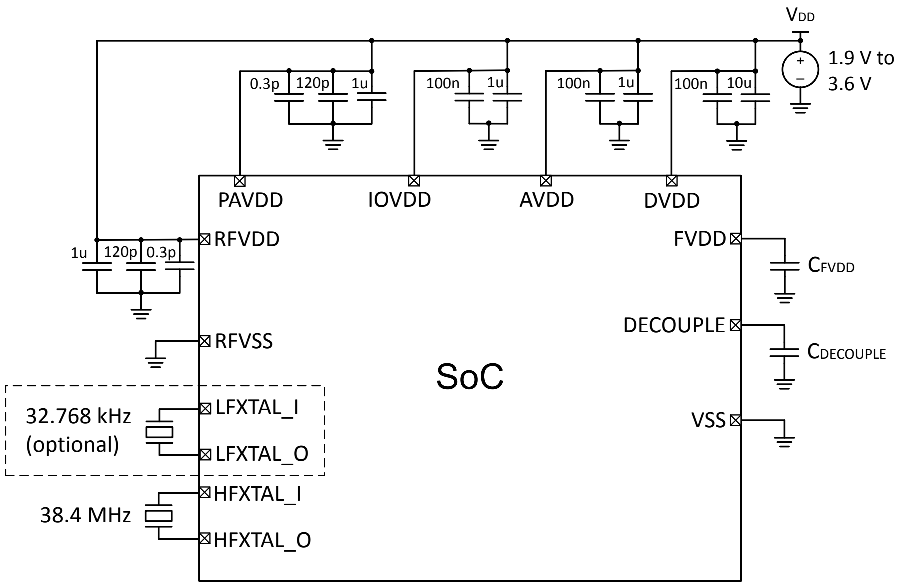


Figure 5.1. Single Supply (Min 1.9 V, Max 3.6 V)

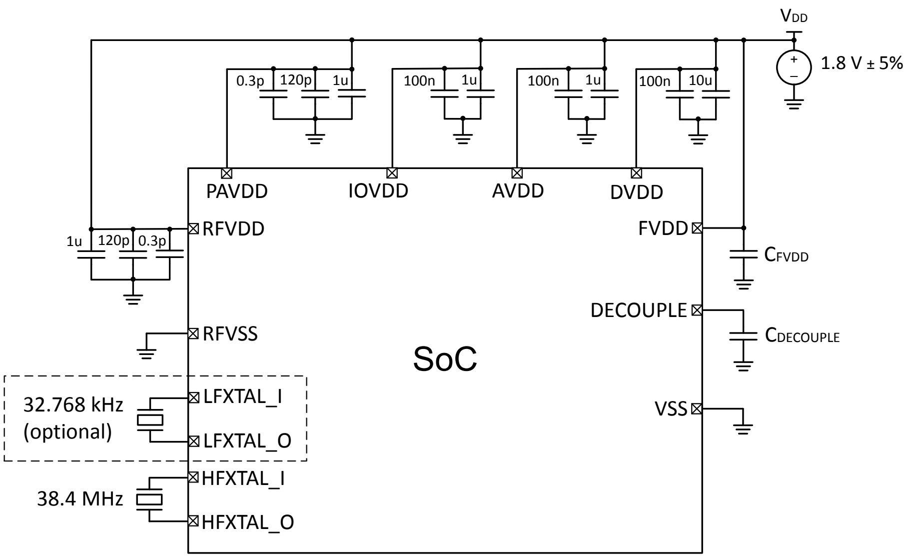


Figure 5.2. Single Supply (1.8 V ± 5%)

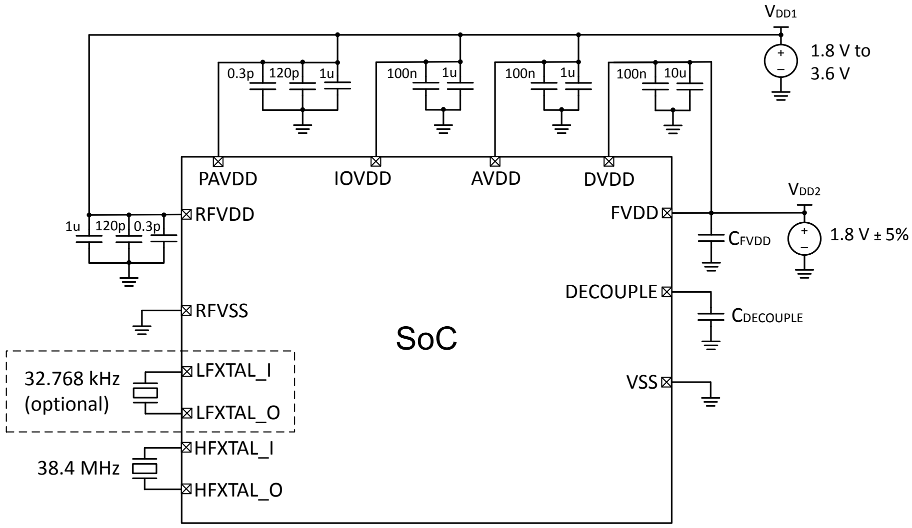


Figure 5.3. Dual Supply

5.2 External Flash Memory

Connections for OPNs using external memory are shown in Figure 5.4 External 1.8 V SPI Flash Connection on page 91. The diagram shows an example where the on-chip flash supply regulator is used to supply FVDD. FVDD may also be powered from an external 1.8 V regulator.

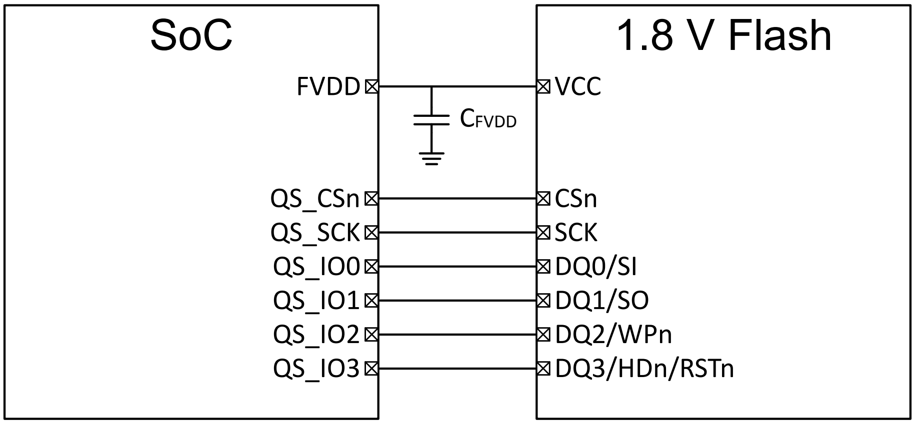


Figure 5.4. External 1.8 V SPI Flash Connection

5.3 LED Pre-Driver

Typical LED pre-driver circuitry is shown in Figure 5.5 LED Pre-Driver on page 92. The figure shows only one LED string, but supports up to two, connected in the same manner. Component values may be different, depending on the power design and requirements of the system.

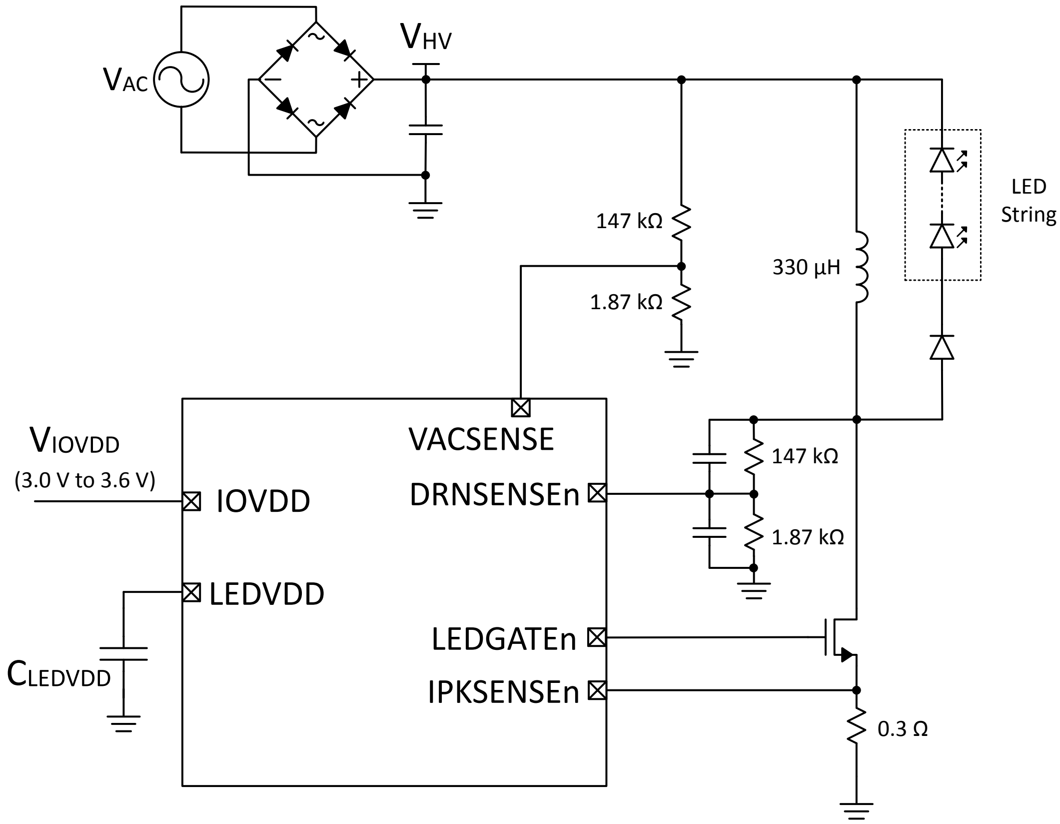


Figure 5.5. LED Pre-Driver

5.4 RF 2.4 GHz Matching Network

The RF matching network circuit diagram used for RF characterization is shown in Figure 5.6 Typical RF Impedance-Matching Network Circuit on page 93. Typical component values are shown in Table 5.1 Component Values on page 93. Refer to the development board Bill of Materials for specific part recommendations including tolerance, component size, recommended manufacturer, and recommended part number.

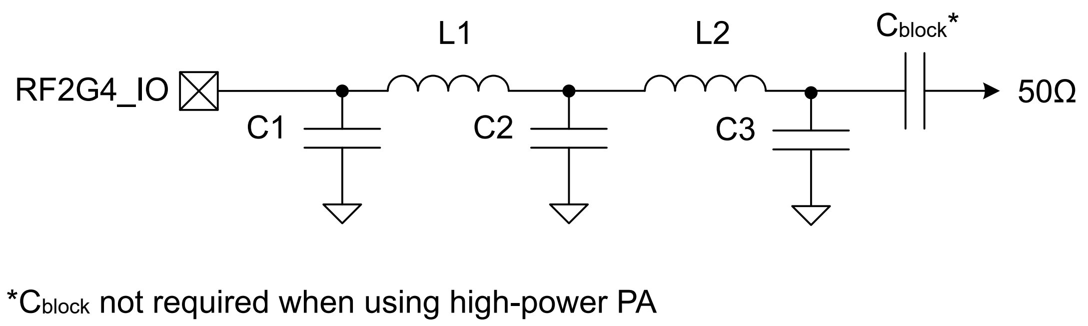


Figure 5.6. Typical RF Impedance-Matching Network Circuit

Table 5.1. Component Values

Designator	Value (QFN32 Package)	Value (QFN40 Package)
C1	1.9 pF	1.9 pF
L1	1.9 nH	1.9 nH
C2	1.8 pF	1.8 pF
L2	1.8 nH	1.8 nH
C3	N/A	N/A
C_{block} (0 dBm PA only)	18 pF	18 pF

5.5 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002.3: "EFR32 Wireless Gecko Series 3 Hardware Design Considerations" contains detailed information on these connections. Application notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 QFN40 Max GPIO Device Pinout

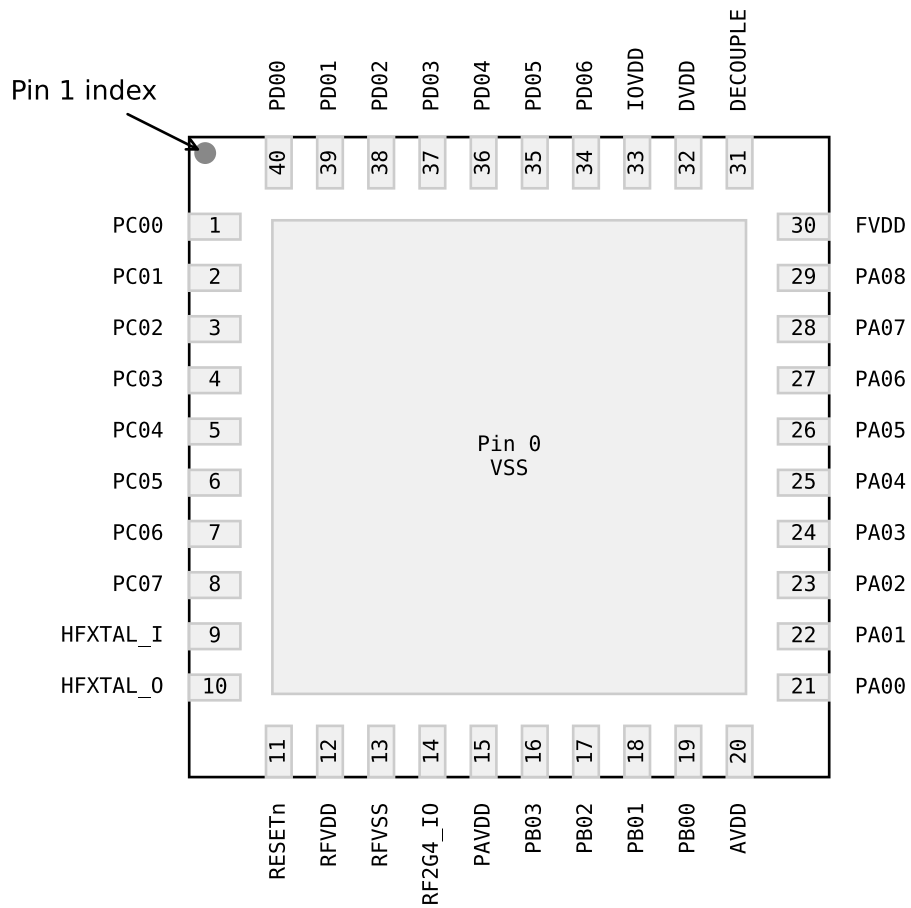


Figure 6.1. QFN40 Max GPIO Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.5 Alternate Function Table, 6.6 Analog Peripheral Connectivity, and 6.7 Digital Peripheral Connectivity.

Table 6.1. QFN40 Max GPIO Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	PC07	8	GPIO
HFXTAL_I	9	High Frequency Crystal Input	HFXTAL_O	10	High Frequency Crystal Output

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	11	Reset Pin. The RESETn pin is internally pulled up to DVDD.	RFVDD	12	Radio power supply
RFVSS	13	Radio Ground	RF2G4_IO	14	2.4 GHz RF input/output
PAVDD	15	Power Amplifier (PA) power supply	PB03	16	GPIO
PB02	17	GPIO	PB01	18	GPIO
PB00	19	GPIO	AVDD	20	Analog power supply
PA00	21	GPIO	PA01	22	GPIO
PA02	23	GPIO	PA03	24	GPIO
PA04	25	GPIO	PA05	26	GPIO
PA06	27	GPIO	PA07	28	GPIO
PA08	29	GPIO	FVDD	30	Decouple output for flash voltage regulator. External decoupling is required at this pin.
DECOUPLE	31	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	DVDD	32	Digital power supply
IOVDD	33	I/O power supply	PD06	34	GPIO
PD05	35	GPIO	PD04	36	GPIO
PD03	37	GPIO	PD02	38	GPIO
PD01	39	GPIO	PD00	40	GPIO

6.2 QFN40 with External Flash Device Pinout

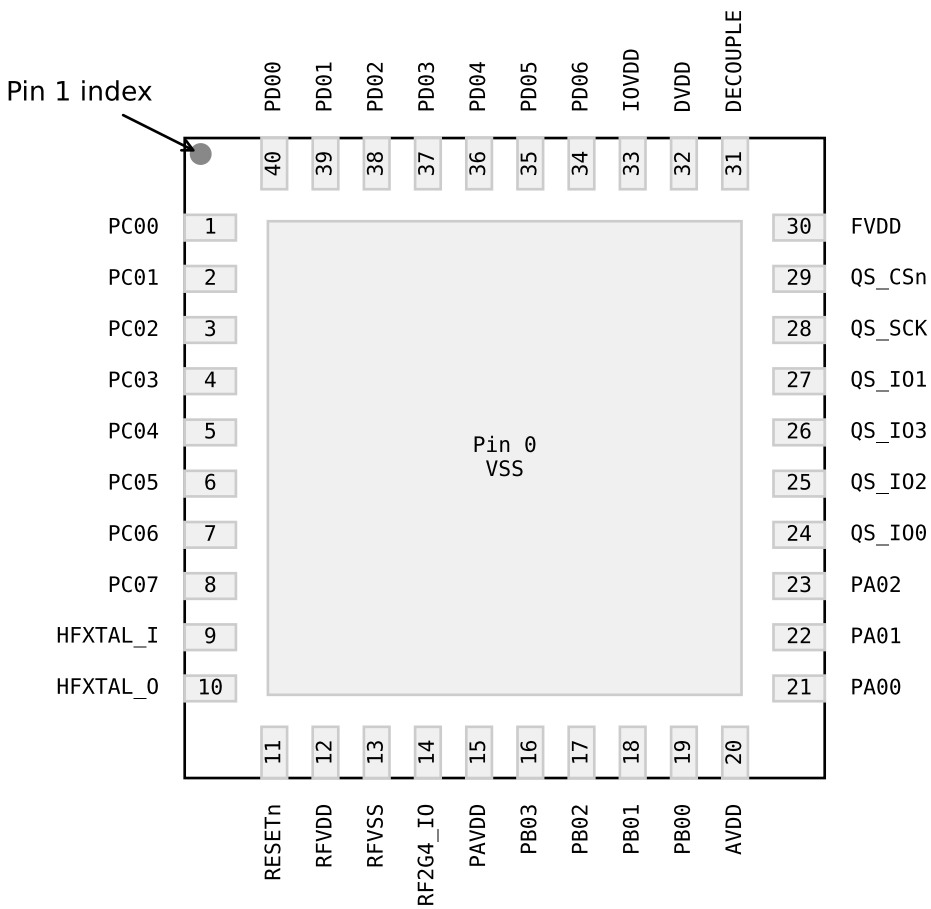


Figure 6.2. QFN40 with External Flash Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.5 Alternate Function Table, 6.6 Analog Peripheral Connectivity, and 6.7 Digital Peripheral Connectivity.

Table 6.2. QFN40 with External Flash Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	PC07	8	GPIO
HFXTAL_I	9	High Frequency Crystal Input	HFXTAL_O	10	High Frequency Crystal Output
RESETn	11	Reset Pin. The RESETn pin is internally pulled up to DVDD.	RFVDD	12	Radio power supply

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RFVSS	13	Radio Ground	RF2G4_IO	14	2.4 GHz RF input/output
PAVDD	15	Power Amplifier (PA) power supply	PB03	16	GPIO
PB02	17	GPIO	PB01	18	GPIO
PB00	19	GPIO	AVDD	20	Analog power supply
PA00	21	GPIO	PA01	22	GPIO
PA02	23	GPIO	QS_IO0	24	Quad SPI Data I/O 0
QS_IO2	25	Quad SPI Data I/O 2	QS_IO3	26	Quad SPI Data I/O 3
QS_IO1	27	Quad SPI Data I/O 1	QS_SCK	28	Quad SPI Clock
QS_CSn	29	Quad SPI Chip Select	FVDD	30	Decouple output for flash voltage regulator. External decoupling is required at this pin.
DECOUPLE	31	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	DVDD	32	Digital power supply
IOVDD	33	I/O power supply	PD06	34	GPIO
PD05	35	GPIO	PD04	36	GPIO
PD03	37	GPIO	PD02	38	GPIO
PD01	39	GPIO	PD00	40	GPIO

6.3 QFN32 Max GPIO Device Pinout

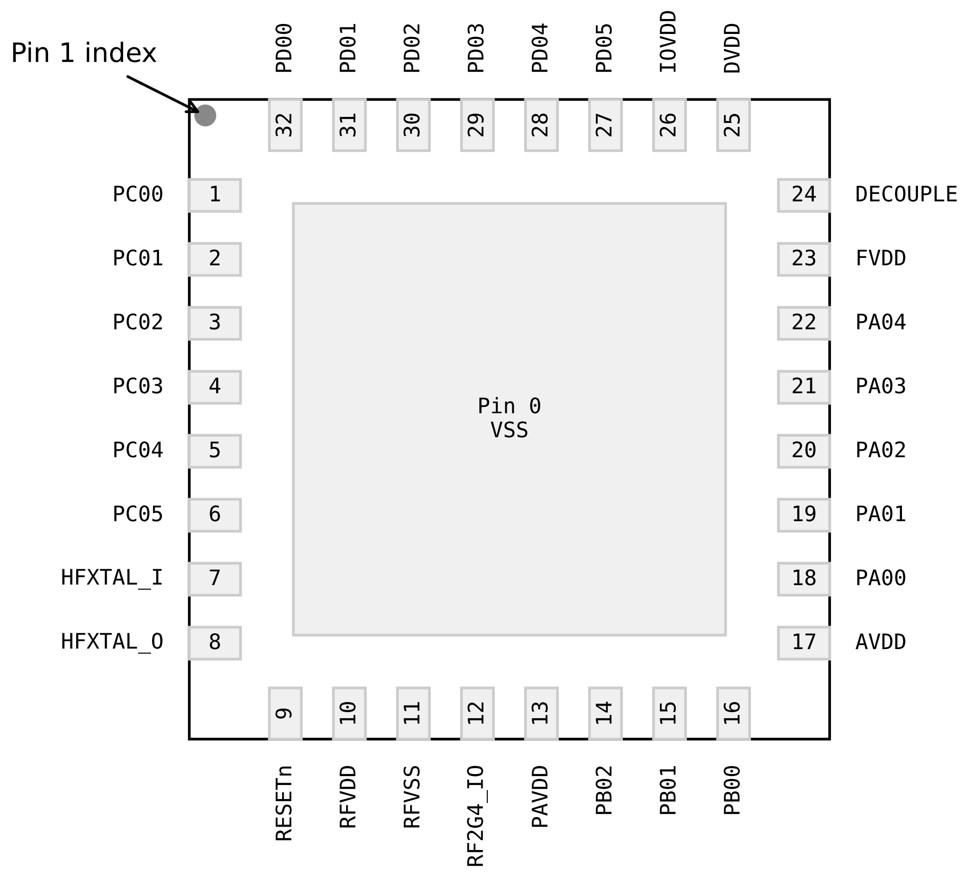


Figure 6.3. QFN32 Max GPIO Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.5 Alternate Function Table, 6.6 Analog Peripheral Connectivity, and 6.7 Digital Peripheral Connectivity.

Table 6.3. QFN32 Max GPIO Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
HFXTAL_I	7	High Frequency Crystal Input	HFXTAL_O	8	High Frequency Crystal Output
RESETn	9	Reset Pin. The RESETn pin is internally pulled up to DVDD.	RFVDD	10	Radio power supply
RFVSS	11	Radio Ground	RF2G4_IO	12	2.4 GHz RF input/output

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PAVDD	13	Power Amplifier (PA) power supply	PB02	14	GPIO
PB01	15	GPIO	PB00	16	GPIO
AVDD	17	Analog power supply	PA00	18	GPIO
PA01	19	GPIO	PA02	20	GPIO
PA03	21	GPIO	PA04	22	GPIO
FVDD	23	Decouple output for flash voltage regulator. External decoupling is required at this pin.	DECOUPLE	24	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
DVDD	25	Digital power supply	IOVDD	26	I/O power supply
PD05	27	GPIO	PD04	28	GPIO
PD03	29	GPIO	PD02	30	GPIO
PD01	31	GPIO	PD00	32	GPIO

6.4 QFN32 with LED Pre-Drive Device Pinout

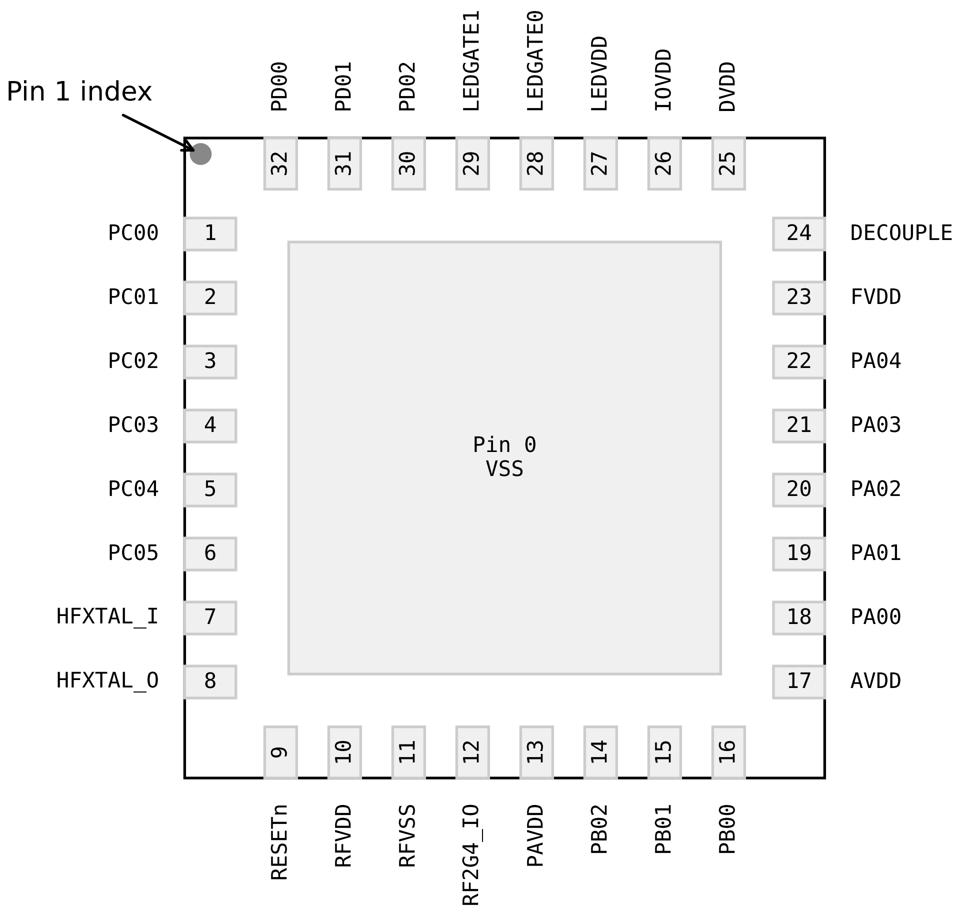


Figure 6.4. QFN32 with LED Pre-Drive Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.5 Alternate Function Table, 6.6 Analog Peripheral Connectivity, and 6.7 Digital Peripheral Connectivity.

Table 6.4. QFN32 with LED Pre-Drive Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
HFXTAL_I	7	High Frequency Crystal Input	HFXTAL_O	8	High Frequency Crystal Output
RESETn	9	Reset Pin. The RESETn pin is internally pulled up to DVDD.	RFVDD	10	Radio power supply
RFVSS	11	Radio Ground	RF2G4_IO	12	2.4 GHz RF input/output

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PAVDD	13	Power Amplifier (PA) power supply	PB02	14	GPIO
PB01	15	GPIO	PB00	16	GPIO
AVDD	17	Analog power supply	PA00	18	GPIO
PA01	19	GPIO	PA02	20	GPIO
PA03	21	GPIO	PA04	22	GPIO
FVDD	23	Decouple output for flash voltage regulator. External decoupling is required at this pin.	DECOUPLE	24	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
DVDD	25	Digital power supply	IOVDD	26	I/O power supply
LEDVDD	27	LED predrive boost supply	LEDGATE0	28	LED predrive gate driver 0
LEDGATE1	29	LED predrive gate driver 1	PD02	30	GPIO
PD01	31	GPIO	PD00	32	GPIO

6.5 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows GPIO pins with support for dedicated functions across the different package options.

Table 6.5. GPIO Alternate Function Table

GPIO	Alternate Functions	QFN40 Max GPIO Package[1]	QFN40 with External Flash Package[2]	QFN32 Max GPIO Package[3]	QFN32 with LED Pre-Drive Package[4]
PA00	ADC0.VREFP	Yes	Yes	Yes	Yes
PA01	GPIO.SWCLK	Yes	Yes	Yes	Yes
PA02	GPIO.SWDIO	Yes	Yes	Yes	Yes
PA03	GPIO.SWV	Yes		Yes	Yes
	GPIO.TDO	Yes		Yes	Yes
	GPIO.TRACEDATA0	Yes		Yes	Yes
PA04	GPIO.TDI	Yes		Yes	Yes
	GPIO.TRACECLK	Yes		Yes	Yes
PA05	GPIO.TRACEDATA1	Yes			
	GPIO.EM4WU0	Yes			
PA06	GPIO.TRACEDATA2	Yes			
PA07	GPIO.TRACEDATA3	Yes			
PB01	ETAMPDET.ETAMPIN0	Yes	Yes	Yes	Yes
	GPIO.EM4WU3	Yes	Yes	Yes	Yes
PB03	GPIO.EM4WU4	Yes	Yes		
PC00	ETAMPDET.ETAMPIN1	Yes	Yes	Yes	Yes
	GPIO.EM4WU6	Yes	Yes	Yes	Yes
PC01	ETAMPDET.ETAMPOUT0	Yes	Yes	Yes	Yes
PC02	ETAMPDET.ETAMPOUT1	Yes	Yes	Yes	Yes
PC05	GPIO.EM4WU7	Yes	Yes	Yes	Yes
PC07	GPIO.EM4WU8	Yes	Yes		
PD00	LFXO.LFXTAL_O	Yes	Yes	Yes	Yes
PD01	LFXO.LFXTAL_I	Yes	Yes	Yes	Yes
	LFXO.LF_EXTCLK	Yes	Yes	Yes	Yes
PD02	GPIO.EM4WU9	Yes	Yes	Yes	Yes
PD05	GPIO.EM4WU10	Yes	Yes	Yes	

Note:
1. QFN40 Max GPIO Package includes OPNs SiBG301M104LGLB0 and SiBG301M104LILB0
2. QFN40 with External Flash Package includes OPN SiBG301M104XILB0
3. QFN32 Max GPIO Package includes OPNs SiBG301M104LGHB0 and SiBG301M104LIHB0
4. QFN32 with LED Pre-Drive Package includes OPNs SiBG301M114KGHB0 and SiBG301M114KIHB0

6.6 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIOs. The following table indicates which peripherals are available on each GPIO port. When a differential connection is being used, positive inputs are restricted to the EVEN pins and negative inputs are restricted to the ODD pins. When a single-ended connection is being used, positive input is available on all pins. See the device reference manual for more details on the ABUS and analog peripherals. Note that some functions may not be available on all device variants.

Table 6.6. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACMP1	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
LEDDRV0	DRNSENSE					Yes	Yes	Yes	Yes
	IPKSENSE					Yes	Yes	Yes	Yes
	VACSENSE					Yes	Yes	Yes	Yes

6.7 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIOs. The following table indicates which peripherals are available on each GPIO port. Note that some functions may not be available on all device variants.

Table 6.7. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
ACMP1.DIGOUT	Available	Available	Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUSART0.CS	Available	Available		
EUSART0.CTS	Available	Available		
EUSART0.RTS	Available	Available		
EUSART0.RX	Available	Available		
EUSART0.SCLK	Available	Available		
EUSART0.TX	Available	Available		
EUSART1.CS	Available	Available	Available	Available
EUSART1.CTS	Available	Available	Available	Available
EUSART1.RTS	Available	Available	Available	Available
EUSART1.RX	Available	Available	Available	Available
EUSART1.SCLK	Available	Available	Available	Available
EUSART1.TX	Available	Available	Available	Available
EUSART2.CS			Available	Available
EUSART2.CTS			Available	Available
EUSART2.RTS			Available	Available
EUSART2.RX			Available	Available
EUSART2.SCLK			Available	Available
EUSART2.TX			Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
I2C2.SCL			Available	Available
I2C2.SDA			Available	Available
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
LFXO.LFXO_CLK_LV_RAW			Available	Available
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PCNT0.S0IN	Available	Available		
PCNT0.S1IN	Available	Available		
PIXELRZ0.RZ_TX_OUT	Available	Available	Available	Available
PIXELRZ1.RZ_TX_OUT	Available	Available	Available	Available
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
PRS.ASYNCH11			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
RAC.LNAEN	Available	Available	Available	Available
RAC.PAEN	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available	Available	Available
TIMER2.CC1	Available	Available	Available	Available
TIMER2.CC2	Available	Available	Available	Available
TIMER2.CC3	Available	Available	Available	Available
TIMER2.CC4	Available	Available	Available	Available
TIMER2.CC5	Available	Available	Available	Available
TIMER2.CC6	Available	Available	Available	Available
TIMER2.CDTI0	Available	Available	Available	Available
TIMER2.CDTI1	Available	Available	Available	Available
TIMER2.CDTI2	Available	Available	Available	Available
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CC3			Available	Available
TIMER3.CC4			Available	Available
TIMER3.CC5			Available	Available
TIMER3.CC6			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

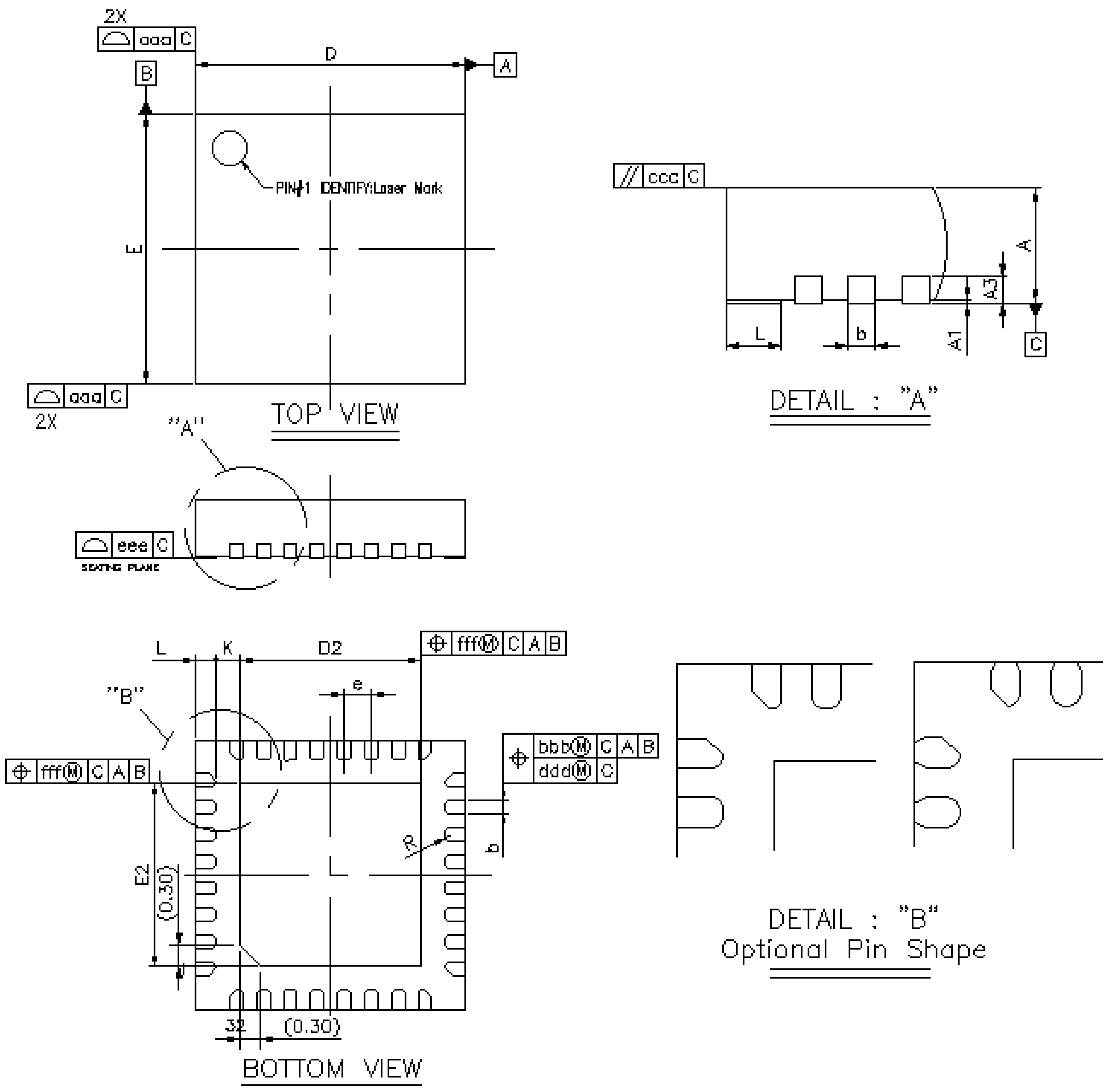


Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.40 BSC	
L	0.20	0.30	0.40
K	0.20	—	—
R	0.075	—	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QFN32 PCB Land Pattern

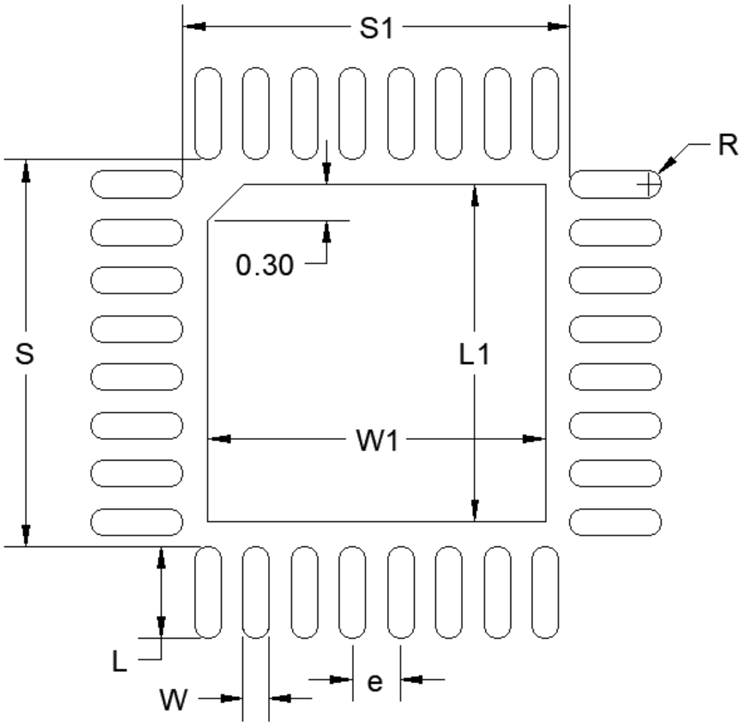


Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Typ
S	3.21
S1	3.21
e	0.40
W	0.22
L	0.76
W1	2.80
L1	2.80
R	0.11

Dimension	Typ

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
5. All pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
6. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.101 mm (4 mils).
8. The ratio of stencil aperture to land pad size can be 1:1 for the perimeter pads.
9. A 2x2 array of 1.10 mm square openings on a 1.30 mm pitch should be used for the center ground pad.
10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for small body components.
12. **Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.**

7.3 QFN32 Package Marking

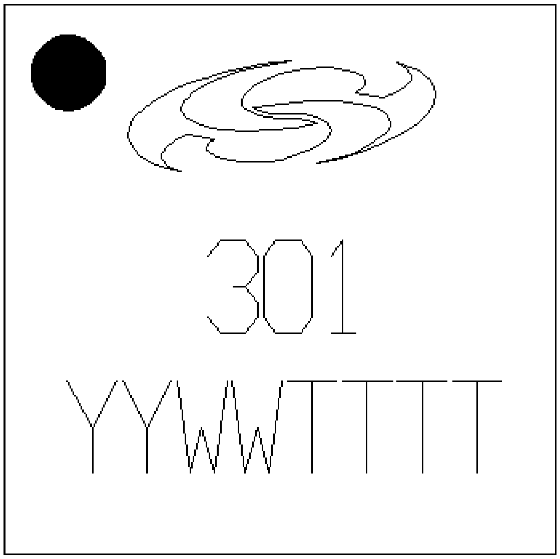


Figure 7.3. QFN32 Package Marking

The package marking consists of:

- Line 1:
  - 1-3) Product Code (301)
- Line 2:
  - 1-2) The last 2 digits of the assembly year
  - 3-4) The 2-digit workweek when the device was assembled
  - 5-8) A manufacturing trace code

8. QFN40 Package Specifications

8.1 QFN40 Package Dimensions

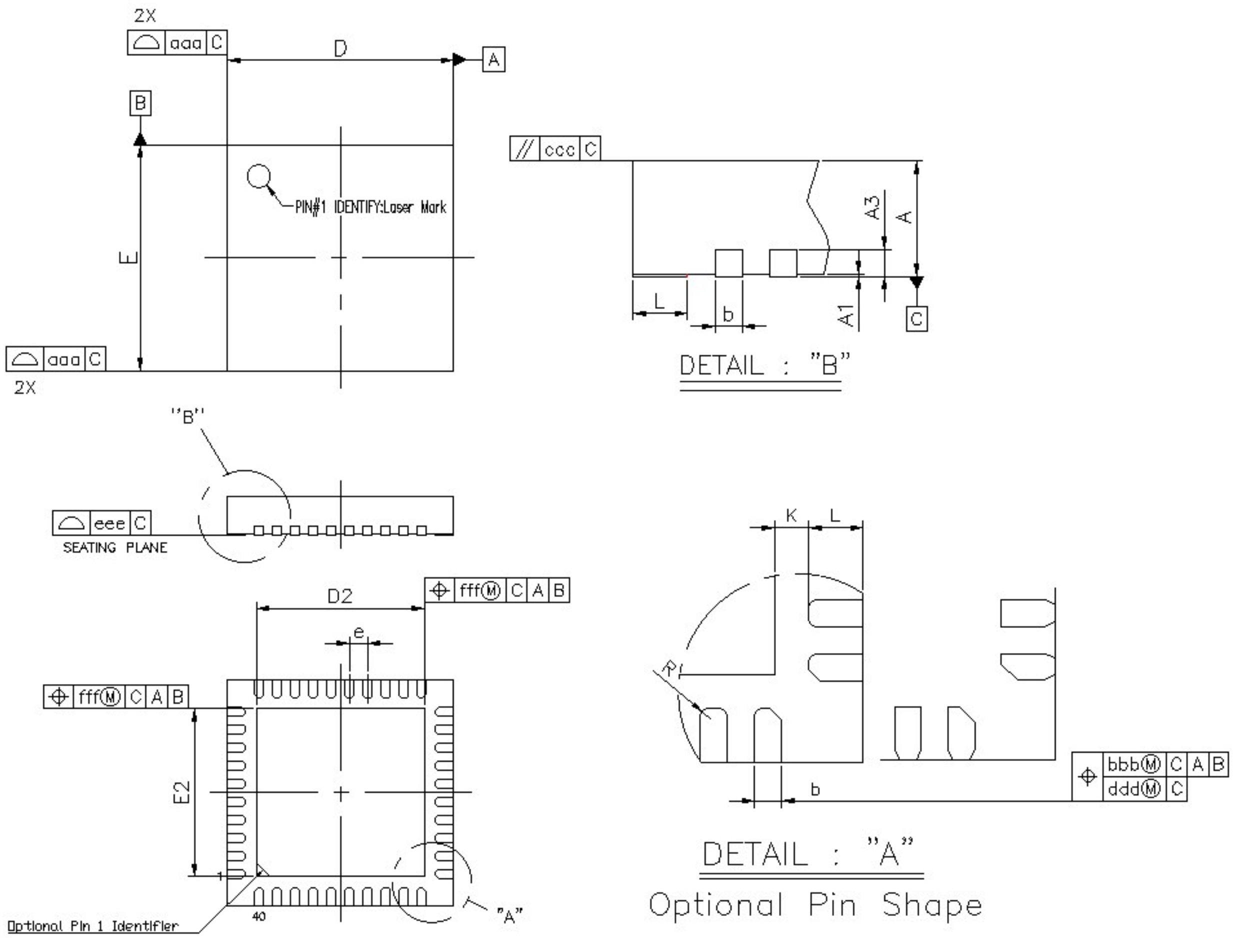


Figure 8.1. QFN40 Package Drawing

Table 8.1. QFN40 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.55	3.70	3.85
E2	3.55	3.70	3.85
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.075	—	—
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Package external pad (epad) may have pin one chamfer.

8.2 QFN40 PCB Land Pattern

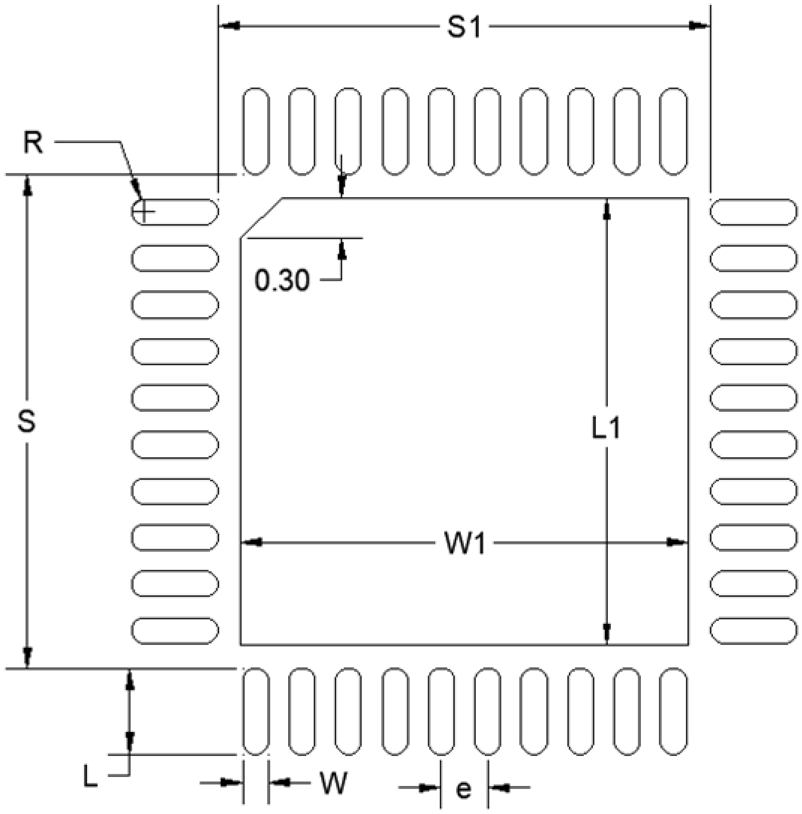


Figure 8.2. QFN40 PCB Land Pattern Drawing

Table 8.2. QFN40 PCB Land Pattern Dimensions

Dimension	Typ
S1	4.25
S	4.25
L1	3.85
W1	3.85
e	0.40
W	0.22
L	0.74
R	0.11

Dimension	Typ

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
4. The stencil thickness should be 0.101 mm (4 mils).
5. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
6. A 3x3 array of 0.90 mm square openings on a 1.20 mm pitch can be used for the center ground pad.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.
9. **Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.**

8.3 QFN40 Package Marking

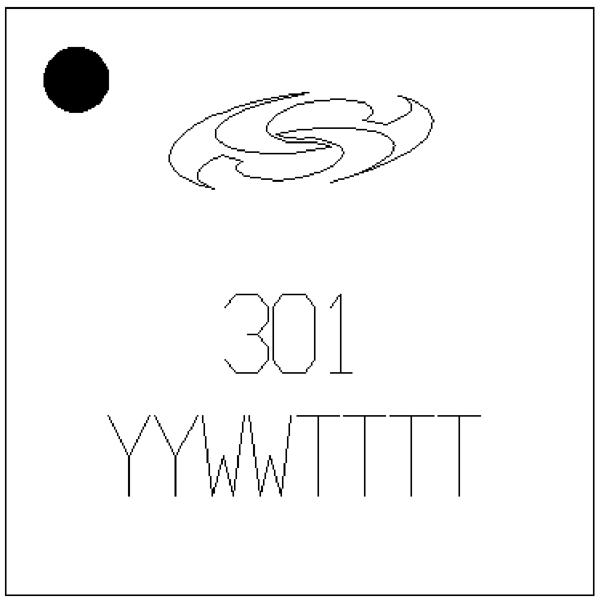


Figure 8.3. QFN40 Package Marking

The package marking consists of:
- Line 1:
  - 1-3) Product Code (301)
- Line 2:
  - 1-2) The last 2 digits of the assembly year
  - 3-4) The 2-digit workweek when the device was assembled
  - 5-8) A manufacturing trace code

9. Revision History

Revision 0.5

August, 2025

- Initial Revision

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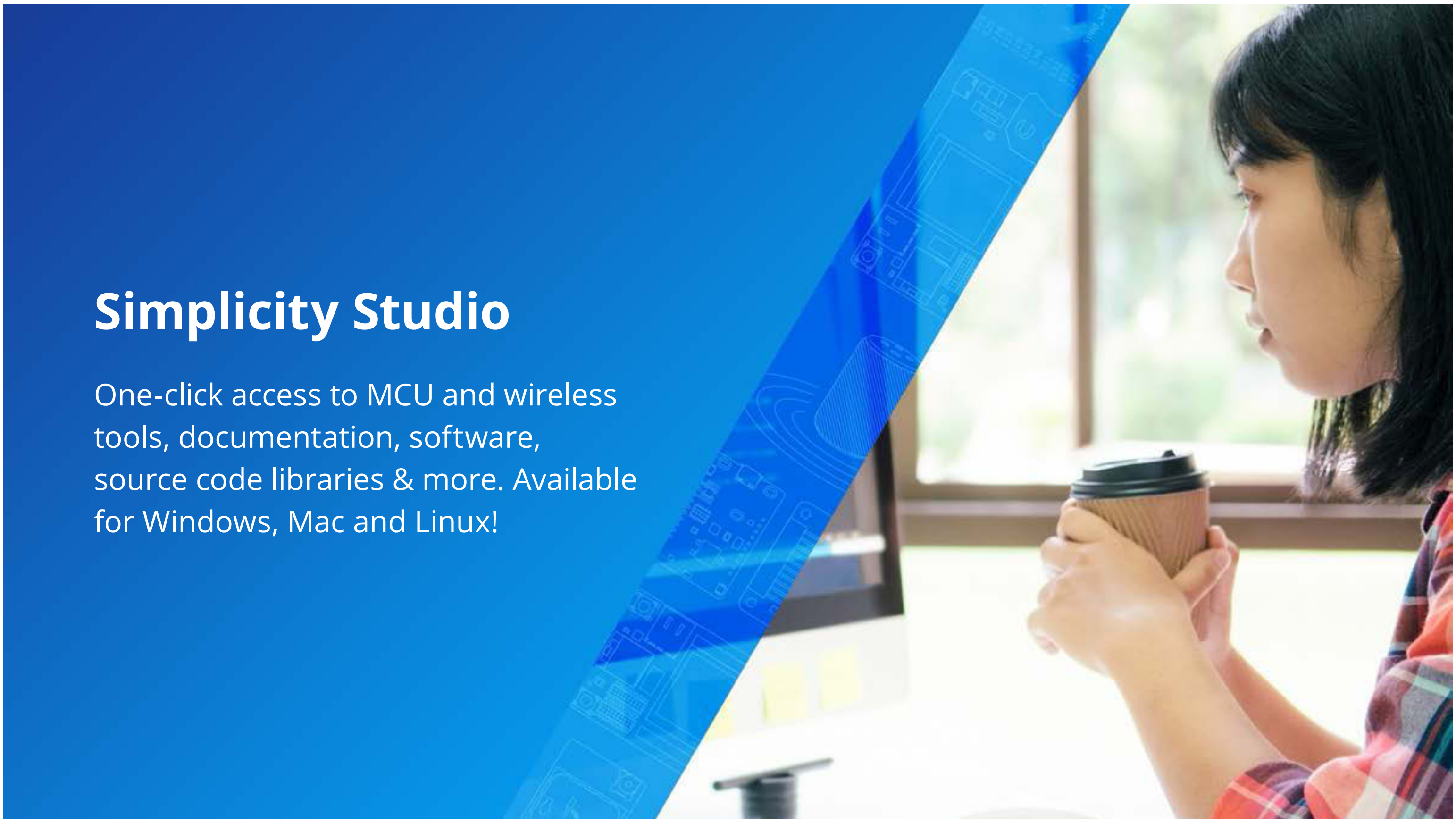

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