





# 74CBTLV3257

Quad 1-of-2 multiplexer/demultiplexer

Rev. 10 — 13 November 2025

Product data sheet

## 1. General description

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The 74CBTLV3257 provides a quad 1-of-2 high-speed multiplexer/demultiplexer with common select (S) and output enable ( $\overline{OE}$ ) inputs. The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. When pin  $\overline{OE}$  = LOW, one of the two switches is selected (low-impedance ON-state) with pin S. When pin  $\overline{OE}$  = HIGH, all switches are in the high-impedance OFF-state, independent of pin S.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire  $V_{CC}$  range from 2.3 V to 3.6 V.

To ensure the high-impedance OFF-state during power-up or power-down,  $\overline{OE}$  should be tied to the  $V_{CC}$  through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

## 2. Features and benefits

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- Supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- 5  $\Omega$  switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74CBTLV3257D</a>	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	<a href="#">SOT109-1</a>
<a href="#">74CBTLV3257DS</a>	-40 °C to +125 °C	SSOP16 [1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	<a href="#">SOT519-1</a>
<a href="#">74CBTLV3257PW</a>	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	<a href="#">SOT403-1</a>
<a href="#">74CBTLV3257BQ</a>	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	<a href="#">SOT763-1</a>
<a href="#">74CBTLV3257GU</a>	-40 °C to +125 °C	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 × 2.60 × 0.50 mm	<a href="#">SOT1161-1</a>

[1] Also known as QSOP16.

### 4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74CBTLV3257D	74CBTLV3257D
74CBTLV3257DS	TLV3257
74CBTLV3257PW	TLV3257
74CBTLV3257BQ	TV3257
74CBTLV3257GU	b57

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



Fig. 1. Logic diagram

## 6. Pinning information

### 6.1. Pinning



## 6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO16, (T)SSOP16 and DHVQFN16	XQFN16	
S	1	15	select input
1B1 to 4B1	2, 5, 11, 14	16, 3, 9, 12	B1 input/output
1B2 to 4B2	3, 6, 10, 13	1, 4, 8, 11	B2 input/output
1A to 4A	4, 7, 9, 12	2, 5, 7, 10	A input/output
GND	8	6	ground (0 V)
$\overline{\text{OE}}$	15	13	output enable input (active LOW)
V <sub>CC</sub>	16	14	supply voltage

## 7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Inputs		Function switch
$\overline{\text{OE}}$	S	
L	L	nA = nB1
L	H	nA = nB2
H	X	disconnect nA and nBn

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage	control inputs [1]	-0.5	+4.6	V
$V_{SW}$	switch voltage	enable and disable mode [2]	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	-50	-	mA
$I_{SK}$	switch clamping current	$V_I < -0.5$ V	-50	-	mA
$I_{SW}$	switch current	$V_{SW} = 0$ V to $V_{CC}$	-	$\pm 128$	mA
$I_{CC}$	supply current		-	+100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		SOT109-1 (SO16) SOT519-1 (SSOP16) SOT403-1 (TSSOP16) SOT763-1 (DHVQFN16) [3]	-	500	mW
		SOT1161-1 (XQFN16)	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.

[2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed

[3] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.

For SOT519-1 (SSOP16) packages:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package:  $P_{tot}$  derates linearly with 11.2 mW/K above 106 °C.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		2.3	3.6	V
$V_I$	input voltage		0	3.6	V
$V_{SW}$	switch voltage	enable and disable mode	0	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.6 V [1]	0	200	ns/V

[1] Applies to control signal levels.

## 10. Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.0 V	-	-	0.8	-	0.8	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
I <sub>I</sub>	input leakage current	pin $\overline{\text{OE}}$ , S; V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	-	±1	-	±20	µA
I <sub>S(OFF)</sub>	OFF-state leakage current	V <sub>CC</sub> = 3.6 V; see Fig. 2	-	-	±1	-	±20	µA
I <sub>S(ON)</sub>	ON-state leakage current	V <sub>CC</sub> = 3.6 V; see Fig. 3	-	-	±1	-	±20	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V	-	-	±10	-	±50	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>SW</sub> = GND or V <sub>CC</sub> ; V <sub>CC</sub> = 3.6 V; I <sub>O</sub> = 0 A	-	-	10	-	50	µA
ΔI <sub>CC</sub>	additional supply current	pin $\overline{\text{OE}}$ , S; V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; V <sub>SW</sub> = GND or V <sub>CC</sub> [2]	-	-	300	-	2000	µA
C <sub>I</sub>	input capacitance	pin $\overline{\text{OE}}$ , S; V <sub>CC</sub> = 3.3 V; V <sub>I</sub> = 0 V to 3.3 V	-	0.9	-	-	-	pF
C <sub>S(OFF)</sub>	OFF-state capacitance	V <sub>CC</sub> = 3.3 V; V <sub>I</sub> = 0 V to 3.3 V	-	5.2	-	-	-	pF
C <sub>S(ON)</sub>	ON-state capacitance	V <sub>CC</sub> = 3.3 V; V <sub>I</sub> = 0 V to 3.3 V	-	14.3	-	-	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

[2] One input at 3 V, other inputs at V<sub>CC</sub> or GND.

### 10.1. Test circuits



### 10.2. ON resistance

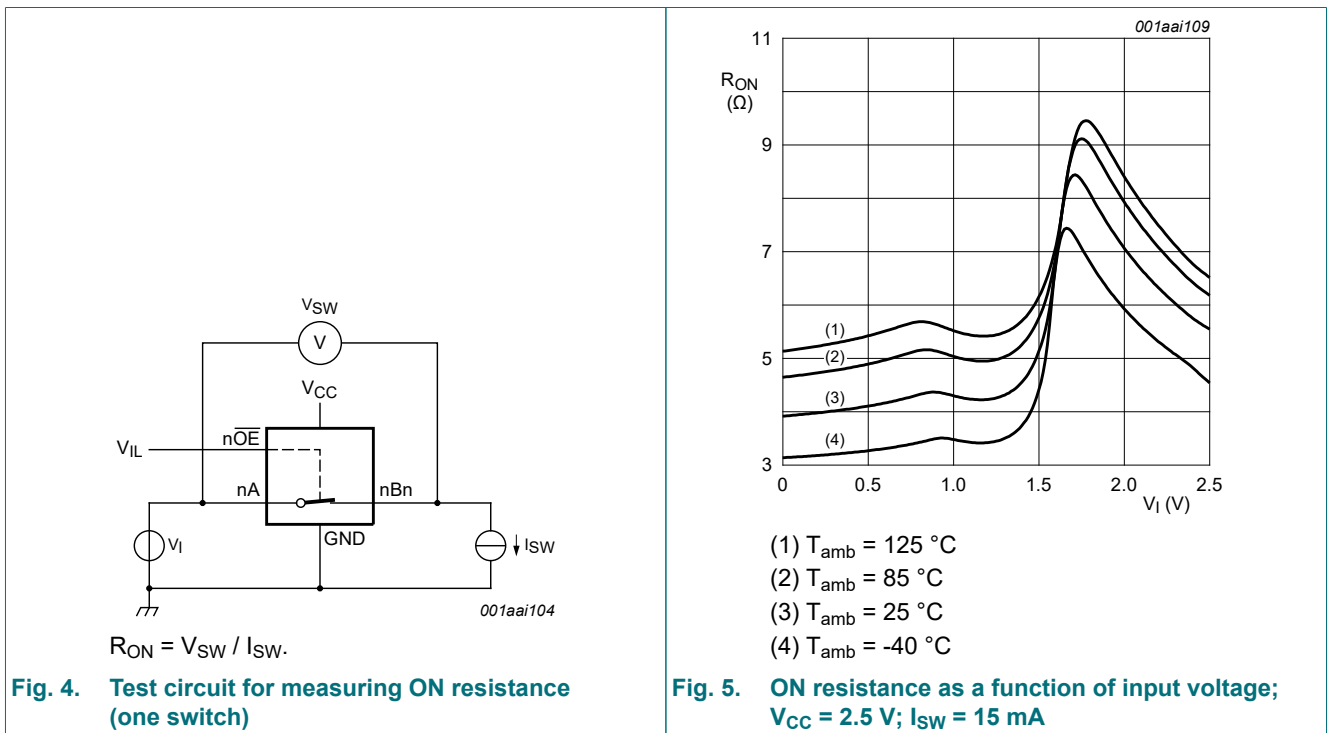
**Table 8. Resistance  $R_{ON}$**

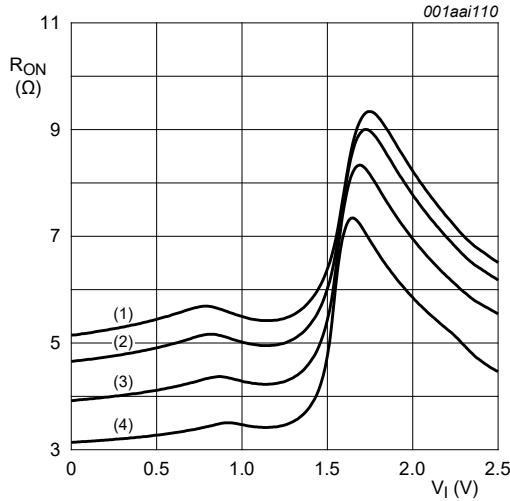
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 4.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$			$T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$		Unit
			Min	Typ[1]	Max	Min	Max	
$R_{ON}$	ON resistance	$V_{CC} = 2.3\text{ V to }2.7\text{ V};$ see Fig. 5 to Fig. 7 [2]						
		$I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$	-	4.2	8.0	-	15.0	$\Omega$
		$I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$	-	4.2	8.0	-	15.0	$\Omega$
		$I_{SW} = 15\text{ mA}; V_I = 1.7\text{ V}$	-	8.4	40.0	-	60.0	$\Omega$
		$V_{CC} = 3.0\text{ V to }3.6\text{ V};$ see Fig. 8 to Fig. 10						
		$I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$	-	4.0	7.0	-	11.0	$\Omega$
		$I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$	-	4.0	7.0	-	11.0	$\Omega$
$I_{SW} = 15\text{ mA}; V_I = 2.4\text{ V}$	-	6.2	15.0	-	25.5	$\Omega$		

- [1] Typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$  and nominal  $V_{CC}$ .
- [2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

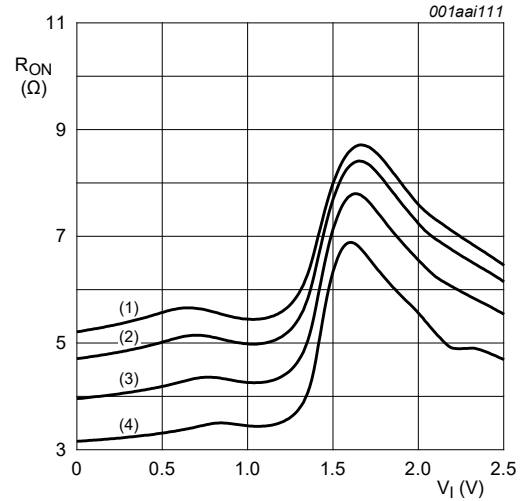
### 10.3. ON resistance test circuit and graphs





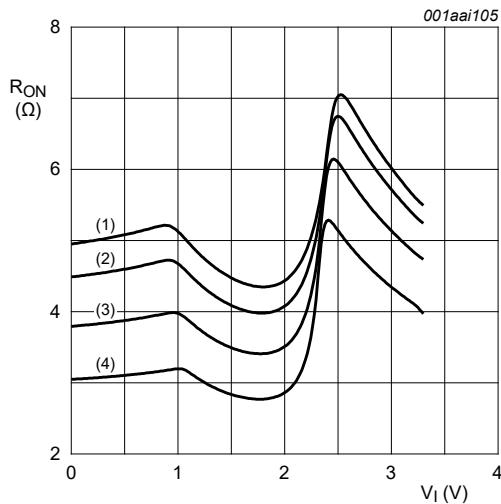
- (1)  $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

**Fig. 6.** ON resistance as a function of input voltage;  $V_{CC} = 2.5\text{ V}$ ;  $I_{SW} = 24\text{ mA}$



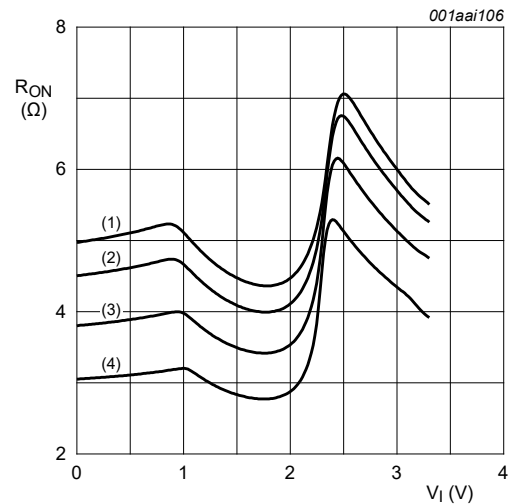
- (1)  $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

**Fig. 7.** ON resistance as a function of input voltage;  $V_{CC} = 2.5\text{ V}$ ;  $I_{SW} = 64\text{ mA}$



- (1)  $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

**Fig. 8.** ON resistance as a function of input voltage;  $V_{CC} = 3.3\text{ V}$ ;  $I_{SW} = 15\text{ mA}$



- (1)  $T_{amb} = 125\text{ }^{\circ}\text{C}$
- (2)  $T_{amb} = 85\text{ }^{\circ}\text{C}$
- (3)  $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (4)  $T_{amb} = -40\text{ }^{\circ}\text{C}$

**Fig. 9.** ON resistance as a function of input voltage;  $V_{CC} = 3.3\text{ V}$ ;  $I_{SW} = 24\text{ mA}$



- (1)  $T_{amb} = 125\text{ °C}$
- (2)  $T_{amb} = 85\text{ °C}$
- (3)  $T_{amb} = 25\text{ °C}$
- (4)  $T_{amb} = -40\text{ °C}$

Fig. 10. ON resistance as a function of input voltage;  $V_{CC} = 3.3\text{ V}$ ;  $I_{SW} = 64\text{ mA}$

## 11. Dynamic characteristics

Table 9. Dynamic characteristics

$GND = 0\text{ V}$ ; for test circuit see Fig. 13.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ[1]	Max	Min	Max	
$t_{pd}$	propagation delay	nA to nBn or nBn to nA; see Fig. 11 [2] [3]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.15	-	0.25	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	0.15	-	0.25	ns
		S to nA; see Fig. 11 [3]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.8	6.1	1.0	6.7	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.2	5.3	1.0	5.8	ns
$t_{en}$	enable time	$\overline{OE}$ to nA or nBn; see Fig. 12 [4]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.2	5.6	1.0	6.2	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	2.0	5.0	1.0	5.5	ns
		S to nBn; see Fig. 12 [4]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.5	6.1	1.0	6.7	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.0	5.3	1.0	5.8	ns

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t <sub>dis</sub>	disable time	OĒ to nA or nBn; see Fig. 12 [5]						
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.6	5.5	1.0	6.1	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.1	5.5	1.0	6.1	ns
		S to nBn; see Fig. 12 [5]						
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.6	4.8	1.0	5.3	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.2	4.5	1.0	5.0	ns

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C and at nominal V<sub>CC</sub>.
- [2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
- [3] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [4] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.
- [5] t<sub>dis</sub> is the same as t<sub>PHZ</sub> and t<sub>PLZ</sub>.

### 11.1. Waveforms and test circuit



Table 10. Measurement points

Supply voltage	Input			Output		
V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
3.0 V to 3.6 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.0 ns	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V



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Test data is given in [Table 11](#).

Definitions for test circuit:

R<sub>L</sub> = Load resistance;

C<sub>L</sub> = Load capacitance including jig and probe capacitance;

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>O</sub> of the pulse generator;

V<sub>EXT</sub> = External voltage for measuring switching times.

Fig. 13. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Load		V <sub>EXT</sub>		
V <sub>CC</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
2.3 V to 2.7 V	30 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
3.0 V to 3.6 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>

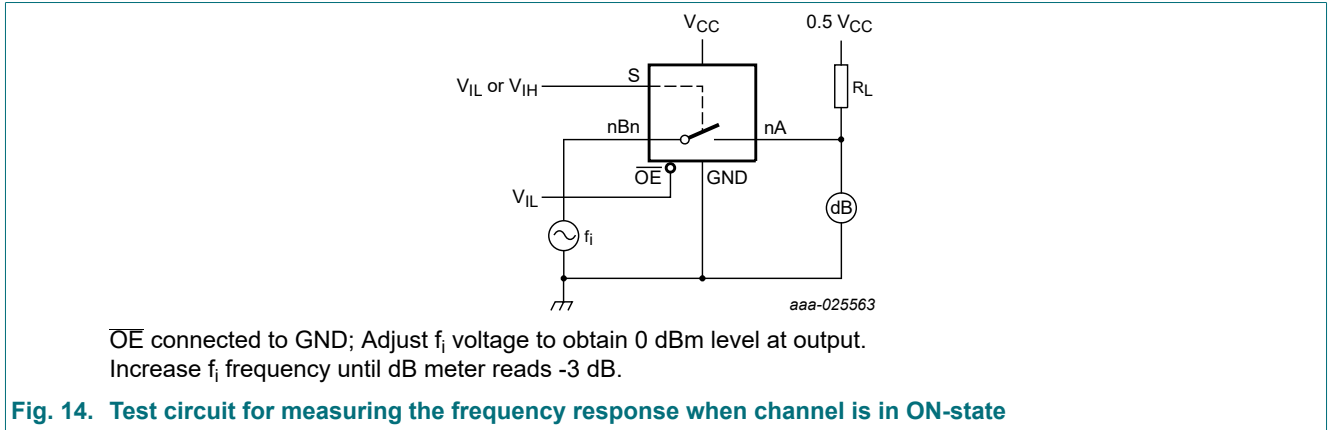
11.2. Additional dynamic characteristics

Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $V_I = GND$  or  $V_{CC}$  (unless otherwise specified);  $t_r = t_f \leq 2.5$  ns.

Symbol	Parameter	Conditions	$T_{amb} = 25\text{ }^\circ\text{C}$			Unit
			Min	Typ	Max	
$f_{(-3dB)}$	-3 dB frequency response	$V_{CC} = 3.3$ V; $R_L = 50\ \Omega$ ; see Fig. 14 [1]	-	398	-	MHz

[1]  $f_i$  is biased at  $0.5 \times V_{CC}$ .



12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Fig. 15. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1



Fig. 16. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



Fig. 17. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1



Fig. 18. Package outline SOT763-1 (DHVQFN16)

**XQFN16:** plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 x 2.60 x 0.50 mm

SOT1161-1



Fig. 19. Package outline SOT1161-1 (XQFN16)

## 13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLV3257 v.10	20251113	Product data sheet	-	74CBTLV3257 v.9
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 7</a>: Conditions for <math>V_{IH}</math> and <math>V_{IL}</math> have been extended.</li> </ul>			
74CBTLV3257 v.9	20240201	Product data sheet	-	74CBTLV3257 v.8
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li><a href="#">Fig. 15</a>, <a href="#">Fig. 17</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153</li> </ul>			
74CBTLV3257 v.8	20230321	Product data sheet	-	74CBTLV3257 v.7
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 5</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74CBTLV3257 v.7	20190409	Product data sheet	-	74CBTLV3257 v.6
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Link corrected in <a href="#">Section 11</a>.</li> </ul>			
74CBTLV3257 v.6	20171211	Product data sheet	-	74CBTLV3257 v.5
Modifications:	<ul style="list-style-type: none"> <li>Type number 74CBTLV3257GU (SOT1161-1 / XQFN16) added.</li> </ul>			
74CBTLV3257 v.5	20161111	Product data sheet	-	74CBTLV3257 v.4
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 11.2</a> added.</li> </ul>			
74CBTLV3257 v.4	20111216	Product data sheet	-	74CBTLV3257 v.3
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated.</li> </ul>			
74CBTLV3257 v.3	20110106	Product data sheet	-	74CBTLV3257 v.2
74CBTLV3257 v.2	20101126	Product data sheet	-	74CBTLV3257 v.1
74CBTLV3257 v.1	20100112	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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