



**THE DATASHEET OF
PESD5Z3.3-QX**





PESD36VS2UT-Q

Low capacitance unidirectional double ESD protection diode

6 May 2022

Product data sheet

1. General description

Low capacitance unidirectional double ElectroStatic Discharge (ESD) protection diode in a SOT23 (TO-236AB) small Surface-Mounted Device (SMD) plastic package designed to protect up to two signal lines from the damage caused by ESD and other transients.

2. Features and benefits

- Unidirectional ESD protection of two lines
- Low diode capacitance: $C_d = 17 \text{ pF}$
- Max. peak pulse power: $P_{PP} = 160 \text{ W}$
- Low clamping voltage: $V_{CL} = 55 \text{ V}$
- Ultra low leakage current: $I_{RM} \leq 1 \text{ uA}$
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); $I_{PP} = 2.5 \text{ A}$
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- SIM card protection
- Portable electronics
- Communication systems
- 10/100 Mbit/s Ethernet

4. Quick reference data

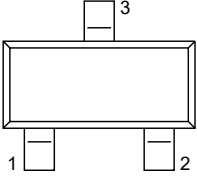
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		[1]	-	-	36	V
C_d	diode capacitance	$f = 1 \text{ MHz}; V_R = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	17	35	pF

[1] Measured from pin 1 or 2 to pin 3.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 <p style="text-align: center;">SOT23</p>	 <p style="text-align: center;"><small>006aaa154</small></p>
2	K2	cathode (diode 2)		
3	A	common anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD36VS2UT-Q	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PESD36VS2UT-Q	L F %

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{PPM}	rated peak pulse power	$t_p = 8/20 \mu s$	[1] [2]	-	160	W
I_{PPM}	rated peak pulse current		[1] [2]	-	2.5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[3] [2]	-	30	kV
		machine model	[2]	-	400	V
		MIL-STD-883 (human body model)		-	8	kV

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Measured from pin 1 or 2 to pin 3.

[3] Device stressed with ten non-repetitive ESD pulses.

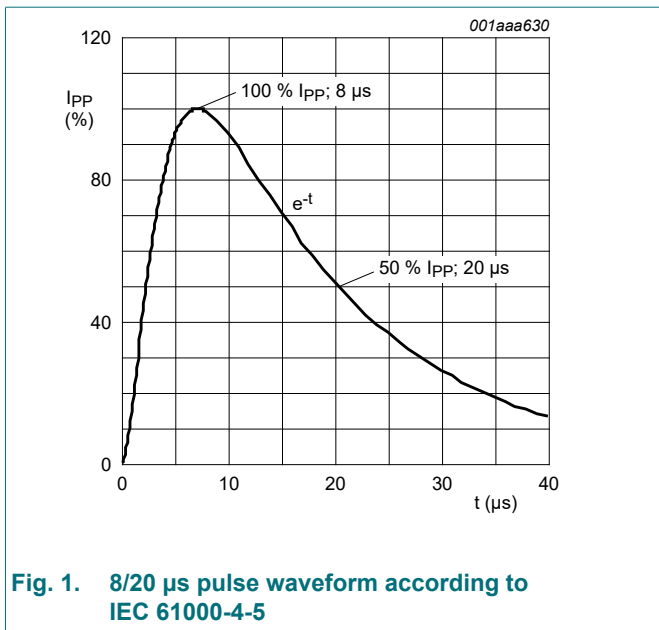


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

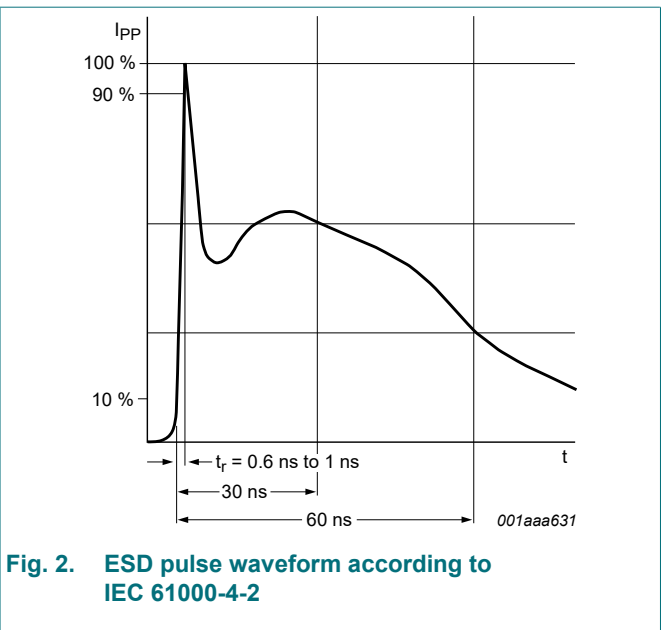


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

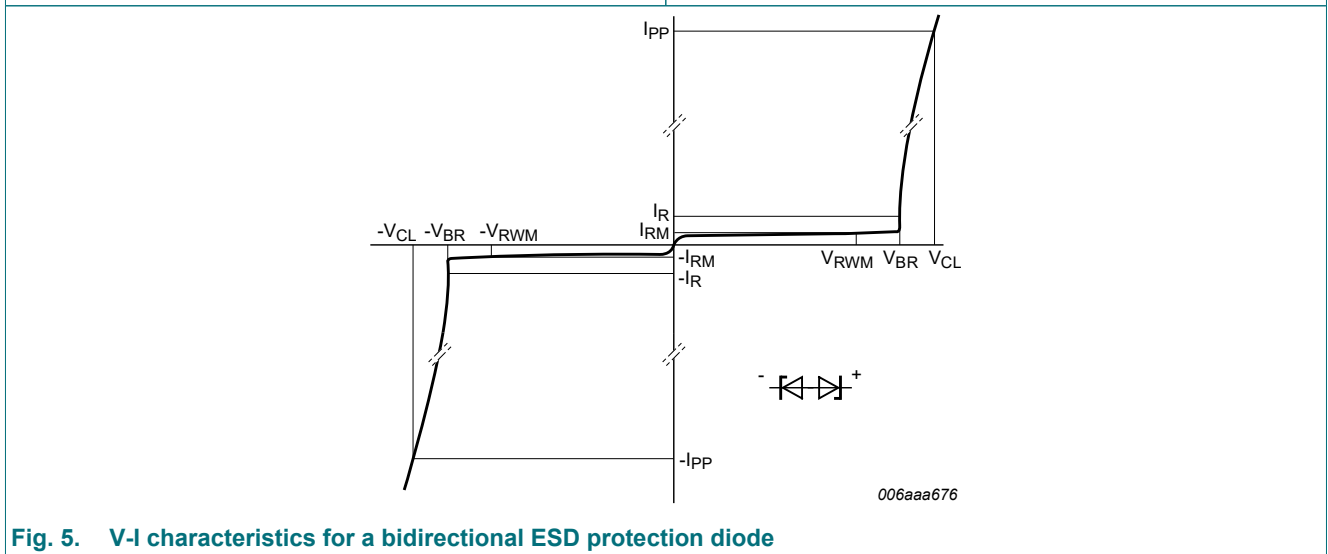
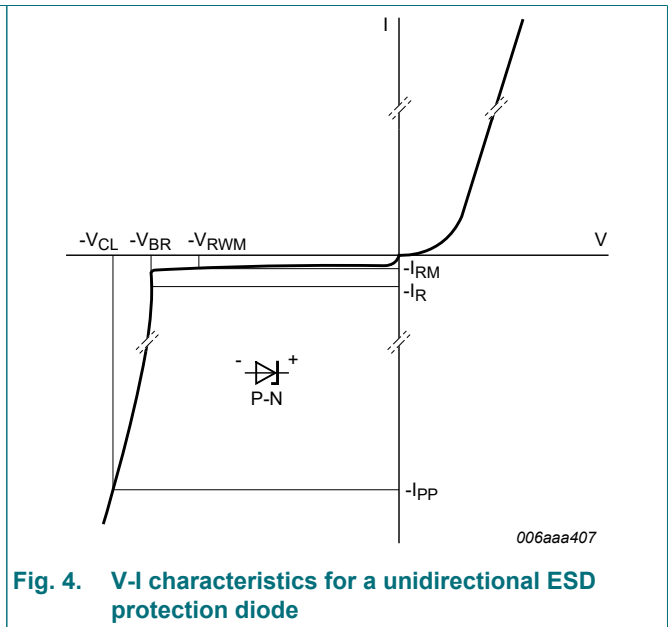
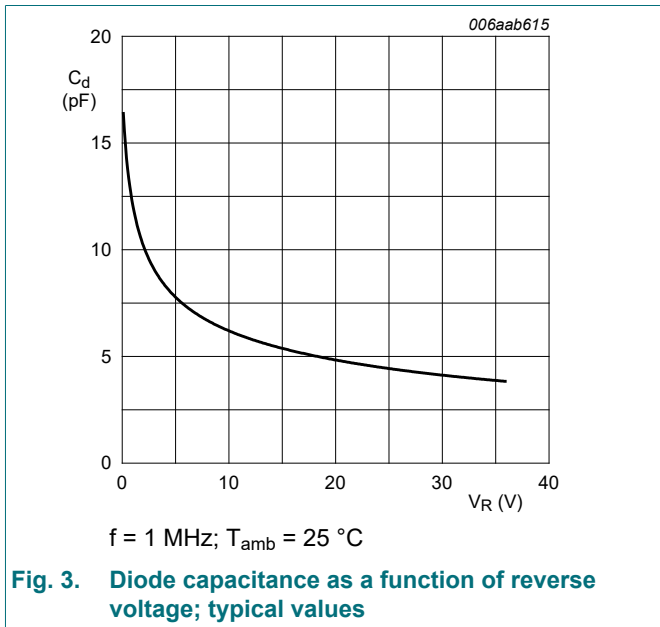
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		[1]	-	-	36	V
V_{BR}	breakdown voltage	$I_R = 5 \text{ mA}$; $T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	40	44	-	V
I_{RM}	reverse leakage current	$V_{RWM} = 30 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	0.02	1	μA
C_d	diode capacitance	$f = 1 \text{ MHz}$; $V_R = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	17	35	pF
V_{CL}	clamping voltage	$I_{PP} = 1 \text{ A}$; $T_{amb} = 25 \text{ }^\circ\text{C}$	[1] [2]	-	55	60	V
R_{diff}	differential resistance	$I_R = 0.5 \text{ mA}$; $T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	-	300	Ω

[1] Measured from pin 1 or 2 to pin 3.

[2] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.



Low capacitance unidirectional double ESD protection diode

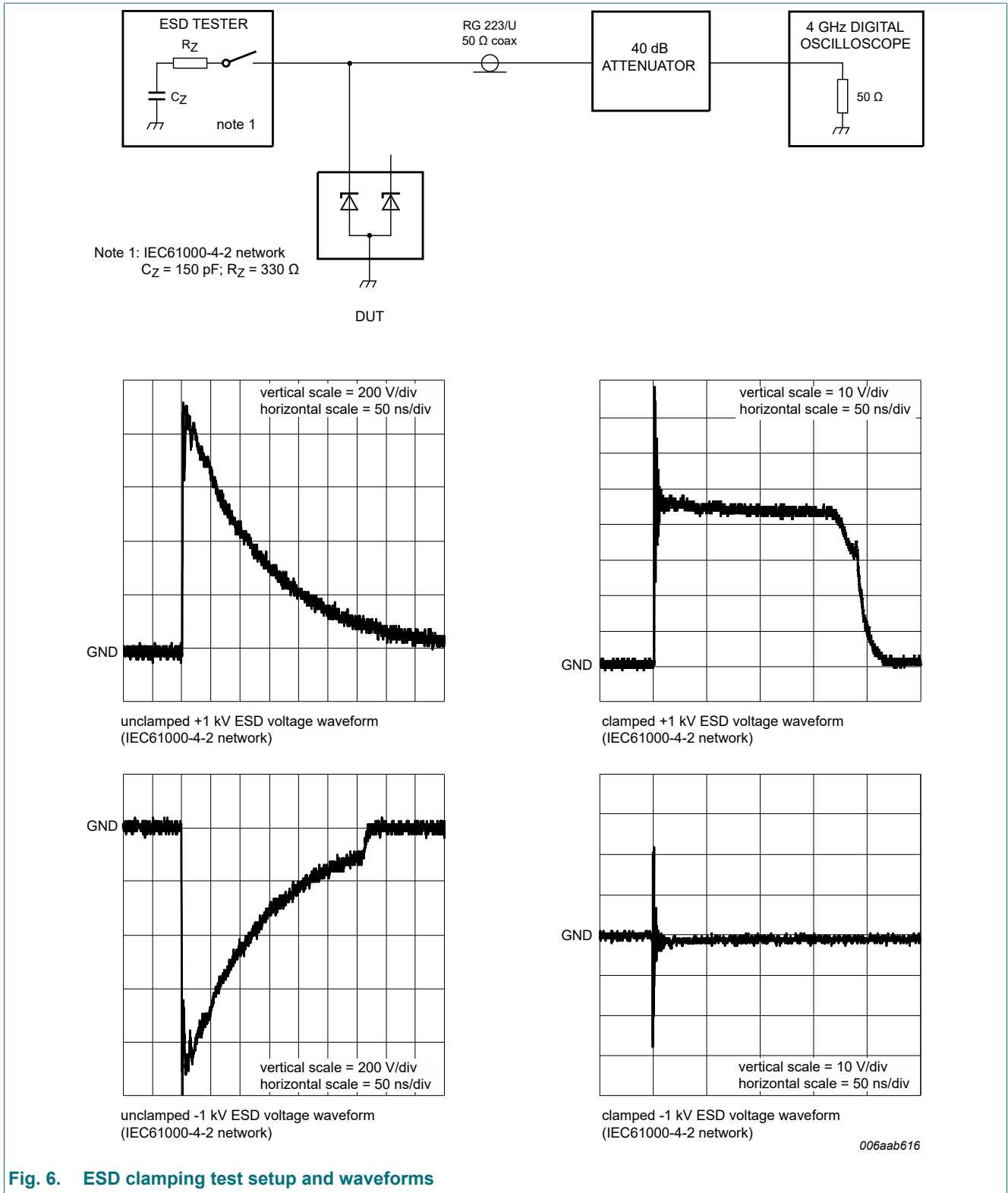
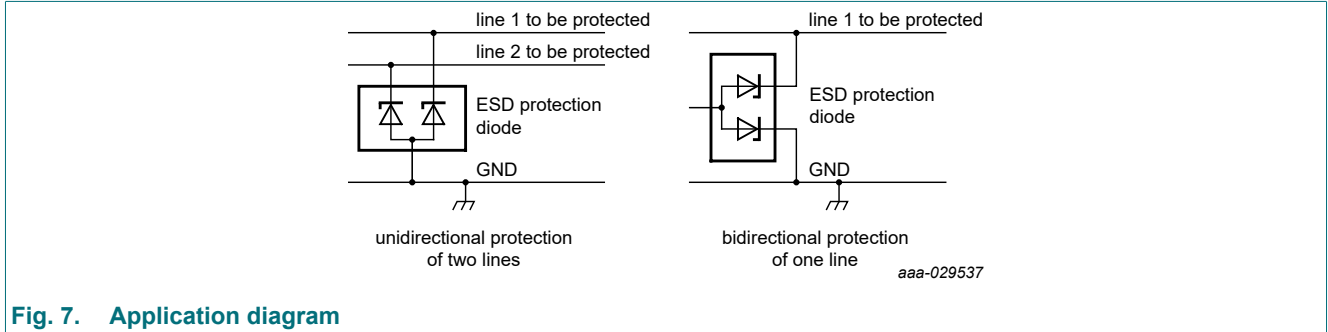


Fig. 6. ESD clamping test setup and waveforms

10. Application information

The device is designed for the protection of up to two unidirectional data or signal lines from the damage caused by ESD and surge pulses. The devices may be used on lines where the signal polarities are either positive or negative with respect to ground.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

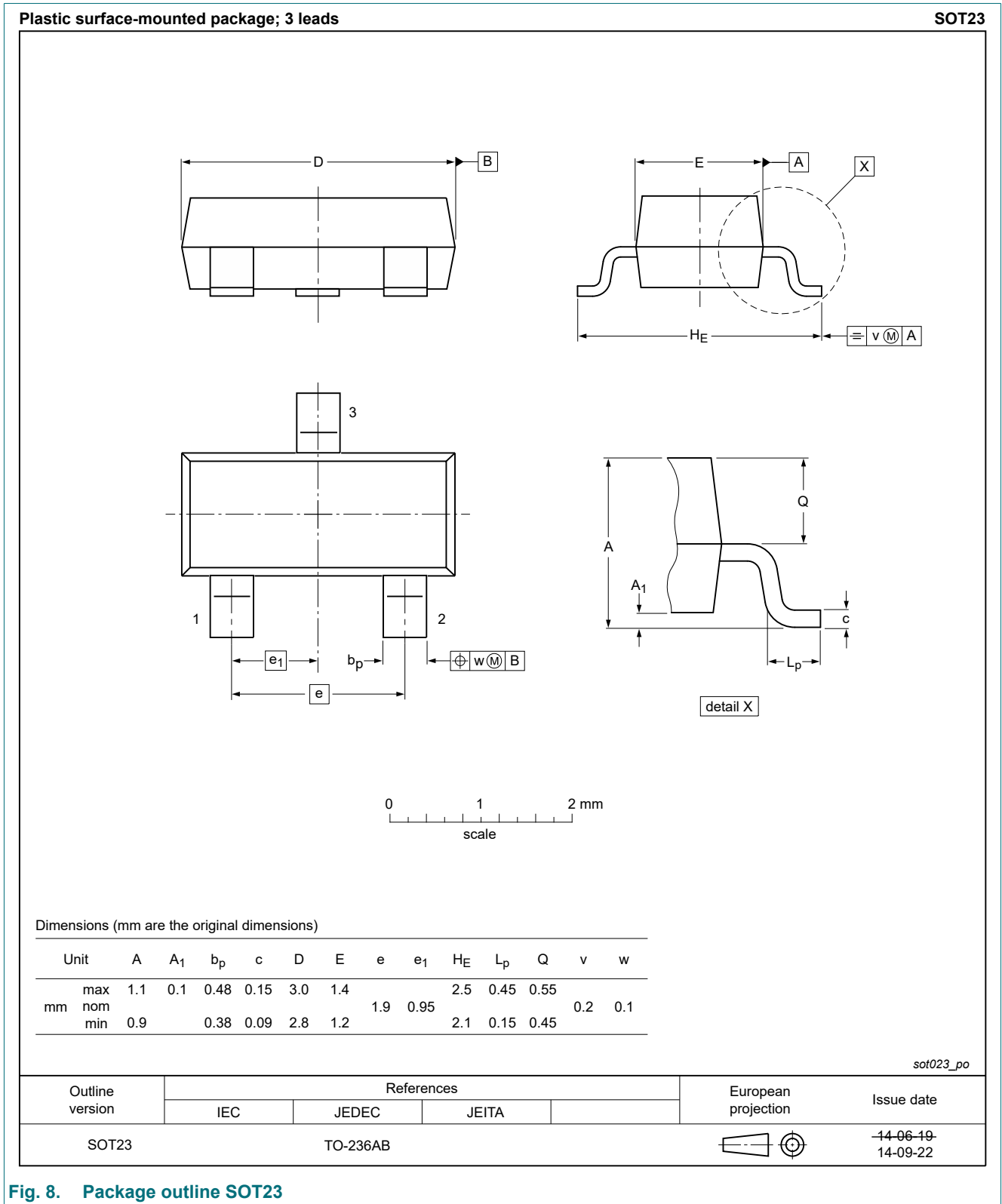


Fig. 8. Package outline SOT23

13. Soldering

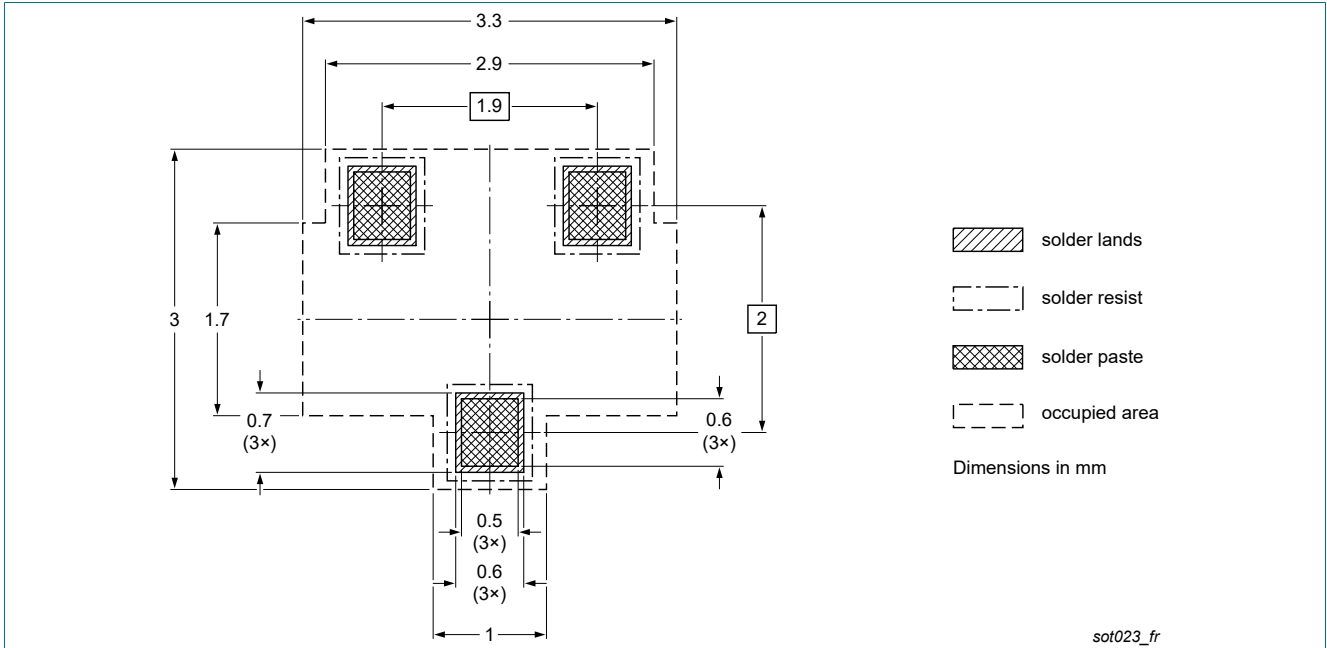


Fig. 9. Reflow soldering footprint for SOT23

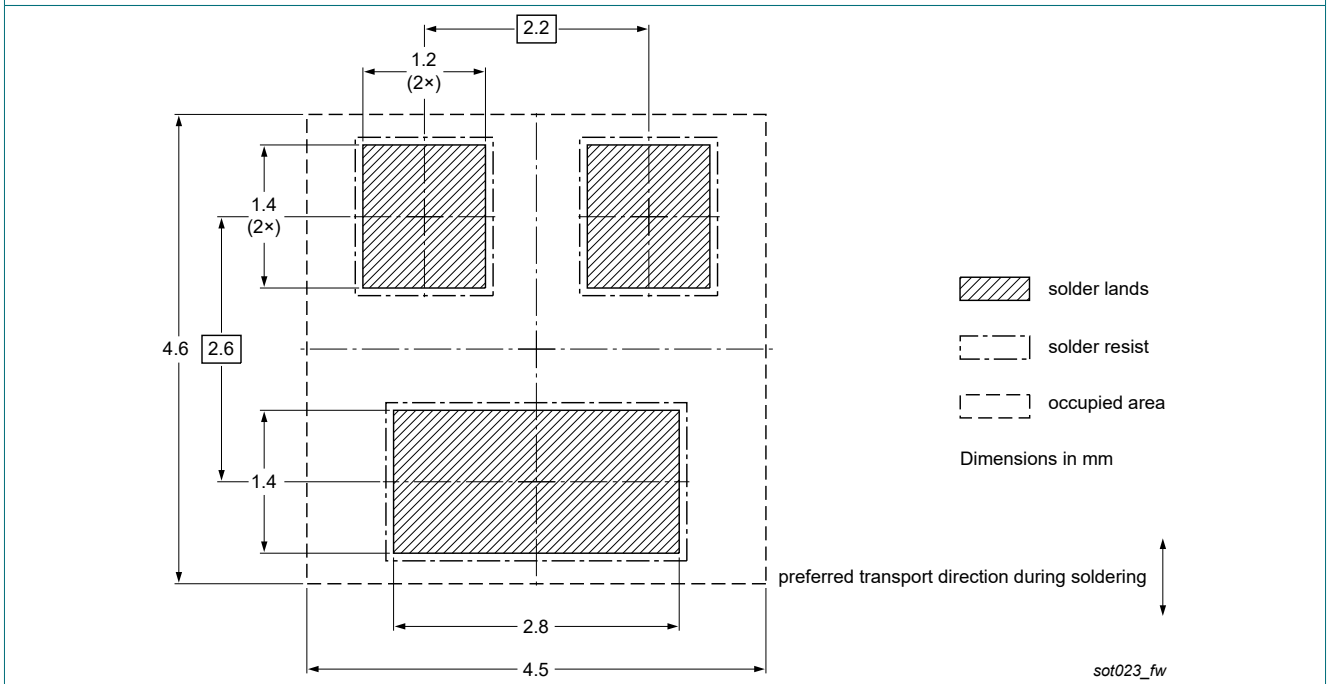


Fig. 10. Wave soldering footprint for SOT23

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD36VS2UT-Q v.1	20220506	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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