



**THE DATASHEET OF
PDTC124ET-QR**





PDTC114ET-Q

50 V, 100 mA NPN resistor-equipped transistor;
R1 = 10 k Ω , R2 = 10 k Ω

7 October 2021

Product data sheet

1. General description

NPN Resistor-Equipped Transistor (RET) in a small SOT23 Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA114ET-Q

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Digital application in automotive and industrial segments
- Cost-saving alternative for BC847-Q series in digital applications
- Controlling IC inputs
- Switching loads

4. Quick reference data

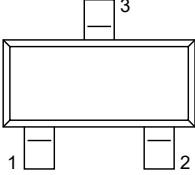
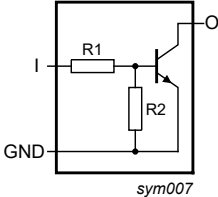
Table 1. Quick reference data

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|------------------|---------------------------|------------|-----|-----|-----|-----|------------|
| V _{CEO} | collector-emitter voltage | open base | | - | - | 50 | V |
| I _O | output current | | | - | - | 100 | mA |
| R1 | bias resistor 1 | | [1] | 7 | 10 | 13 | k Ω |
| R2/R1 | bias resistor ratio | | [1] | 0.8 | 1 | 1.2 | |

[1] See "Section 11: Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|--------------------|---|--|
| 1 | I | input (base) |  <p style="text-align: center;">SOT23</p> |  <p style="text-align: center;"><i>sym007</i></p> |
| 2 | GND | ground (emitter) | | |
| 3 | O | output (collector) | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|--|---------|
| | Name | Description | Version |
| PDTC114ET-Q | SOT23 | plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body | SOT23 |

7. Marking

Table 4. Marking codes

| Type number | Marking code ^[1] |
|-------------|-----------------------------|
| PDTC114ET-Q | %16 |

[1] % = placeholder for manufacturing site code

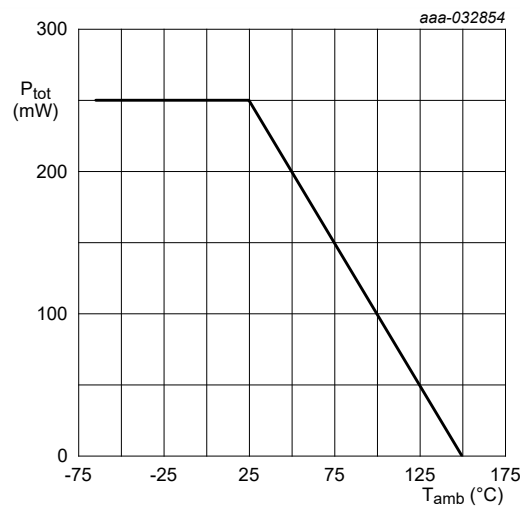
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------|---------------------------|-----------------------------|-----|-----|-----|------|
| V_{CBO} | collector-base voltage | open emitter | | - | 50 | V |
| V_{CEO} | collector-emitter voltage | open base | | - | 50 | V |
| V_{EBO} | emitter-base voltage | open collector | | - | 10 | V |
| V_I | input voltage | positive | | - | 40 | V |
| | | negative | | - | -10 | V |
| I_O | output current | | | - | 100 | mA |
| P_{tot} | total power dissipation | $T_{amb} \leq 25\text{ °C}$ | [1] | - | 250 | mW |
| T_J | junction temperature | | | - | 150 | °C |
| T_{amb} | ambient temperature | | | -65 | 150 | °C |
| T_{stg} | storage temperature | | | -65 | 150 | °C |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

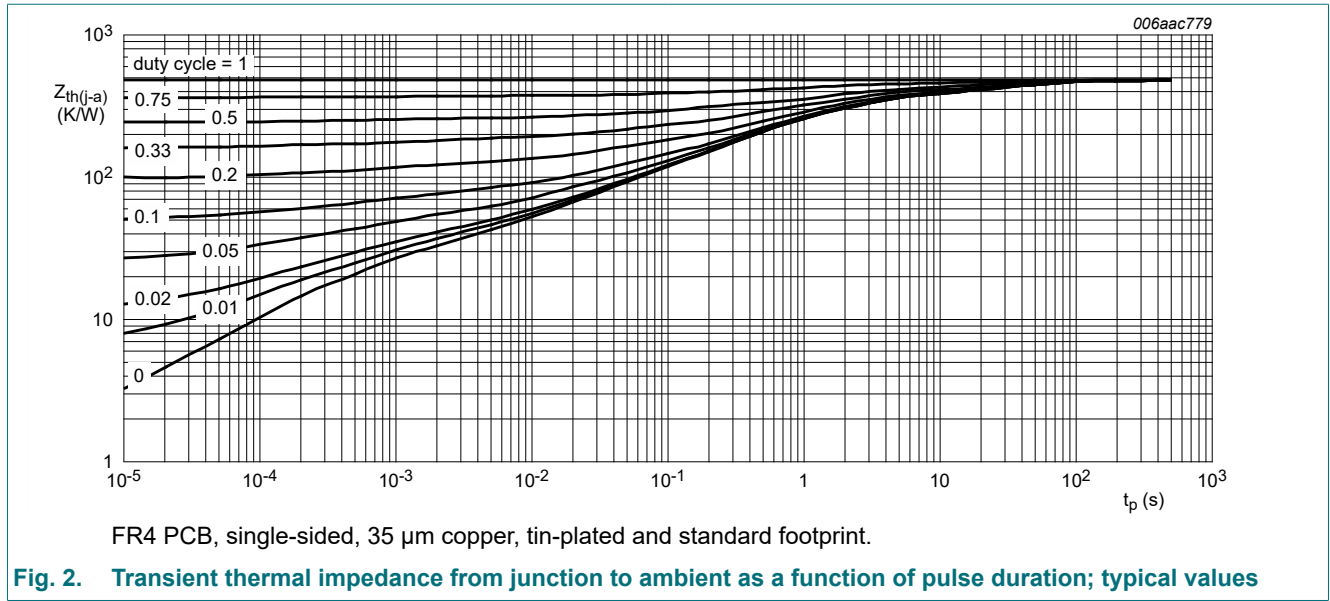
Fig. 1. Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---------------|---|-------------|-----|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 500 | K/W |

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.

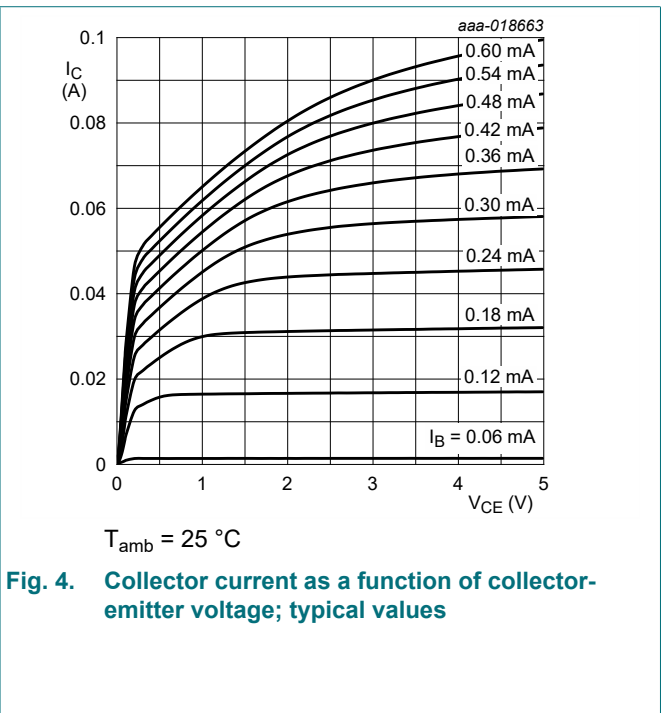
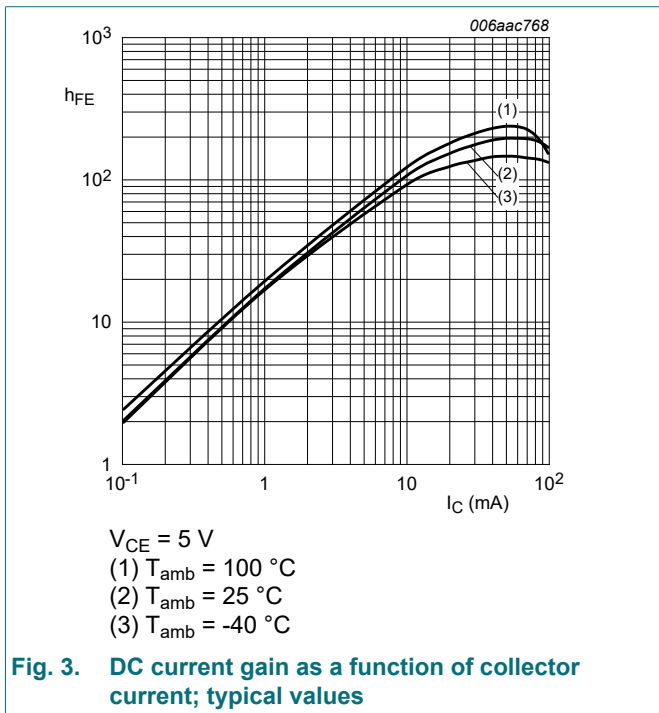


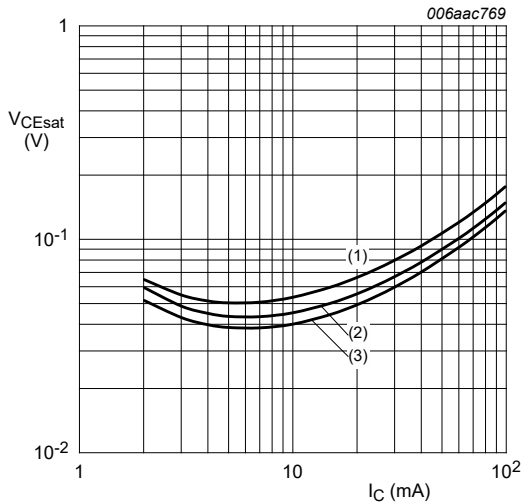
10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|---------------|--------------------------------------|---|-----|-----|-----|---------|-----|
| $V_{(BR)CBO}$ | collector-base breakdown voltage | $I_C = 100 \mu A; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$ | 50 | - | - | V | |
| $V_{(BR)CEO}$ | collector-emitter breakdown voltage | $I_C = 2 \text{ mA}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$ | 50 | - | - | V | |
| I_{CBO} | collector-base cut-off current | $V_{CB} = 50 \text{ V}; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$ | - | - | 100 | nA | |
| I_{CEO} | collector-emitter cut-off current | $V_{CE} = 30 \text{ V}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$ | - | - | 100 | nA | |
| | | $V_{CE} = 30 \text{ V}; I_B = 0 A; T_j = 150 \text{ }^\circ C$ | - | - | 5 | μA | |
| I_{EBO} | emitter-base cut-off current | $V_{EB} = 5 \text{ V}; I_C = 0 A; T_{amb} = 25 \text{ }^\circ C$ | - | - | 400 | μA | |
| h_{FE} | DC current gain | $V_{CE} = 5 \text{ V}; I_C = 5 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$ | 30 | - | - | | |
| V_{CEsat} | collector-emitter saturation voltage | $I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$ | - | - | 100 | mV | |
| $V_{I(off)}$ | off-state input voltage | $V_{CE} = 5 \text{ V}; I_C = 100 \mu A; T_{amb} = 25 \text{ }^\circ C$ | - | 1.1 | 0.8 | V | |
| $V_{I(on)}$ | on-state input voltage | $V_{CE} = 0.3 \text{ V}; I_C = 10 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$ | 2.5 | 1.8 | - | V | |
| R1 | bias resistor 1 | | [1] | 7 | 10 | 13 | kΩ |
| R2/R1 | bias resistor ratio | | [1] | 0.8 | 1 | 1.2 | |
| C_c | collector capacitance | $V_{CB} = 10 \text{ V}; I_E = 0 A; i_e = 0 A; f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$ | - | - | 2.5 | pF | |
| f_T | transition frequency | $V_{CE} = 5 \text{ V}; I_C = 10 \text{ mA}; f = 100 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$ | [2] | - | 230 | - | MHz |

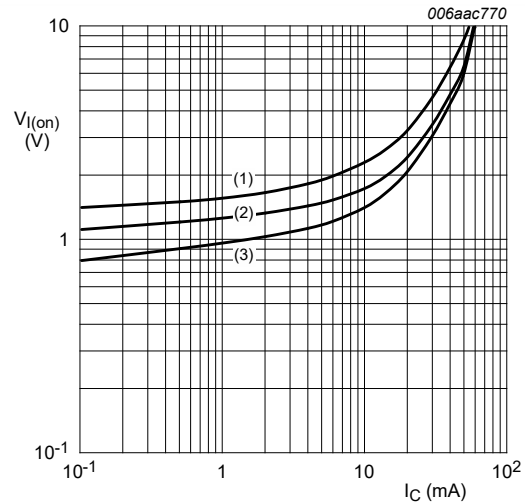
- [1] See "Section 11: Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor.





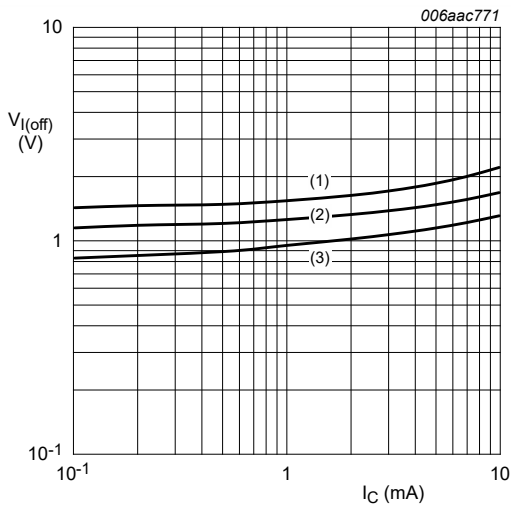
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = -40\text{ }^\circ\text{C}$

Fig. 5. Collector-emitter saturation voltage as a function of collector current; typical values



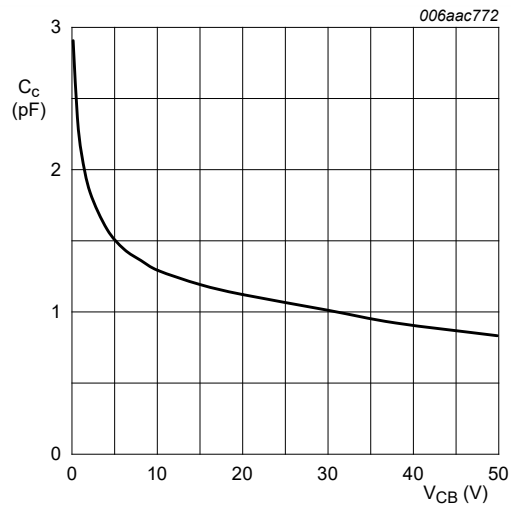
$V_{CE} = 0.3\text{ V}$
 (1) $T_{amb} = -40\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = 100\text{ }^\circ\text{C}$

Fig. 6. On-state input voltage as a function of collector current; typical values



$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = -40\text{ }^\circ\text{C}$
 (2) $T_{amb} = 25\text{ }^\circ\text{C}$
 (3) $T_{amb} = 100\text{ }^\circ\text{C}$

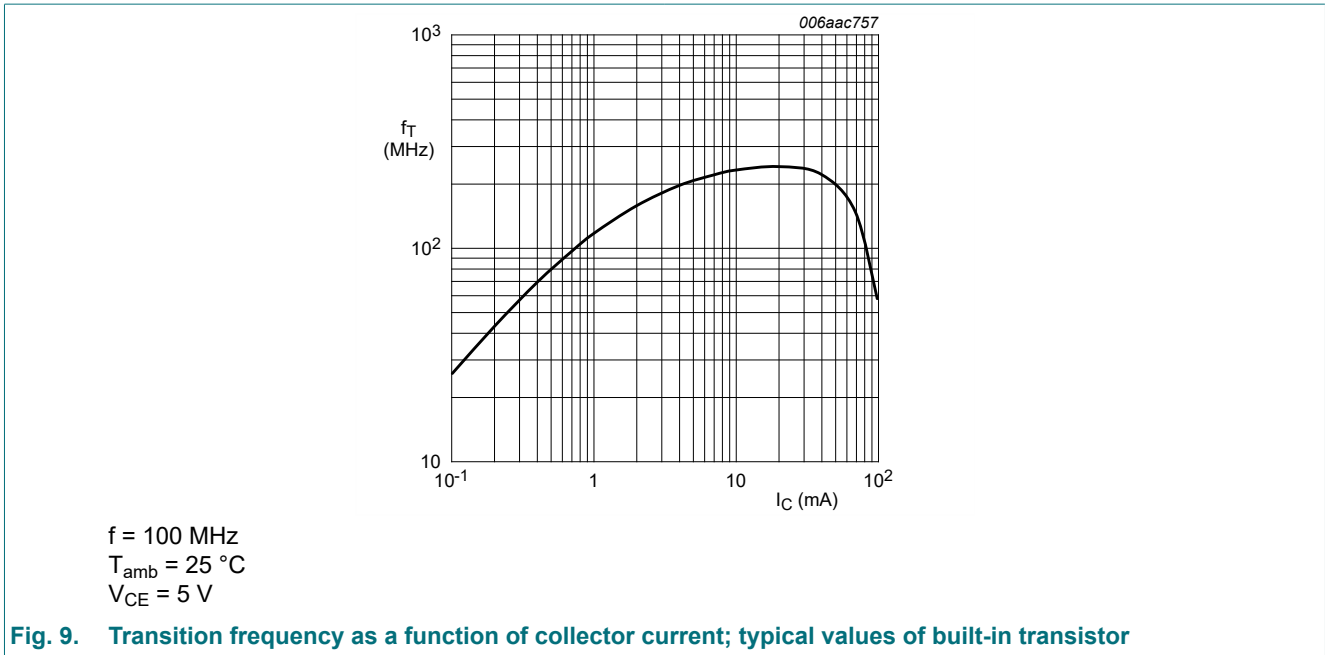
Fig. 7. Off-state input voltage as a function of collector current; typical values



$f = 1\text{ MHz}$
 $T_{amb} = 25\text{ }^\circ\text{C}$

Fig. 8. Collector capacitance as a function of collector-base voltage; typical values

50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 kΩ, R2 = 10 kΩ



11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I12) - V(I11)}{I12 - I11}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$

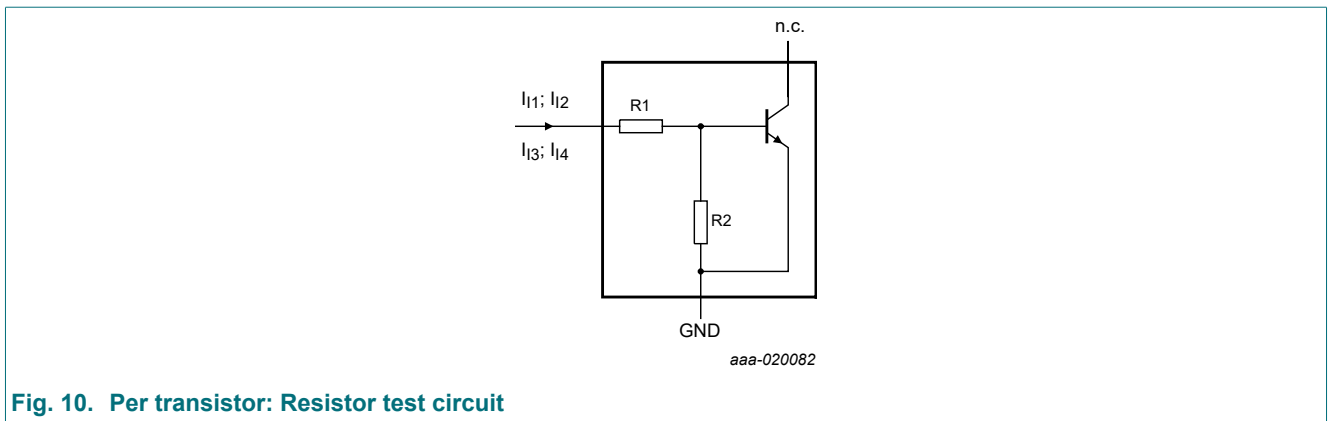


Fig. 10. Per transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

| Type number | R1 (kΩ) | R2 (kΩ) | Test conditions | | | |
|-------------|---------|---------|-----------------|--------|---------|---------|
| | | | I11 | I12 | I13 | I14 |
| PDTC114ET-Q | 10 | 10 | 350 μA | 450 μA | -350 μA | -450 μA |

12. Package outline

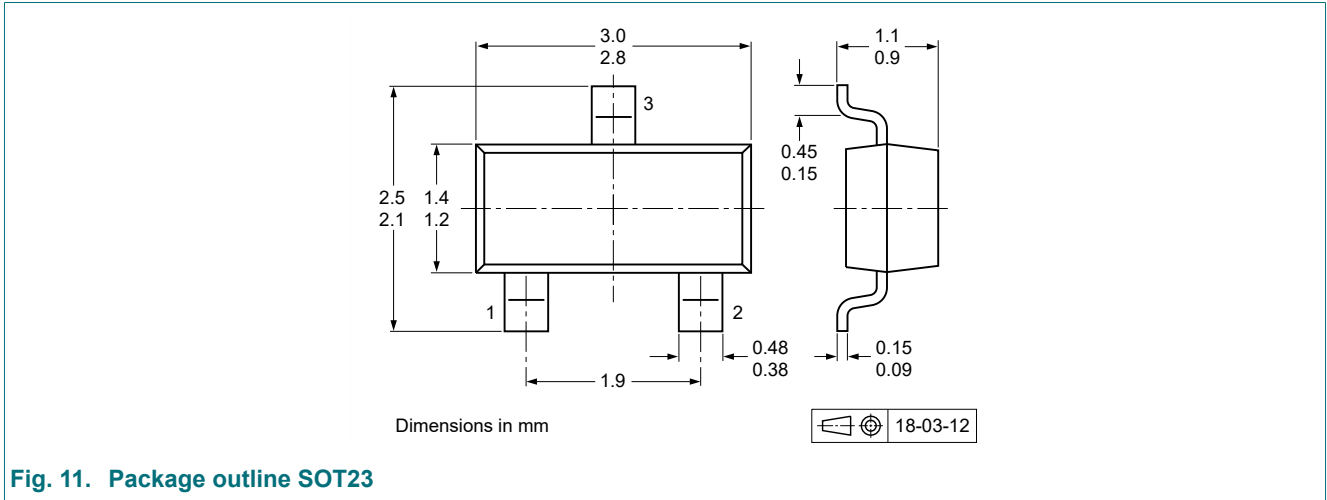


Fig. 11. Package outline SOT23

13. Soldering

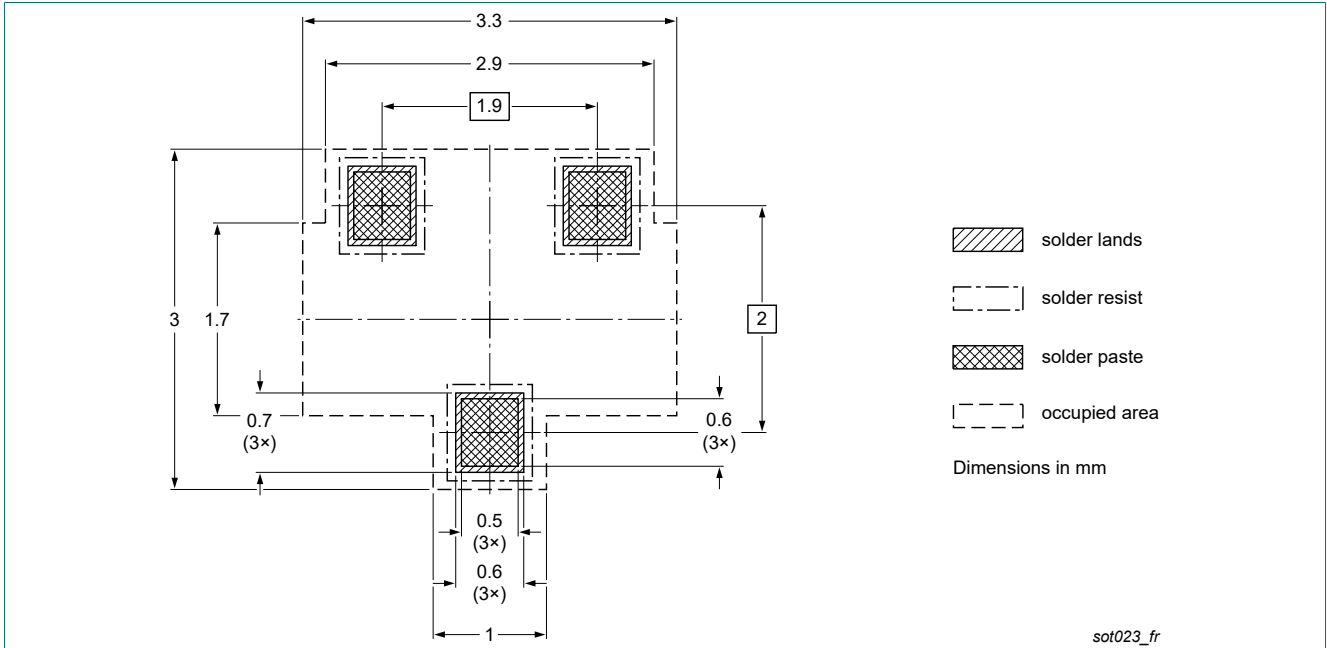


Fig. 12. Reflow soldering footprint for SOT23

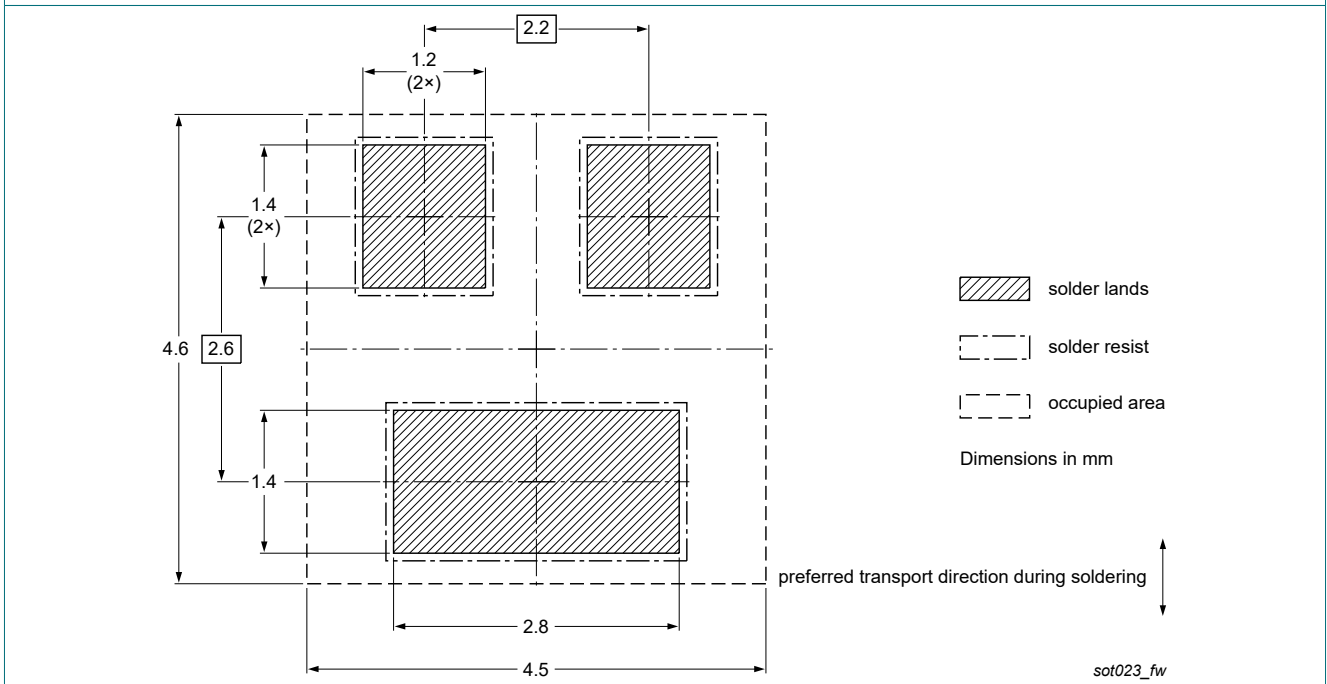


Fig. 13. Wave soldering footprint for SOT23

14. Revision history

Table 9. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--|--------------------|---------------|-----------------|
| PDTC114ET-Q v.2 | 20211007 | Product data sheet | - | PDTC114ET-Q v.1 |
| Modification: | <ul style="list-style-type: none"> • Complete rework • General description: added new line at the end • Applications: Clarification updated • Limiting values: deleted parameter I_{CM} • Characteristics: I_{CEO} max limit is updated to 100 nA • Characteristics: V_{CEsat} limit is now updated to 100 mV • Characteristics: added new graphics • Characteristics: Updated the graphics conditions • Characteristics: $V_{(BR)EBO}$ values is removed • Test information: Included resistor calculation, resistor test circuit and resistor test condition | | | |
| PDTC114ET-Q v.1 | 20210625 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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