THE DATASHEET OF

MPC1055L1R0C

MP6615

40V, 8A, H-Bridge DC Motor Driver

DESCRIPTION

The MP6615 is an H-bridge DC motor driver with a full bridge consisting of four N-channel power MOSFETs. The device also integrates pre-drivers, gate driver power supplies, and current-sense amplifiers.

The MP6615 provides 11mΩ MOSFETs at 25°C and can deliver up to 8A of continuous output current (I_{OUT}), depending on the thermal and PCB layout. The device uses an internal charge pump to generate the gate driver supply voltage for the high-side MOSFETs (HS-FETs). A trickle charge circuit maintains sufficient gate driver voltage to operate at 100% duty cycle.

Internal safety features include thermal shutdown, under-voltage lockout (UVLO), and over-current protection (OCP).

The MP6615 is available in a TQFN-26 (6mmx6mm) package.

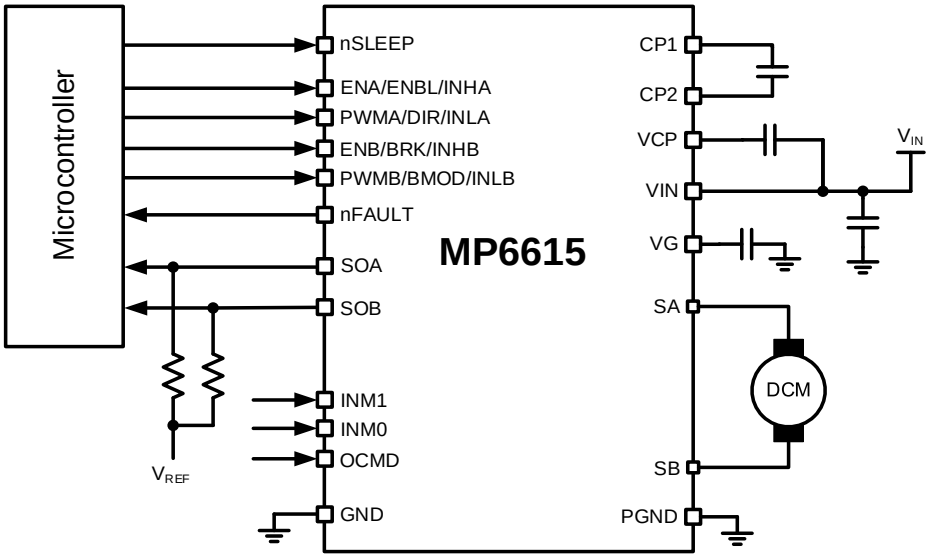
FEATURES

- 4.75V to 40V Operating Input Voltage (V_{IN}) Range
- Internal Full H-Bridge Driver
- 8A of Continuous Output Current (I_{OUT})
- MOSFET On Resistance ($R_{DS(ON)}$): 11mΩ per MOSFET
- Internal Charge Pump Supports 100% Duty Cycle Operation
- Under-Voltage Lockout (UVLO) and Over-Voltage Protection (OVP)
- Thermal Shutdown Protection
- Over-Current Protection (OCP)
- Integrated Bidirectional Current-Sense Amplifiers
- Available in a TQFN-26 (6mmx6mm) Package

APPLICATIONS

- Brushed DC Motors
- Door Locks and Latch Motors
- Seat Actuators

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6615GQKT*	TQFN-26 (6mmx6mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6615GQKT-Z).

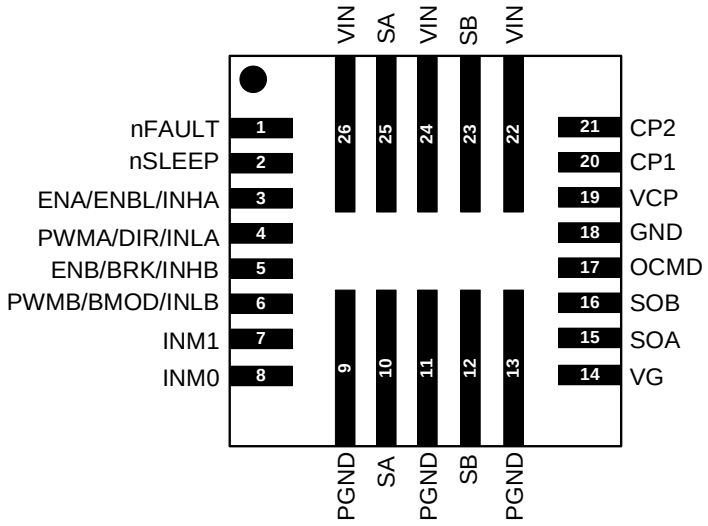
TOP MARKING

MPSYYWW
MP6615
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6615: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



TQFN-26 (6mmx6mm)

PIN FUNCTIONS

Pin #	Name	Description
1	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output. During fault conditions, nFAULT is pulled logic low.
2	nSLEEP	**Sleep mode input.** Pull the nSLEEP pin logic low to enter low-power sleep mode; pull nSLEEP logic high for normal operation. nSLEEP has an internal pull-down resistor.
3	ENA/ENBL/ INHA	**Can be configured for the ENA, ENBL, or INHA function.** ENA: If INM[1:0] = 00, the ENA pin acts as the enable input for phase A. Pull ENA high to enable phase A. ENBL: If INM[1:0] = 01, the ENBL pin acts as enable input for the H-bridge. Pull ENBL high to enable the entire H-bridge. INHA: If INM[1:0] = 10, the INHA pin acts as the phase A enable input for the high-side MOSFET (HS-FET).
4	PWMA/DIR/ INLA	**Can be configured for the PWM, DIR, or INLA function.** PWMA: If INM[1:0] = 00, the PWMA pin acts as the pulse-width modulation (PWM) input for phase A. DIR: If INM[1:0] = 01, the DIR pin acts as the direction input for the H-bridge. INLA: If INM[1:0] = 10, the INLA pin acts as the enable input for the phase A low-side MOSFET (LS-FET).
5	ENB/BRK/ INHB	**Can be configured for the ENB, BRK, or INHB function.** ENB: If INM[1:0] = 00, the ENB pin acts as the enable input for phase B. Pull ENB high to enable phase B. BRK: If INM[1:0] = 01, the BRK pin acts as the brake input for the H-bridge. Pull BRK high to force the H-bridge to enter brake mode. INHB: If INM[1:0] = 10, the INHB pin acts as the enable input for the phase B HS-FET.
6	PWMB/BMOD/ INLB	**Can be configured for the PWMB, BMOD, or INLB function.** PWMB: If INM[1:0] = 00, the PWMB pin acts as the PWM input for phase B. BMOD: If INM[1:0] = 01, the BMOD pin acts as the brake mode input for the H-bridge. Pull BMOD high to force the HS-FETs to enter brake mode; pull BMOD low to force the LS-FETs to enter brake mode. INLB: If INM[1:0] = 10, the INLB pin acts as the enable input for the phase B LS-FET.
7	INM1	**Input mode selection 1.** If INM[1:0] = 00, the INM1 pin sets the ENx/PWMx input logic. If INM[1:0] = 01, INM1 sets the ENBL/DIR input logic. If INM[1:0] = 10, INM1 sets the INHx/INLx input logic.
8	INM0	**Input mode selection 0.** If INM[1:0] = 00, the INM0 pin sets the ENx/PWMx input logic. If INM[1:0] = 01, INM0 sets the ENBL/DIR input logic. If INM[1:0] = 10, INM0 sets the INHx/INLx input logic.
9, 11, 13	PGND	**Power ground.** Connect the PGND pin directly to GND.
10, 25	SA	**Phase A output.**
22, 24, 26	VIN	**Input supply voltage.**
12, 23	SB	**Phase B output.**
14	VG	**Low-side (LS) gate drive output.** Connect a 4.7µF, 10V ceramic capacitor with X7R dielectrics from the VG pin to ground.
15	SOA	**Current-sense output A.**
16	SOB	**Current-sense output B.**

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
17	OCMD	**Over-current protection (OCP) mode.** Connect the OCMD pin to GND for latch-off mode. Leave OCMD open or connect the pin to a logic high voltage for retry mode.
18	GND	**Ground.**
19	VCP	**Charge pump output.** Connect a 1µF, 16V ceramic capacitor with X7R dielectrics between the VCP and VIN pins.
20	CP1	**Charge pump capacitor.** Connect a 100nF ceramic capacitor with X7R dielectrics rated for at least the input voltage (V_{IN}) between the CP1 and CP2 pins.
21	CP2	

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .....-0.3V to +45V
CP2, VCP .....V_{IN} to V_{IN} + 6.5V
SA, SB .....-0.3V to +45V
All other pins to GND/PGND.....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
TQFN-26 (6mmx6mm).....5.84W
Storage temperature..... -55°C to +150°C
Junction temperature (T_J) .....150°C
Lead temperature (solder) .....260°C

ESD Ratings

Human body model (HBM) 2kV
Charged-device model (CDM) 2kV

Recommended Operating Conditions (3)

Input voltage (V_{IN}).....4.75V to 40V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TQFN-26 (6mmx6mm)..... 21.4....12.8 . °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, PGND = GND = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		4.75		40	V
Quiescent current	I_Q	nSLEEP = 1, ENx = 0		2.6	5	mA
	I_{SLEEP}	nSLEEP = 0		1		µA
Control Logic						
Logic-low input threshold	V_{IL}				0.8	V
Logic-high input threshold	V_{IH}		2			V
Logic input current	I_{IN_H}	V_{IH} = 5V	-20		+20	µA
	I_{IN_L}	V_{IL} = 0V	-20		+20	µA
Power up delay	t_{PUD}	At V_{IN} rising or nSLEEP rising		1		ms
Internal pull-down resistance	R_{PD}	All logic inputs		500		kΩ
nFAULT pull-down on resistance	$R_{DS(ON)\_nFAULT}$			10		Ω
Protection Circuits						
Under-voltage lockout (UVLO) threshold	V_{UVLO}	V_{IN} rising	4.1	4.4	4.75	V
UVLO hysteresis	ΔV_{UVLO}			480		mV
OVP threshold	V_{OVP}	V_{IN} rising	45	48	51	V
OVP hysteresis	ΔV_{OVP}			1.6		V
High-side (HS) over-current protection (OCP) threshold	I_{OCP_HS}		16	25		A
Low-side (LS) OCP threshold	I_{OCP_LS}		16	25		A
OCP deglitch time (5)	t_{OCD}			0.4		µs
OCP retry time	t_{OCR}			2		ms
Thermal shutdown (5)	T_{TSD}			150		°C
Thermal shutdown hysteresis (5)	ΔT_{TSD}			25		°C
Current Sense						
Current-sense ratio		Phase A	1/12700	1/11000	1/10000	A/A
		Phase B	1/11900	1/10500	1/9600	
Current-sense output offset current	I_{SOx}	Phase A current = 0A	-30	-5	+20	µA
		Phase B current = 0A	-32	-5	+22	µA
Current-sense output voltage swing (5)			0		5	V
Current-sense minimum load impedance (5)		Pull-up		1.8		kΩ
		Pull-down		1		kΩ

ELECTRICAL CHARACTERISTICS *(continued)*

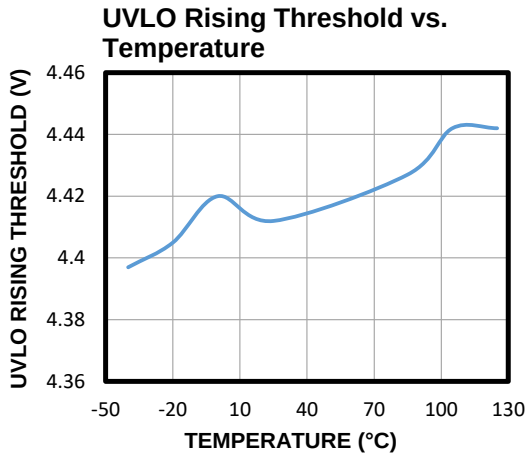
V_{IN} = 24V, PGND = GND = 0V, unless otherwise noted.

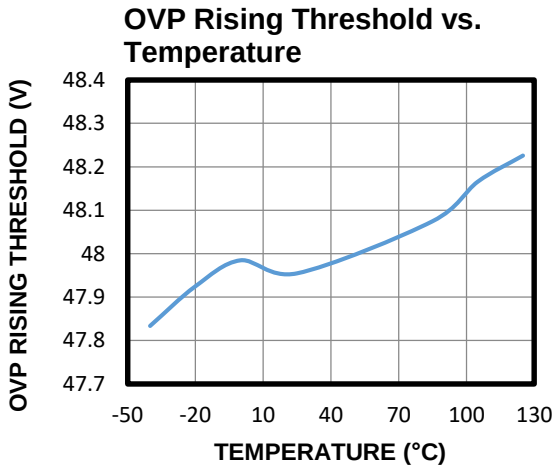
Parameter	Symbol	Condition	Min	Typ	Max	Units
Outputs						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 1A, T_J = 25°C		11	19	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	I_{OUT} = 1A, T_J = 25°C		11	19	
Output rising time (5)		I_{OUT} = 1A		0.47		V/ns
Output falling time (5)		I_{OUT} = 1A		1.27		V/ns
Charge Pump						
Charge pump output voltage	V_{VCP}			V_{IN} + 5		V
Charge pump frequency	f_{CP}			2000		kHz

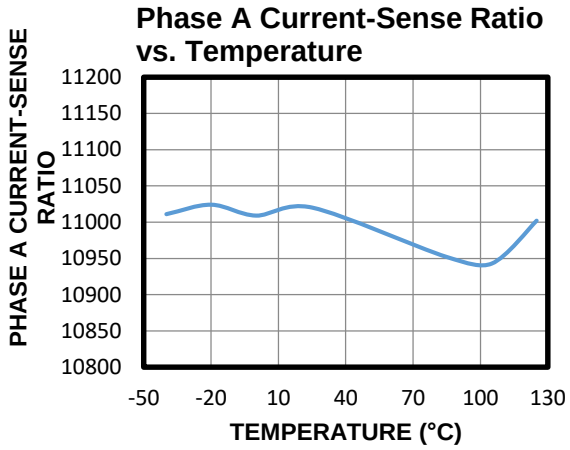
Notes:

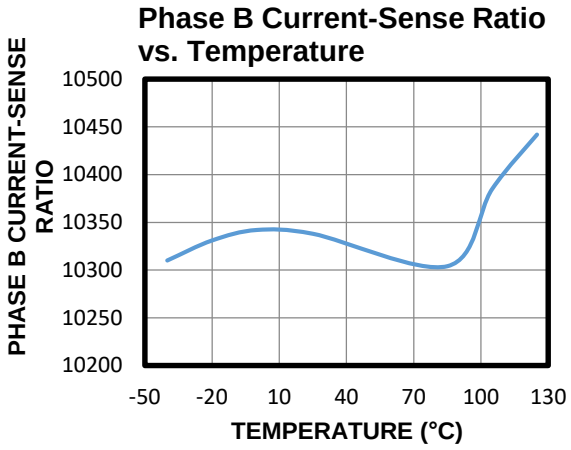
5) Not tested in production.

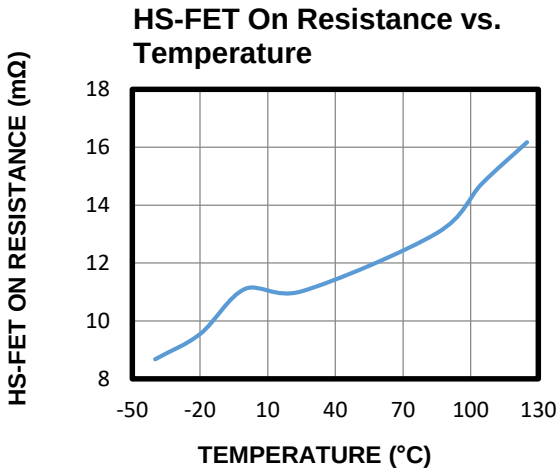
TYPICAL CHARACTERISTICS

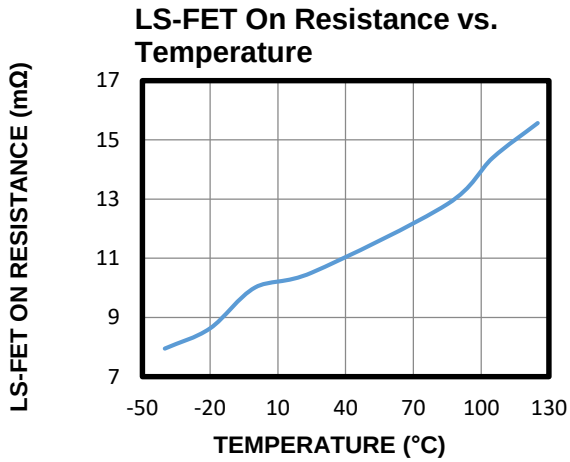








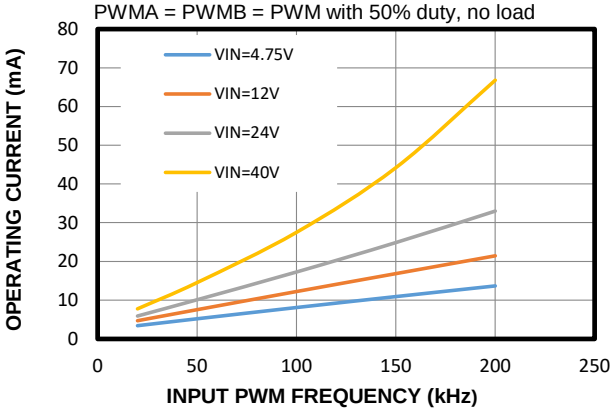




TYPICAL CHARACTERISTICS *(continued)*

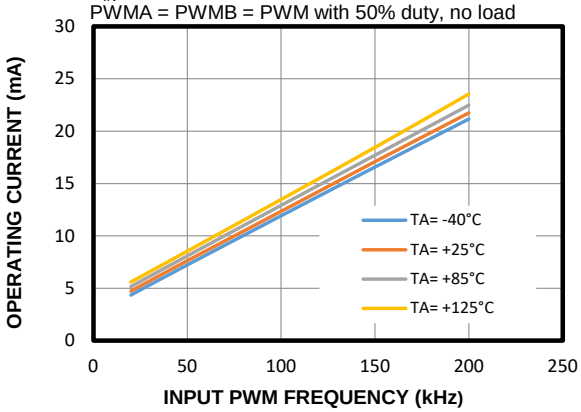
Operating Current vs. Input PWM Frequency

T_A = 25°C, INM1 = INM0 = 0, ENA = ENB = 1, PWMA = PWMB = PWM with 50% duty, no load



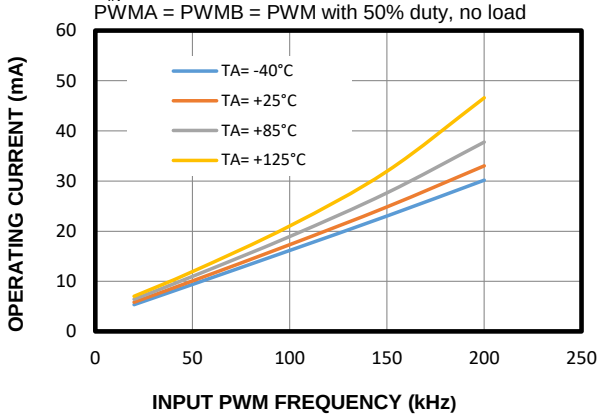
Operating Current vs. Input PWM Frequency

V_{IN} = 12V, INM1 = INM0 = 0, ENA = ENB = 1, PWMA = PWMB = PWM with 50% duty, no load



Operating Current vs. Input PWM Frequency

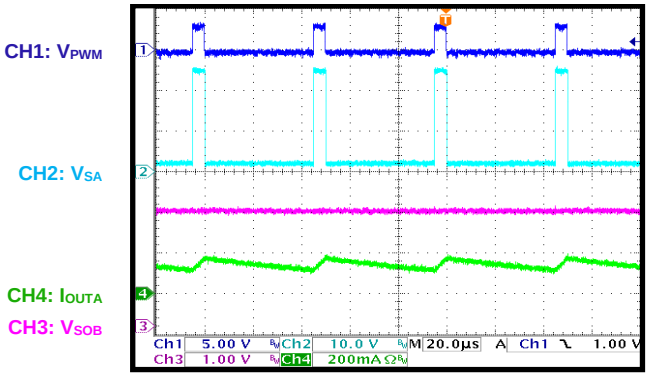
V_{IN} = 24V, INM1 = INM0 = 0, ENA = ENB = 1, PWMA = PWMB = PWM with 50% duty, no load



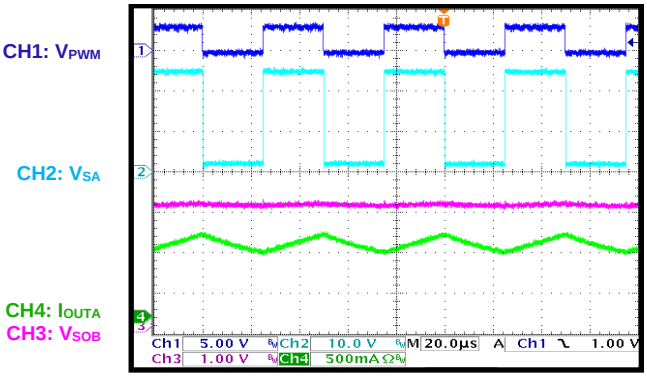
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, INM0 = INM1= 0V, ENA = ENB = 5V, PWMA = 20kHz, PWMB = 0V, V_{REF} = 5V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load: 10Ω + 2mH, unless otherwise noted.

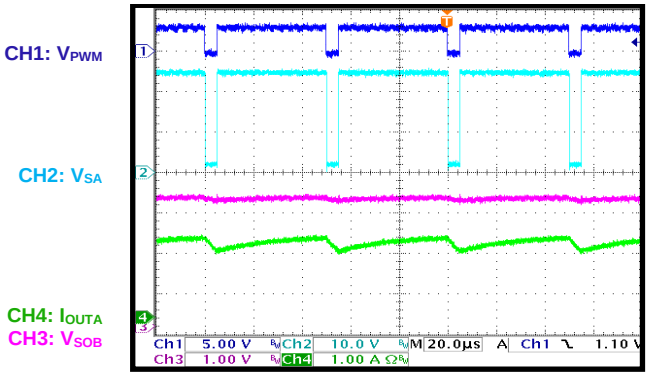
Steady State
Duty = 10%



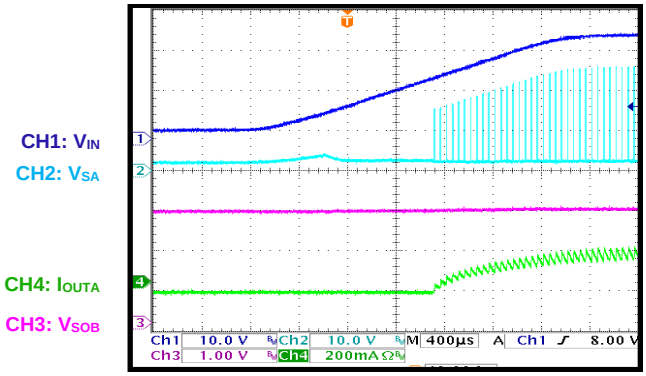
Steady State
Duty = 50%



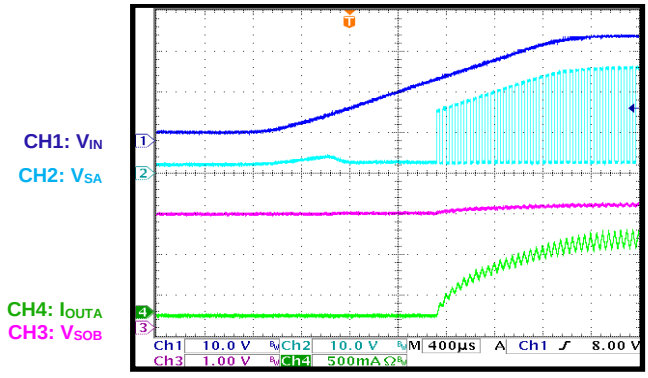
Steady State
Duty = 90%



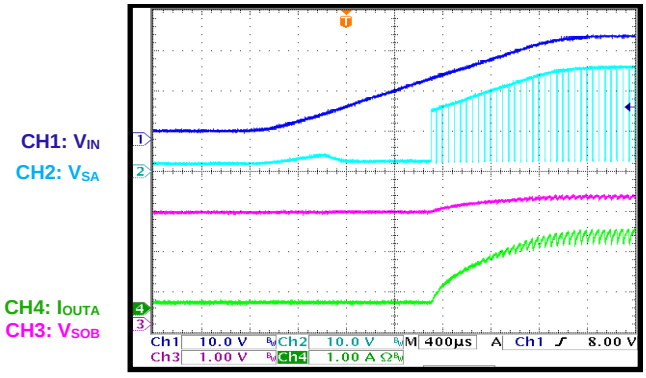
Start-Up
Duty = 10%



Start-Up
Duty = 50%



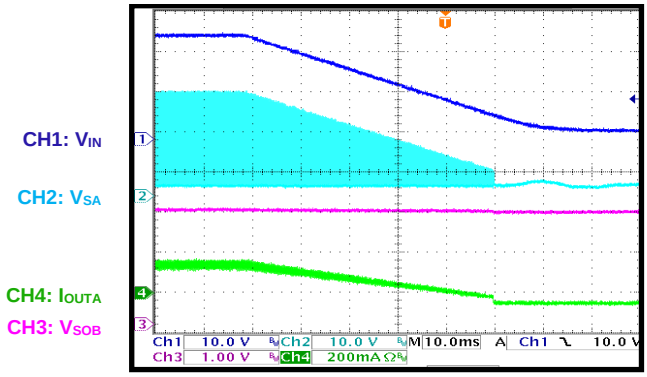
Start-Up
Duty = 90%



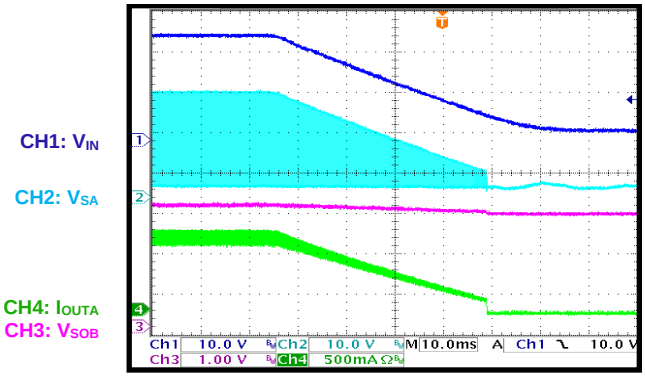
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, INM0 = INM1= 0V, ENA = ENB = 5V, PWMA = 20kHz, PWMB = 0V, V_{REF} = 5V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load: 10Ω + 2mH, unless otherwise noted.

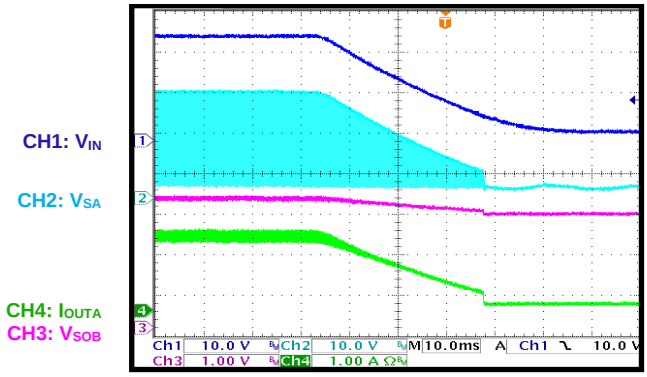
Shutdown
Duty = 10%



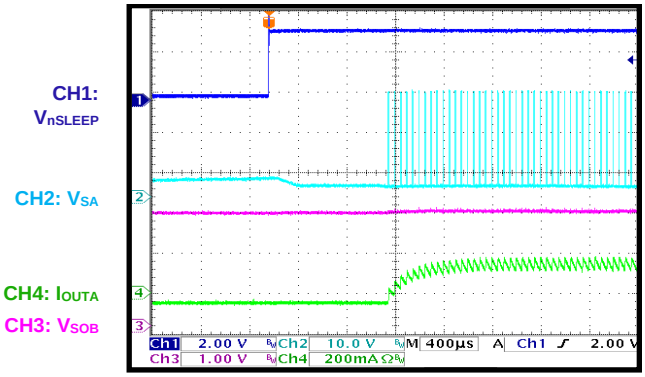
Shutdown
Duty = 50%



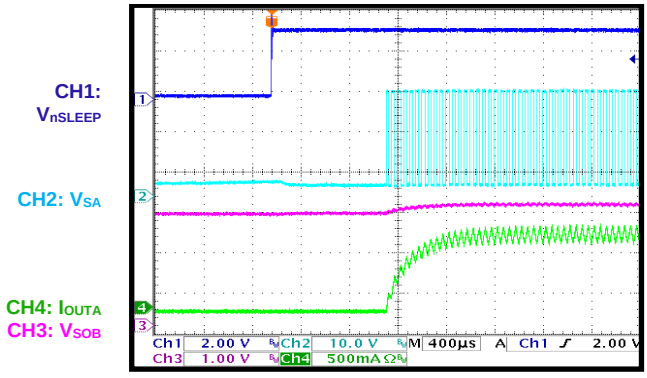
Shutdown
Duty = 90%



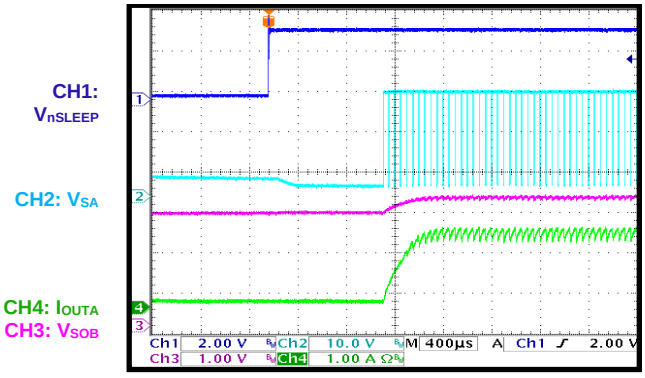
Sleep Recovery
Duty = 10%



Sleep Recovery
Duty = 50%



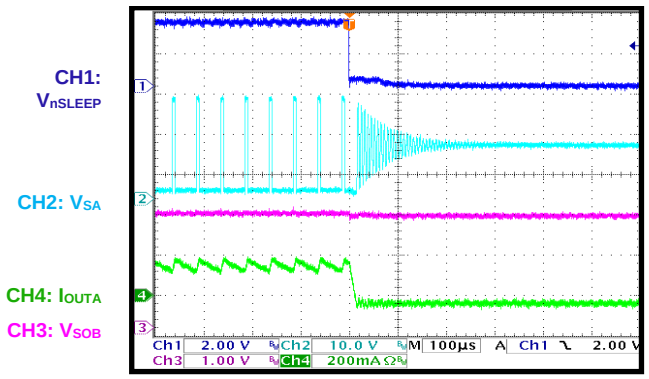
Sleep Recovery
Duty = 90%



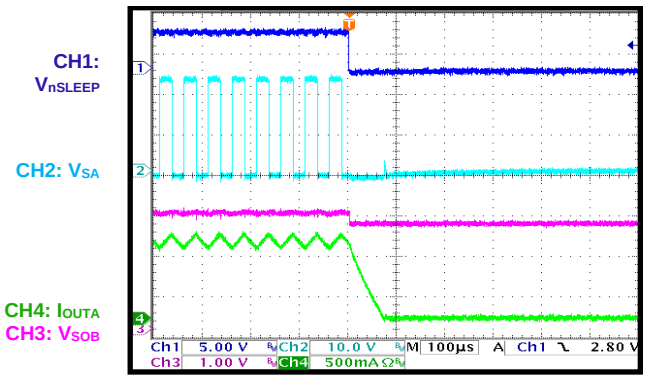
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, INM0 = INM1= 0V, ENA = ENB = 5V, PWMA = 20kHz, PWMB = 0V, V_{REF} = 5V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load: 10Ω + 2mH, unless otherwise noted.

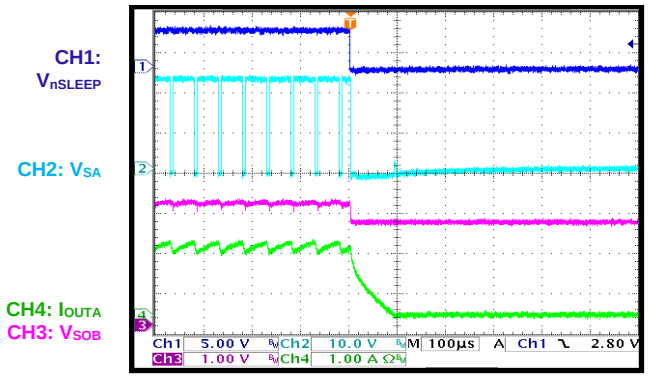
Sleep Entry
Duty = 10%



Sleep Entry
Duty = 50%



Sleep Entry
Duty = 90%



FUNCTIONAL BLOCK DIAGRAM

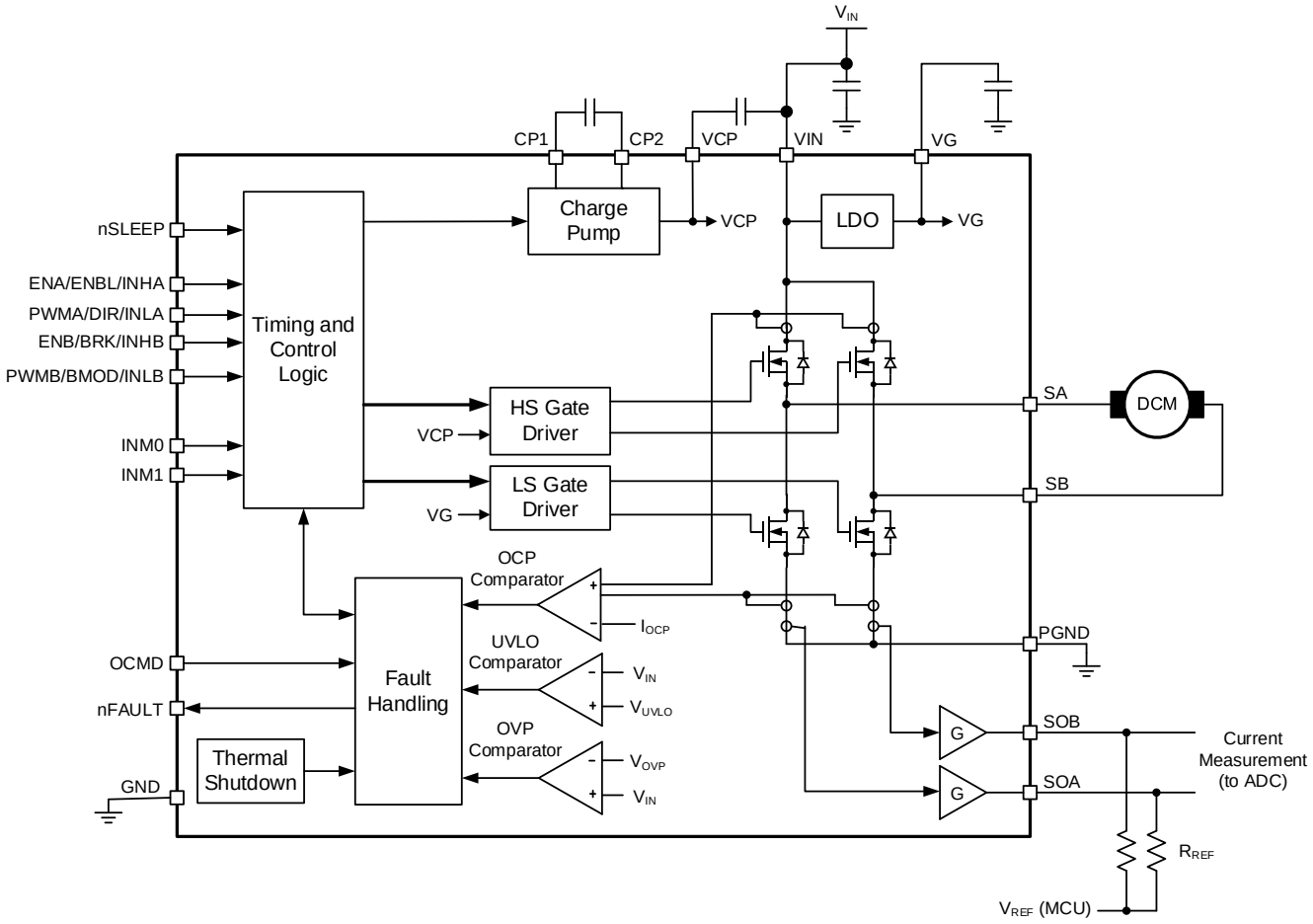


Figure 1: Functional Block Diagram

OPERATION

Input Logic

Three configurable input modes are available on the MP6615, allowing for several different control methods to be used. The INM1 and INM0 pins configure the input interface. Table 1 shows the input logic when INM[1:0] = 00.

Table 1: Input Logic for INM[1:0] = 00 (6)

ENx	PWMx	Sx
H	H	VIN
H	L	GND
L	-	Hi-Z

Note:

6) "x" means A or B.

Table 2 shows the input logic when INM[1:0] = 01.

Table 2: Input Logic for INM[1:0] = 01

ENBL	DIR	BRK	BMOD	SA	SB
L	-	-	-	Hi-Z	Hi-Z
H	-	H	L	GND	GND
H	-	H	H	VIN	VIN
H	L	L	-	GND	VIN
H	H	L	-	VIN	GND

Table 3 shows the input logic when INM[1:0] = 10.

Table 3: Input Logic for INM[1:0] = 10 (7)

INHx	INLx	Sx
L	L	Hi-Z
L	H	GND
H	L	VIN
H	H	Hi-Z

Note:

7) "x" means A or B.

Note that the logic inputs have internal, 500kΩ pull-down resistors.

nSLEEP Operation

Pull the nSLEEP pin low to force the MP6615 to enter low-power sleep mode. In this mode, all the internal circuits are disabled. All inputs are ignored when nSLEEP is active low. Once the MP6615 exits sleep mode, approximately 1ms must pass before the device responds to the inputs. nSLEEP has a 500kΩ pull-down resistor.

Current-Sense Amplifiers

The internal current-sensing circuits detect the current flowing in each of the two outputs. An output pin for each phase sources or sinks a current that is proportional to the current flowing in each phase. It should be noted that only the current flowing in the low-side MOSFET (LS-FET) is sensed in both the forward and reverse directions.

To convert this current into a voltage (e.g. input to an analog-to-digital converter (ADC)), place a termination resistor (R_{REF}) between SOx (where x = A or B) and a reference voltage (V_{REF}). When there is no current flowing, the resulting output is equal to V_{REF}. When current is flowing, the SOx pin voltage (V_{SOx}) (where x = A or B) can be above or below V_{REF}. V_{SOx} can be calculated with Equation (1):

$$V_{SOx} = V_{REF} + (R_{REF} \times I_{LOAD}) / 11{,}000 \quad (1)$$

When using an ADC with inputs that are ratiometric to its supply voltage, connect two equal-value resistors to the ADC supply and ground to terminate the outputs. The resulting ADC code is half-scale at 0A.

Figure 2 shows a simplified diagram of the current measurement circuit.

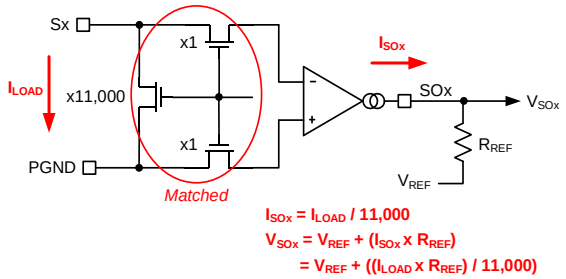


Figure 2: Current Measurement Circuit

Automatic Synchronous Rectification

When driving a current through an inductive load with both of the output MOSFETs turned off, the recirculation current must continue flowing. Typically, this current passes through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MP6615 implements an automatic synchronous rectification feature.

When both the high-side MOSFET (HS-FET) and LS-FET are turned off and the voltage on an Sx output pin is pulled below ground, the LS-FET turns on until the current flowing through it reaches close to 0A, or until the HS-FET is commanded to turn on. Similarly, if Sx exceeds V_{IN}, the HS-FET turns on until the current is close to 0A, or the LS-FET turns on.

nFAULT Output

The MP6615 provides an nFAULT output pin, which is pulled active low if a fault condition occurs, such as over-current protection (OCP) or over-temperature protection (OTP). nFAULT is an open-drain output and must be pulled up by an external pull-up resistor.

Input Under-Voltage Lockout (UVLO) Protection

If the input voltage (V_{IN}) falls below the under-voltage lockout (UVLO) threshold (V_{UVLO}), all circuitry in the device is disabled and the internal logic resets. Once V_{IN} exceeds V_{UVLO}, the device automatically resumes normal operation.

Over-Voltage Protection (OVP)

If V_{IN} exceeds the over-voltage protection (OVP) threshold (V_{OVP}), all output MOSFETs are disabled and nFAULT is not pulled active low. Once V_{IN} falls below V_{OVP}, the device automatically resumes normal operation.

Thermal Shutdown

If the die temperature exceeds safe limits, all output MOSFETs are disabled and nFAULT is pulled low. Once the die temperature falls to a safe level, the device resumes normal operation.

Over-Current Protection (OCP)

The over-current protection (OCP) circuit disables the gate driver to limit the current through each MOSFET. If the over-current (OC) limit is reached and lasts longer than the OC deglitch time, then all four output MOSFETs are disabled (outputs have high impedance), and nFAULT is pulled low. During this time, synchronous rectification is used to decay the current.

If the OCMD pin is logic low or connected directly to GND, then the device remains in latch-off state until V_{IN} falls below V_{UVLO}. If OCMD is open or pulled logic high, then the outputs are disabled for 2ms (typically) and are re-enabled automatically.

OC conditions on both high-side (HS) and low-side (LS) devices (e.g. a short to ground, supply, or across the motor winding) result in an OC shutdown.

Figure 3 shows a simplified diagram of the OCP circuit for one output.

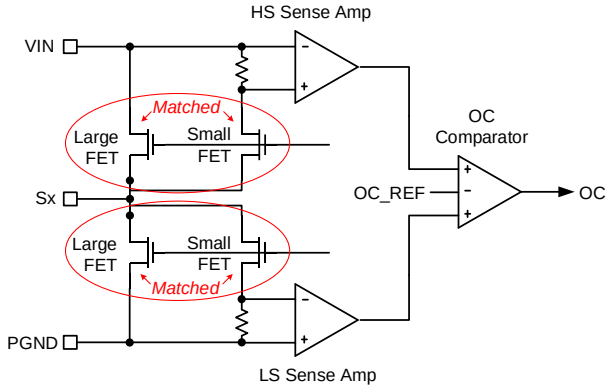


Figure 3: OCP Measurement Circuit

Charge Pump and VG Regulator

An internal low-dropout (LDO) regulator generates a LS gate drive voltage of about 5.5V. A 4.7µF to 10µF bypass capacitor must be placed from VG to ground.

A charge pump generates the gate drive for the HS-FETs. The charge pump requires two external capacitors: a 0.1µF ceramic capacitor rated for at least V_{IN} between the CP1 and CP2 pins, and a 1µF ceramic capacitor rated for at least 10V between VIN and VCP.

APPLICATIONS INFORMATION

Selecting the External Charge Pump Capacitors

Table 4 shows the recommended external charge pump capacitors.

Table 4: External Charge Pump Capacitor Selection

Specifications of Charge Pump and VG Capacitors	Min	Typ	Max	Units
CP1 to CP2 capacitance		0.1		µF
CP1 to CP2 capacitor voltage	V_{IN}			V
VCP to VIN capacitance		1		µF
VCP to VIN capacitor voltage	10			V
VG capacitance	4.7		10	µF
VG capacitor voltage	10			V

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and Figure 5, and follow the guidelines below:

1. Place the supply bypass capacitor and charge pump capacitor as close to the IC as possible (ideally, place these capacitors on the same PCB layer between VIN and GND, VG and GND, CP1 and CP2, and VCP and VIN).
2. Supply bypass capacitors and charge pump capacitors can also be placed on the opposite side of the PCB directly under the IC. Use vias to make these connections.
3. Place as much copper as possible on the long pads.
4. Place large copper areas on the pads, as well as on the same outer copper layer as the device.
5. Place thermal vias inside the pad area to move heat to the copper layers.
6. If via-in-pad construction is not allowed, place multiple vias just outside the pad area.

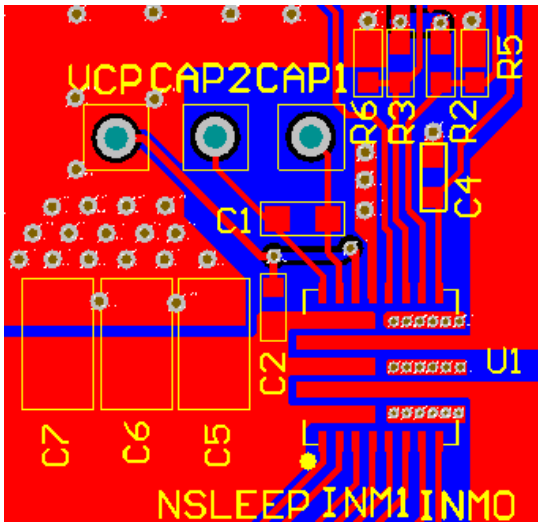


Figure 4: Recommended PCB Layout

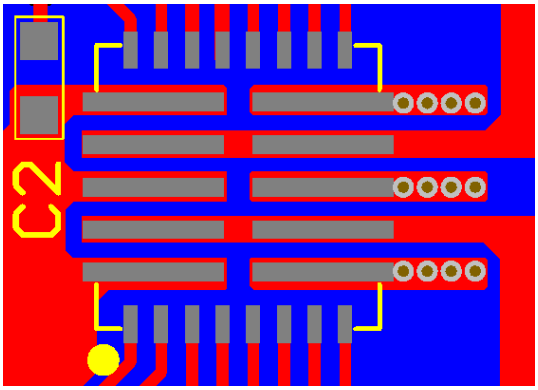


Figure 5: Thermal Vias Outside Pads

TYPICAL APPLICATION CIRCUIT

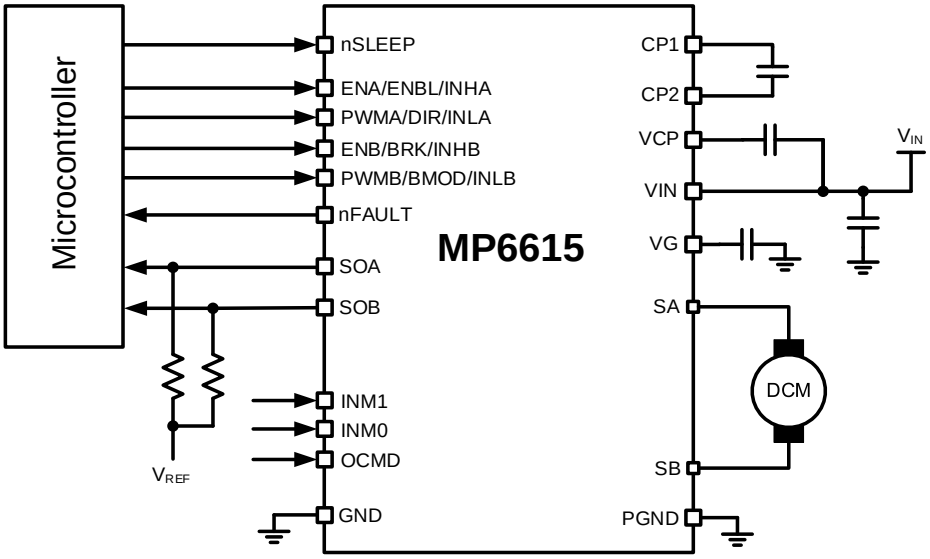
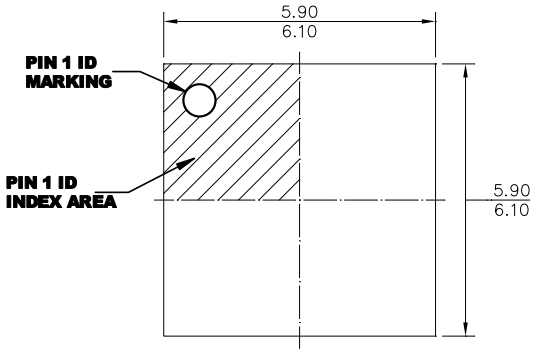


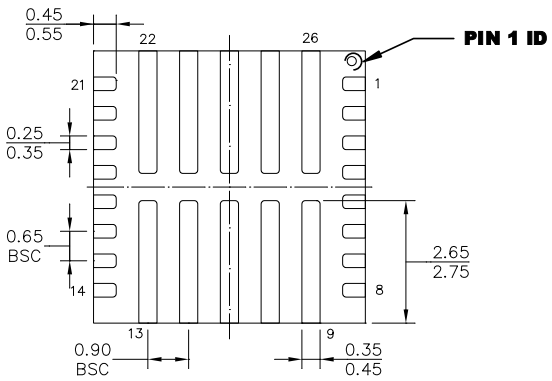
Figure 6: Typical Application Circuit

PACKAGE INFORMATION

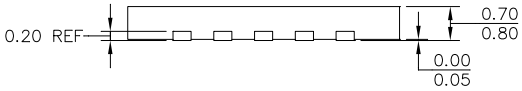
TQFN-26 (6mmx6mm)



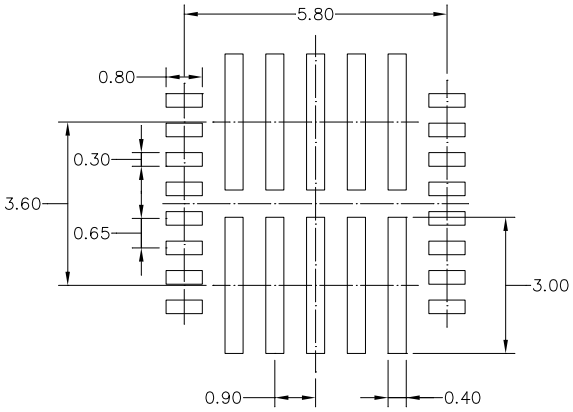
TOP VIEW



BOTTOM VIEW



SIDE VIEW

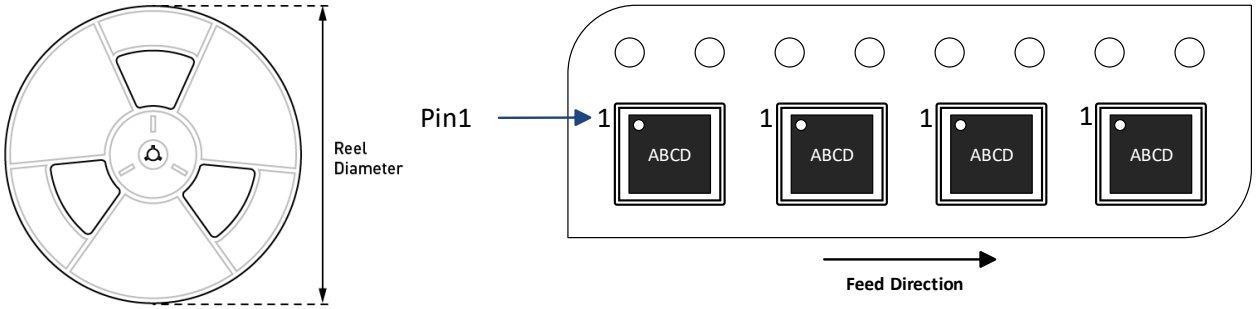


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6615GQKT-Z	TQFN-26 (6mmx6mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/5/2023	Initial Release	-

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MPC1055L1R0C on WIN SOURCE
- Kemet Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management