



THE DATASHEET OF PSMN4R8-100YSEX





PSMN4R8-100YSE

N-channel 100 V, 4.8 mOhm MOSFET with enhanced SOA in LFAK56E

25 June 2021

Product data sheet

1. General description

N-channel enhancement mode MOSFET in a LFAK56E package qualified to 175 °C. Part of Nexperia's "ASFETs for hotswap" portfolio, the PSMN4R8-100YSE delivers very low R_{DSon} and a very strong linear-mode (SOA) performance in a high-reliability copper-clip LFAK56E package. PSMN4R8-100YSE complements the latest "hot-swap" controllers – robust enough to withstand substantial inrush currents during turn-on, low R_{DSon} to minimize I^2R losses delivering optimum efficiency when turned fully ON and an 80% smaller footprint than existing D2PAK types.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R conduction losses
- LFAK56E package for applications that demand the highest performance and reliability in a 30 mm² footprint

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ Fig. 2	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 1	-	-	294	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ Fig. 12	-	3.6	4.8	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C};$ Fig. 13	-	5.6	7.7	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ °C};$ Fig. 14 ; Fig. 15	4	15.3	35	nC
$Q_{G(tot)}$	total gate charge		40	80	120	nC

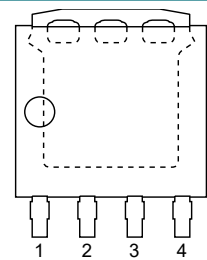
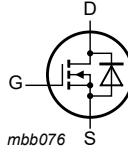
N-channel 100 V, 4.8 mOhm MOSFET with enhanced SOA in LFPAK56E

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 52.6 \text{ A}$; $V_{sup} \leq 100 \text{ V}$; $R_{GS} = 50 \text{ }\Omega$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped; $t_p = 95 \text{ }\mu\text{s}$; Fig. 4	[1]	-	-	325	mJ
Source-drain diode							
Q_r	recovered charge	$I_S = 25 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 50 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 18	-	40	-	nC	

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFPAK56E; Power-SO8 (SOT1023)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN4R8-100YSE	LFPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LFPAK56); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN4R8-100YSE	4E8S10J

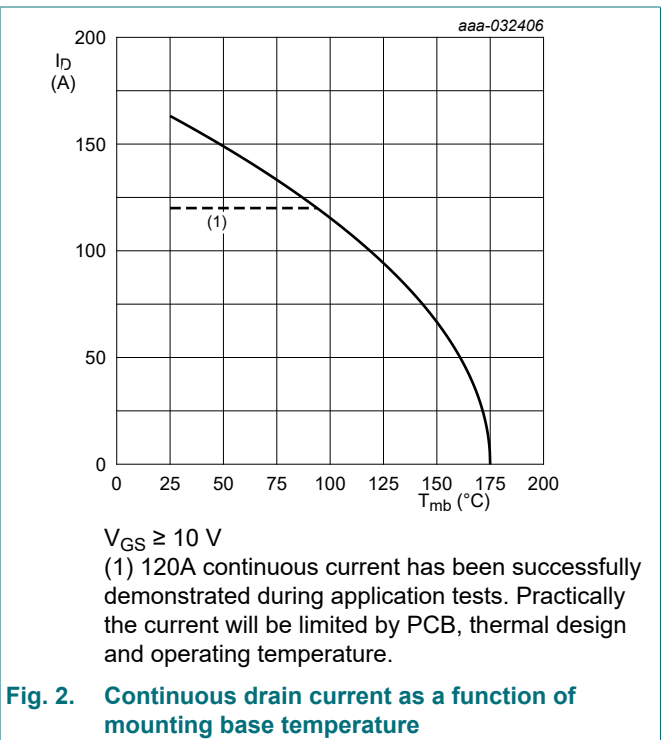
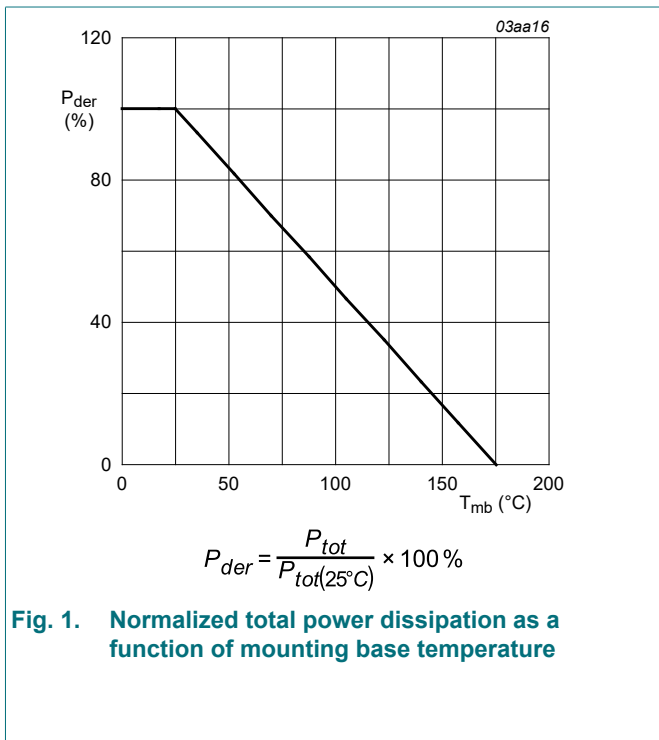
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	100	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	100	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	294	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	120	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	115	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	653	A
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	120	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	653	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 52.6 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 95 μs; Fig. 4	[1]	-	325 mJ
I _{AS}	non-repetitive avalanche current	V _{sup} = 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 4	[1]	-	52.6 A

[1] Protected by 100% test



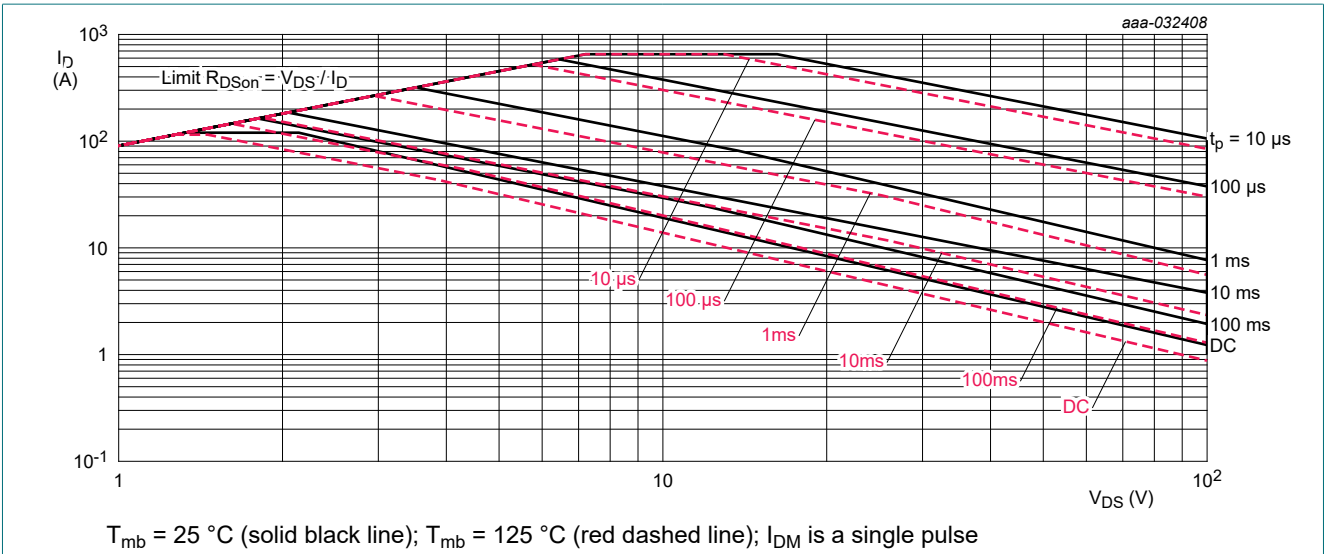


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

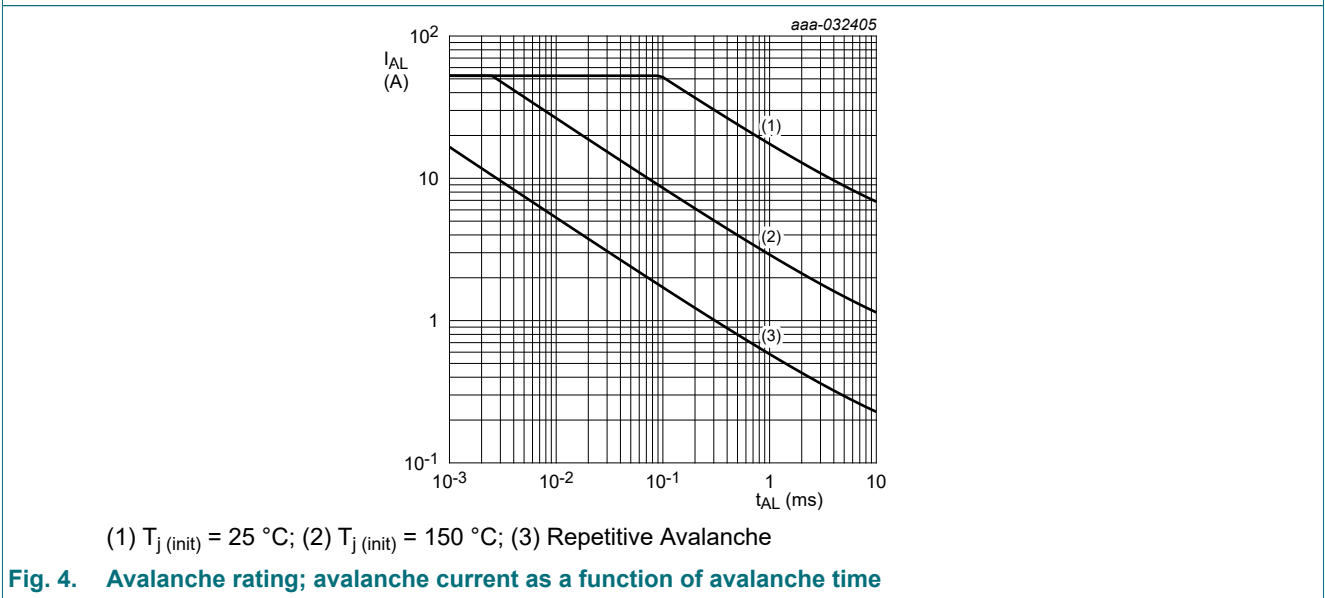


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	42	-	K/W
		Fig. 7	-	85	-	K/W

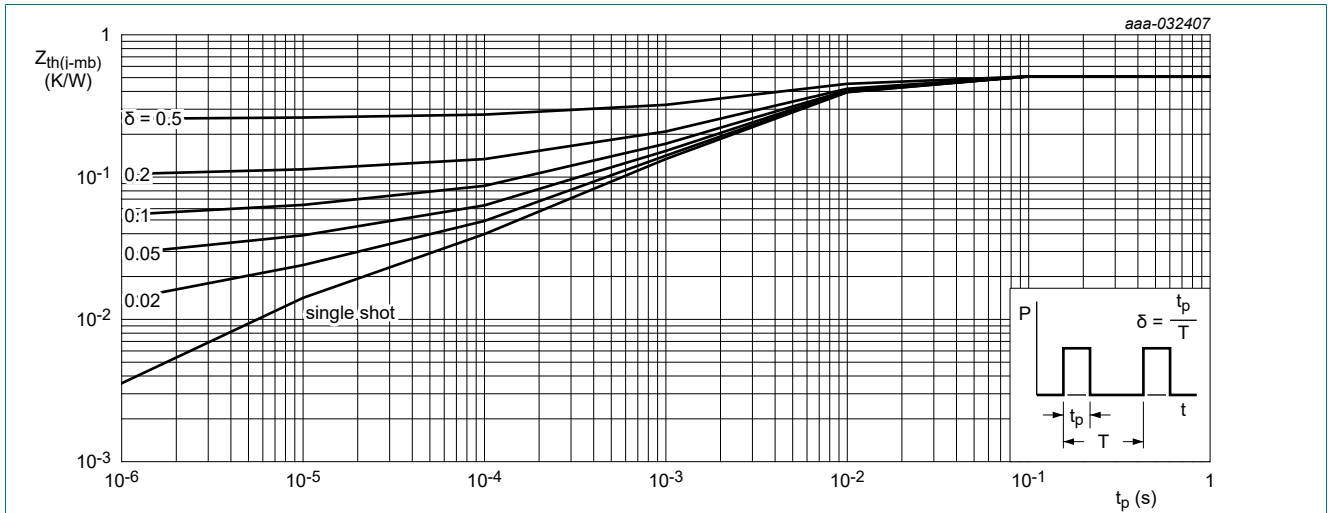


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

Copper area 25.4 mm square; 70 μm thick on FR4 board

70 μm thick copper on FR4 board

Fig. 6. PCB layout for thermal resistance from junction to ambient

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$; Fig. 11	2	2.6	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.6	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-6.1	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.03	1	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	15	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{Dson}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 12	-	3.6	4.8	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C$; Fig. 13	-	5.6	7.7	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$; Fig. 13	-	8	11	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.4	0.83	1.7	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 14 ; Fig. 15	40	80	120	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$	-	40	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 14 ; Fig. 15	17	29	41	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	16.4	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	12.6	-	nC
Q_{GD}	gate-drain charge		4	15.3	35	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 14 ; Fig. 15	-	5.2	-	V
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 16	3550	5920	8290	pF
C_{oss}	output capacitance		800	1335	2140	pF
C_{rss}	reverse transfer capacitance		2	19	50	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 2 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	22	-	ns
t_r	rise time		-	24	-	ns
$t_{d(off)}$	turn-off delay time		-	36	-	ns
t_f	fall time		-	28	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 17	-	0.82	1	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	40	-	ns
Q_r	recovered charge	$V_{DS} = 50 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 18	-	40	-	nC

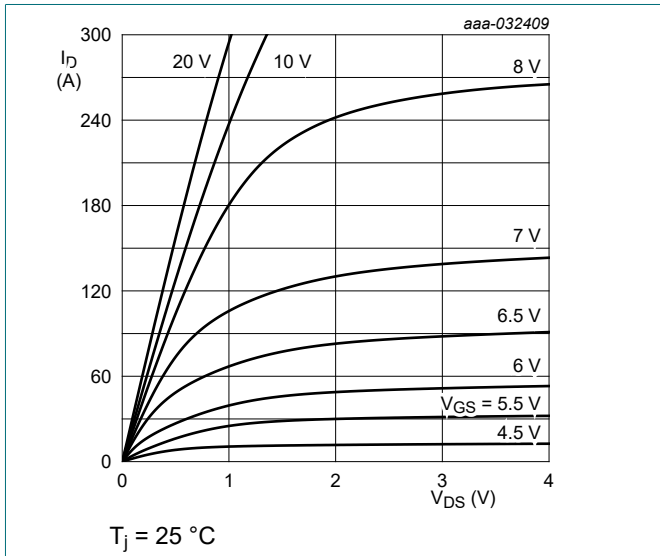


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

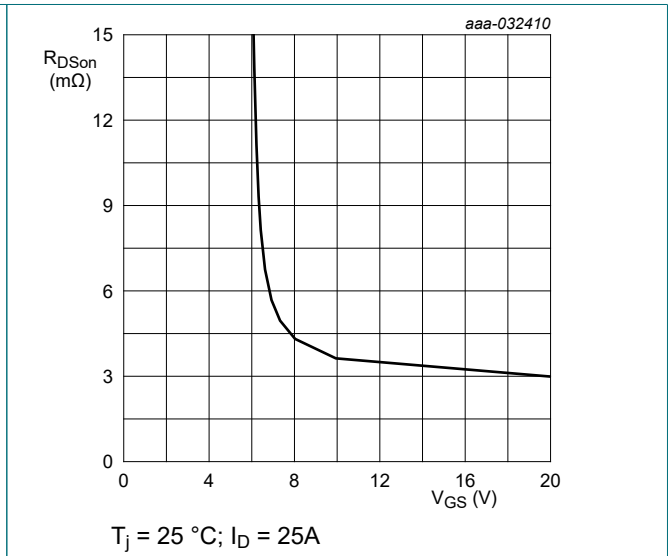


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

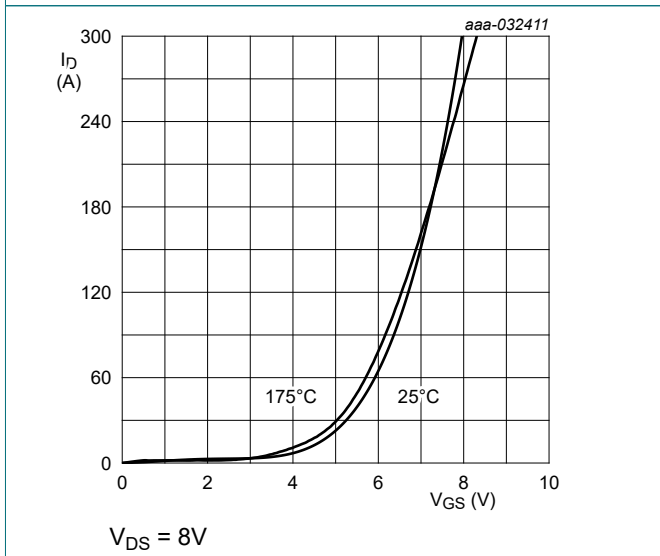


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

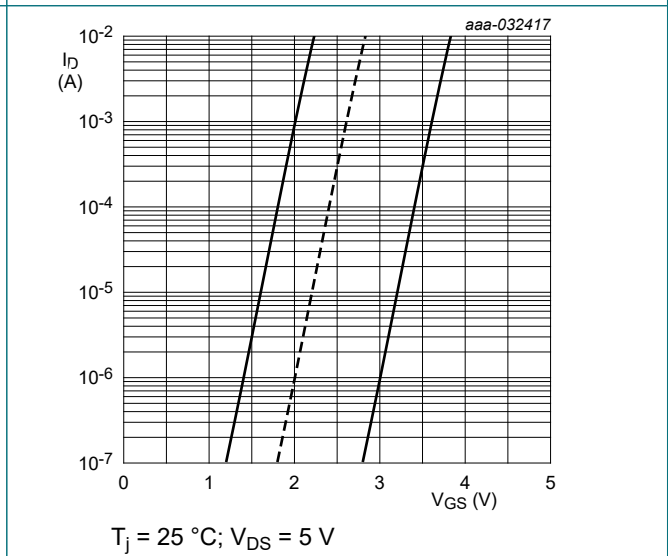


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

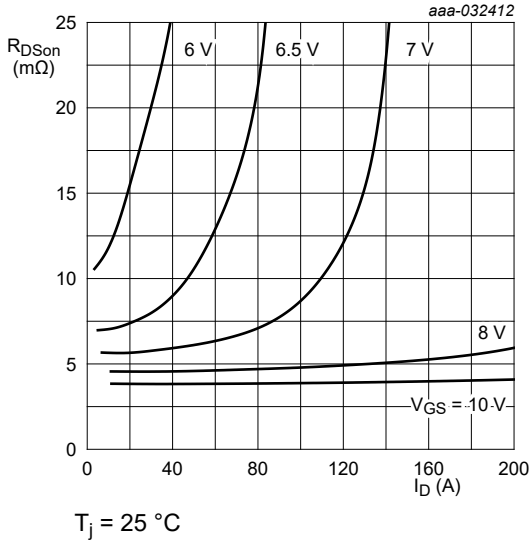
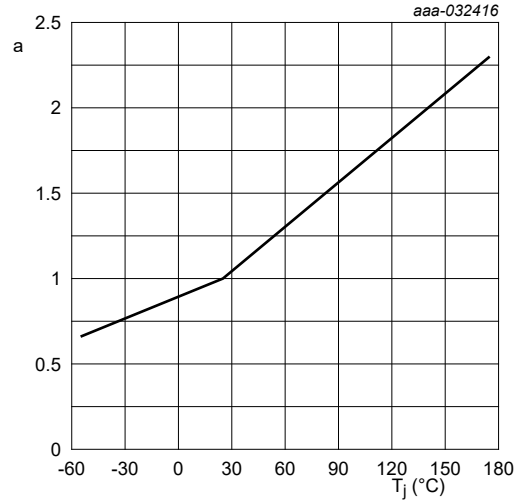


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

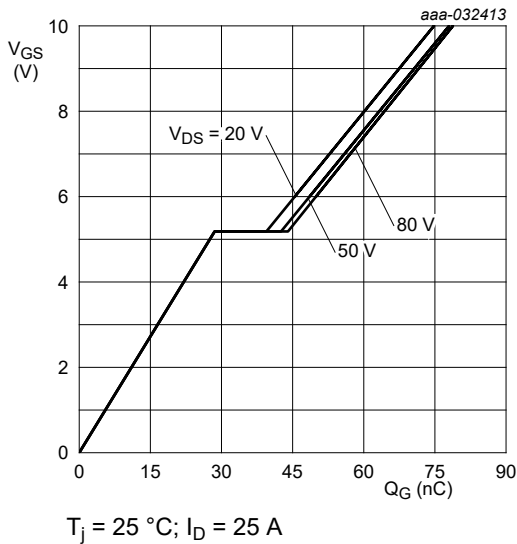


Fig. 14. Gate-source voltage as a function of gate charge; typical values

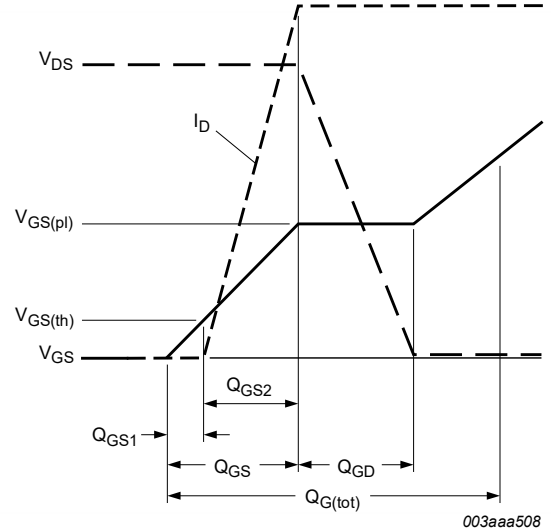


Fig. 15. Gate charge waveform definitions

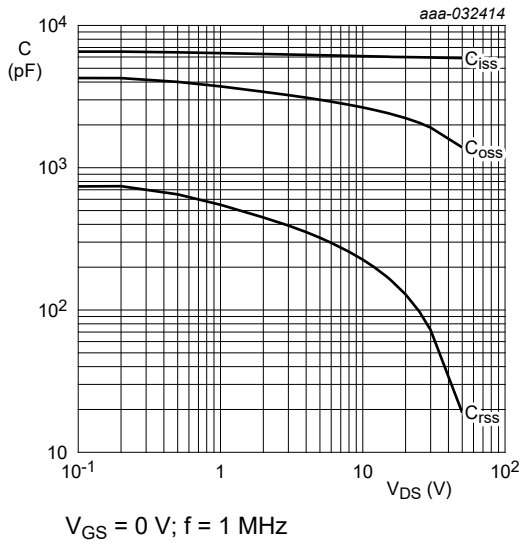


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

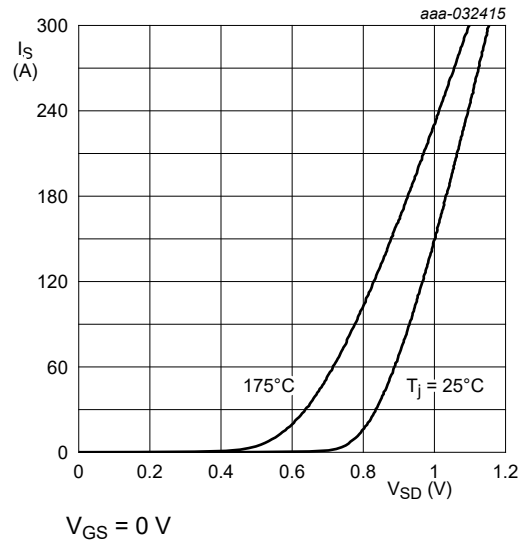


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

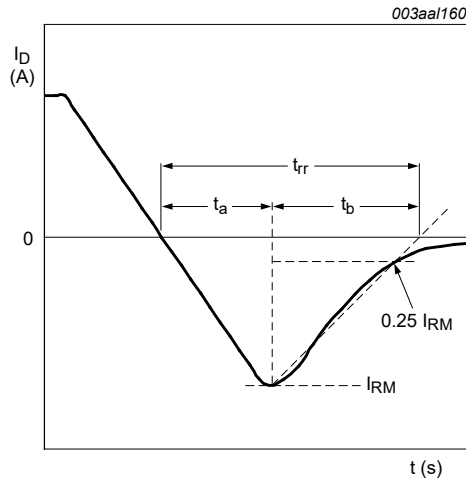


Fig. 18. Reverse recovery timing definition

11. Package outline

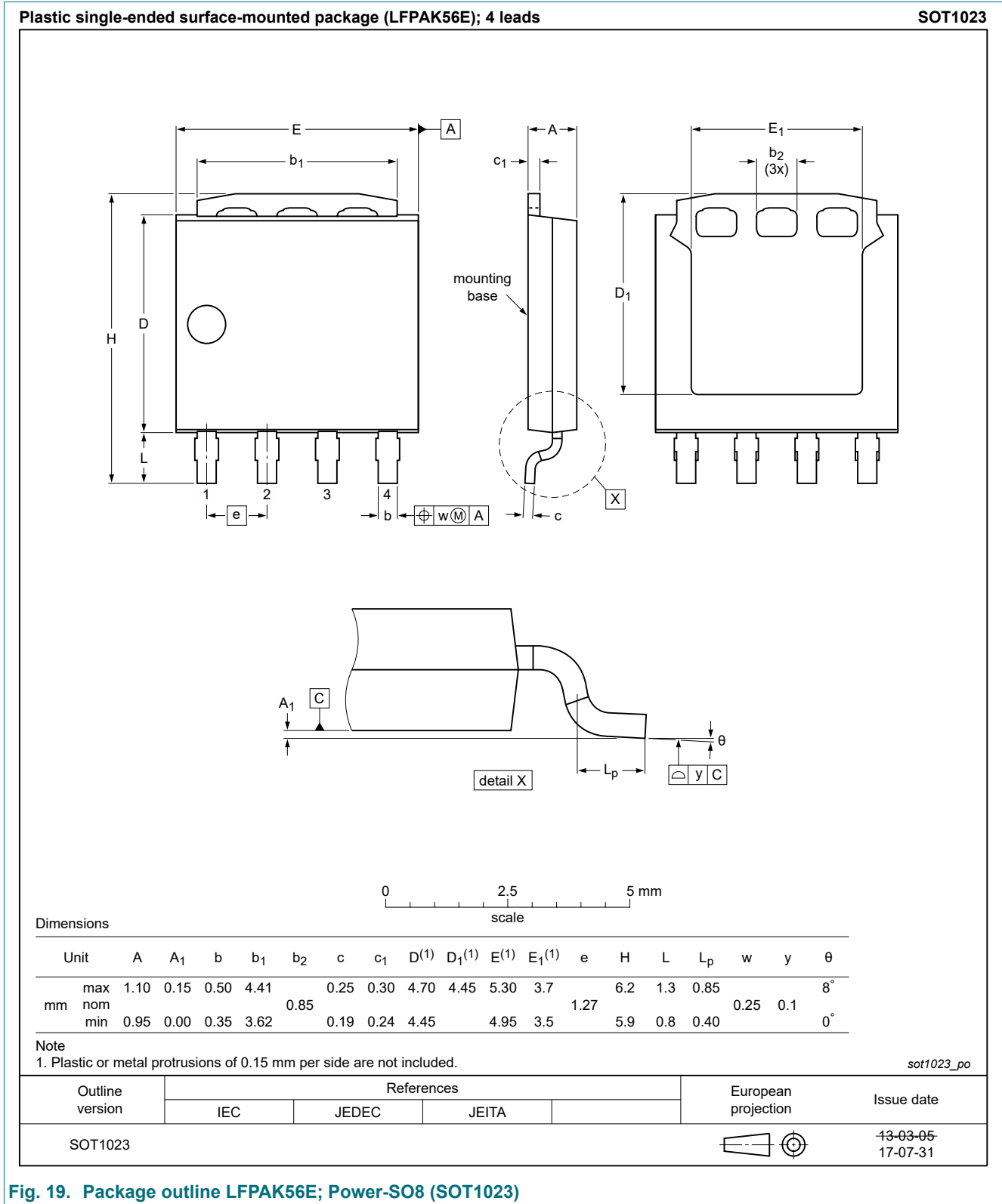


Fig. 19. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering

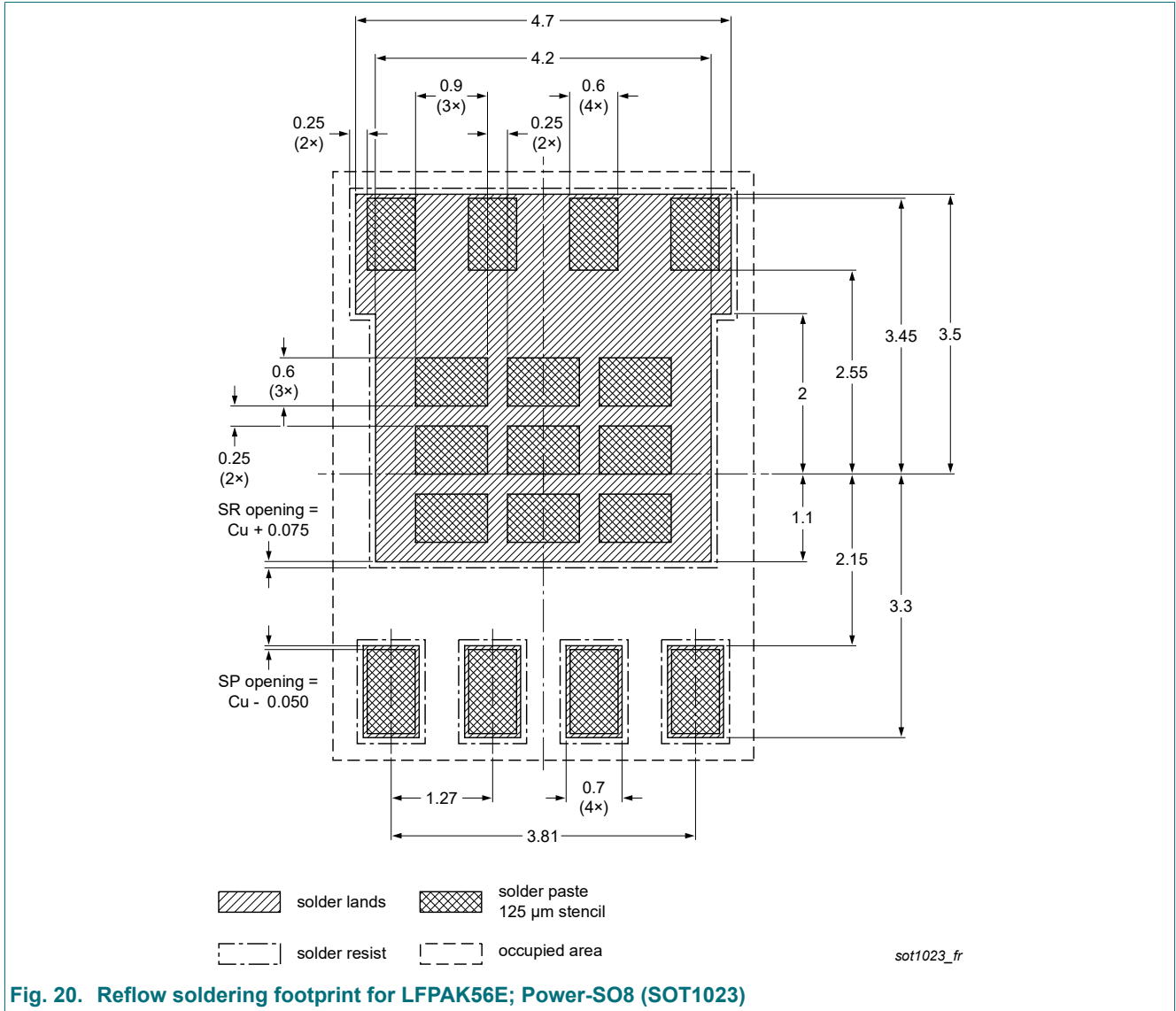


Fig. 20. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

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Contents



1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	3
9. Thermal characteristics.....	5
10. Characteristics.....	6
11. Package outline.....	10
12. Soldering.....	11
13. Legal information.....	12

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