



# THE DATASHEET OF PUMD3-QX





# PUMD3-Q

50 V, 100 mA NPN/PNP resistor-equipped double transistor;  
R1 = 10 kΩ, R2 = 10 kΩ

7 October 2021

Product data sheet

## 1. General description

NPN/PNP Resistor-Equipped double Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PUMH11-Q

PNP/PNP complement: PUMB11-Q

## 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

## 3. Applications

- Digital application in automotive and industrial segments
- Cost-saving alternative for BC847-Q/BC857-Q series in digital applications
- Controlling IC inputs
- Switching loads

## 4. Quick reference data

Table 1. Quick reference data

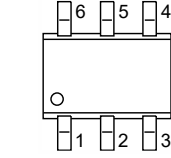
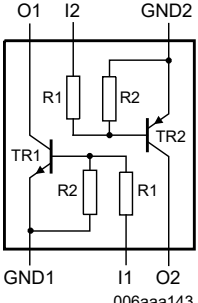
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor, for the PNP transistor with negative polarity</b>						
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	50	V
I <sub>O</sub>	output current		-	-	100	mA
R1	bias resistor 1		[1]	10	13	kΩ
R2/R1	bias resistor ratio		[1]	1	1.2	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$ 

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>TSSOP6 (SOT363)</p>	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMD3-Q	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

## 7. Marking

Table 4. Marking codes

Type number	Marking code <sup>[1]</sup>
PUMD3-Q	D%3

[1] % = placeholder for manufacturing site code

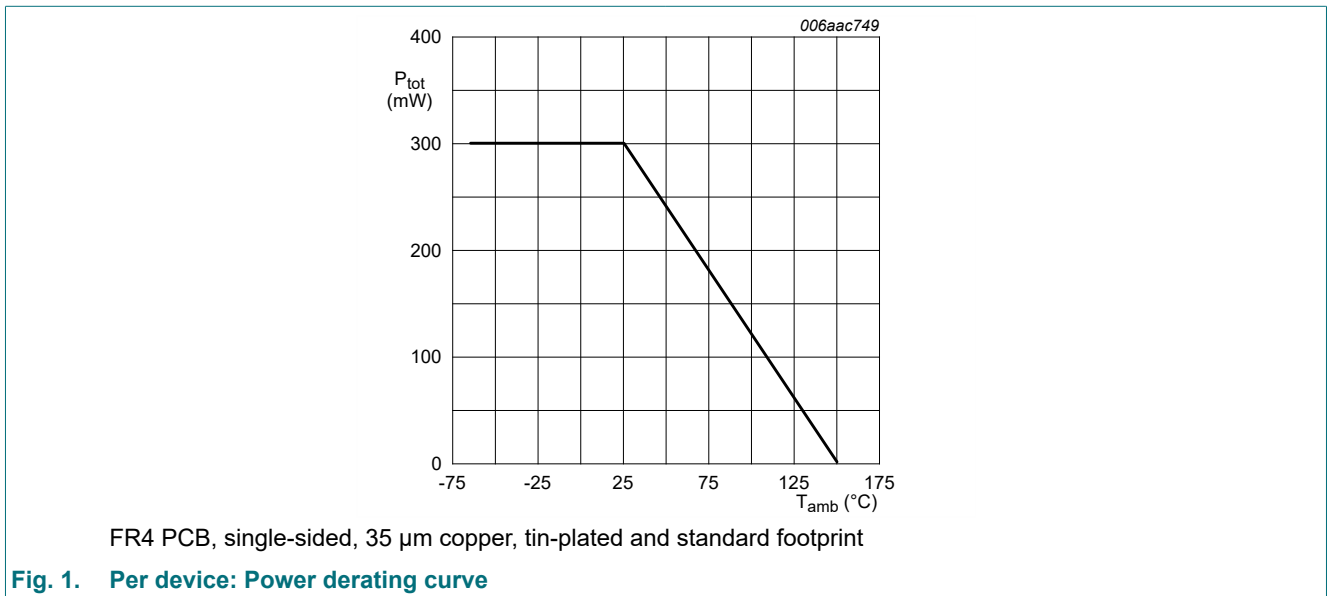
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Per transistor, for the PNP transistor with negative polarity</b>						
V <sub>CBO</sub>	collector-base voltage	open emitter		-	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	10	V
V <sub>I</sub>	input voltage	input voltage TR1		-	40	V
				-	-10	V
		input voltage TR2		-	10	V
				-	-40	V
I <sub>O</sub>	output current		-	100	mA	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	200	mW
<b>Per device</b>						
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	300	mW
T <sub>j</sub>	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.

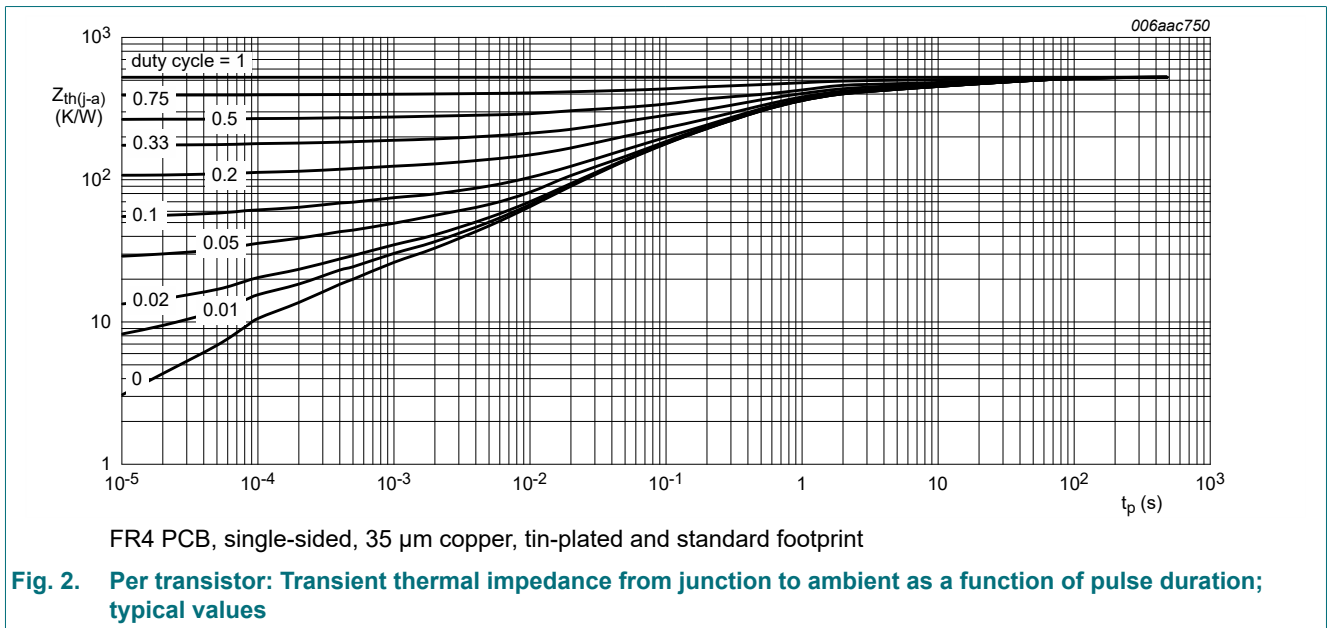


## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.



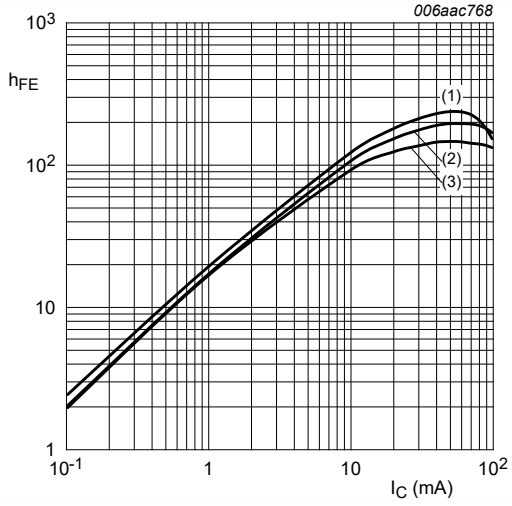
## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor, for the PNP transistor with negative polarity</b>							
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100 \mu\text{A}; I_E = 0 \text{ A}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	50	-	-	V	
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}; I_B = 0 \text{ A}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	50	-	-	V	
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50 \text{ V}; I_E = 0 \text{ A}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	100	nA	
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}; I_B = 0 \text{ A}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	100	nA	
		$V_{CE} = 30 \text{ V}; I_B = 0 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	-	5	$\mu\text{A}$	
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_C = 0 \text{ mA}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	400	$\mu\text{A}$	
$h_{FE}$	DC current gain	$V_{CE} = 5 \text{ V}; I_C = 5 \text{ mA}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	30	-	-		
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	100	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5 \text{ V}; I_C = 100 \mu\text{A}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	1.1	0.8	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_C = 10 \text{ mA}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	2.5	1.8	-	V	
R1	bias resistor 1		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
<b>TR1 (NPN)</b>							
$C_c$	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A}; f = 1 \text{ MHz}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	2.5	pF	
$f_T$	transition frequency	$V_{CE} = 5 \text{ V}; I_C = 10 \text{ mA}; f = 100 \text{ MHz}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[2]	230	-	MHz	
<b>TR2 (PNP)</b>							
$C_c$	collector capacitance	$V_{CB} = -10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A}; f = 1 \text{ MHz}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	3	pF	
$f_T$	transition frequency	$V_{CE} = -5 \text{ V}; I_C = -10 \text{ mA}; f = 100 \text{ MHz}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[2]	180	-	MHz	

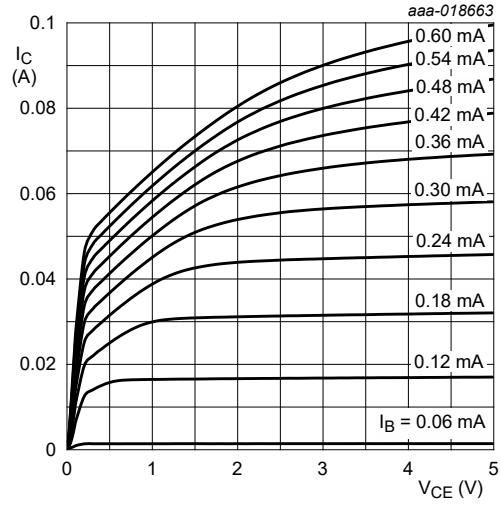
[1] See "Section 11: Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor



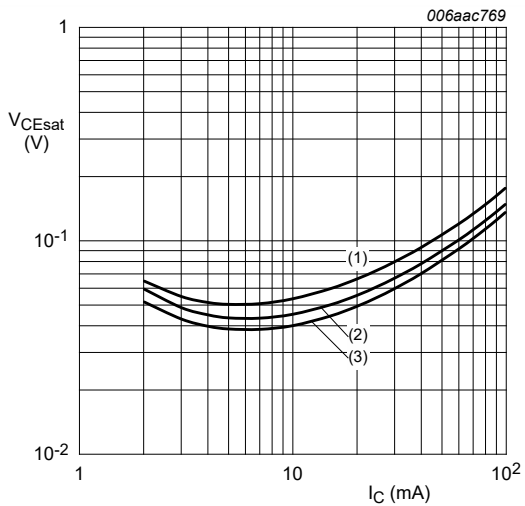
$V_{CE} = 5\text{ V}$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40\text{ }^\circ\text{C}$

**Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values**



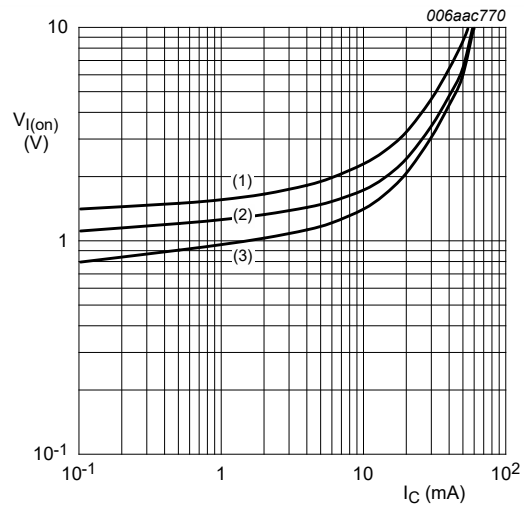
$T_{amb} = 25\text{ }^\circ\text{C}$

**Fig. 4. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values**



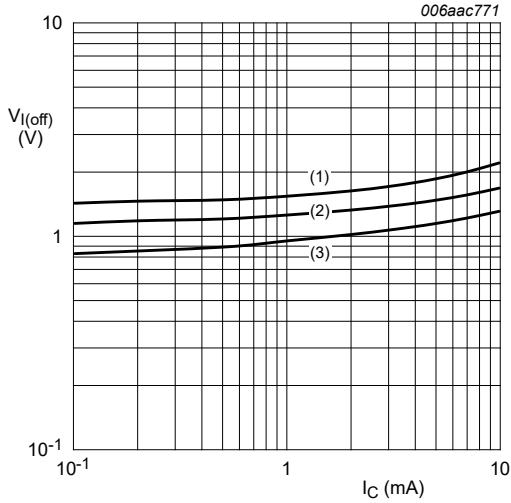
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40\text{ }^\circ\text{C}$

**Fig. 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



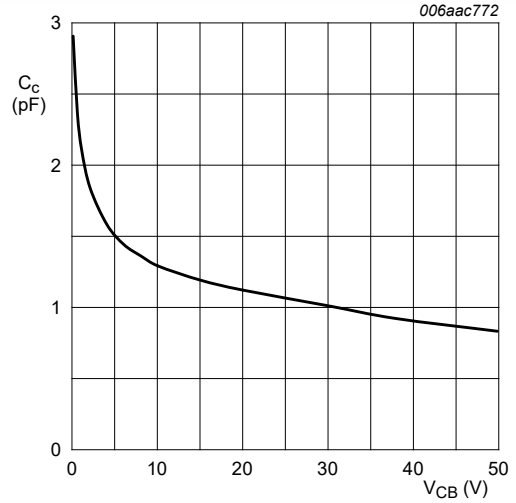
$V_{CE} = 0.3\text{ V}$   
 (1)  $T_{amb} = -40\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

**Fig. 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values**



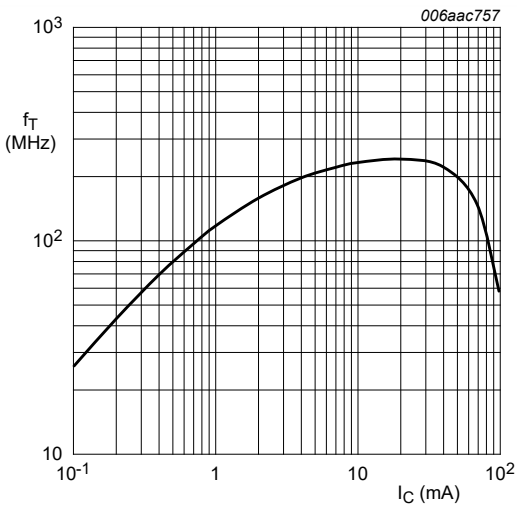
$V_{CE} = 5\text{ V}$   
 (1)  $T_{amb} = -40\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig. 7. TR1 (NPN): Off-state input voltage as a function of collector current; typical values**



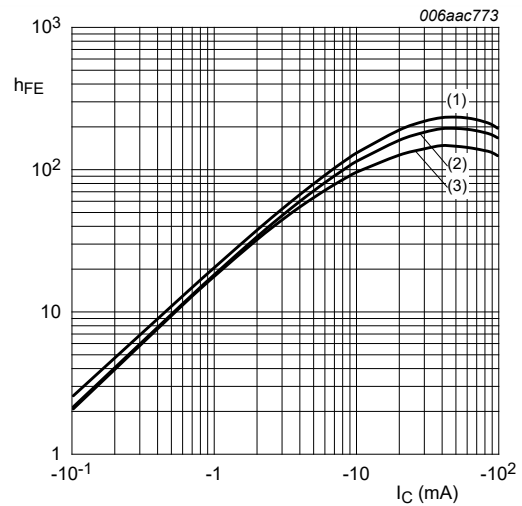
$f = 1\text{ MHz}$   
 $T_{amb} = 25\text{ °C}$

**Fig. 8. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values**



$f = 100\text{ MHz}$   
 $T_{amb} = 25\text{ °C}$   
 $V_{CE} = 5\text{ V}$

**Fig. 9. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor**



$V_{CE} = -5\text{ V}$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -40\text{ °C}$

**Fig. 10. TR2 (PNP): DC current gain as a function of collector current; typical values**

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 10 kΩ

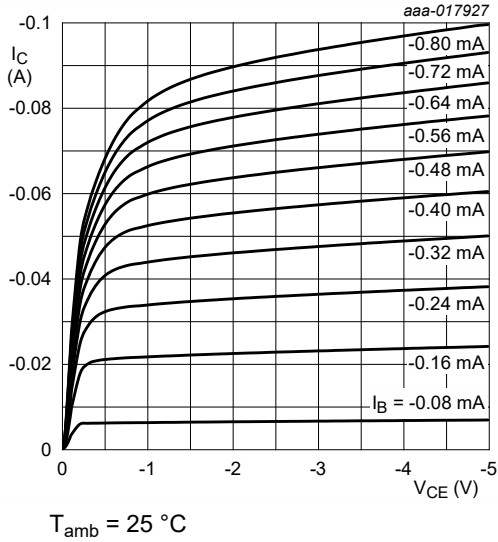


Fig. 11. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values

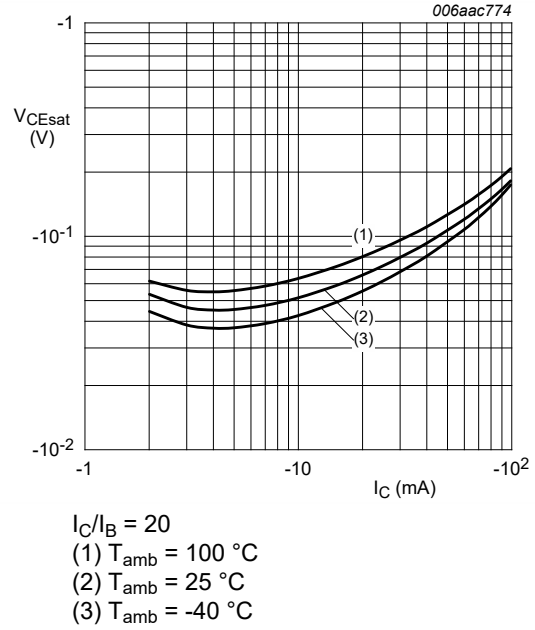


Fig. 12. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

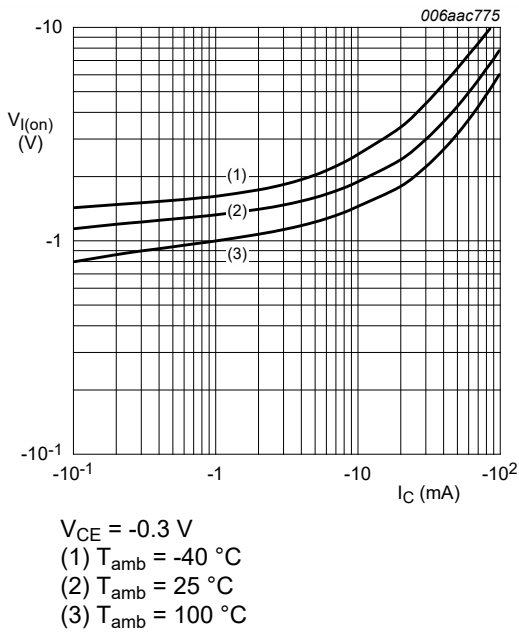


Fig. 13. TR2 (PNP): On-state input voltage as a function of collector current; typical values

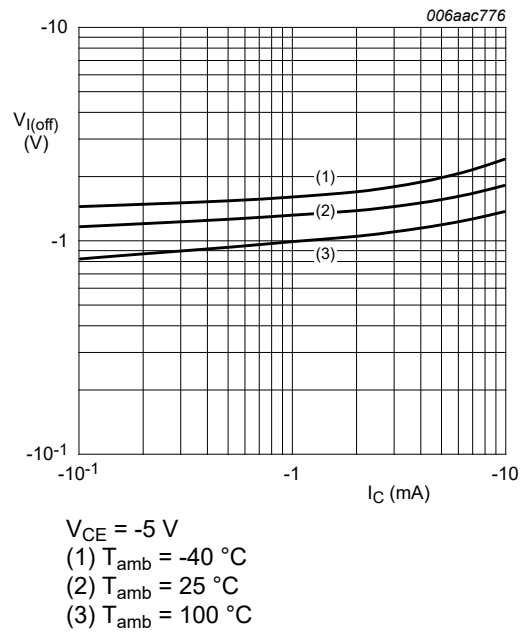
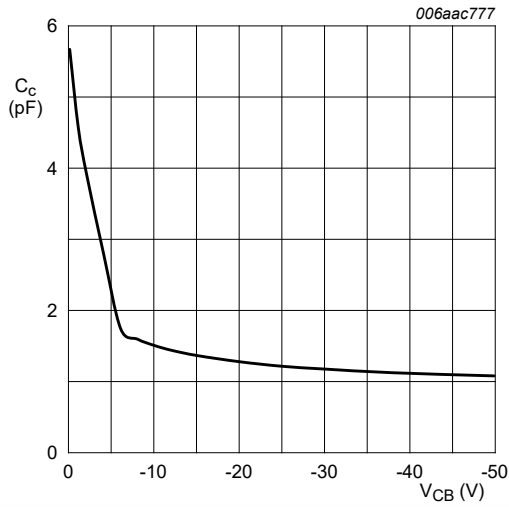
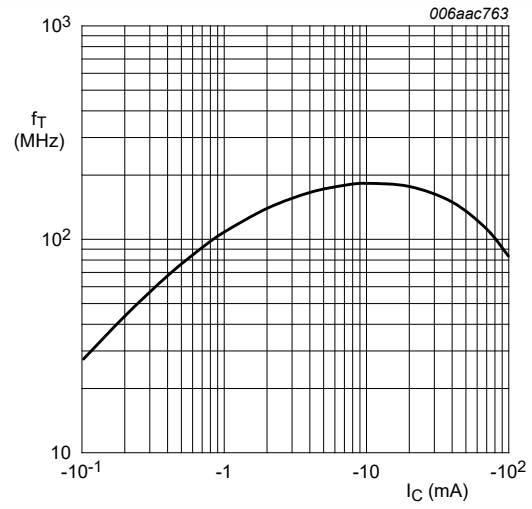


Fig. 14. TR2 (PNP): Off-state input voltage as a function of collector current; typical values



$f = 1 \text{ MHz}$   
 $T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig. 15. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values**



$f = 100 \text{ MHz}$   
 $T_{amb} = 25 \text{ }^\circ\text{C}$   
 $V_{CE} = -5 \text{ V}$

**Fig. 16. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor**

## 11. Test information

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

### Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I12) - V(I11)}{I12 - I11}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$

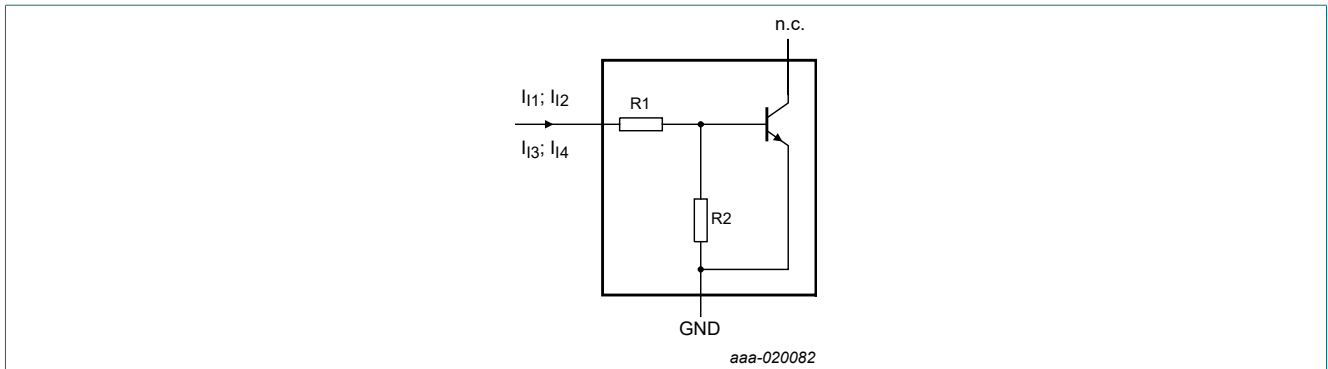


Fig. 17. TR1 (NPN): Resistor test circuit

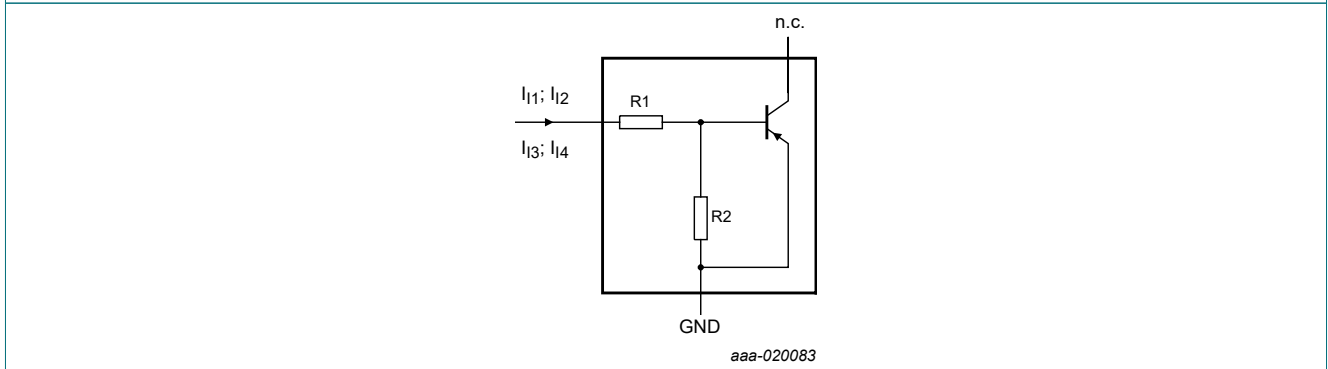


Fig. 18. TR2 (PNP): Resistor test circuit

### Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I <sub>11</sub>	I <sub>12</sub>	I <sub>13</sub>	I <sub>14</sub>
<b>Per transistor, for the PNP with negative polarity</b>						
PUMD3-Q	10	10	350 μA	450 μA	-350 μA	-450 μA

## 12. Package outline

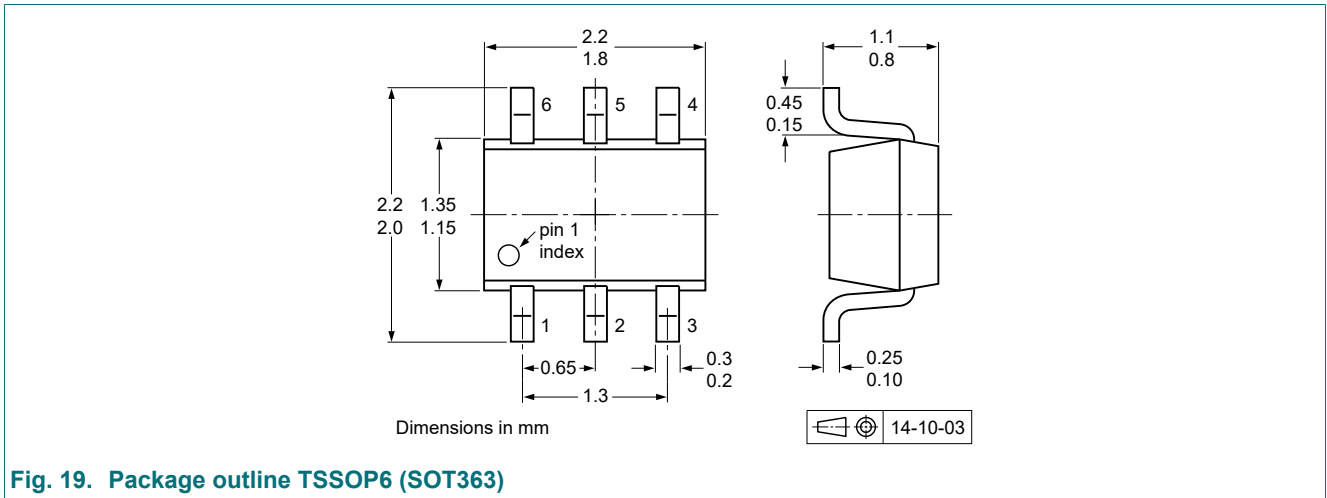


Fig. 19. Package outline TSSOP6 (SOT363)

### 13. Soldering

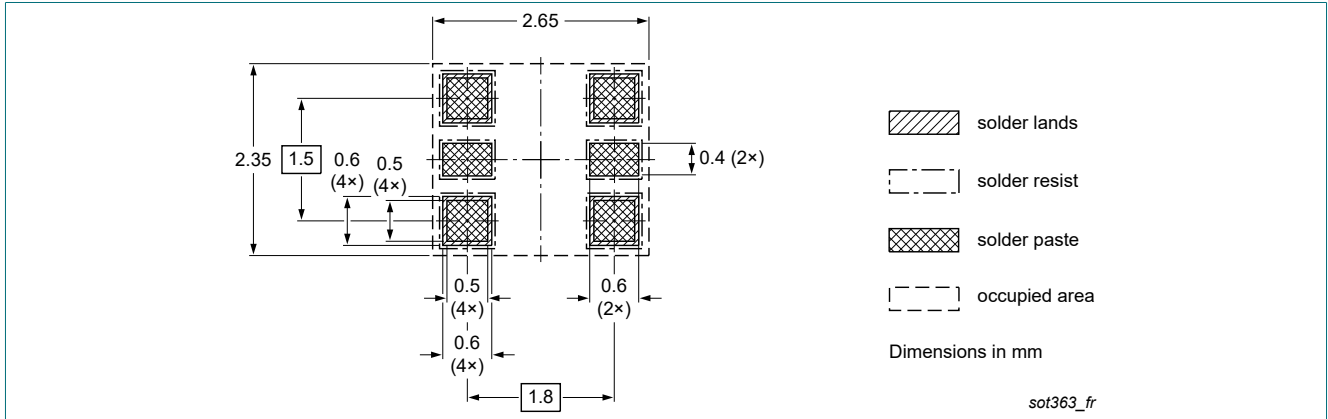


Fig. 20. Reflow soldering footprint for TSSOP6 (SOT363)

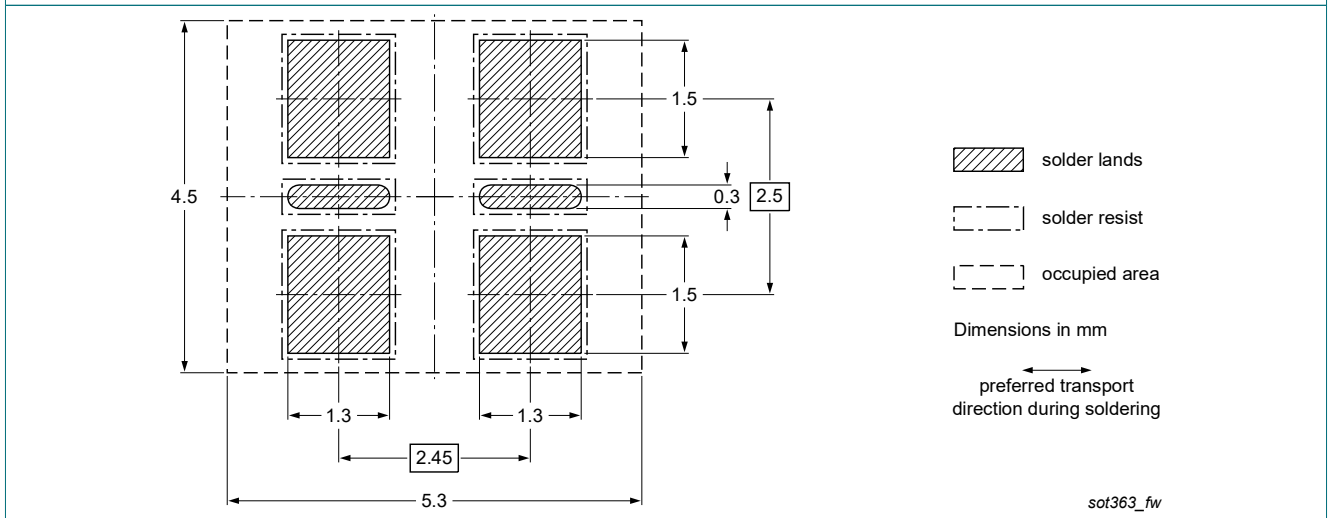


Fig. 21. Wave soldering footprint for TSSOP6 (SOT363)

## 14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMD3-Q v.2	20211007	Product data sheet	-	PUMD3-Q v.1
Modification:	<ul style="list-style-type: none"> <li>• Complete rework</li> <li>• General description: added new lines at the end</li> <li>• Applications: Clarification updated</li> <li>• Pinning: Graphic symbol replaced</li> <li>• Limiting values: deleted parameter <math>I_{CM}</math></li> <li>• Characteristics: <math>I_{CEO}</math> max limit is updated to 100 nA</li> <li>• Characteristics: <math>V_{CEsat}</math> limit is now updated to 100 mV</li> <li>• Characteristics: added new graphics</li> <li>• Characteristics: Updated the graphics conditions</li> <li>• Characteristics: <math>V_{(BR)EBO}</math> values is removed</li> <li>• Test information: Included resistor calculation, resistor test circuit and resistor test condition</li> </ul>			
PUMD3-Q v.1	20210624	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 7 October 2021

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