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Datasheet

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# Renesas RA6M1 Group

Datasheet

## 32-bit MCU

Renesas Advanced (RA) Family
Renesas RA6 Series

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Leading performance 120-MHz Arm® Cortex®-M4 core, 512-KB code flash memory, 256-KB SRAM, Capacitive Touch Sensing Unit, USB 2.0 Full-Speed, SDHI, Quad SPI, security and safety features, and advanced analog.

# Features

### ■ Arm Cortex-M4 Core with Floating Point Unit (FPU)
- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 120 MHz
- Support for 4-GB address space
- On-chip debugging system: JTAG, SWD, and ETM
- Boundary scan and Arm Memory Protection Unit (Arm MPU)

### ■ Memory
- 512-KB code flash memory (40 MHz zero wait states)
- 8-KB data flash memory (125,000 erase/write cycles)
- 256-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

### ■ Connectivity
- USB 2.0 Full-Speed (USBFS) module
  - On-chip transceiver
- Serial Communications Interface (SCI) with FIFO × 7
- Serial Peripheral Interface (SPI) × 2
- $I^2C$ bus interface (IIC) × 2
- CAN module (CAN) × 2
- Serial Sound Interface Enhanced (SSIE)
- SD/MMC Host Interface (SDHI) × 2
- Quad Serial Peripheral Interface (QSPI)
- IrDA interface
- Sampling Rate Converter (SRC)
- External address space
  - 8-bit bus space

### ■ Analog
- 12-bit A/D Converter (ADC12) with 3 sample-and-hold circuits each × 2
- 12-bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 6
- Programmable Gain Amplifier (PGA) × 6
- Temperature Sensor (TSN)

### ■ Timers
- General PWM Timer 32-bit Enhanced High Resolution (GPT32EH) × 4
- General PWM Timer 32-bit Enhanced (GPT32E) × 4
- General PWM Timer 32-bit (GPT32) × 5
- Low Power Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

### ■ Safety
- Error Code Correction (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

### ■ System and Power Management
- Low power modes
- Realtime Clock (RTC) with calendar and VBATT support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 8
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

### ■ Security and Encryption
- AES128/192/256
- 3DES/ARC4
- SHA1/SHA224/SHA256/MD5
- GHASH
- RSA/DSA/ECC
- True Random Number Generator (TRNG)

### ■ Human Machine Interface (HMI)
- Capacitive Touch Sensing Unit (CTSU)

### ■ Multiple Clock Sources
- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

### ■ General-Purpose I/O Ports
- Up to 76 input/output pins
  - Up to 9 CMOS input
  - Up to 67 CMOS input/output
    - Up to 14 input/output 5 V tolerant
    - Up to 13 high current (20 mA)

### ■ Operating Voltage
- VCC: 2.7 to 3.6 V

### ■ Operating Temperature and Packages
- Ta = -40°C to +105°C
  - 100-pin LGA (7 mm × 7 mm, 0.65 mm pitch)
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)

# 1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M4 core running up to 120 MHz with the following features:

- 512-KB code flash memory
- 256-KB SRAM
- Capacitive Touch Sensing Unit (CTSU)
- USBFS
- SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- 12-bit A/D Converter (ADC12)
- 12-bit D/A Converter (DAC12)
- Analog peripherals.

## 1.1 Function Outline

**Table 1.1 Arm core**

| Feature | Functional description |
|---|---|
| Arm Cortex-M4 core | • Maximum operating frequency: up to 120 MHz<br>• Arm Cortex-M4 core:<br>- Revision: r0p1-01rel0<br>- Armv7E-M architecture profile<br>- Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008.<br>• Arm Memory Protection Unit (Arm MPU):<br>- Armv7 Protected Memory System Architecture<br>- 8 protect regions.<br>• SysTick timer:<br>- Driven by SYSTICCLK (LOCO) or ICLK. |

**Table 1.2 Memory**

| Feature | Functional description |
|---|---|
| Code flash memory | 512-KB code flash memory. See section 50, Flash Memory in User's Manual. |
| Data flash memory | 8-KB data flash memory. See section 50, Flash Memory in User's Manual. |
| Memory Mirror Function (MMF) | The Memory Mirror Function (MMF) can be configured to mirror the target application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. Your application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual. |
| Option-setting memory | The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual. |
| SRAM | On-chip high-speed SRAM with either parity-bit or Error Correction Code (ECC). The first 32 KB of SRAM0 provides error correction capability using ECC. Parity check is performed for other areas. See section 48, SRAM in User's Manual. |
| Standby SRAM | On-chip SRAM that can retain data in Deep Software Standby mode. See section 49, Standby SRAM in User's Manual. |

**Table 1.3 System (1 of 2)**

| Feature | Functional description |
|---|---|
| Operating modes | Two operating modes:<br>• Single-chip mode<br>• SCI or USB boot mode.<br>See section 3, Operating Modes in User's Manual. |
| Resets | 14 resets:<br>• RES pin reset<br>• Power-on reset<br>• Voltage monitor 0 reset<br>• Voltage monitor 1 reset<br>• Voltage monitor 2 reset<br>• Independent watchdog timer reset<br>• Watchdog timer reset<br>• Deep Software Standby reset<br>• SRAM parity error reset<br>• SRAM ECC error reset<br>• Bus master MPU error reset<br>• Bus slave MPU error reset<br>• Stack pointer error reset<br>• Software reset.<br>See section 6, Resets in User's Manual. |
| Low Voltage Detection (LVD) | The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual. |
| Clocks | • Main clock oscillator (MOSC)<br>• Sub-clock oscillator (SOSC)<br>• High-speed on-chip oscillator (HOCO)<br>• Middle-speed on-chip oscillator (MOCO)<br>• Low-speed on-chip oscillator (LOCO)<br>• PLL frequency synthesizer<br>• IDWT-dedicated on-chip oscillator<br>• Clock out support.<br>See section 9, Clock Generation Circuit in User's Manual. |
| Clock Frequency Accuracy Measurement Circuit (CAC) | The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.<br>When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.<br>See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual. |
| Interrupt Controller Unit (ICU) | The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual. |
| Key Interrupt Function (KINT) | A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual. |
| Low power modes | Power consumption can be reduced in multiple ways, such as by setting clock dividers, controlling EBCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes in User's Manual. |
| Battery backup function | A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. See section 12, Battery Backup Function in User's Manual. |
| Register write protection | The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection in User's Manual. |
| Memory Protection Unit (MPU) | Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU) in User's Manual. |

**Table 1.3 System (2 of 2)**

| Feature | Functional description |
|---|---|
| Watchdog Timer (WDT) | The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and used as the condition for detecting when the system runs out of control. See section 27, Watchdog Timer (WDT) in User's Manual. |
| Independent Watchdog Timer (IWDT) | The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 28, Independent Watchdog Timer (IWDT) in User's Manual. |

**Table 1.4 Event link**

| Feature | Functional description |
|---|---|
| Event Link Controller (ELC) | The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual. |

**Table 1.5 Direct memory access**

| Feature | Functional description |
|---|---|
| Data Transfer Controller (DTC) | A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual. |
| DMA Controller (DMAC) | An 8-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual. |

**Table 1.6 External bus interface**

| Feature | Functional description |
|---|---|
| External buses | • CS area (EXBIU): Connected to the external devices (external memory interface)<br>• QSPI area (EXBIUT2): Connected to the QSPI (external device interface). |

**Table 1.7 Timers (1 of 2)**

| Feature | Functional description |
|---|---|
| General PWM Timer (GPT) | The General PWM Timer (GPT) is a 32-bit timer with 13 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual. |
| Port Output Enable for GPT (POEG) | Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG) in User's Manual. |
| Low Power Asynchronous General-Purpose Timer (AGT) | The Low Power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 25, Low Power Asynchronous General-Purpose Timer (AGT) in User's Manual. |

**Table 1.7 Timers (2 of 2)**

| Feature | Functional description |
|---|---|
| Realtime Clock (RTC) | The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings.<br>For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years.<br>For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.<br>See section 26, Realtime Clock (RTC) in User's Manual. |

**Table 1.8 Communication interfaces (1 of 2)**

| Feature | Functional description |
|---|---|
| Serial Communications Interface (SCI) | The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces:<br>• Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))<br>• 8-bit clock synchronous interface<br>• Simple IIC (master-only)<br>• Simple SPI<br>• Smart card interface.<br>The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol.<br>Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 30, Serial Communications Interface (SCI) in User's Manual. |
| IrDA Interface (IrDA) | The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 31, IrDA Interface in User's Manual. |
| $I^2C$ bus interface (IIC) | The 2-channel $I^2C$ bus interface (IIC) conforms with and provides a subset of the NXP $I^2C$ (Inter-Integrated Circuit) bus interface functions. See section 32, $I^2C$ Bus Interface (IIC) in User's Manual. |
| Serial Peripheral Interface (SPI) | Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 34, Serial Peripheral Interface (SPI) in User's Manual. |
| Serial Sound Interface Enhanced (SSIE) | The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting $I^2S$ (Inter-Integrated Sound) 2ch, 4ch, 6ch, 8ch, Word Select (WS) Continue/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 37, Serial Sound Interface Enhanced (SSIE) in User's Manual. |
| Quad Serial Peripheral Interface (QSPI) | The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 35, Quad Serial Peripheral Interface (QSPI) in User's Manual. |
| Controller Area Network (CAN) module | The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications.<br>The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 33, Controller Area Network (CAN) Module in User's Manual. |
| USB 2.0 Full-Speed Module (USBFS) module | The USB 2.0 Full-Speed (USBFS) module can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0.<br>The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 29, USB 2.0 Full-Speed Module (USBFS) in User's Manual. |

**Table 1.8 Communication interfaces (2 of 2)**

| Feature | Functional description |
|---|---|
| SD/MMC Host Interface (SDHI) | The SDHI and MultiMediaCard (MMC) interface module provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1-bit and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA).<br>The MMC interface supports 1-bit and 4-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. See section 39, SD/MMC Host Interface (SDHI) in User's Manual. |

**Table 1.9 Analog**

| Feature | Functional description |
|---|---|
| 12-bit A/D Converter (ADC12) | Two units of successive approximation 12-bit A/D Converter (ADC12) are provided. Analog input channels are selectable up to 11 in unit 0 and up to 8 in unit 1. Each 2 analog inputs of unit 0 and 1 are assigned to same port (AN005/AN105, AN006/AN106), up to 17 ports are available as analog input. The temperature sensor output and an internal reference voltage are selectable for conversion of each unit 0 and 1. The A/D conversion accuracy is selectable from 12-bit, 10-bit, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 42, 12-Bit A/D Converter (ADC12) in User's Manual. |
| 12-bit D/A Converter (DAC12) | A 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 43, 12-Bit D/A Converter (DAC12) in User's Manual. |
| Temperature Sensor (TSN) | The on-chip Temperature Sensor (TSN) can determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 44, Temperature Sensor (TSN) in User's Manual. |
| High-Speed Analog Comparator (ACMPHS) | The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result.<br>Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA.<br>Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 45, High-Speed Analog Comparator (ACMPHS) in User's Manual. |

**Table 1.10 Human machine interfaces**

| Feature | Functional description |
|---|---|
| Capacitive Touch Sensing Unit (CTSU) | The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that fingers do not come into direct contact with the electrodes. See section 46, Capacitive Touch Sensing Unit (CTSU) in User's Manual. |

**Table 1.11 Data processing (1 of 2)**

| Feature | Functional description |
|---|---|
| Cyclic Redundancy Check (CRC) calculator | The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 36, Cyclic Redundancy Check (CRC) Calculator in User's Manual. |
| Data Operation Circuit (DOC) | The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 47, Data Operation Circuit (DOC) in User's Manual. |

**Table 1.11 Data processing (2 of 2)**

| Feature | Functional description |
|---|---|
| Sampling Rate Converter (SRC) | The Sampling Rate Converter (SRC) converts the sampling rate of data produced by various audio decoders, such as the WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported.<br>See section 38, Sampling Rate Converter (SRC) in User's Manual. |

**Table 1.12 Security**

| Feature | Functional description |
|---|---|
| Secure Crypto Engine 7 (SCE7) | • Security algorithms:<br>- Symmetric algorithms: AES, 3DES, and ARC4<br>- Asymmetric algorithms: RSA, DSA, and ECC.<br>• Other support features:<br>- TRNG (True Random Number Generator)<br>- Hash-value generation: SHA1, SHA224, SHA256, GHASH, and MD5<br>- 128-bit unique ID. |

**Table 1.13 I/O ports**

| Feature | Functional description |
|---|---|
| Programmable I/O ports | • I/O ports for the 100-pin LGA, 100-pin LQFP<br>- I/O pins: 67<br>- Input pins: 9<br>- Pull-Up resistors: 68<br>- Open-drain outputs: 67<br>- 5-V tolerance: 14<br>• I/O ports for the 64-pin LQFP, 64-pin QFN<br>- I/O pins: 35<br>- Input pins: 5<br>- Pull-Up resistors: 36<br>- Open-drain outputs: 35<br>- 5-V tolerance: 9 |

## 1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset, some individual devices within the group have a subset of the features.

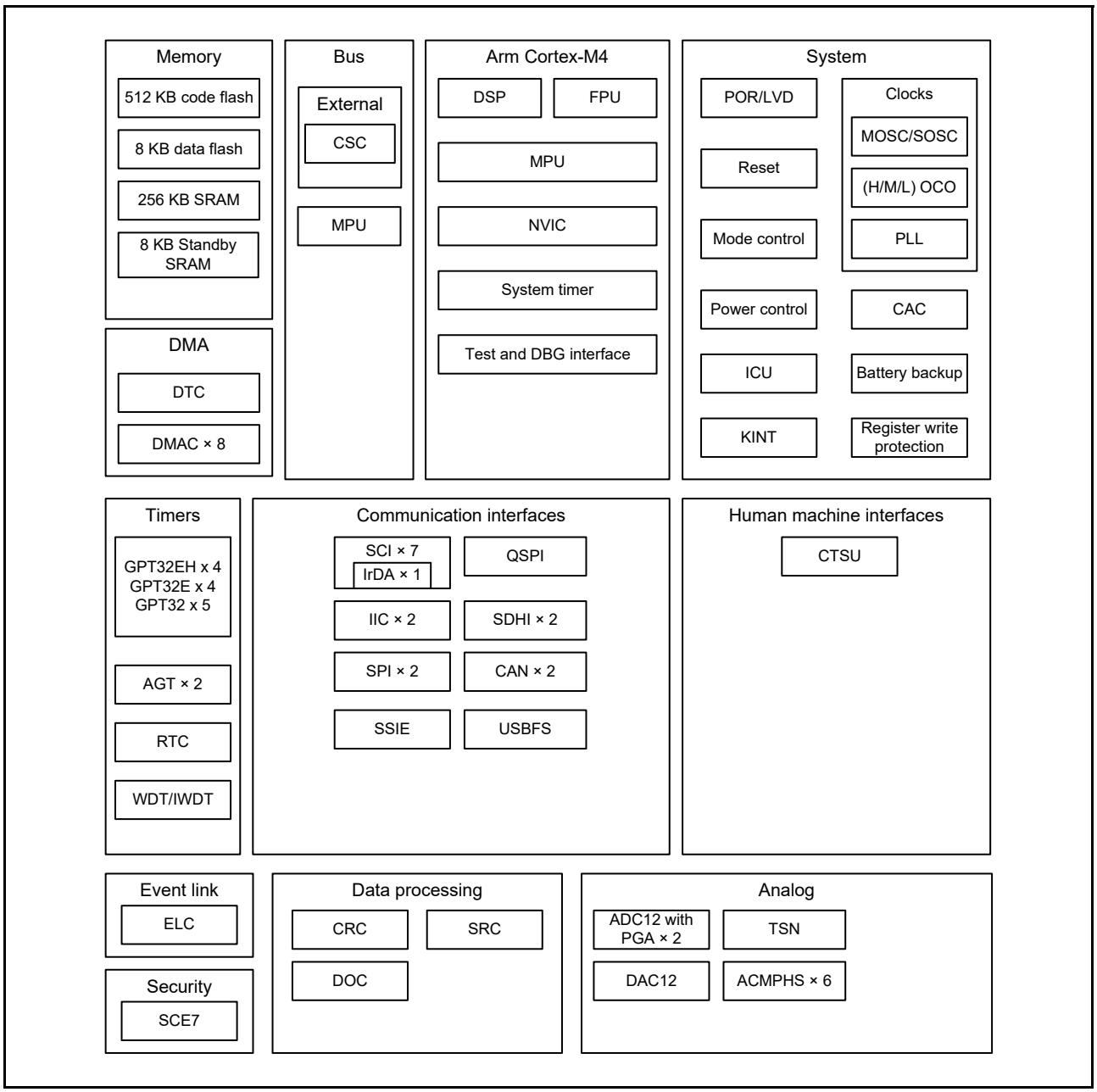



**Figure 1.1 Block diagram**

## 1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.14 shows a list of products.

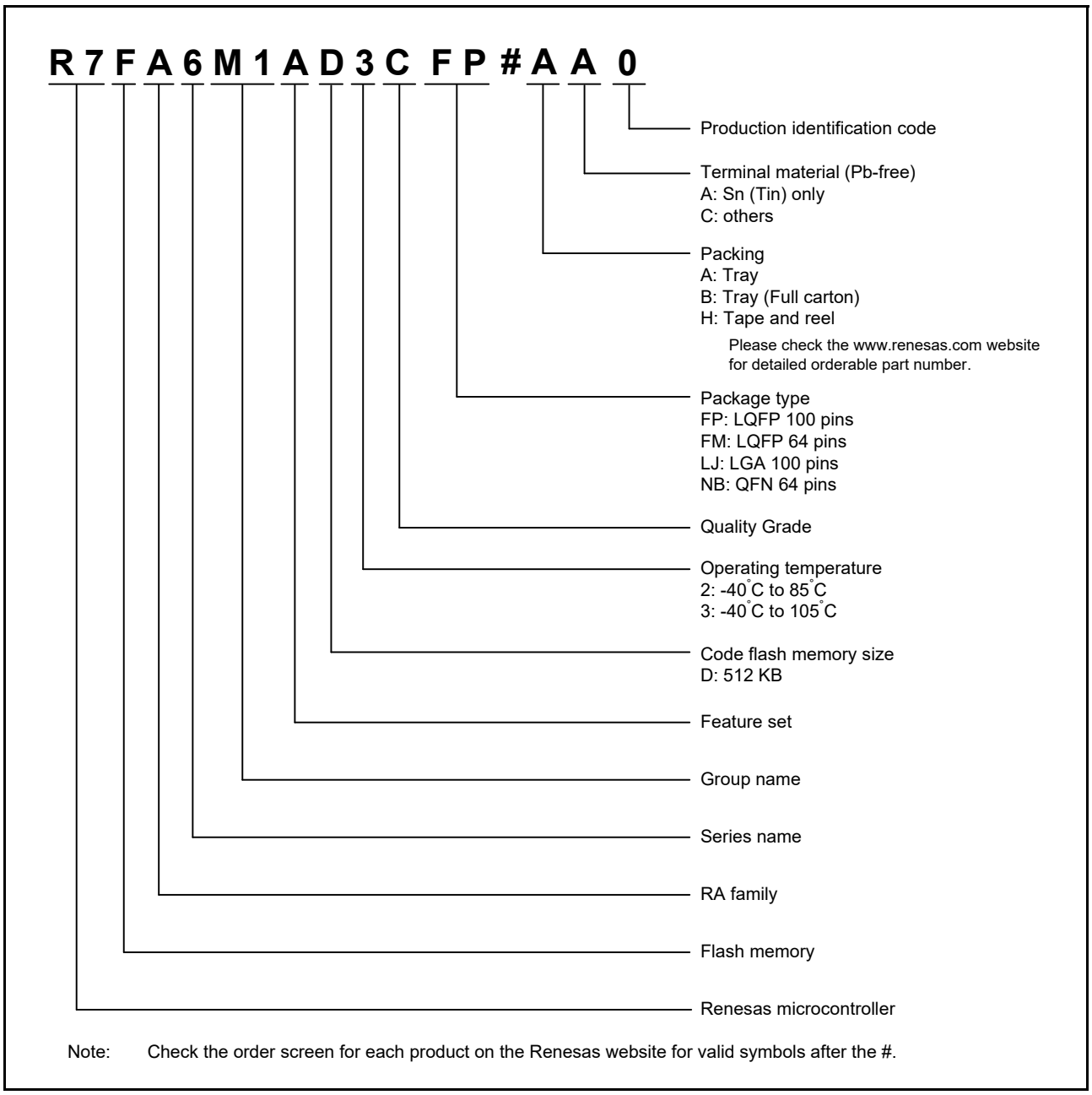



**Figure 1.2 Part numbering scheme**

**Table 1.14 Product list**

| Product part number | Package code | Code flash | Data flash | SRAM | Operating temperature |
|---|---|---|---|---|---|
| R7FA6M1AD2CLJ | PTLG0100JA-A | 512 KB | 8 KB | 256 KB | -40 to +85°C |
| R7FA6M1AD3CLJ | | | | | -40 to +105°C |
| R7FA6M1AD3CFP | PLQP0100KB-B | | | | -40 to +105°C |
| R7FA6M1AD3CFM | PLQP0064KB-C | | | | -40 to +105°C |
| R7FA6M1AD3CNB | PWQN0064LA-A | | | | -40 to +105°C |

## 1.4 Function Comparison

**Table 1.15 Functional comparison**

| Function | | Part numbers | | | |
|---|---|---|---|---|---|
| | | R7FA6M1AD2CLJ/ R7FA6M1AD3CLJ | R7FA6M1AD3CFP | R7FA6M1AD3CFM | R7FA6M1AD3CNB |
| Pin count | | 100 | | 64 | |
| Package | | LGA | LQFP | LQFP | QFN |
| Code flash memory | | 512 KB | | | |
| Data flash memory | | 8 KB | | | |
| SRAM | | 256 KB | | | |
| | Parity | 224 KB | | | |
| | ECC | 32 KB | | | |
| Standby SRAM | | 8 KB | | | |
| System | CPU clock | 120 MHz | | | |
| | Backup registers | 512 B | | | |
| | ICU | Yes | | | |
| | KINT | 8 | | | |
| Event link | ELC | Yes | | | |
| DMA | DTC | Yes | | | |
| | DMAC | 8 | | | |
| BUS | External bus | 8-bit bus | | No | |
| Timers | GPT32EH | 4 | | | |
| | GPT32E | 4 | | 3 | |
| | GPT32 | 5 | | 4 | |
| | AGT | 2 | | | |
| | RTC | Yes | | | |
| | WDT/IWDT | Yes | | | |
| Communication | SCI | 7 | | | |
| | IIC | 2 | | | |
| | SPI | 2 | | | |
| | SSIE | 1 | | No | |
| | QSPI | 1 | | | |
| | SDHI | 2 | | No | |
| | CAN | 2 | | | |
| | USBFS | Yes | | | |
| Analog | ADC12 | Unit0: 11<br>Unit1: 8<br>Shared channel pin: 2*1 | | Unit0: 7<br>Unit1: 3<br>Shared channel pin: 2*1 | |
| | 3ch-S/H | Unit0: 1 (3ch)<br>Unit1: 1 (3ch) | | Unit0: 1 (3ch) | |
| | PGA | Unit0: 3<br>Unit1: 3 | | Unit0: 3 | |
| | DAC12 | 2 | | | |
| | ACMPHS | 6 | | | |
| | TSN | Yes | | | |
| HMI | CTSU | 12 | | 7 | |
| Data processing | CRC | Yes | | | |
| | DOC | Yes | | | |
| | SRC | Yes | | | |
| Security | | SCE7 | | | |
| I/O Ports | I/O Pins | 67 | | 35 | |
| | Input pins | 9 | | 5 | |
| | Pull-up resistors | 68 | | 36 | |
| | open-drain outputs | 67 | | 35 | |
| | 5-V tolerance | 14 | | 9 | |

Note 1. Some input channels of the ADC units are sharing same port pin.

## 1.5 Pin Functions

**Table 1.16 Pin functions (1 of 4)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| Power supply | VCC | Input | Power supply pin. This is used as the digital power supply for the respective modules and internal voltage regulator, and used to monitor the voltage of the POR/LVD. Connect this pin to the system power supply. Connect it to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin. |
| | VCL0 | Input | Connect this pin to VSS through a 0.1-μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin. |
| | VCL | Input | |
| | VSS | Input | Ground pin. Connect to the system power supply (0 V). |
| | VBATT | Input | Backup power pin |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | XCIN | Input | Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN. |
| | XCOUT | Output | |
| | EBCLK | Output | Outputs the external bus clock for external devices |
| | CLKOUT | Output | Clock output pin |
| Operating mode control | MD | Input | Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state. |
| System control | RES | Input | Reset signal input pin. The MCU enters the reset state when this signal goes low. |
| CAC | CACREF | Input | Measurement reference clock input pin |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQ0 to IRQ13 | Input | Maskable interrupt request pins |
| KINT | KR00 to KR07 | Input | A key interrupt can be generated by inputting a falling edge to the key interrupt input pins |
| On-chip emulator | TMS | I/O | On-chip emulator or boundary scan pins |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TCLK | Output | This pin outputs the clock for synchronization with the trace data |
| | TDATA0 to TDATA3 | Output | Trace data output |
| | SWDIO | I/O | Serial wire debug data input/output pin |
| | SWCLK | Input | Serial wire clock pin |
| | SWO | Output | Serial wire trace output pin |
| External bus interface | RD | Output | Strobe signal indicating that reading from the external bus interface space is in progress, active-low |
| | WR0 | Output | Strobe signal indicating that writing to the external bus interface space is in progress, active-low |
| | ALE | Output | Address latch signal when address/data multiplexed bus is selected |
| | WAIT | Input | Input pin for wait request signals in access to the external space, active-low |
| | CS0, CS1, CS4 to CS7 | Output | Select signals for CS areas, active-low |
| | A00 to A12 | Output | Address bus |
| | D00 to D07 | I/O | Data bus |
| | A00/D00 to A07/D07 | I/O | Address/data multiplexed bus |

**Table 1.16 Pin functions (2 of 4)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| GPT | GTETRGA, GTETRGB, GTETRGC, GTETRGD | Input | External trigger input pins |
| | GTIOC0A to GTIOC12A, GTIOC0B to GTIOC12B | I/O | Input capture, output compare, or PWM output pins |
| | GTIU | Input | Hall sensor input pin U |
| | GTIV | Input | Hall sensor input pin V |
| | GTIW | Input | Hall sensor input pin W |
| | GTOUUP | Output | 3-phase PWM output for BLDC motor control (positive U phase) |
| | GTOULO | Output | 3-phase PWM output for BLDC motor control (negative U phase) |
| | GTOVUP | Output | 3-phase PWM output for BLDC motor control (positive V phase) |
| | GTOVLO | Output | 3-phase PWM output for BLDC motor control (negative V phase) |
| | GTOWUP | Output | 3-phase PWM output for BLDC motor control (positive W phase) |
| | GTOWLO | Output | 3-phase PWM output for BLDC motor control (negative W phase) |
| AGT | AGTEE0, AGTEE1 | Input | External event input enable signals |
| | AGTIO0, AGTIO1 | I/O | External event input and pulse output pins |
| | AGTO0, AGTO1 | Output | Pulse output pins |
| | AGTOA0, AGTOA1 | Output | Output compare match A output pins |
| | AGTOB0, AGTOB1 | Output | Output compare match B output pins |
| RTC | RTCOUT | Output | Output pin for 1-Hz or 64-Hz clock |
| | RTCIC0 to RTCIC2 | Input | Time capture event input pins |
| SCI | SCK0 to SCK4, SCK8, SCK9 | I/O | Input/output pins for the clock (clock synchronous mode) |
| | RXD0 to RXD4, RXD8, RXD9 | Input | Input pins for received data (asynchronous mode/clock synchronous mode) |
| | TXD0 to TXD4, TXD8, TXD9 | Output | Output pins for transmitted data (asynchronous mode/clock synchronous mode) |
| | CTS0_RTS0 to CTS4_RTS4, CTS8_RTS8, CTS9_RTS9 | I/O | Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low |
| | SCL0 to SCL4, SCL8, SCL9 | I/O | Input/output pins for the IIC clock (simple IIC mode) |
| | SDA0 to SDA4, SDA8, SDA9 | I/O | Input/output pins for the IIC data (simple IIC mode) |
| | SCK0 to SCK4, SCK8, SCK9 | I/O | Input/output pins for the clock (simple SPI mode) |
| | MISO0 to MISO4, MISO8, MISO9 | I/O | Input/output pins for slave transmission of data (simple SPI mode) |
| | MOSI0 to MOSI4, MOSI8, MOSI9 | I/O | Input/output pins for master transmission of data (simple SPI mode) |
| | SS0 to SS4, SS8, SS9 | Input | Chip-select input pins (simple SPI mode), active-low |
| IIC | SCL0, SCL1 | I/O | Input/output pins for the clock |
| | SDA0, SDA1 | I/O | Input/output pins for data |
| SSIE | SSIBCK0 | I/O | SSIE serial bit clock pins |
| | SSILRCK0/SSIFS0 | I/O | LR clock/frame synchronization pins |
| | SSITXD0 | Output | Serial data output pins |
| | SSIRXD0 | Input | Serial data input pins |
| | AUDIO_CLK | Input | External clock pin for audio (input oversampling clock) |

**Table 1.16 Pin functions (3 of 4)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| SPI | RSPCKA, RSPCKB | I/O | Clock input/output pin |
| | MOSIA, MOSIB | I/O | Input or output pins for data output from the master |
| | MISOA, MISOB | I/O | Input or output pins for data output from the slave |
| | SSLA0, SSLB0 | I/O | Input or output pin for slave selection |
| | SSLA1 to SSLA3, SSLB1 to SSLB3 | Output | Output pins for slave selection |
| QSPI | QSPCLK | Output | QSPI clock output pin |
| | QSSL | Output | QSPI slave output pin |
| | QIO0 to QIO3 | I/O | Data0 to Data3 |
| CAN | CRX0, CRX1 | Input | Receive data |
| | CTX0, CTX1 | Output | Transmit data |
| USBFS | VCC_USB | Input | Power supply pins |
| | VSS_USB | Input | Ground pins |
| | USB_DP | I/O | D+ I/O pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus |
| | USB_DM | I/O | D- I/O pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus |
| | USB_VBUS | Input | USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller. |
| | USB_EXICEN | Output | Low-power control signal for external power supply (OTG) chip |
| | USB_VBUSEN | Output | VBUS (5 V) supply enable signal for external power supply chip |
| | USB_OVRCURA, USB_OVRCURB | Input | Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected. |
| | USB_ID | Input | Connect the MicroAB connector ID input signal to this pin during operation in OTG mode |
| SDHI | SD0CLK, SD1CLK | Output | SD clock output pins |
| | SD0CMD, SD1CMD | I/O | Command output pin and response input signal pins |
| | SD0DAT0 to SD0DAT3, SD1DAT0 to SD1DAT3 | I/O | SD and MMC data bus pins |
| | SD0CD | Input | SD card detection pins |
| | SD0WP | Input | SD write-protect signals |
| Analog power supply | AVCC0 | Input | Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin. |
| | AVSS0 | Input | Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin. |
| | VREFH0 | Input | Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to VCC when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002. |
| | VREFL0 | Input | Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002 |
| | VREFH | Input | Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to VCC when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter. |
| | VREFL | Input | Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to VSS when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter. |

**Table 1.16 Pin functions (4 of 4)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| ADC12 | AN000 to AN003, AN005 to AN007, AN016 to AN018, AN020 | Input | Input pins for the analog signals to be processed by the ADC12. AN005 & AN105 and AN006 & AN106 are assigned to same port pin |
| | AN100 to AN102, AN105 to AN107, AN116, AN117 | Input | |
| | ADTRG0 | Input | Input pins for the external trigger signals that start the A/D conversion |
| | ADTRG1 | Input | |
| | PGAVSS000, PGAVSS100 | Input | Differential input pins |
| DAC12 | DA0, DA1 | Output | Output pins for the analog signals processed by the D/A converter |
| ACMPHS | VCOUT | Output | Comparator output pin |
| | IVREF0 to IVREF3 | Input | Reference voltage input pins for comparator |
| | IVCMP0 to IVCMP3 | Input | Analog voltage input pins for comparator |
| CTSU | TS01 to TS12 | Input | Capacitive touch detection pins (touch pins) |
| | TSCAP | - | Secondary power supply pin for the touch driver |
| I/O ports | P000 to P007 | Input | General-purpose input pins |
| | P008, P014, P015 | I/O | General-purpose input/output pins |
| | P100 to P115 | I/O | General-purpose input/output pins |
| | P200 | Input | General-purpose input pin |
| | P201, P205 to P214 | I/O | General-purpose input/output pins |
| | P300 to P307 | I/O | General-purpose input/output pins |
| | P400 to P415 | I/O | General-purpose input/output pins |
| | P500 to P504, P508 | I/O | General-purpose input/output pins |
| | P600 to P602, P608 to P610 | I/O | General-purpose input/output pins |
| | P708 | I/O | General-purpose input/output pin |

## 1.6 Pin Assignments

Figure 1.3 to Figure 1.6 show the pin assignments.

R7FA6M1AD2CLJ

| | A | B | C | D | E | F | G | H | J | K | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 10 | P407 | P409 | P412 | VCC | P212/ EXTAL | XCOUT | VCL0 | P403 | P400 | P000 | 10 |
| 9 | USB_DM | USB_DP | P411 | VSS | P213/ XTAL | XCIN | VBATT | P405 | P401 | P001 | 9 |
| 8 | VCC_ USB | VSS_ USB | P207 | P413 | P415 | P708 | P404 | P003 | P004 | P002 | 8 |
| 7 | P205 | P214 | P206 | P408 | P414 | P406 | P006 | P007 | P008 | P005 | 7 |
| 6 | P209 | P208 | P210 | P211 | P410 | P402 | P508 | AVSS0 | VREFL0 | VREFH0 | 6 |
| 5 | P200 | P201/MD | P307 | RES | P113 | P600 | P504 | AVCC0 | VREFL | VREFH | 5 |
| 4 | VCC | P304 | P305 | P306 | P115 | P601 | P503 | P100 | P015 | P014 | 4 |
| 3 | VSS | P303 | P110/TDI | P111 | P609 | P602 | P107 | P103 | VSS | VCC | 3 |
| 2 | P300/ TCK/ SWCLK | P302 | P301 | P114 | P610 | VSS | P106 | P101 | P501 | P502 | 2 |
| 1 | P108/ TMS/ SWDIO | P109/ TDO | P112 | P608 | VCC | VCL | P105 | P104 | P102 | P500 | 1 |
| | A | B | C | D | E | F | G | H | J | K | |

**Figure 1.3 Pin assignment for 100-pin LGA (top view)**

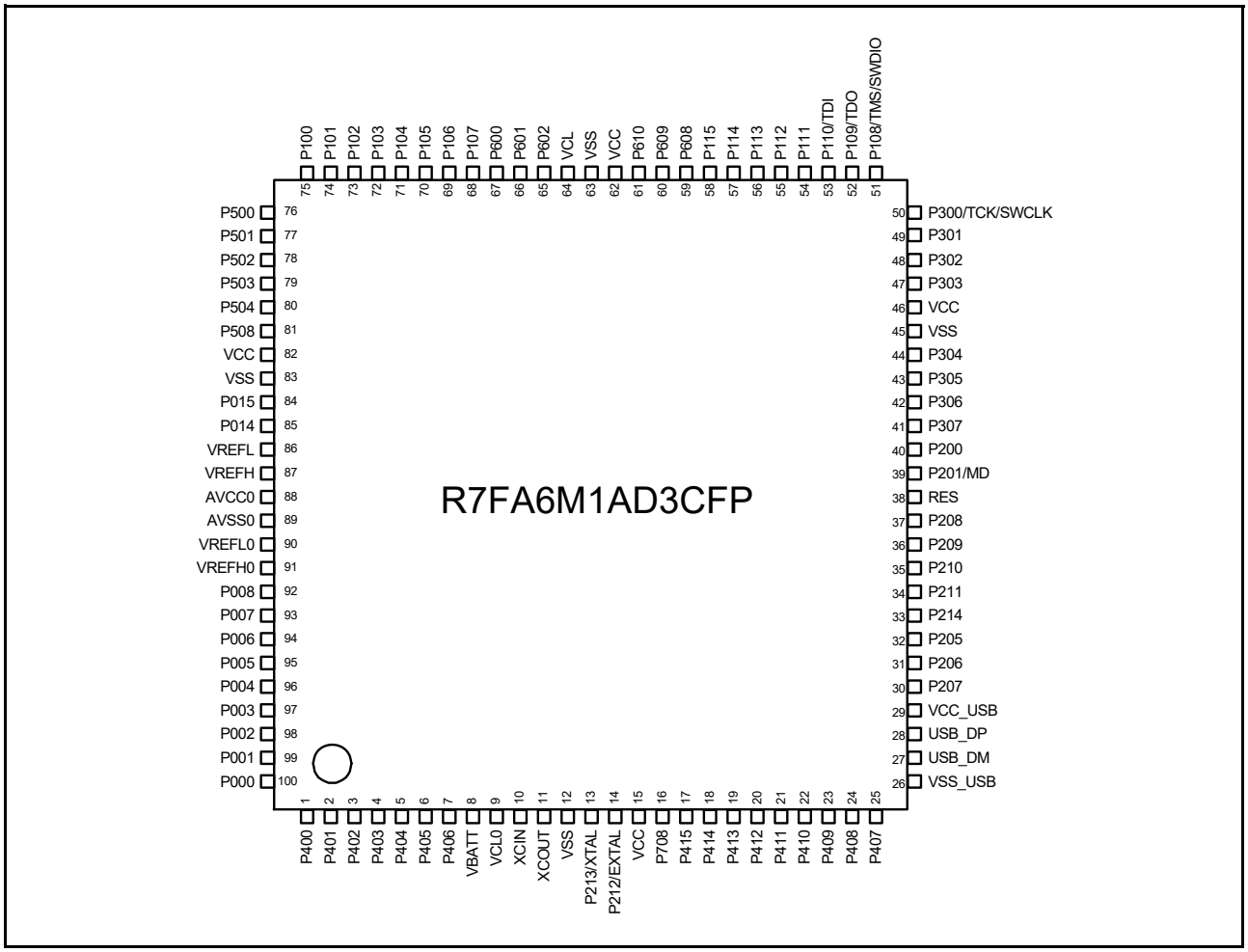



**Figure 1.4 Pin assignment for 100-pin LQFP (top view)**

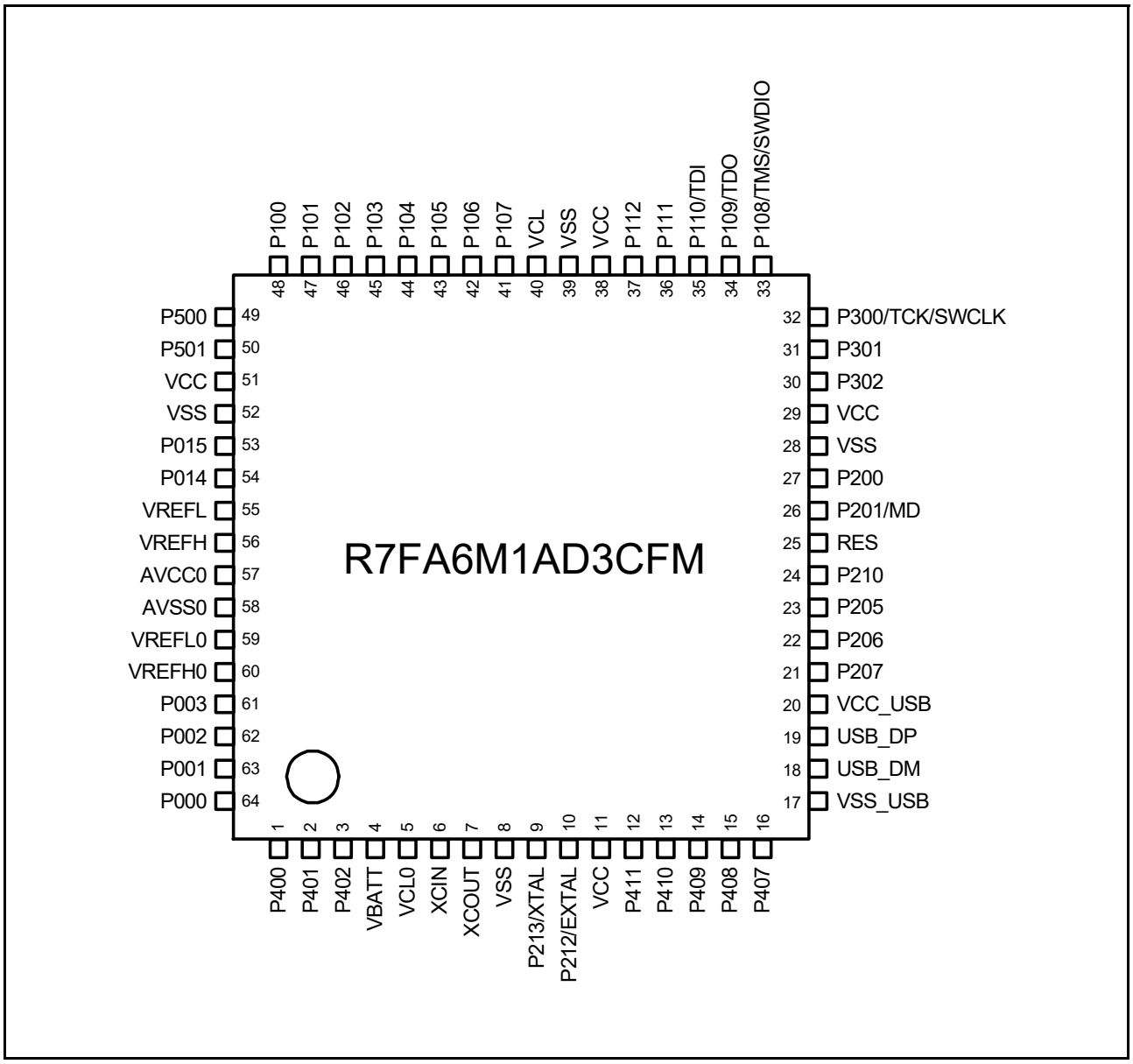
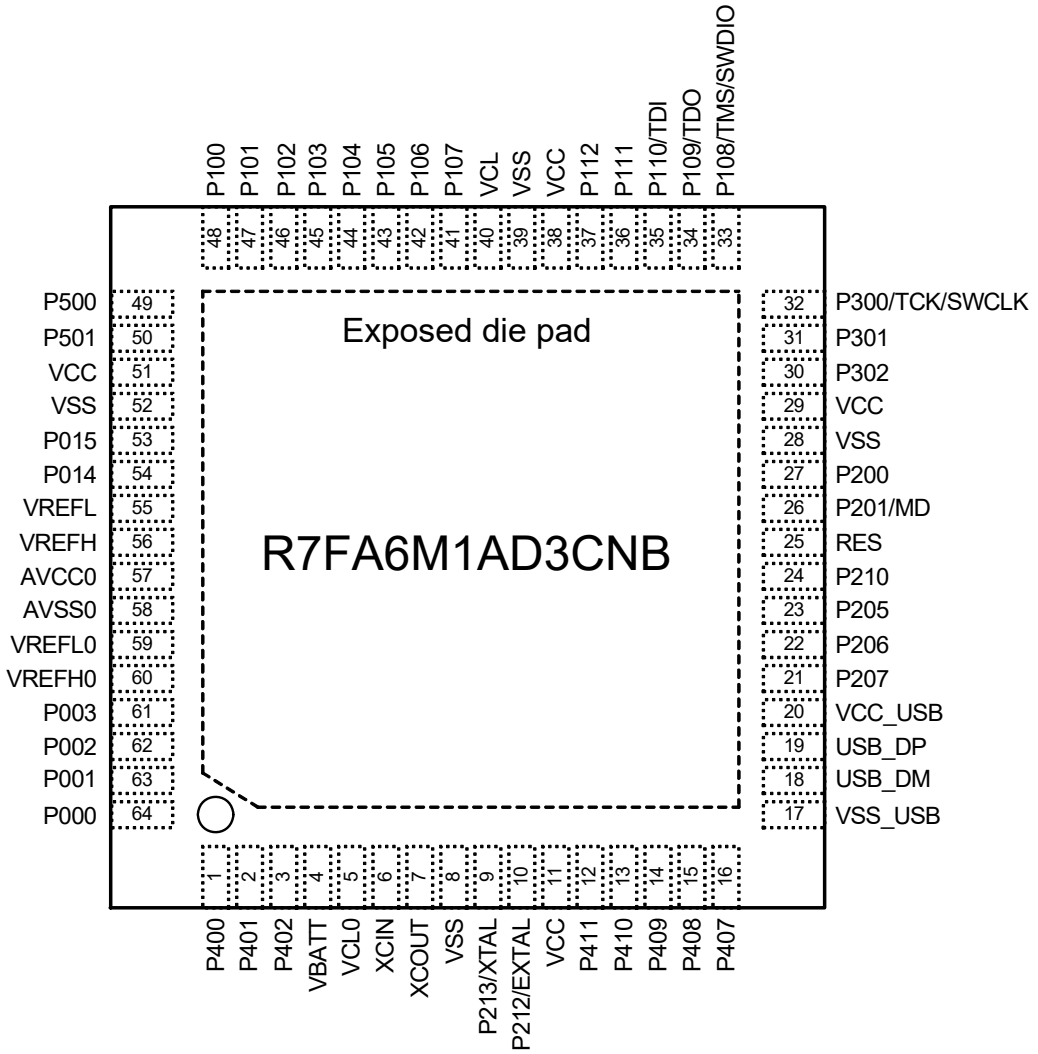



**Figure 1.5 Pin assignment for 64-pin LQFP (top view)**




Note: Exposed die pad is recommended to connect to VSS.

**Figure 1.6 Pin assignment for 64-pin QFN (top view)**

## 1.7 Pin Lists

| Pin number | | | | Power, System, Clock, Debug, CAC | Interrupt | I/O port | External bus | Timers | | | | Communication interfaces | | | | | | | Analog | | HMI |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LGA100 | LQFP100 | LQFP64 | QFN64 | | | | | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,8 (30 MHz) | SCI1,3,9 (30 MHz) | IIC | SPI, QSPI | SSIE | SDHI | ADC12 | DAC12, ACMPHS | CTSU |
| J10 | 1 | 1 | 1 | - | IRQ0 | P400 | - | AGTIO1 | - | GTIOC6A | - | - | SCK4 | - | SCL0_A | - | AUDIO_CLK | - | ADTRG1 | - | - |
| J9 | 2 | 2 | 2 | - | IRQ5-DS | P401 | - | - | GTETRGA | GTIOC6B | - | CTX0 | CTS4_RTS4/SS4 | - | SDA0_A | - | - | - | - | - | - |
| F6 | 3 | 3 | 3 | CACREF | IRQ4-DS | P402 | - | AGTIO0/AGTIO1 | - | - | RTCIC0 | CRX0 | - | - | - | - | AUDIO_CLK | - | - | - | - |
| H10 | 4 | - | - | - | - | P403 | - | AGTIO0/AGTIO1 | - | GTIOC3A | RTCIC1 | - | - | - | - | - | SSIBCK0_A | - | - | - | - |
| G8 | 5 | - | - | - | - | P404 | - | - | - | GTIOC3B | RTCIC2 | - | - | - | - | - | SSILRCK0/SSIFS0_A | - | - | - | - |
| H9 | 6 | - | - | - | - | P405 | - | - | - | GTIOC1A | - | - | - | - | - | - | SSITXD0_A | - | - | - | - |
| F7 | 7 | - | - | - | - | P406 | - | - | - | GTIOC1B | - | - | - | - | - | - | SSIRXD0_A | - | - | - | - |
| G9 | 8 | 4 | 4 | VBATT | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| G10 | 9 | 5 | 5 | VCL0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| F9 | 10 | 6 | 6 | XCIN | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| F10 | 11 | 7 | 7 | XCOUT | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| D9 | 12 | 8 | 8 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| E9 | 13 | 9 | 9 | XTAL | IRQ2 | P213 | - | - | GTETRGC | GTIOC0A | - | - | - | TXD1/MOSI1/SDA1 | - | - | - | - | ADTRG1 | - | - |
| E10 | 14 | 10 | 10 | EXTAL | IRQ3 | P212 | - | AGTEE1 | GTETRGD | GTIOC0B | - | - | - | RXD1/MISO1/SCL1 | - | - | - | - | - | - | - |
| D10 | 15 | 11 | 11 | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| F8 | 16 | - | - | CACREF | IRQ11 | P708 | - | - | - | - | - | - | - | RXD1/MISO1/SCL1 | - | SSLA3_B | AUDIO_CLK | - | - | - | TS12 |
| E8 | 17 | - | - | - | IRQ8 | P415 | - | - | - | GTIOC0A | - | USB_VBUSEN | - | - | - | SSLA2_B | - | SD0CD | - | - | TS11 |
| E7 | 18 | - | - | - | IRQ9 | P414 | - | - | - | GTIOC0B | - | - | - | - | - | SSLA1_B | - | SD0WP | - | - | TS10 |
| D8 | 19 | - | - | - | - | P413 | - | - | GTOUUP | - | - | - | CTS0_RTS0/SS0 | - | - | SSLA0_B | - | SD0CLK_A | - | - | TS09 |
| C10 | 20 | - | - | - | - | P412 | - | AGTEE1 | GTOULO | - | - | - | SCK0 | - | - | RSPCKA_B | - | SD0CMD_A | - | - | TS08 |
| C9 | 21 | 12 | 12 | - | IRQ4 | P411 | - | AGTOA1 | GTOVUP | GTIOC9A | - | - | TXD0/MOSI0/SDA0 | CTS3_RTS3/SS3 | - | MOSIA_B | - | SD0DAT0_A | - | - | TS07 |
| E6 | 22 | 13 | 13 | - | IRQ5 | P410 | - | AGTOB1 | GTOVLO | GTIOC9B | - | - | RXD0/MISO0/SCL0 | SCK3 | - | MISOA_B | - | SD0DAT1_A | - | - | TS06 |
| B10 | 23 | 14 | 14 | - | IRQ6 | P409 | - | - | GTOWUP | GTIOC10A | - | USB_EXICEN | - | TXD3/MOSI3/SDA3 | - | - | - | - | - | - | TS05 |
| D7 | 24 | 15 | 15 | - | IRQ7 | P408 | - | - | GTOWLO | GTIOC10B | - | USB_ID | - | RXD3/MISO3/SCL3 | SCL0_B | - | - | - | - | - | TS04 |
| A10 | 25 | 16 | 16 | - | - | P407 | - | AGTIO0 | - | - | RTCOUT | USB_VBUS | CTS4_RTS4/SS4 | - | SDA0_B | - | - | - | ADTRG0 | - | TS03 |
| B8 | 26 | 17 | 17 | VSS_USB | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| A9 | 27 | 18 | 18 | - | - | - | - | - | - | - | - | USB_DM | - | - | - | - | - | - | - | - | - |
| B9 | 28 | 19 | 19 | - | - | - | - | - | - | - | - | USB_DP | - | - | - | - | - | - | - | - | - |
| A8 | 29 | 20 | 20 | VCC_USB | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| C8 | 30 | 21 | 21 | - | - | P207 | - | - | - | - | - | - | - | - | - | QSSL | - | - | - | - | TS02 |
| C7 | 31 | 22 | 22 | - | IRQ0-DS | P206 | WAIT | - | GTIU | - | - | USB_VBUSEN | RXD4/MISO4/SCL4 | - | SDA1_A | - | - | SD0DAT2_A | - | - | TS01 |
| A7 | 32 | 23 | 23 | CLKOUT | IRQ1-DS | P205 | - | AGTO1 | GTIV | GTIOC4A | - | USB_OVRCURA-DS | TXD4/MOSI4/SDA4 | CTS9_RTS9/SS9 | SCL1_A | - | - | SD0DAT3_A | - | - | TSCAP |
| B7 | 33 | - | - | TCLK | - | P214 | - | - | GTIU | - | - | - | - | - | - | QSPCLK | - | SD0CLK_B | - | - | - |
| D6 | 34 | - | - | TDATA0 | - | P211 | CS7 | - | GTIV | - | - | - | - | - | - | QIO0 | - | SD0CMD_B | - | - | - |
| C6 | 35 | 24 | 24 | TDATA1 | - | P210 | CS6 | - | GTIW | - | - | - | - | - | - | QIO1 | - | SD0CD | - | - | - |
| A6 | 36 | - | - | TDATA2 | - | P209 | CS5 | - | GTOVUP | - | - | - | - | - | - | QIO2 | - | SD0WP | - | - | - |
| B6 | 37 | - | - | TDATA3 | - | P208 | CS4 | - | GTOVLO | - | - | - | - | - | - | QIO3 | - | SD0DAT0_B | - | - | - |
| D5 | 38 | 25 | 25 | RES | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| B5 | 39 | 26 | 26 | MD | - | P201 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| A5 | 40 | 27 | 27 | - | NMI | P200 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| C5 | 41 | - | - | - | - | P307 | A12 | - | GTOUUP | - | - | - | - | - | - | QIO0 | - | - | - | - | - |
| D4 | 42 | - | - | - | - | P306 | A11 | - | GTOULO | - | - | - | - | - | - | QSSL | - | - | - | - | - |
| C4 | 43 | - | - | - | IRQ8 | P305 | A10 | - | GTOWUP | - | - | - | - | - | - | QSPCLK | - | - | - | - | - |
| B4 | 44 | - | - | - | IRQ9 | P304 | A09 | - | GTOWLO | GTIOC7A | - | - | - | - | - | - | - | - | - | - | - |
| A3 | 45 | 28 | 28 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| A4 | 46 | 29 | 29 | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| B3 | 47 | - | - | - | - | P303 | A08 | - | - | GTIOC7B | - | - | - | - | - | - | - | - | - | - | - |
| B2 | 48 | 30 | 30 | - | IRQ5 | P302 | A07 | - | GTOUUP | GTIOC4A | - | - | TXD2/MOSI2/SDA2 | - | - | SSLB3_B | - | - | - | - | - |
| C2 | 49 | 31 | 31 | - | IRQ6 | P301 | A06 | AGTIO0 | GTOULO | GTIOC4B | - | - | RXD2/MISO2/SCL2 | CTS9_RTS9/SS9 | - | SSLB2_B | - | - | - | - | - |
| A2 | 50 | 32 | 32 | TCK/SWCLK | - | P300 | - | - | GTOUUP | GTIOC0A_A | - | - | - | - | - | SSLB1_B | - | - | - | - | - |
| A1 | 51 | 33 | 33 | TMS/SWDIO | - | P108 | - | - | GTOULO | GTIOC0B_A | - | - | - | CTS9_RTS9/SS9 | - | SSLB0_B | - | - | - | - | - |

| Pin number | | | | | | | | Timers | | | | Communication interfaces | | | | | | | Analog | | HMI |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LGA100 | LQFP100 | LQFP64 | QFN64 | Power, System, Clock, Debug, CAC | Interrupt | I/O port | External bus | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,8 (30 MHz) | SCI1,3,9 (30 MHz) | IIC | SPI, QSPI | SSIE | SDHI | ADC12 | DAC12, ACMPHS | CTSU |
| B1 | 52 | 34 | 34 | CLKOUT/TDO/SWO | - | P109 | - | - | GTOVUP | GTIOC1A_A | - | CTX1 | - | TXD9/MOSI9/SDA9 | - | MOSIB_B | - | - | - | - | - |
| C3 | 53 | 35 | 35 | TDI | IRQ3 | P110 | - | - | GTOVLO | GTIOC1B_A | - | CRX1 | CTS2_RTS2/SS2 | RXD9/MISO9/SCL9 | - | MISOB_B | - | - | - | VCOUT | - |
| D3 | 54 | 36 | 36 | - | IRQ4 | P111 | A05 | - | - | GTIOC3A_A | - | - | SCK2 | SCK9 | - | RSPCKB_B | - | - | - | - | - |
| C1 | 55 | 37 | 37 | - | - | P112 | A04 | - | - | GTIOC3B_A | - | - | TXD2/MOSI2/SDA2 | SCK1 | - | SSLB0_B | SSIBCK0_B | - | - | - | - |
| E5 | 56 | - | - | - | - | P113 | A03 | - | - | GTIOC2A | - | - | RXD2/MISO2/SCL2 | - | - | - | SSILRCK0/SSIFS0_B | - | - | - | - |
| D2 | 57 | - | - | - | - | P114 | A02 | - | - | GTIOC2B | - | - | - | - | - | - | SSIRXD0_B | - | - | - | - |
| E4 | 58 | - | - | - | - | P115 | A01 | - | - | GTIOC4A | - | - | - | - | - | - | SSITXD0_B | - | - | - | - |
| D1 | 59 | - | - | - | - | P608 | A00 | - | - | GTIOC4B | - | - | - | - | - | - | - | - | - | - | - |
| E3 | 60 | - | - | - | - | P609 | CS1 | - | - | GTIOC5A | - | CTX1 | - | - | - | - | - | - | - | - | - |
| E2 | 61 | - | - | - | - | P610 | CS0 | - | - | GTIOC5B | - | CRX1 | - | - | - | - | - | - | - | - | - |
| E1 | 62 | 38 | 38 | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| F2 | 63 | 39 | 39 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| F1 | 64 | 40 | 40 | VCL | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| F3 | 65 | - | - | - | - | P602 | EBCLK | - | - | GTIOC7B | - | - | - | TXD9 | - | - | - | - | - | - | - |
| F4 | 66 | - | - | - | - | P601 | WR0 | - | - | GTIOC6A | - | - | - | RXD9 | - | - | - | - | - | - | - |
| F5 | 67 | - | - | CLKOUT/CACREF | - | P600 | RD | - | - | GTIOC6B | - | - | - | SCK9 | - | - | - | - | - | - | - |
| G3 | 68 | 41 | 41 | - | KR07 | P107 | D07[A07/D07] | AGTOA0 | - | GTIOC8A | - | - | CTS8_RTS8/SS8 | - | - | QIO3 | - | - | - | - | - |
| G2 | 69 | 42 | 42 | - | KR06 | P106 | D06[A06/D06] | AGTOB0 | - | GTIOC8B | - | - | SCK8 | - | - | SSLA3_A/QIO2 | - | - | - | - | - |
| G1 | 70 | 43 | 43 | - | IRQ0/KR05 | P105 | D05[A05/D05] | - | GTETRGA | GTIOC1A | - | - | TXD8/MOSI8/SDA8 | - | - | SSLA2_A/QIO1 | - | - | - | - | - |
| H1 | 71 | 44 | 44 | - | IRQ1/KR04 | P104 | D04[A04/D04] | - | GTETRGB | GTIOC1B | - | - | RXD8/MISO8/SCL8 | - | - | SSLA1_A/QIO0 | - | - | - | - | - |
| H3 | 72 | 45 | 45 | - | KR03 | P103 | D03[A03/D03] | - | GTOWUP | GTIOC2A_A | - | CTX0 | CTS0_RTS0/SS0 | - | - | SSLA0_A | - | - | - | - | - |
| J1 | 73 | 46 | 46 | - | KR02 | P102 | D02[A02/D02] | AGTO0 | GTOWLO | GTIOC2B_A | - | CRX0 | SCK0 | - | - | RSPCKA_A | - | - | ADTRG0 | - | - |
| H2 | 74 | 47 | 47 | - | IRQ1/KR01 | P101 | D01[A01/D01] | AGTEE0 | GTETRGB | GTIOC5A | - | - | TXD0/MOSI0/SDA0 | CTS1_RTS1/SS1 | SDA1_B | MOSIA_A | - | - | - | - | - |
| H4 | 75 | 48 | 48 | - | IRQ2/KR00 | P100 | D00[A00/D00] | AGTIO0 | GTETRGA | GTIOC5B | - | - | RXD0/MISO0/SCL0 | SCK1 | SCL1_B | MISOA_A | - | - | - | - | - |
| K1 | 76 | 49 | 49 | - | - | P500 | - | AGTOA0 | GTIU | GTIOC11A | - | USB_VBUSEN | - | - | - | QSPCLK | - | SD1CLK_A | AN016 | IVREF0 | - |
| J2 | 77 | 50 | 50 | - | IRQ11 | P501 | - | AGTOB0 | GTIV | GTIOC11B | - | USB_OVRCURA | - | - | - | QSSL | - | SD1CMD_A | AN116 | IVREF1 | - |
| K2 | 78 | - | - | - | IRQ12 | P502 | - | - | GTIW | GTIOC12A | - | USB_OVRCURB | - | - | - | QIO0 | - | SD1DAT0_A | AN017 | IVCMP0 | - |
| G4 | 79 | - | - | - | - | P503 | - | - | GTETRGC | GTIOC12B | - | USB_EXICEN | - | - | - | QIO1 | - | SD1DAT1_A | AN117 | - | - |
| G5 | 80 | - | - | - | - | P504 | ALE | - | GTETRGD | - | - | USB_ID | - | - | - | QIO2 | - | SD1DAT2_A | AN018 | - | - |
| G6 | 81 | - | - | - | - | P508 | - | - | - | - | - | - | - | - | - | - | - | SD1DAT3_A | AN020 | - | - |
| K3 | 82 | 51 | 51 | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| J3 | 83 | 52 | 52 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| J4 | 84 | 53 | 53 | - | IRQ13 | P015 | - | - | - | - | - | - | - | - | - | - | - | - | AN006/AN106 | DA1/IVCMP1 | - |
| K4 | 85 | 54 | 54 | - | - | P014 | - | - | - | - | - | - | - | - | - | - | - | - | AN005/AN105 | DA0/IVREF3 | - |
| J5 | 86 | 55 | 55 | VREFL | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| K5 | 87 | 56 | 56 | VREFH | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| H5 | 88 | 57 | 57 | AVCC0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| H6 | 89 | 58 | 58 | AVSS0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| J6 | 90 | 59 | 59 | VREFL0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| K6 | 91 | 60 | 60 | VREFH0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| J7 | 92 | - | - | - | IRQ12-DS | P008 | - | - | - | - | - | - | - | - | - | - | - | - | AN003 | - | - |
| H7 | 93 | - | - | - | - | P007 | - | - | - | - | - | - | - | - | - | - | - | - | PGAVSS100/AN107 | - | - |
| G7 | 94 | - | - | - | IRQ11-DS | P006 | - | - | - | - | - | - | - | - | - | - | - | - | AN102 | IVCMP2 | - |
| K7 | 95 | - | - | - | IRQ10-DS | P005 | - | - | - | - | - | - | - | - | - | - | - | - | AN101 | IVCMP2 | - |
| J8 | 96 | - | - | - | IRQ9-DS | P004 | - | - | - | - | - | - | - | - | - | - | - | - | AN100 | IVCMP2 | - |
| H8 | 97 | 61 | 61 | - | - | P003 | - | - | - | - | - | - | - | - | - | - | - | - | PGAVSS000/AN007 | - | - |
| K8 | 98 | 62 | 62 | - | IRQ8-DS | P002 | - | - | - | - | - | - | - | - | - | - | - | - | AN002 | IVCMP2 | - |

| Pin number | | | | Power, System, Clock, Debug, CAC | Interrupt | I/O port | External bus | Timers | | | | Communication interfaces | | | | | | | Analog | | HMI |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LGA100 | LQFP100 | LQFP64 | QFN64 | | | | | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,8 (30 MHz) | SCI1,3,9 (30 MHz) | IIC | SPI, QSPI | SSIE | SDHI | ADC12 | DAC12, ACMPHS | CTSU |
| K9 | 99 | 63 | 63 | - | IRQ7-DS | P001 | - | - | - | - | - | - | - | - | - | - | - | - | AN001 | IVCMP2 | - |
| K10 | 100 | 64 | 64 | - | IRQ6-DS | P000 | - | - | - | - | - | - | - | - | - | - | - | - | AN000 | IVCMP2 | - |

Note: Some pin names have the added suffix of _A and _B. When assigning the GPT, IIC, SPI, SSIE, and SDHI functionality, select the functional pins with the same suffix.

# 2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = VSS_USB = 0 V
- $T_a = T_{opr}$.

Figure 2.1 shows the timing conditions.

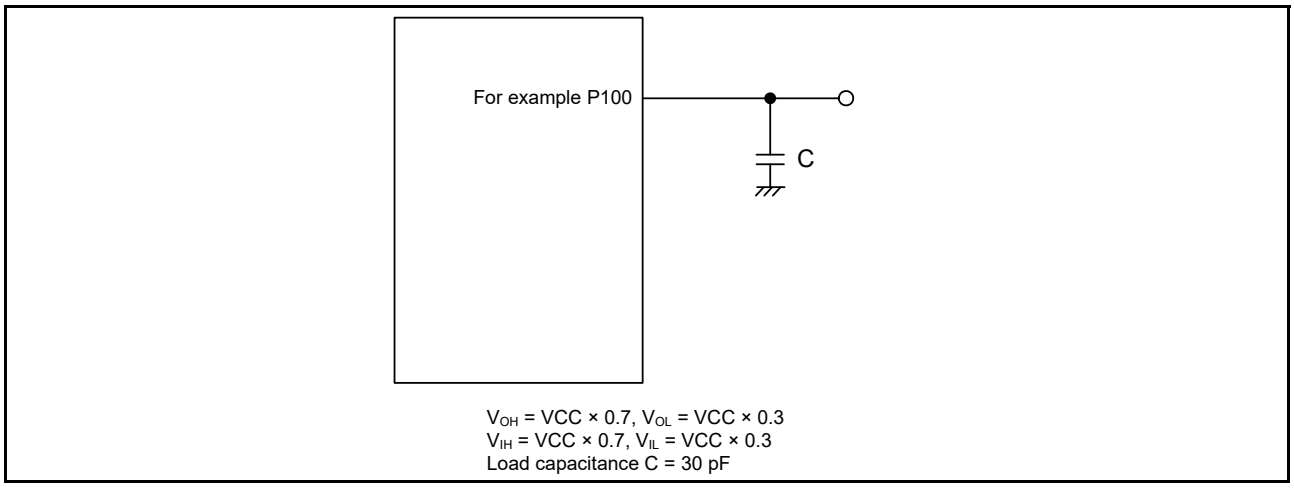



**Figure 2.1 Input or output timing measurement conditions**

The measurement conditions for the timing specification of each peripheral are recommended for the best peripheral operation. However, make sure to adjust the driving abilities of each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the A/C specification of each function is not guaranteed.

## 2.1 Absolute Maximum Ratings

**Table 2.1 Absolute maximum ratings**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage | VCC, VCC_USB *2 | -0.3 to +4.0 | V |
| VBATT power supply voltage | VBATT | -0.3 to +4.0 | V |
| Input voltage (except for 5 V-tolerant ports*1) | $V_{in}$ | -0.3 to VCC + 0.3 | V |
| Input voltage (5 V-tolerant ports*1) | $V_{in}$ | -0.3 to + VCC + 4.0 (max. 5.8) | V |
| Reference power supply voltage | VREFH/VREFH0 | -0.3 to AVCC0 + 0.3 | V |
| Analog power supply voltage | AVCC0 *2 | -0.3 to +4.0 | V |
| Analog input voltage (except for P000 to P007) | $V_{AN}$ | -0.3 to AVCC0 + 0.3 | V |
| Analog input voltage (P000 to P007) when PGA differential input is disabled | $V_{AN}$ | -0.3 to AVCC0 + 0.3 | V |
| Analog input voltage (P000 to P002, P004 to P006) when PGA differential input is enabled | $V_{AN}$ | -1.3 to AVCC0 + 0.3 | V |
| Analog input voltage (P003, P007) when PGA differential input is enabled | $V_{AN}$ | -0.8 to AVCC0 + 0.3 | V |
| Operating temperature*3, *4, *5 | $T_{opr}$ | -40 to +85<br>-40 to +105 | °C |
| Storage temperature | $T_{stg}$ | -55 to +125 | °C |

**Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.**

Note 1. Ports P205, P206, P400, P401, P407 to P415, and P708 are 5 V tolerant.
Note 2. Connect AVCC0 and VCC_USB to VCC.
Note 3. See section 2.2.1, $T_j/T_a$ Definition.
Note 4. Contact Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.
Note 5. The upper limit of operating temperature is +85°C or +105°C, depending on the product. For details, see section 1.3, Part Numbering.

**Table 2.2 Recommended operating conditions**

| Parameter | Symbol | Value | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power supply voltages | VCC | When USB is not used | 2.7 | - | 3.6 | V |
| | | When USB is used | 3.0 | - | 3.6 | V |
| | VSS | | - | 0 | - | V |
| USB power supply voltages | VCC_USB | | - | VCC | - | V |
| | VSS_USB | | - | 0 | - | V |
| VBATT power supply voltage | VBATT | | 1.65*2 | - | 3.6 | V |
| Analog power supply voltages | AVCC0*1 | | - | VCC | - | V |
| | AVSS0 | | - | 0 | - | V |

Note 1. Connect AVCC0 to VCC. When the A/D converter, the D/A converter, or the comparator are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.
Note 2. Low CL crystal cannot be used below VBATT = 1.8V.

## 2.2 DC Characteristics

### 2.2.1 $T_j/T_a$ Definition

**Table 2.3 DC characteristics**
Conditions: Products with operating temperature ($T_a$) -40 to +105°C.

| Parameter | | Symbol | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Permissible junction temperature | 100-pin LQFP<br>64-pin LQFP | $T_j$ | - | 125 | °C | High-speed mode<br>Low-speed mode<br>Subosc-speed mode. |
| | 64-pin QFN | | | 117 | | |
| | 100-pin LGA | | | 105 | | |

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W),
where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.
The upper limit of operating temperature is +85°C or +105°C, depending on the product. For details, see section 1.3, Part Numbering.

### 2.2.2 I/O $V_{IH}$, $V_{IL}$

**Table 2.4 I/O $V_{IH}$, $V_{IL}$**

| Parameter | | | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Input voltage (except for Schmitt trigger input pins) | Peripheral function pin | EXTAL(external clock input), WAIT, SPI (except RSPCK) | | | $V_{IH}$ | VCC × 0.8 | - | - | V |
| | | | | | $V_{IL}$ | - | - | VCC × 0.2 | |
| | | D00 to D07 | | | $V_{IH}$ | VCC × 0.7 | - | - | |
| | | | | | $V_{IL}$ | - | - | VCC × 0.3 | |
| | | IIC (SMBus)*1 | | | $V_{IH}$ | 2.1 | - | - | |
| | | | | | $V_{IL}$ | - | - | 0.8 | |
| | | IIC (SMBus)*2 | | | $V_{IH}$ | 2.1 | - | VCC + 3.6 (max 5.8) | |
| | | | | | $V_{IL}$ | - | - | 0.8 | |
| Schmitt trigger input voltage | Peripheral function pin | IIC (except for SMBus)*1 | | | $V_{IH}$ | VCC × 0.7 | - | - | V |
| | | | | | $V_{IL}$ | - | - | VCC × 0.3 | |
| | | | | | $\Delta V_T$ | VCC × 0.05 | - | - | |
| | | IIC (except for SMBus)*2 | | | $V_{IH}$ | VCC × 0.7 | - | VCC + 3.6 (max 5.8) | V |
| | | | | | $V_{IL}$ | - | - | VCC × 0.3 | |
| | | | | | $\Delta V_T$ | VCC × 0.05 | - | - | |
| | | 5 V-tolerant ports*3, *7 | | | $V_{IH}$ | VCC × 0.8 | - | VCC + 3.6 (max 5.8) | |
| | | | | | $V_{IL}$ | - | - | VCC × 0.2 | |
| | | | | | $\Delta V_T$ | VCC × 0.05 | - | - | |
| | | RTCIC0, RTCIC1, RTCIC2 | When using the battery backup function | When VBATT power supply is selected | $V_{IH}$ | VBATT × 0.8 | - | VBATT + 0.3 | |
| | | | | | $V_{IL}$ | - | - | VBATT × 0.2 | |
| | | | | | $\Delta V_T$ | VBATT × 0.05 | - | - | |
| | | | | When VCC power supply is selected | $V_{IH}$ | VCC × 0.8 | - | Higher voltage either VCC + 0.3 V or VBATT + 0.3 V | |
| | | | | | $V_{IL}$ | - | - | VCC × 0.2 | |
| | | | | | $\Delta V_T$ | VCC × 0.05 | - | - | |
| | | | When not using the battery backup function | | $V_{IH}$ | VCC × 0.8 | - | VCC + 0.3 | |
| | | | | | $V_{IL}$ | - | - | VCC × 0.2 | |
| | | | | | $\Delta V_T$ | VCC × 0.05 | - | - | |
| | | Other input pins*4 | | | $V_{IH}$ | VCC × 0.8 | - | - | |
| | | | | | $V_{IL}$ | - | - | VCC × 0.2 | |
| | | | | | $\Delta V_T$ | VCC × 0.05 | - | - | |
| | Ports | 5 V-tolerant ports*5, *7 | | | $V_{IH}$ | VCC × 0.8 | - | VCC + 3.6 (max 5.8) | V |
| | | | | | $V_{IL}$ | - | - | VCC × 0.2 | |
| | | Other input pins*6 | | | $V_{IH}$ | VCC × 0.8 | - | - | |
| | | | | | $V_{IL}$ | - | - | VCC × 0.2 | |

Note 1. SCL1_B, SDA1_B (total 2 pins).
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SCL1_A, SDA1_A (total 6 pins).

Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P708 (total 15 pins).
Note 4. All input pins except for the peripheral function pins already described in the table.
Note 5. P205, P206, P400, P401, P407 to P415, P708 (total 14 pins).
Note 6. All input pins except for the ports already described in the table.
Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the breakdown voltage.

### 2.2.3 I/O $I_{OH}$, $I_{OL}$

**Table 2.5 I/O $I_{OH}$, $I_{OL}$**

| Parameter | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Permissible output current (average value per pin) | Ports P008, P201 | - | $I_{OH}$ | - | - | -2.0 | mA |
| | | | $I_{OL}$ | - | - | 2.0 | mA |
| | Ports P014, P015 | - | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | Ports P205, P206, P407 to P415, P602, P708 (total 13 pins) | Low drive*1 | $I_{OH}$ | - | - | -2.0 | mA |
| | | | $I_{OL}$ | - | - | 2.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | High drive*3 | $I_{OH}$ | - | - | -20 | mA |
| | | | $I_{OL}$ | - | - | 20 | mA |
| | Other output pins*4 | Low drive*1 | $I_{OH}$ | - | - | -2.0 | mA |
| | | | $I_{OL}$ | - | - | 2.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | High drive*3 | $I_{OH}$ | - | - | -16 | mA |
| | | | $I_{OL}$ | - | - | 16 | mA |
| Permissible output current (max value per pin) | Ports P008, P201 | - | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | Ports P014, P015 | - | $I_{OH}$ | - | - | -8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| | Ports P205, P206, P407 to P415, P602, P708 (total 13 pins) | Low drive*1 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | - | - | -8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| | | High drive*3 | $I_{OH}$ | - | - | -40 | mA |
| | | | $I_{OL}$ | - | - | 40 | mA |
| | Other output pins*4 | Low drive*1 | $I_{OH}$ | - | - | -4.0 | mA |
| | | | $I_{OL}$ | - | - | 4.0 | mA |
| | | Middle drive*2 | $I_{OH}$ | - | - | -8.0 | mA |
| | | | $I_{OL}$ | - | - | 8.0 | mA |
| | | High drive*3 | $I_{OH}$ | - | - | -32 | mA |
| | | | $I_{OL}$ | - | - | 32 | mA |
| Permissible output current (max value of total of all pins) | Maximum of all output pins | | $\Sigma I_{OH\ (max)}$ | - | - | -80 | mA |
| | | | $\Sigma I_{OL\ (max)}$ | - | - | 80 | mA |

**Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.**

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected

driving ability is retained in Deep Software Standby mode.
Note 4. Except for P000 to P007, P200, which are input ports.

### 2.2.4 I/O $V_{OH}$, $V_{OL}$, and Other Characteristics

**Table 2.6 I/O $V_{OH}$, $V_{OL}$, and other characteristics**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Output voltage | IIC | | $V_{OL}$ | - | - | 0.4 | V | $I_{OL}$ = 3.0 mA |
| | | | $V_{OL}$ | - | - | 0.6 | | $I_{OL}$ = 6.0 mA |
| | IIC*1 | | $V_{OL}$ | - | - | 0.4 | | $I_{OL}$ = 15.0 mA (ICFER.FMPE = 1) |
| | | | $V_{OL}$ | - | 0.4 | - | | $I_{OL}$ = 20.0 mA (ICFER.FMPE = 1) |
| | Ports P205, P206, P407 to P415, P602, P708 (total of 13 pins)*2 | | $V_{OH}$ | VCC - 1.0 | - | - | | $I_{OH}$ = -20 mA VCC = 3.3 V |
| | | | $V_{OL}$ | - | - | 1.0 | | $I_{OL}$ = 20 mA VCC = 3.3 V |
| | Other output pins | | $V_{OH}$ | VCC - 0.5 | - | - | | $I_{OH}$ = -1.0 mA |
| | | | $V_{OL}$ | - | - | 0.5 | | $I_{OL}$ = 1.0 mA |
| Input leakage current | RES | | $\|I_{in}\|$ | - | - | 5.0 | μA | $V_{in}$ = 0 V $V_{in}$ = 5.5 V |
| | Ports P000 to P002, P004 to P006, P200 | | | - | - | 1.0 | | $V_{in}$ = 0 V $V_{in}$ = VCC |
| | Ports P003, P007 | Before initialization*3 | | - | - | 45.0 | | $V_{in}$ = 0 V $V_{in}$ = VCC |
| | | After initialization*4 | | - | - | 1.0 | | $V_{in}$ = 0 V $V_{in}$ = VCC |
| Three-state leakage current (off state) | 5 V-tolerant ports | | $\|I_{TSI}\|$ | - | - | 5.0 | μA | $V_{in}$ = 0 V $V_{in}$ = 5.5 V |
| | Other ports (except for ports P000 to P007, P200) | | | - | - | 1.0 | | $V_{in}$ = 0 V $V_{in}$ = VCC |
| Input pull-up MOS current | Ports P0 to P7 (except for ports P000 to P007) | | $I_p$ | -300 | - | -10 | μA | VCC = 2.7 to 3.6 V $V_{in}$ = 0 V |
| Input capacitance | USB_DP, USB_DM, and ports P003, P007, P014, P015, P400, P401 | | $C_{in}$ | - | - | 16 | pF | Vbias = 0 V Vamp = 20 mV f = 1 MHz $T_a$ = 25°C |
| | Other input pins | | | - | - | 8 | | |

Note 1. SCL0_A, SDA0_A (total 2 pins).
Note 2. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. P0nPFS.ASEL(n = 3 or 7) = 1
Note 4. P0nPFS.ASEL(n = 3 or 7) = 0

## 2.2.5 Operating and Standby Current

**Table 2.7 Operating and standby current (1 of 2)**

| Parameter | | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | High-speed mode | Maximum*2 | | $I_{CC}$*3 | - | - | 87 | mA | ICLK = 120 MHz<br>PCLKA = 120 MHz<br>PCLKB = 60 MHz<br>PCLKC = 60 MHz<br>PCLKD = 120 MHz<br>FCLK = 60 MHz<br>BCLK = 120 MHz |
| | | CoreMark®*5 | | | - | 17 | - | | |
| | | Normal mode | All peripheral clocks enabled, while (1) code executing from flash*4 | | - | 24 | - | | |
| | | | All peripheral clocks disabled, while (1) code executing from flash*5, *6 | | - | 12 | - | | |
| | | Sleep mode*5, *6 | | | - | 9 | 33.5 | | |
| | | Increase during BGO operation | Data flash P/E | | - | 6 | - | | |
| | | | Code flash P/E | | - | 8 | - | | |
| | Low-speed mode*5 | | | | - | 1.2 | - | | ICLK = 1 MHz |
| | Subosc-speed mode*5 | | | | - | 1.0 | - | | ICLK = 32.768 kHz |
| | Software Standby mode | | | | - | 1.3 | 13 | | Ta ≤ 85°C |
| | | | | | - | 1.3 | 21 | | Ta ≤ 105°C |
| | Deep Software Standby mode | Power supplied to Standby SRAM and USB resume detecting unit | | | - | 28 | 65 | μA | Ta ≤ 85°C |
| | | | | | - | 28 | 93 | | Ta ≤ 105°C |
| | | Power not supplied to SRAM or USB resume detecting unit | Power-on reset circuit low power function disabled | | - | 11.6 | 28 | | Ta ≤ 85°C |
| | | | | | - | 11.6 | 32 | | Ta ≤ 105°C |
| | | | Power-on reset circuit low power function enabled | | - | 4.9 | 21 | | Ta ≤ 85°C |
| | | | | | - | 4.9 | 26 | | Ta ≤ 105°C |
| | | Increase when the RTC and AGT are operating | When the low-speed on-chip oscillator (LOCO) is in use | | - | 4.4 | - | | - |
| | | | When a crystal oscillator for low clock loads is in use | | - | 1.0 | - | | - |
| | | | When a crystal oscillator for standard clock loads is in use | | - | 1.4 | - | | - |
| | RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate) | | When a crystal oscillator for low clock loads is in use | | - | 0.9 | - | | VBATT = 1.8 V, VCC = 0 V |
| | | | | | - | 1.1 | - | | VBATT = 3.3 V, VCC = 0 V |
| | | | When a crystal oscillator for standard clock loads is in use | | - | 1.0 | - | | VBATT = 1.8 V, VCC = 0 V |
| | | | | | - | 1.6 | - | | VBATT = 3.3 V, VCC = 0 V |
| Analog power supply current | During 12-bit A/D conversion | | | $AI_{CC}$ | - | 0.8 | 1.1 | mA | - |
| | During 12-bit A/D conversion with S/H amp | | | | - | 2.3 | 3.3 | mA | - |
| | PGA (1ch) | | | | - | 1 | 3 | mA | - |
| | ACMPHS (1 unit) | | | | - | 100 | 150 | μA | - |
| | Temperature sensor | | | | - | 0.1 | 0.2 | mA | - |
| | During D/A conversion (per unit) | | Without AMP output | | - | 0.1 | 0.2 | mA | - |
| | | | With AMP output | | - | 0.6 | 1.1 | mA | - |
| | Waiting for A/D, D/A conversion (all units) | | | | - | 0.9 | 1.6 | mA | - |
| | ADC12, DAC12 in standby modes (all units)*7 | | | | - | 2 | 8 | μA | - |
| Reference power supply current (VREFH0) | During 12-bit A/D conversion (unit 0) | | | $AI_{REFH0}$ | - | 70 | 120 | μA | - |
| | Waiting for 12-bit A/D conversion (unit 0) | | | | - | 0.07 | 0.5 | μA | - |
| | ADC12 in standby modes (unit 0) | | | | - | 0.07 | 0.5 | μA | - |
| Reference power supply current (VREFH) | During 12-bit A/D conversion (unit 1) | | | $AI_{REFH}$ | - | 70 | 120 | μA | - |
| | During D/A conversion (per unit) | | Without AMP output | | - | 0.1 | 0.4 | mA | - |
| | | | With AMP ouput | | - | 0.1 | 0.4 | mA | - |
| | Waiting for 12-bit A/D (unit 1), D/A (all units) conversion | | | | - | 0.07 | 0.8 | μA | - |
| | ADC12 unit 1 in standby modes | | | | - | 0.07 | 0.8 | μA | - |

**Table 2.7 Operating and standby current (2 of 2)**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| USB operating current | Low speed | USB | $I_{CCUSBLS}$ | - | 3.5 | 6.5 | mA | VCC_USB |
| | Full speed | USB | $I_{CCUSBFS}$ | - | 4.0 | 10.0 | mA | VCC_USB |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOS transistors in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. $I_{CC}$ depends on f (ICLK) as follows. (ICLK:PCLKA:PCLKB:PCLKC:PCLKD:BCK:EBCLK = 2:2:1:1:2:1:1)
$I_{CC}$ Max. = 0.53 x f + 23 (maximum operation in High-speed mode)
$I_{CC}$ Typ. = 0.08 x f + 2.4 (normal operation in High-speed mode)
$I_{CC}$ Typ. = 0.1 x f + 1.1 (Low-speed mode)
$I_{CC}$ Max. = 0.09 x f + 23 (Sleep mode).
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).
Note 7. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-bit A/D Converter 0 Module Stop bit) and MSTPCRD.MSTPD15 (12-bit A/D Converter 1 Module Stop bit) are in the module-stop state.
See section 42.6.8, Available functions and register settings of AN000 to AN002, AN007, AN100 to AN102, and AN107 in User's Manual.

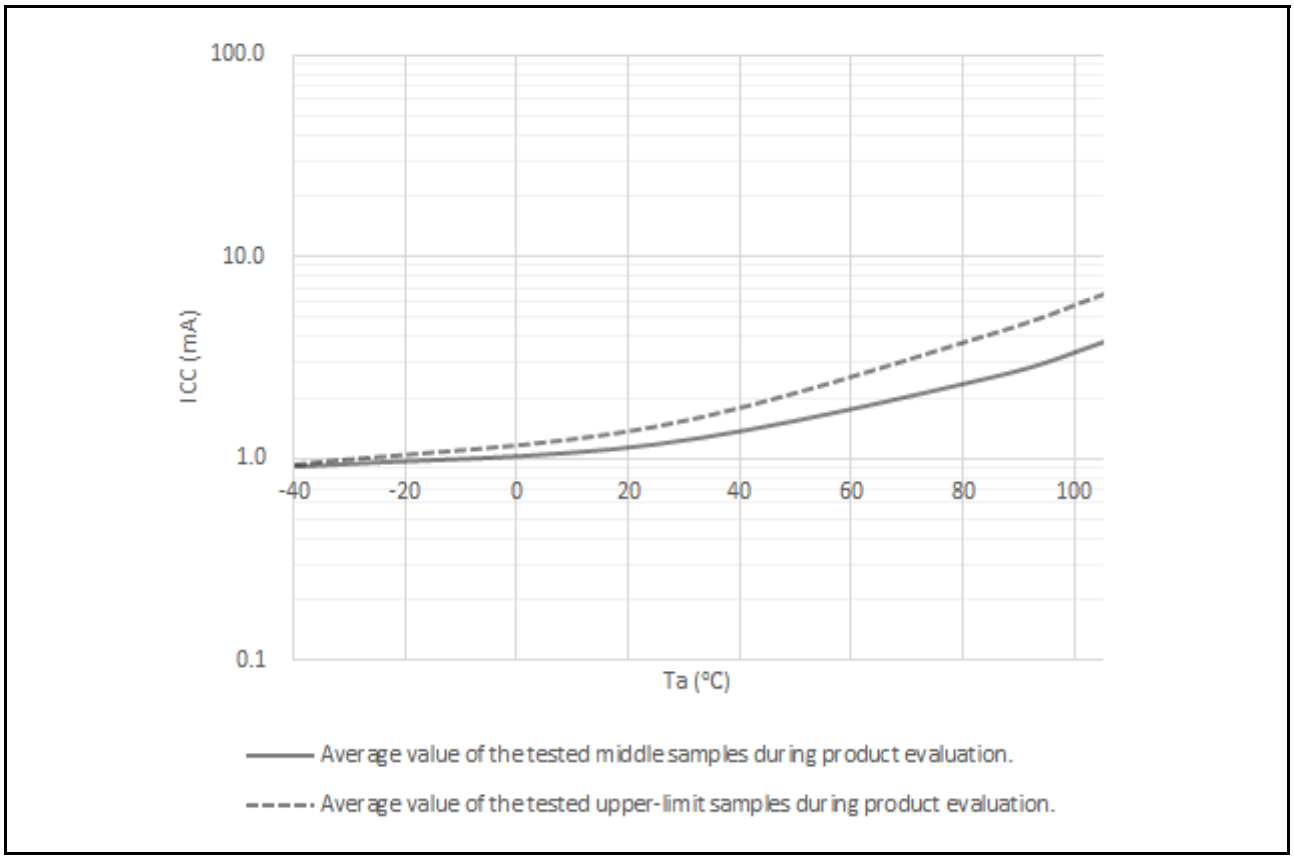



**Figure 2.2 Temperature dependency in Software Standby mode (reference data)**

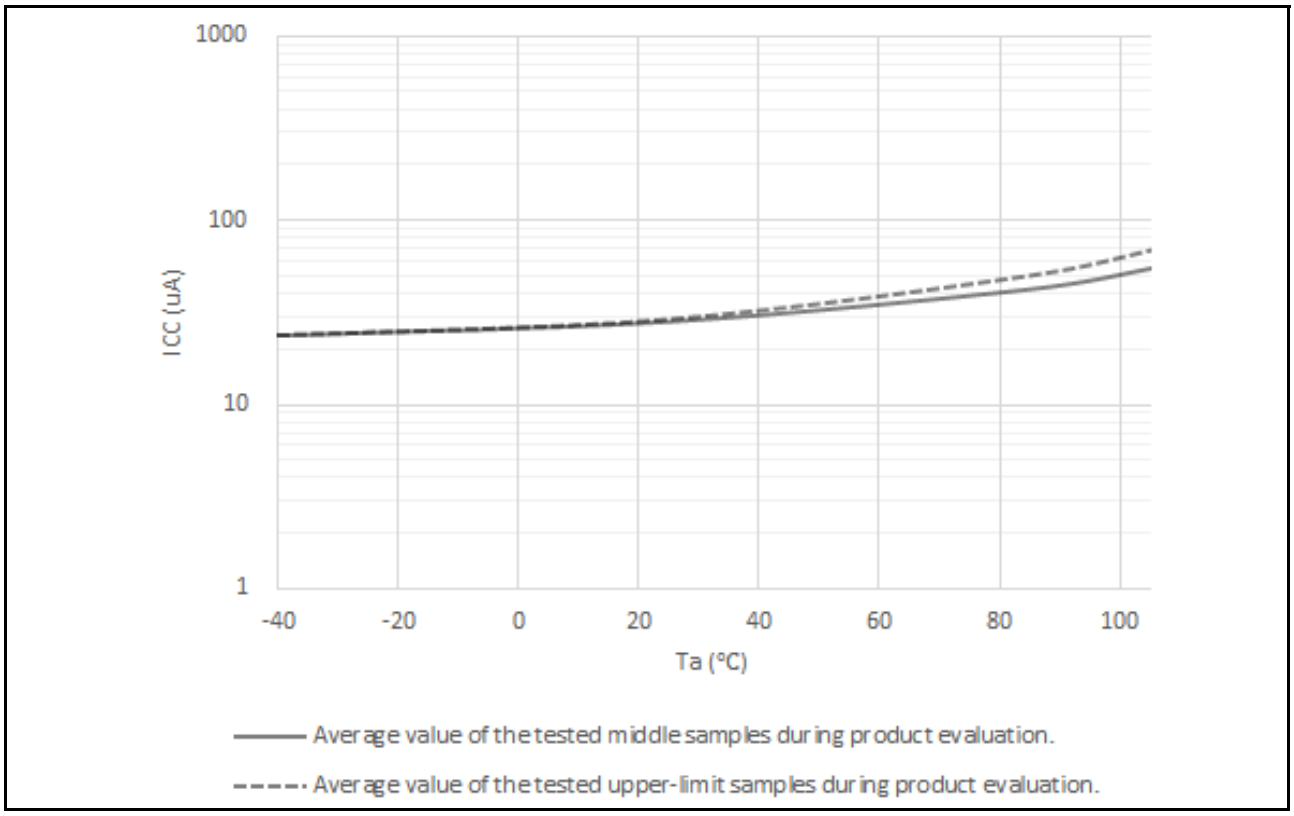



**Figure 2.3** **Temperature dependency in Deep Software Standby mode, power supplied to standby SRAM and USB resume detecting unit (reference data)**

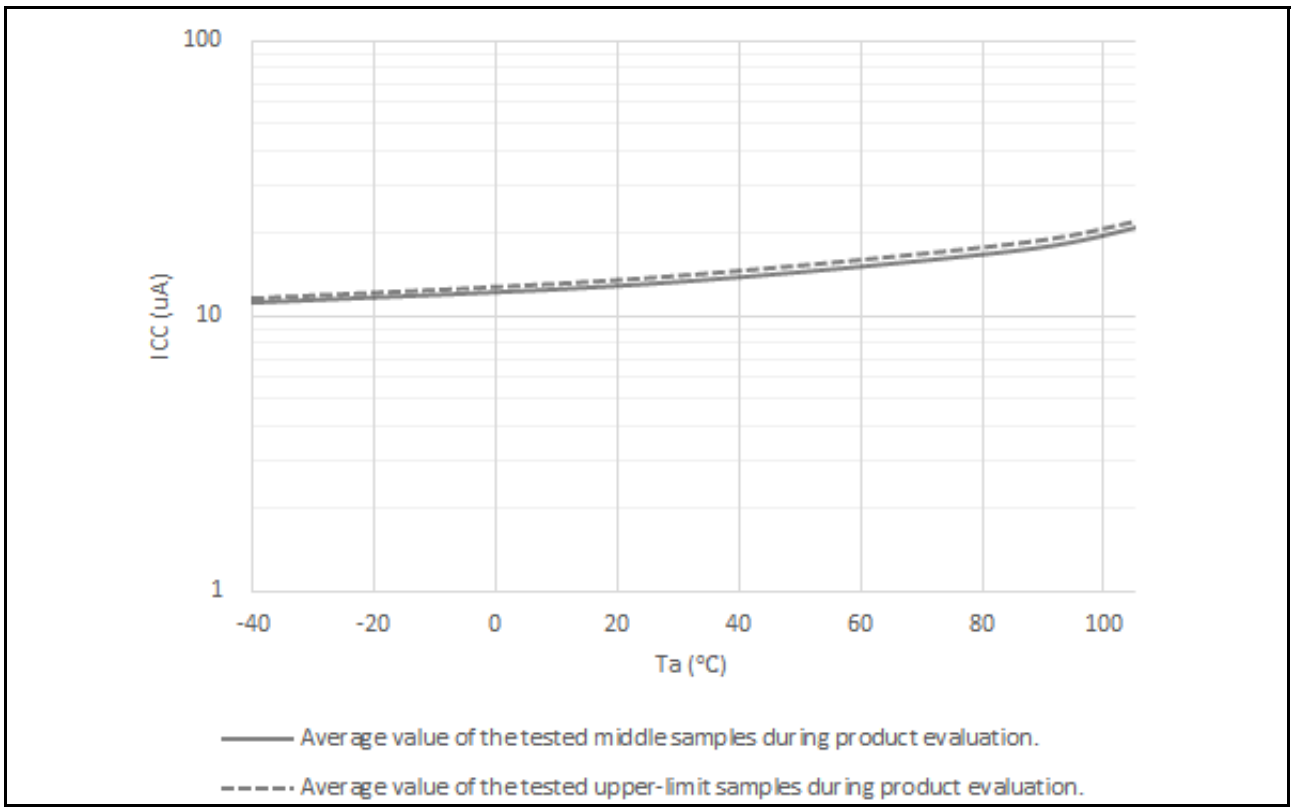



**Figure 2.4** **Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function disabled (reference data)**

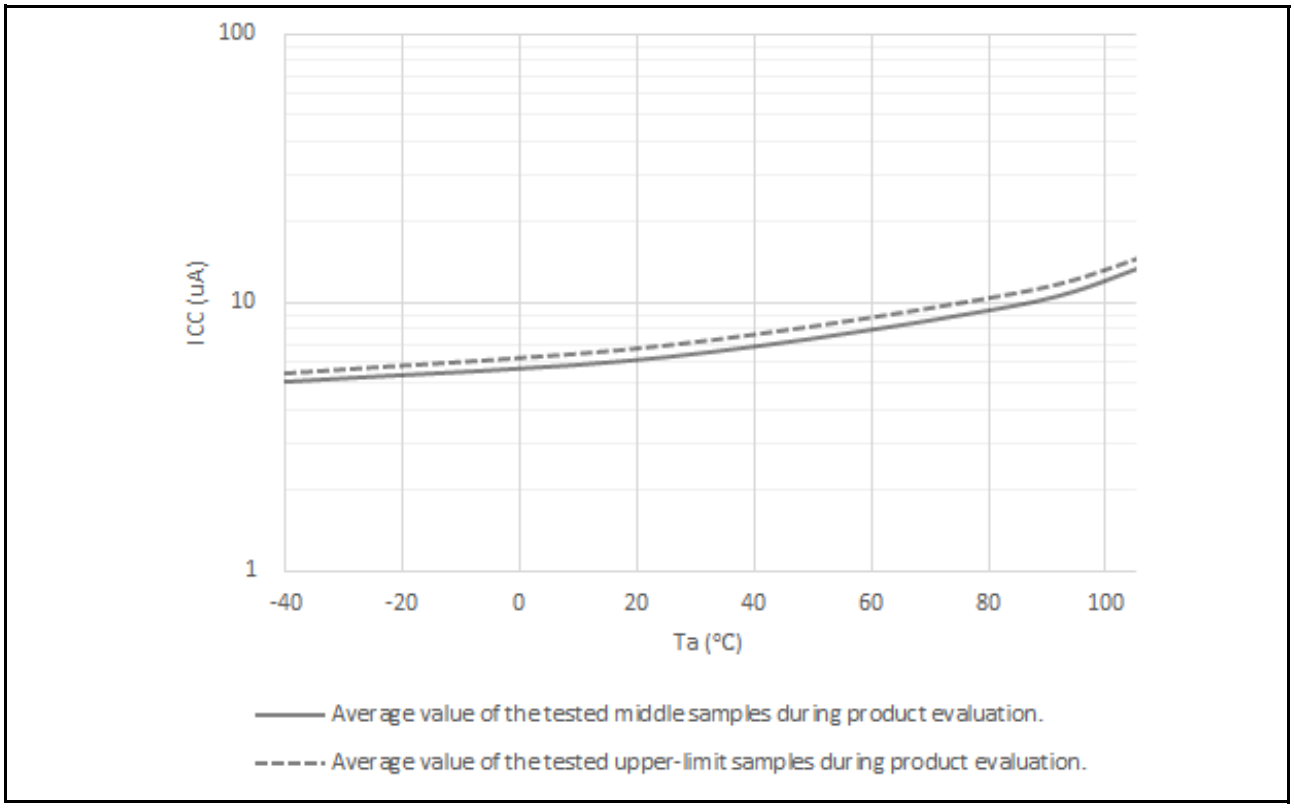



**Figure 2.5 Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low power function enabled (reference data)**

## 2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

**Table 2.8 Rise and fall gradient characteristics**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| VCC rising gradient | Voltage monitor 0 reset disabled at startup | SrVCC | 0.0084 | - | 20 | ms/V | - |
| | Voltage monitor 0 reset enabled at startup | | 0.0084 | - | - | | - |
| | SCI/USB boot mode*1 | | 0.0084 | - | 20 | | - |
| VCC falling gradient*2 | | SfVCC | 0.0084 | - | - | ms/V | - |

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.
Note 2. This applies when VBATT is used.

**Table 2.9 Rise and fall gradient and ripple frequency characteristics**

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Allowable ripple frequency | $f_{r\ (VCC)}$ | - | - | 10 | kHz | Figure 2.6<br>$V_{r\ (VCC)} \leq$ VCC × 0.2 |
| | | - | - | 1 | MHz | Figure 2.6<br>$V_{r\ (VCC)} \leq$ VCC × 0.08 |
| | | - | - | 10 | MHz | Figure 2.6<br>$V_{r\ (VCC)} \leq$ VCC × 0.06 |
| Allowable voltage change rising and falling gradient | dt/dVCC | 1.0 | - | - | ms/V | When VCC change exceeds VCC ±10% |

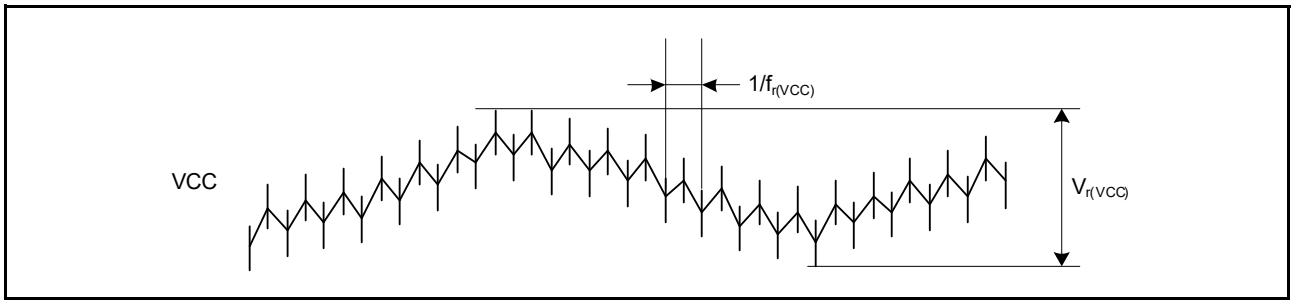



**Figure 2.6 Ripple waveform**

## 2.3 AC Characteristics

### 2.3.1 Frequency

**Table 2.10 Operation frequency value in high-speed mode**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK*2) | f | - | - | 120 | MHz |
| | Peripheral module clock (PCLKA)*2 | | - | - | 120 | |
| | Peripheral module clock (PCLKB)*2 | | - | - | 60 | |
| | Peripheral module clock (PCLKC)*2 | | -*3 | - | 60 | |
| | Peripheral module clock (PCLKD)*2 | | - | - | 120 | |
| | Flash interface clock (FCLK)*2 | | -*1 | - | 60 | |
| | External bus clock (BCLK)*2 | | - | - | 120 | |
| | EBCLK pin output | | - | - | 60 | |

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

**Table 2.11 Operation frequency value in low-speed mode**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK)*2 | f | - | - | 1 | MHz |
| | Peripheral module clock (PCLKA)*2 | | - | - | 1 | |
| | Peripheral module clock (PCLKB)*2 | | - | - | 1 | |
| | Peripheral module clock (PCLKC)*2,*3 | | -*3 | - | 1 | |
| | Peripheral module clock (PCLKD)*2 | | - | - | 1 | |
| | Flash interface clock (FCLK)*1, *2 | | - | - | 1 | |
| | External bus clock (BCLK) | | - | - | 1 | |
| | EBCLK pin output | | - | - | 1 | |

Note 1. Programming or erasing the flash memory is disabled in Low-speed mode.
Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

**Table 2.12 Operation frequency value in Subosc-speed mode**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK)*2 | f | 29.4 | - | 36.1 | kHz |
| | Peripheral module clock (PCLKA)*2 | | - | - | 36.1 | |
| | Peripheral module clock (PCLKB)*2 | | - | - | 36.1 | |
| | Peripheral module clock (PCLKC)*2,*3 | | - | - | 36.1 | |
| | Peripheral module clock (PCLKD)*2 | | - | - | 36.1 | |
| | Flash interface clock (FCLK)*1, *2 | | 29.4 | - | 36.1 | |
| | External bus clock (BCLK)*2 | | - | - | 36.1 | |
| | EBCLK pin output | | - | - | 36.1 | |

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.
Note 2. See section 9, Clock Generation Circuit in User's Manual for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. The ADC12 cannot be used.

## 2.3.2 Clock Timing

**Table 2.13 Clock timing except for sub-clock oscillator (1 of 2)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| EBCLK pin output cycle time | | $t_{Bcyc}$ | 16.6 | - | - | ns | Figure 2.7 |
| EBCLK pin output high pulse width | | $t_{CH}$ | 3.3 | - | - | ns | |
| EBCLK pin output low pulse width | | $t_{CL}$ | 3.3 | - | - | ns | |
| EBCLK pin output rise time | | $t_{Cr}$ | - | - | 5.0 | ns | |
| EBCLK pin output fall time | | $t_{Cf}$ | - | - | 5.0 | ns | |
| EXTAL external clock input cycle time | | $t_{EXcyc}$ | 41.66 | - | - | ns | Figure 2.8 |
| EXTAL external clock input high pulse width | | $t_{EXH}$ | 15.83 | - | - | ns | |
| EXTAL external clock input low pulse width | | $t_{EXL}$ | 15.83 | - | - | ns | |
| EXTAL external clock rise time | | $t_{EXr}$ | - | - | 5.0 | ns | |
| EXTAL external clock fall time | | $t_{EXf}$ | - | - | 5.0 | ns | |
| Main clock oscillator frequency | | $f_{MAIN}$ | 8 | - | 24 | MHz | - |
| Main clock oscillation stabilization wait time (crystal) *1 | | $t_{MAINOSCWT}$ | - | - | -*1 | ms | Figure 2.9 |
| LOCO clock oscillation frequency | | $f_{LOCO}$ | 29.4912 | 32.768 | 36.0448 | kHz | - |
| LOCO clock oscillation stabilization wait time | | $t_{LOCOWT}$ | - | - | 60.4 | μs | Figure 2.10 |
| ILOCO clock oscillation frequency | | $f_{ILOCO}$ | 13.5 | 15 | 16.5 | kHz | - |
| MOCO clock oscillation frequency | | $F_{MOCO}$ | 6.8 | 8 | 9.2 | MHz | - |
| MOCO clock oscillation stabilization wait time | | $t_{MOCOWT}$ | - | - | 15.0 | μs | - |
| HOCO clock oscillator oscillation frequency | Without FLL | $f_{HOCO16}$ | 15.78 | 16 | 16.22 | MHz | -20 ≤ Ta ≤ 105°C |
| | | $f_{HOCO18}$ | 17.75 | 18 | 18.25 | | |
| | | $f_{HOCO20}$ | 19.72 | 20 | 20.28 | | |
| | | $f_{HOCO16}$ | 15.71 | 16 | 16.29 | | -40 ≤ Ta ≤ -20°C |
| | | $f_{HOCO18}$ | 17.68 | 18 | 18.32 | | |
| | | $f_{HOCO20}$ | 19.64 | 20 | 20.36 | | |
| | With FLL | $f_{HOCO16}$ | 15.960 | 16 | 16.040 | | -40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm. |
| | | $f_{HOCO18}$ | 17.955 | 18 | 18.045 | | |
| | | $f_{HOCO20}$ | 19.950 | 20 | 20.050 | | |
| HOCO clock oscillation stabilization wait time*2 | | $t_{HOCOWT}$ | - | - | 64.7 | μs | - |
| FLL stabilization wait time | | $t_{FLLWT}$ | - | - | 1.8 | ms | - |
| PLL clock frequency | | $f_{PLL}$ | 120 | - | 240 | MHz | - |

**Table 2.13 Clock timing except for sub-clock oscillator (2 of 2)**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| PLL clock oscillation stabilization wait time | $t_{PLLWT}$ | - | - | 174.9 | μs | Figure 2.11 |

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (fHOCO) reaches the range for guaranteed operation.

**Table 2.14 Clock timing for the sub-clock oscillator**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Sub-clock frequency | $f_{SUB}$ | - | 32.768 | - | kHz | - |
| Sub-clock oscillation stabilization wait time | $t_{SUBOSCWT}$ | - | - | -*1 | s | Figure 2.12 |

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

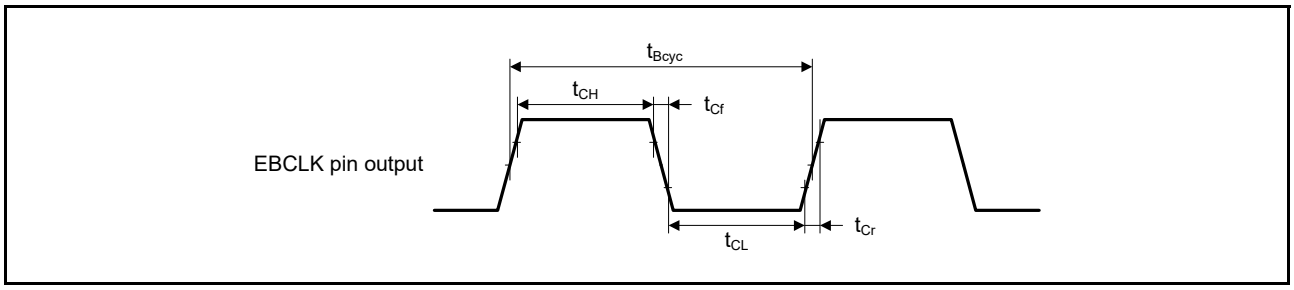



**Figure 2.7 EBCLK output timing**

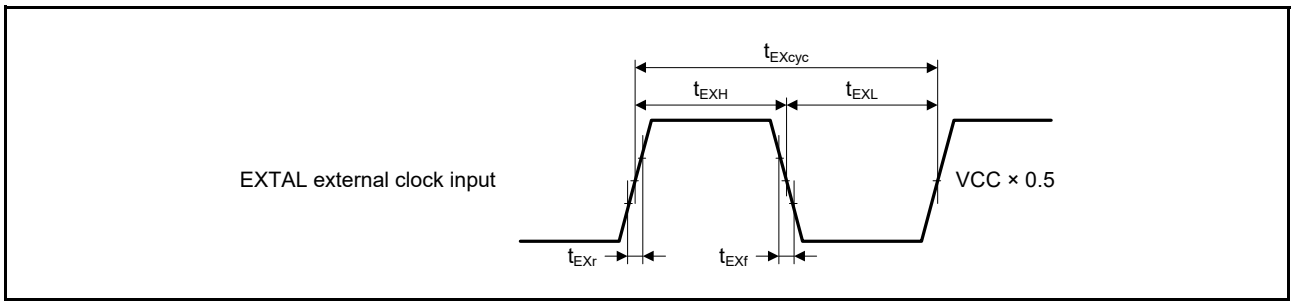



**Figure 2.8 EXTAL external clock input timing**

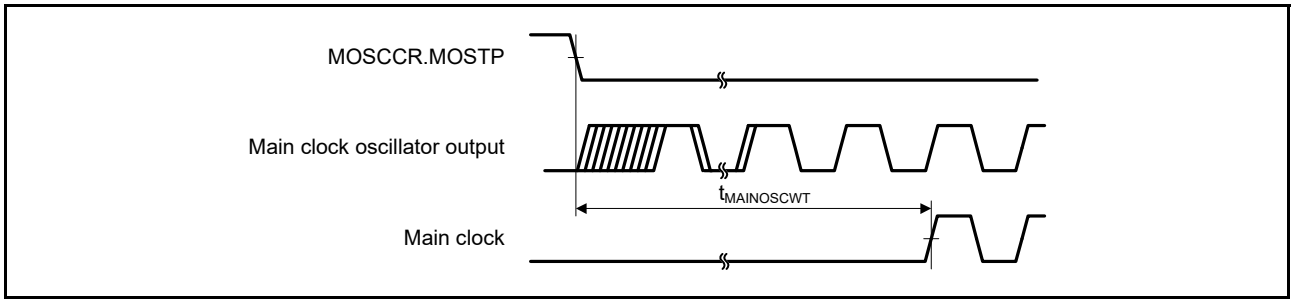



**Figure 2.9 Main clock oscillation start timing**

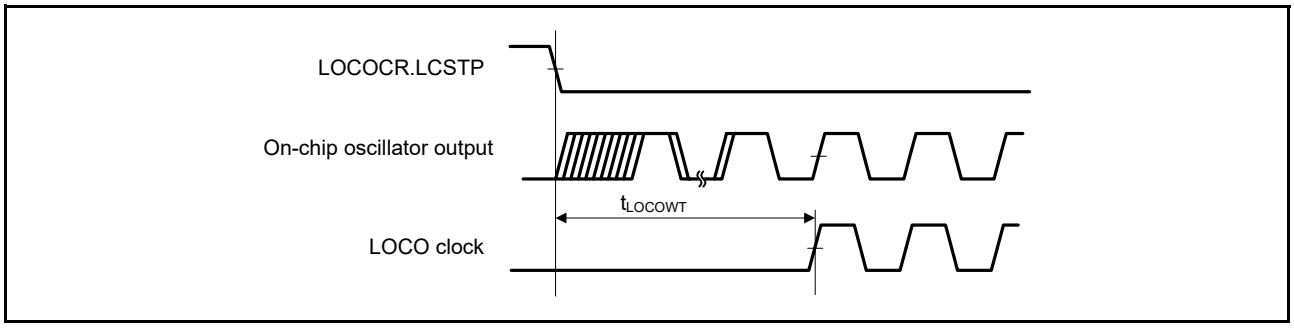



**Figure 2.10 LOCO clock oscillation start timing**

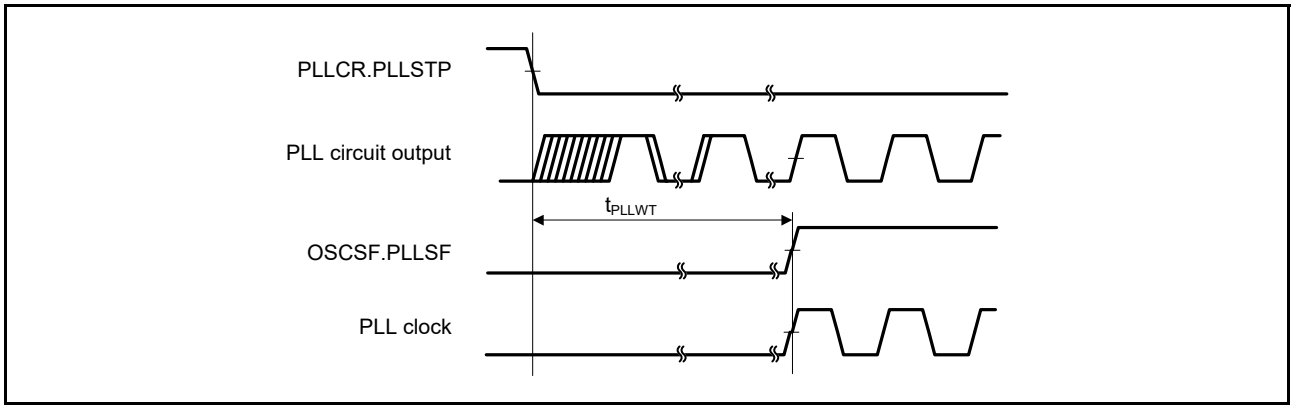



**Figure 2.11 PLL clock oscillation start timing**

Note: Only operate the PLL after the main clock oscillation has stabilized.

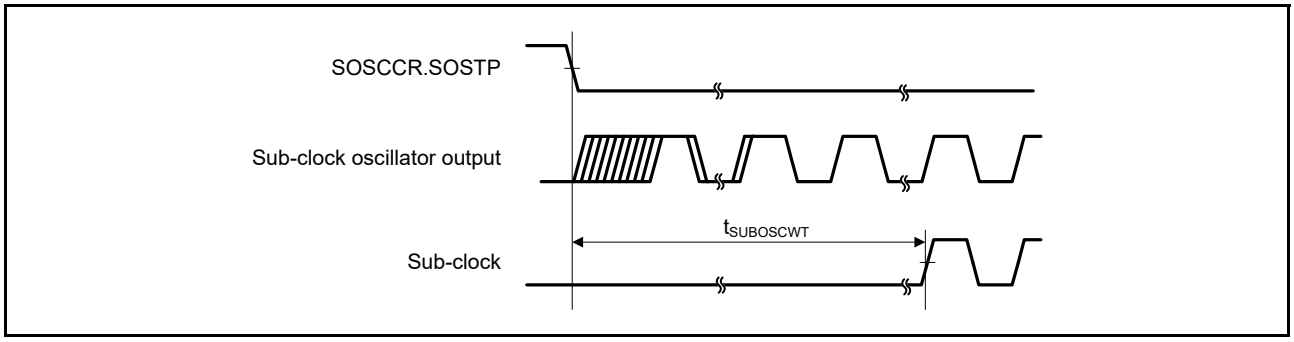



**Figure 2.12 Sub-clock oscillation start timing**

## 2.3.3 Reset Timing

**Table 2.15 Reset timing (1 of 2)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| RES pulse width | Power-on | $t_{RESWP}$ | 1 | - | - | ms | Figure 2.13 |
| | Deep Software Standby mode | $t_{RESWD}$ | 0.6 | - | - | ms | Figure 2.14 |
| | Software Standby mode, Subosc-speed mode | $t_{RESWS}$ | 0.3 | - | - | ms | |
| | All other | $t_{RESW}$ | 200 | - | - | μs | |
| Wait time after RES cancellation | | $t_{RESWT}$ | - | 29 | 32 | μs | Figure 2.13 |

**Table 2.15 Reset timing (2 of 2)**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset) | $t_{RESW2}$ | - | 320 | 390 | μs | - |

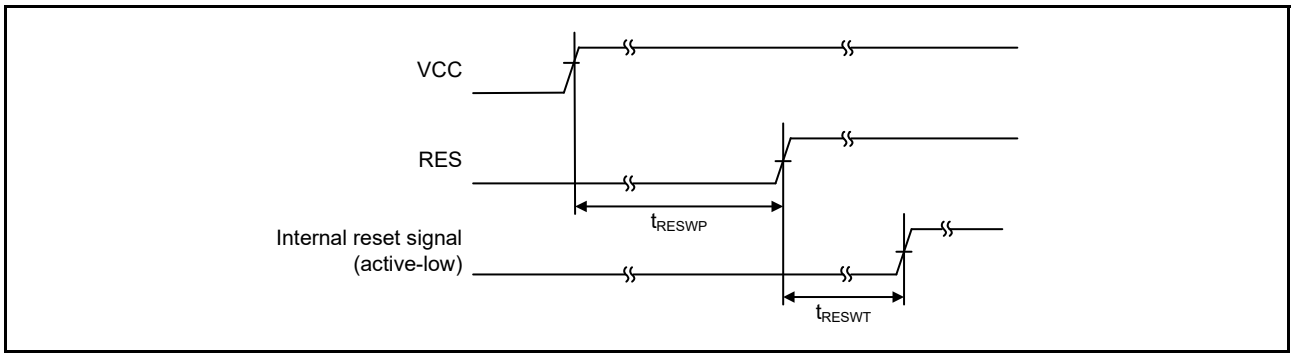



**Figure 2.13 Power-on reset timing**

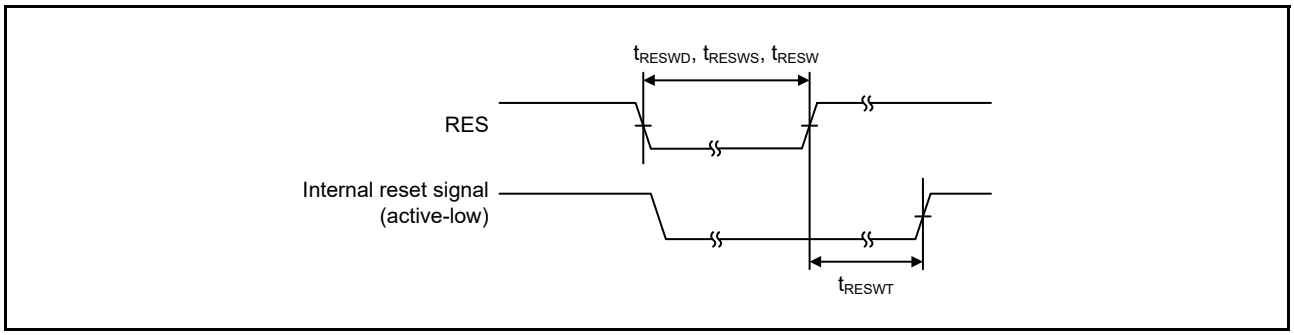



**Figure 2.14 Reset input timing**

## 2.3.4 Wakeup Timing

**Table 2.16 Timing of recovery from low power modes (1 of 2)**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Recovery time from Software Standby mode*1 | Crystal resonator connected to main clock oscillator | System clock source is main clock oscillator*2 | $t_{SBYMC}$ | - | 2.4*9 | 2.8*9 | ms | Figure 2.15 The division ratio of all oscillators is 1. |
| | | System clock source is PLL with main clock oscillator*3 | $t_{SBYPC}$ | - | 2.7*9 | 3.2*9 | ms | |
| | External clock input to main clock oscillator | System clock source is main clock oscillator*4 | $t_{SBYEX}$ | - | 230*9 | 280*9 | μs | |
| | | System clock source is PLL with main clock oscillator*5 | $t_{SBYPE}$ | - | 570*9 | 700*9 | μs | |
| | System clock source is sub-clock oscillator*8 | | $t_{SBYSC}$ | - | 1.2*9 | 1.3*9 | ms | |
| | System clock source is LOCO*8 | | $t_{SBYLO}$ | - | 1.2*9 | 1.4*9 | ms | |
| | System clock source is HOCO*6 | | $t_{SBYHO}$ | - | 240*9, *10 | 300 *9, *10 | μs | |
| | System clock source is MOCO*7 | | $t_{SBYMO}$ | - | 220*9 | 300*9 | μs | |

**Table 2.16 Timing of recovery from low power modes (2 of 2)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Recovery time from Deep Software Standby mode | | $t_{DSBY}$ | - | 0.65 | 1.0 | ms | Figure 2.16 |
| Wait time after cancellation of Deep Software Standby mode | | $t_{DSBYWT}$ | 34 | - | 35 | $t_{cyc}$ | |
| Recovery time from Software Standby mode to Snooze mode | High-speed mode when system clock source is HOCO (20 MHz) | $t_{SNZ}$ | - | 35*9, *10 | 70 *9, *10 | μs | Figure 2.17 |
| | High-speed mode when system clock source is MOCO (8 MHz) | $t_{SNZ}$ | - | 11*9 | 14*9 | μs | |

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPC0 = 0 (CAC module stop)).

Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
$t_{SBYMC}$ (MOSCWTCR = Xh) = $t_{SBYMC}$ (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
$t_{SBYMC}$ (MOSCWTCR = Xh) = $t_{SBYMC}$ (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 01h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
$t_{SBYMC}$ (MOSCWTCR = Xh) = $t_{SBYMC}$ (MOSCWTCR = 01h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 01h))

Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 01h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
$t_{SBYMC}$ (MOSCWTCR = Xh) = $t_{SBYMC}$ (MOSCWTCR = 01h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 01h))

Note 6. The HOCO frequency is 20 MHz.

Note 7. The MOCO frequency is 8 MHz.

Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.

Note 9. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time:
STCONR.STCON[1:0] = 00b:16 μs (typical), 34 μs (maximum)
STCONR.STCON[1:0] = 11b:16 μs (typical), 104 μs (maximum).

Note 10. When the SNZCR.RXDREQEN bit is set to 0, 16 μs (typical) or 18 μs (maximum) is added as the HOCO wait time.

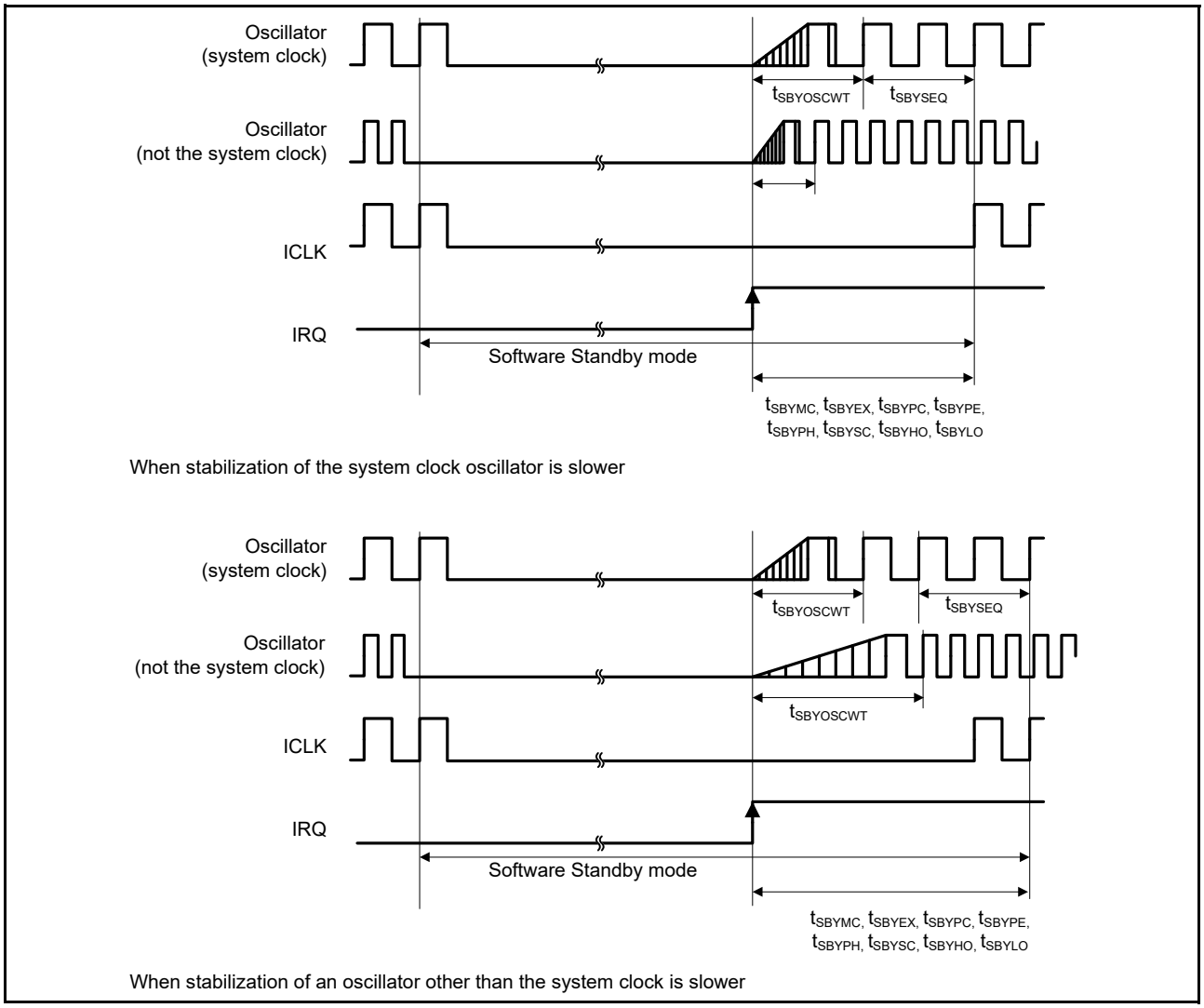



**Figure 2.15 Software Standby mode cancellation timing**

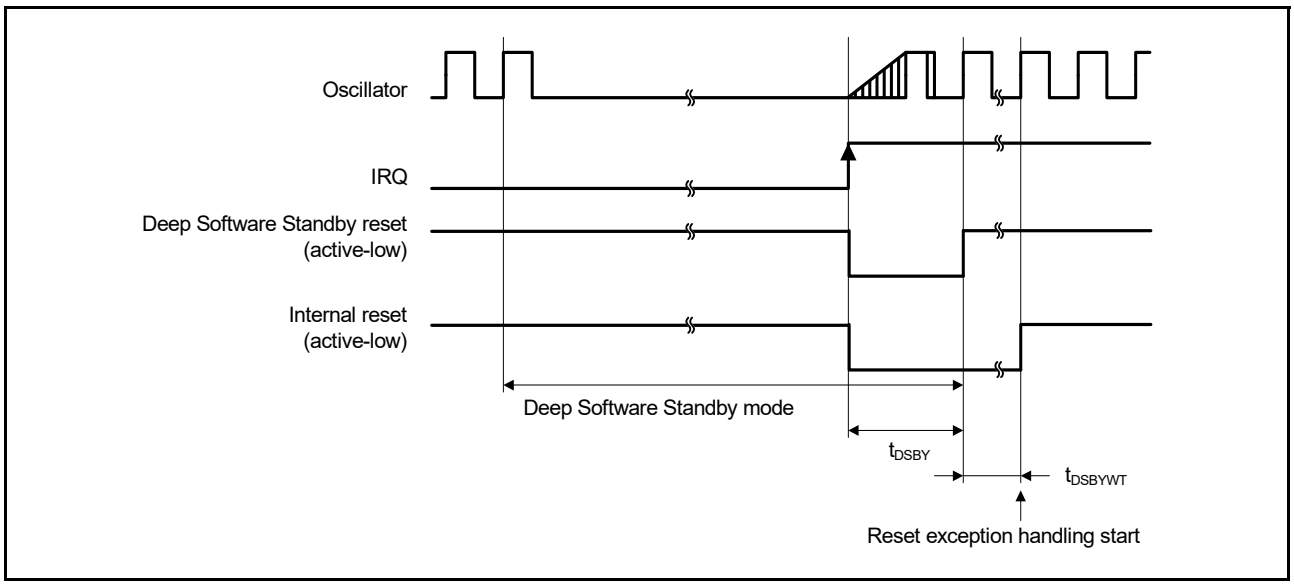
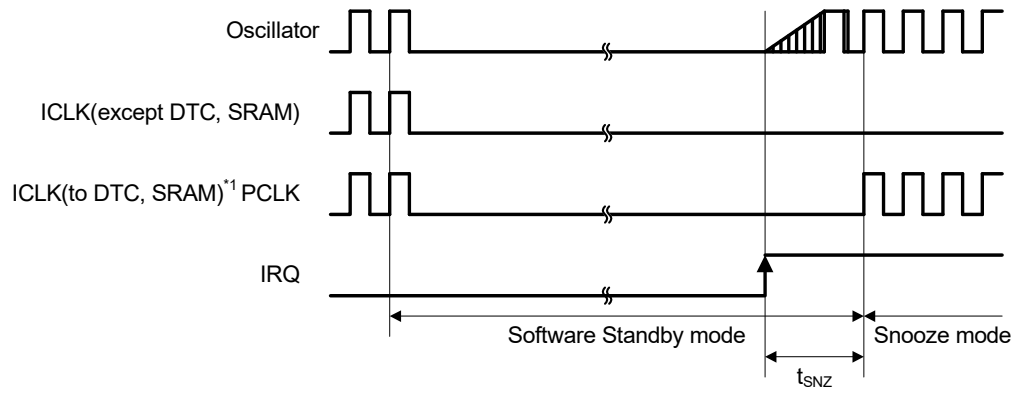



**Figure 2.16 Deep Software Standby mode cancellation timing**




Note 1. When SNZCR.SNZDTCEN is set to 1, ICLK is supplied to DTC and SRAM.

**Figure 2.17 Recovery timing from Software Standby mode to Snooze mode**

## 2.3.5 NMI and IRQ Noise Filter

**Table 2.17 NMI and IRQ noise filter**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | - | - | ns | NMI digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | - | - | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | - | - | | NMI digital filter enabled | $t_{NMICK} \times 3 \leq 200$ ns |
| | | $t_{NMICK} \times 3.5$*2 | - | - | | | $t_{NMICK} \times 3 > 200$ ns |
| IRQ pulse width | $t_{IRQW}$ | 200 | - | - | ns | IRQ digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | - | - | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | - | - | | IRQ digital filter enabled | $t_{IRQCK} \times 3 \leq 200$ ns |
| | | $t_{IRQCK} \times 3.5$*3 | - | - | | | $t_{IRQCK} \times 3 > 200$ ns |

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. $t_{Pcyc}$ indicates the PCLKB cycle.
Note 2. $t_{NMICK}$ indicates the cycle of the NMI digital filter sampling clock.
Note 3. $t_{IRQCK}$ indicates the cycle of the IRQi digital filter sampling clock.

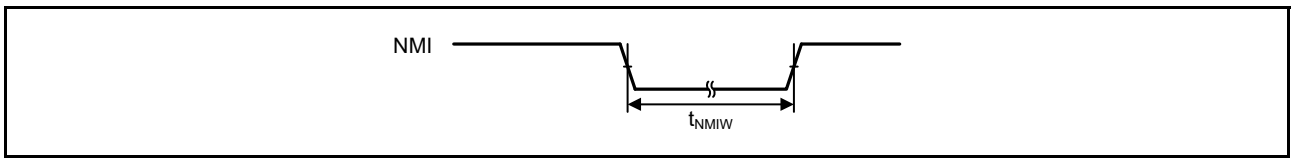



**Figure 2.18 NMI interrupt input timing**

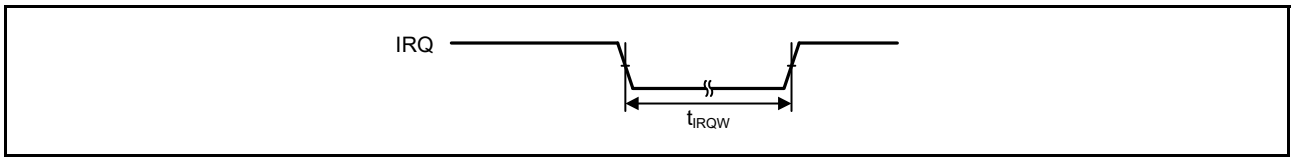



**Figure 2.19 IRQ interrupt input timing**

### 2.3.6 Bus Timing

**Table 2.18 Bus timing**

Conditions:
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz.
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0.
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF.
EBCLK: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
Others: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Address delay | $t_{AD}$ | - | 12.5 | ns | Figure 2.20 to Figure 2.25 |
| CS delay | $t_{CSD}$ | - | 12.5 | ns | |
| ALE delay time | $t_{ALED}$ | - | 12.5 | ns | |
| RD delay | $t_{RSD}$ | - | 12.5 | ns | |
| Read data setup time | $t_{RDS}$ | 12.5 | - | ns | |
| Read data hold time | $t_{RDH}$ | 0 | - | ns | |
| WR0 delay | $t_{WRD}$ | - | 12.5 | ns | |
| Write data delay | $t_{WDD}$ | - | 12.5 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | - | ns | |
| WAIT setup time | $t_{WTS}$ | 12.5 | - | ns | Figure 2.26 |
| WAIT hold time | $t_{WTH}$ | 0 | - | ns | |

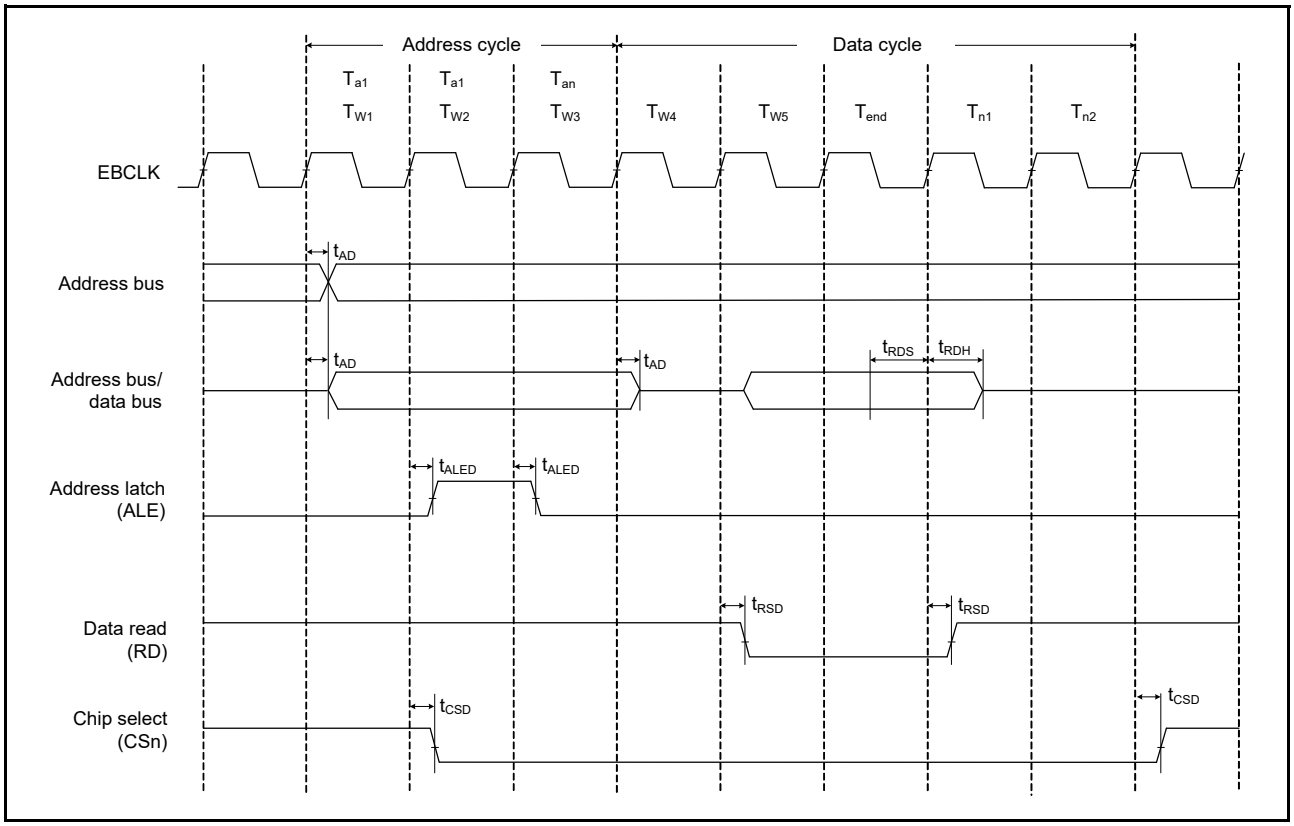



**Figure 2.20 Address/data multiplexed bus read access timing**

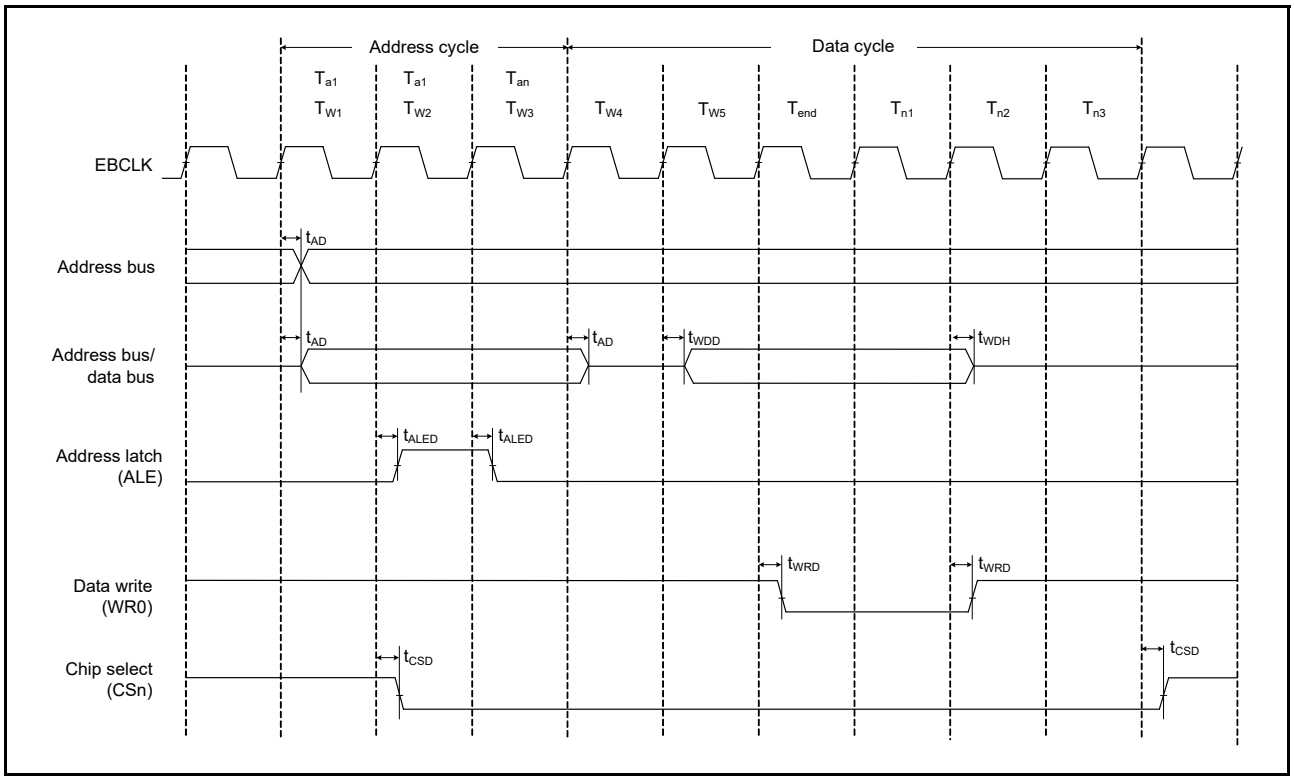



**Figure 2.21 Address/data multiplexed bus write access timing**

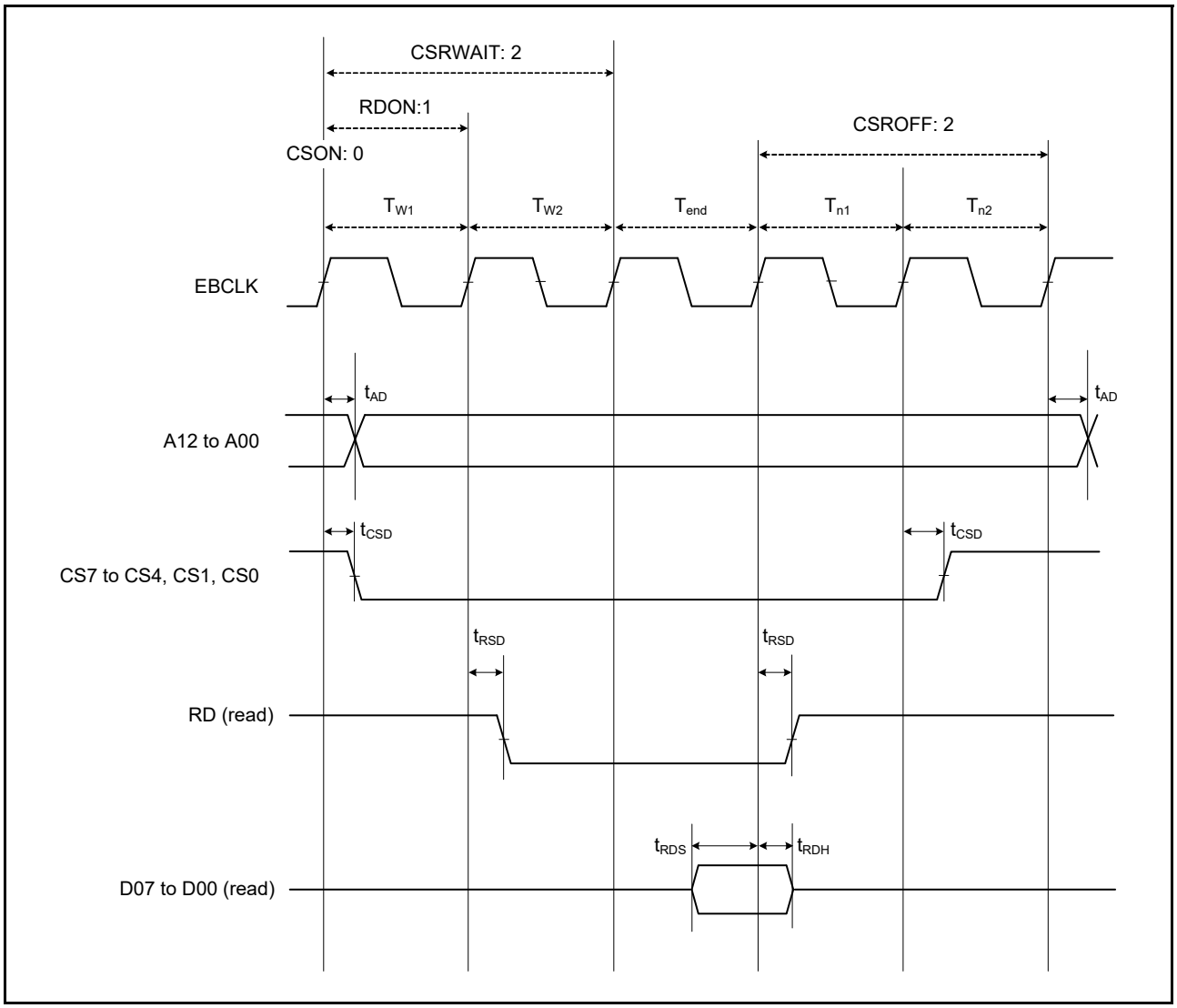
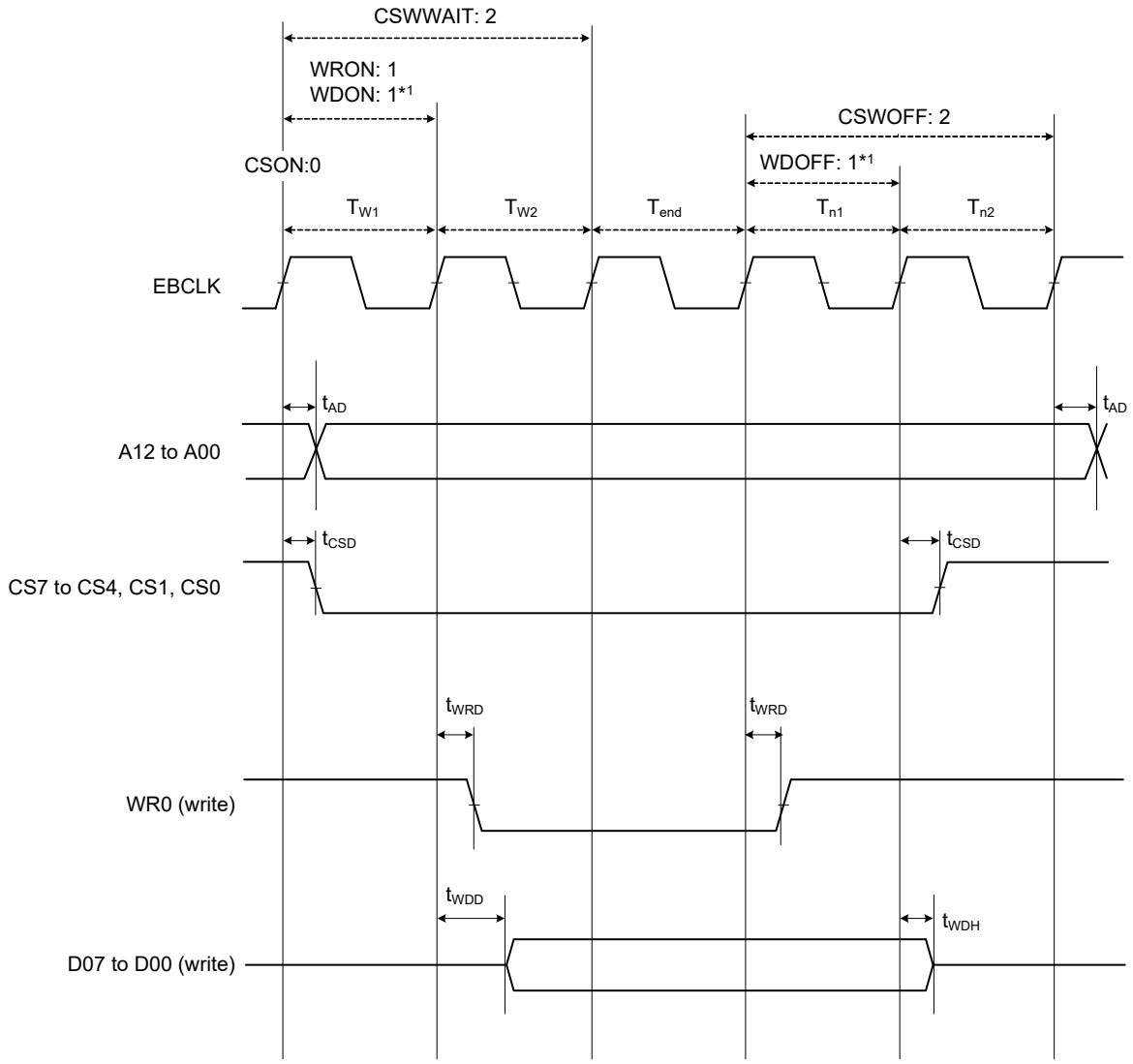



**Figure 2.22 External bus timing for normal read cycle with bus clock synchronized**




Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

**Figure 2.23 External bus timing for normal write cycle with bus clock synchronized**

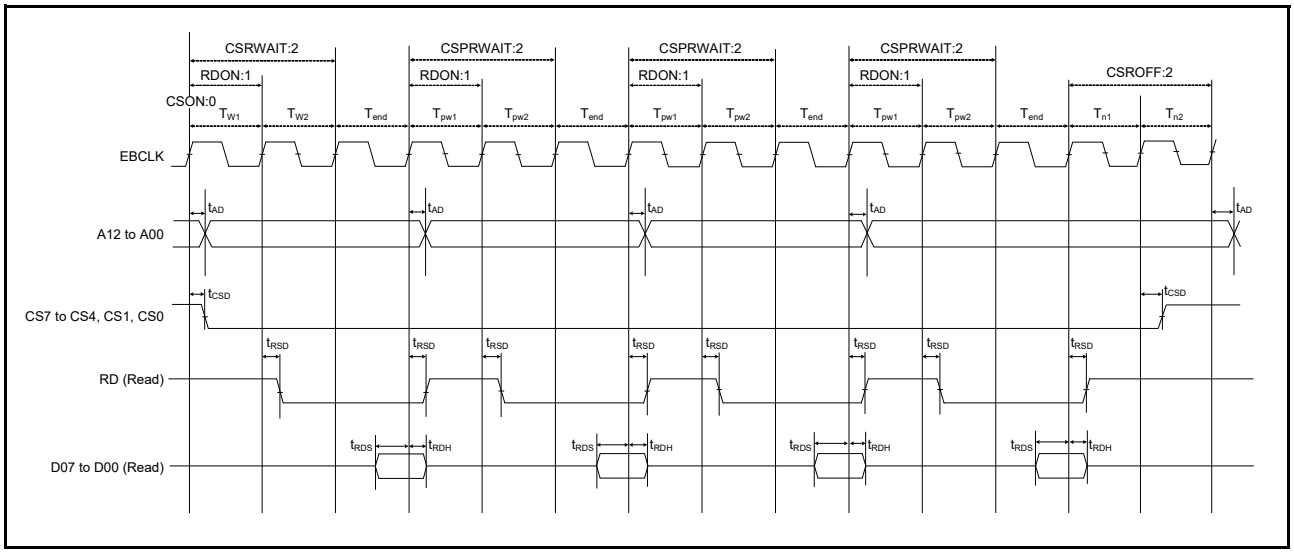



**Figure 2.24 External bus timing for page read cycle with bus clock synchronized**

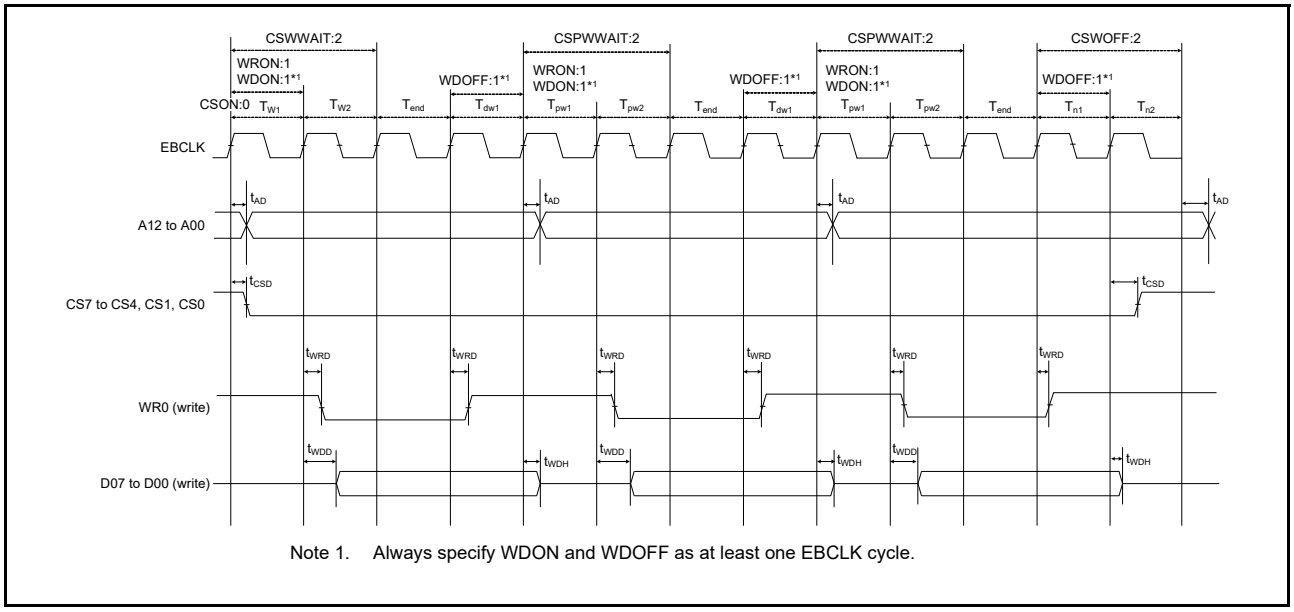



**Figure 2.25 External bus timing for page write cycle with bus clock synchronized**

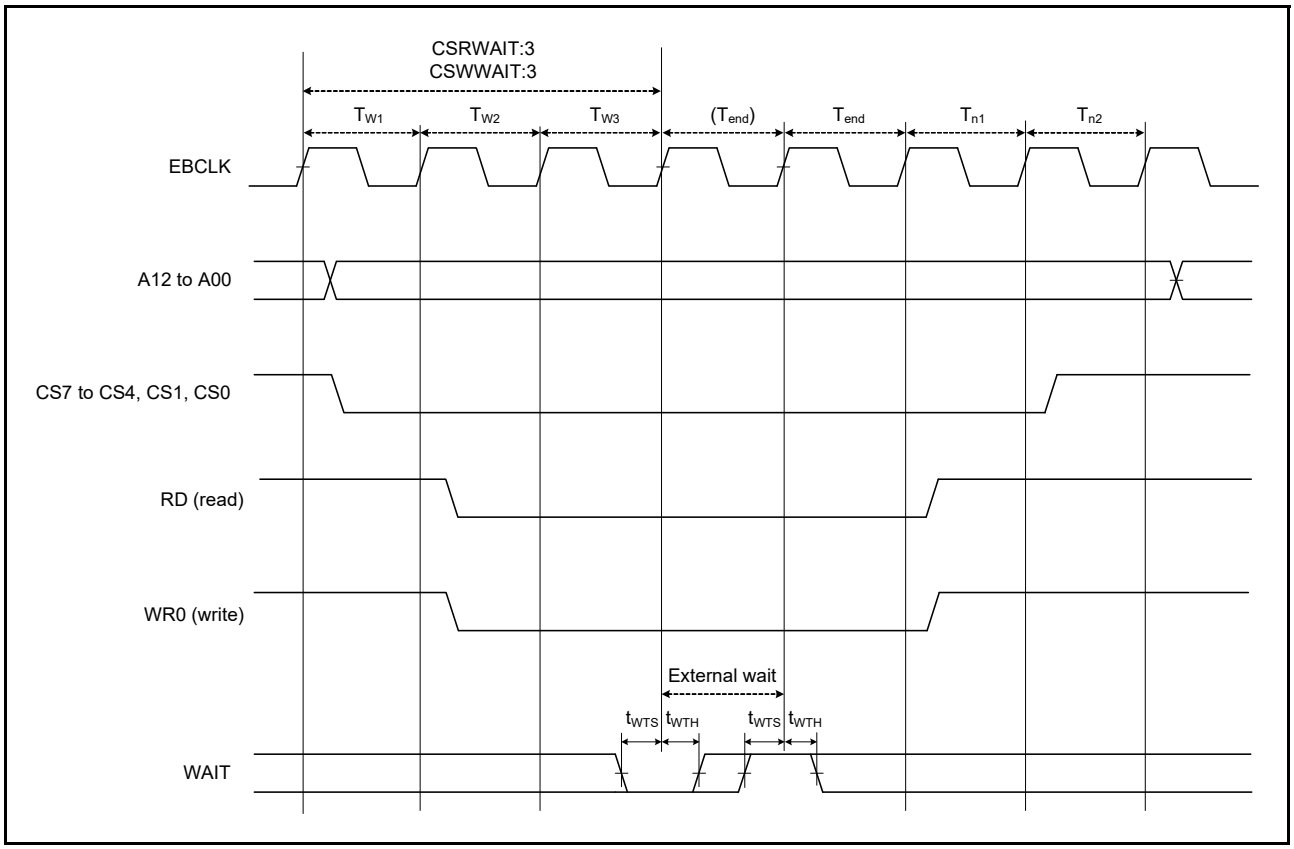



**Figure 2.26 External bus timing for external wait control**

## 2.3.7 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

**Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (1 of 2)**

GPT32 conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| I/O ports | Input data pulse width | | $t_{PRW}$ | 1.5 | - | $t_{Pcyc}$ | Figure 2.27 |
| POEG | POEG input trigger pulse width | | $t_{POEW}$ | 3 | - | $t_{Pcyc}$ | Figure 2.28 |
| GPT32 | Input capture pulse width | Single edge | $t_{GTICW}$ | 1.5 | - | $t_{PDcyc}$ | Figure 2.29 |
| | | Dual edge | | 2.5 | - | | |
| | GTIOCxY output skew (x = 0 to 7, Y= A or B) | Middle drive buffer | $t_{GTISK}$*1 | - | 4 | ns | Figure 2.30 |
| | | High drive buffer | | - | 4 | | |
| | GTIOCxY output skew (x = 8 to 12, Y = A or B) | Middle drive buffer | | - | 4 | | |
| | | High drive buffer | | - | 4 | | |
| | GTIOCxY output skew (x = 0 to 12, Y = A or B) | Middle drive buffer | | - | 6 | | |
| | | High drive buffer | | - | 6 | | |
| | OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO | | $t_{GTOSK}$ | - | 5 | ns | Figure 2.31 |
| GPT (PWM Delay Generation Circuit) | GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A) | | $t_{HRSK}$*2 | - | 2.0 | ns | Figure 2.32 |

**Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (2 of 2)**
GPT32 conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| AGT | AGTIO, AGTEE input cycle | $t_{ACYC}$*3 | 100 | - | ns | Figure 2.33 |
| | AGTIO, AGTEE input high width, low width | $t_{ACKWH}$, $t_{ACKWL}$ | 40 | - | ns | |
| | AGTIO, AGTO, AGTOA, AGTOB output cycle | $t_{ACYC2}$ | 62.5 | - | ns | |
| ADC12 | ADC12 trigger input pulse width | $t_{TRGW}$ | 1.5 | - | $t_{Pcyc}$ | Figure 2.34 |
| KINT | KRn(n = 00 to 07) pulse width | $t_{KR}$ | 250 | - | ns | Figure 2.35 |

Note: $t_{Pcyc}$: PCLKB cycle, $t_{PDcyc}$: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. The load is 30 pF.
Note 3. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

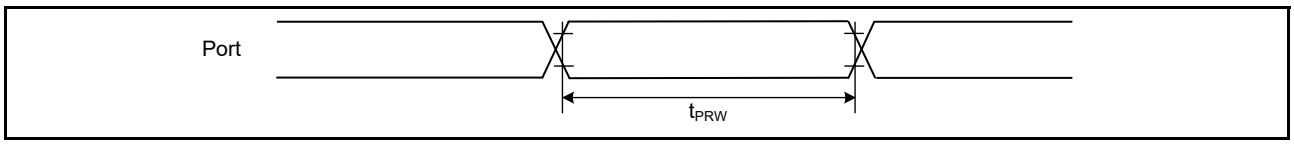



**Figure 2.27 I/O ports input timing**

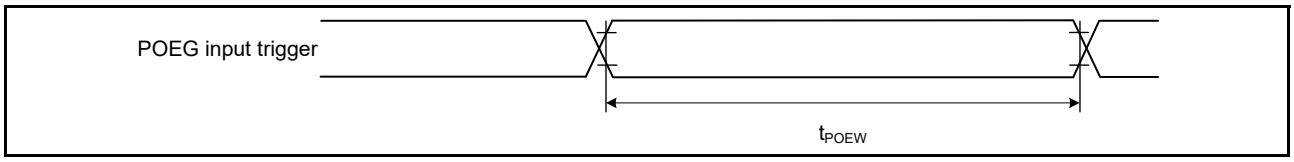



**Figure 2.28 POEG input trigger timing**

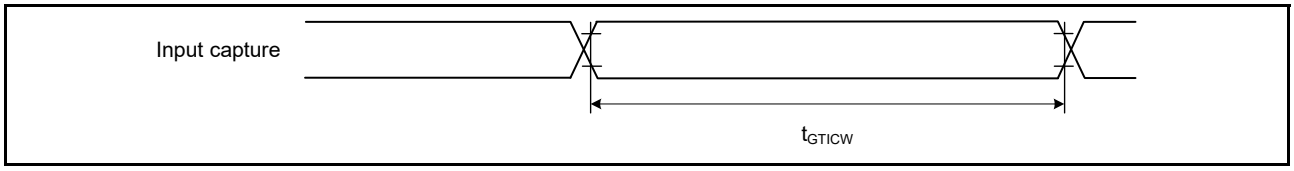



**Figure 2.29 GPT32 input capture timing**

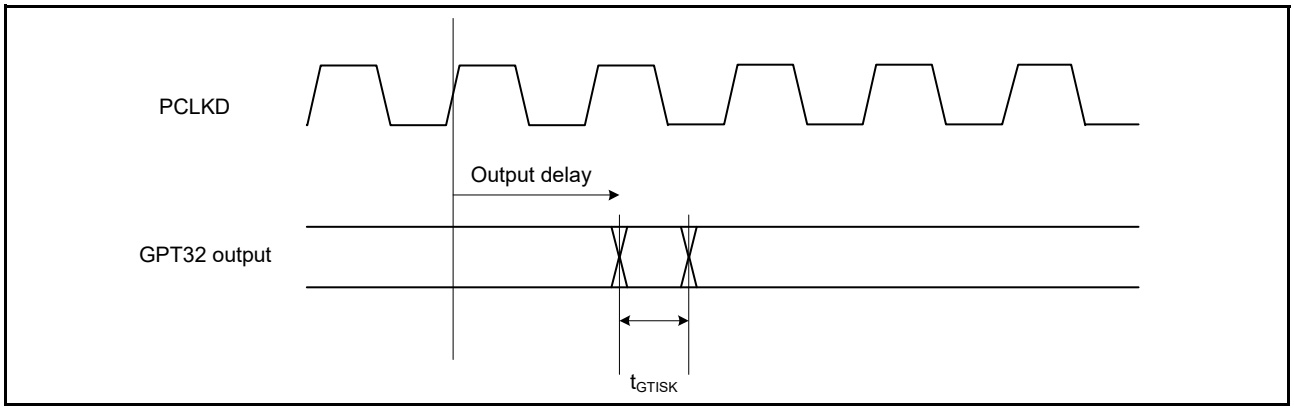



**Figure 2.30 GPT32 output delay skew**

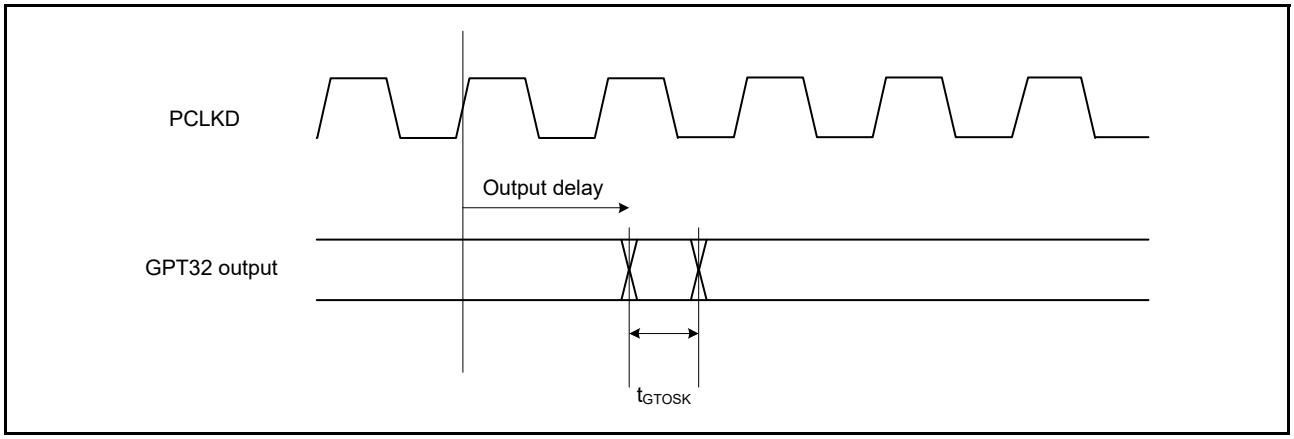



**Figure 2.31 GPT32 output delay skew for OPS**

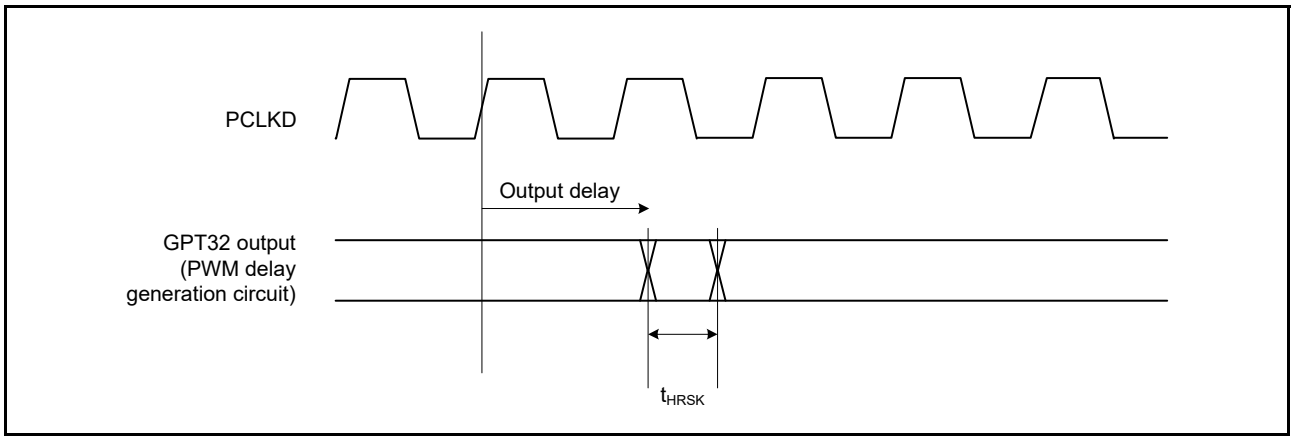



**Figure 2.32 GPT32 (PWM delay generation circuit) output delay skew**

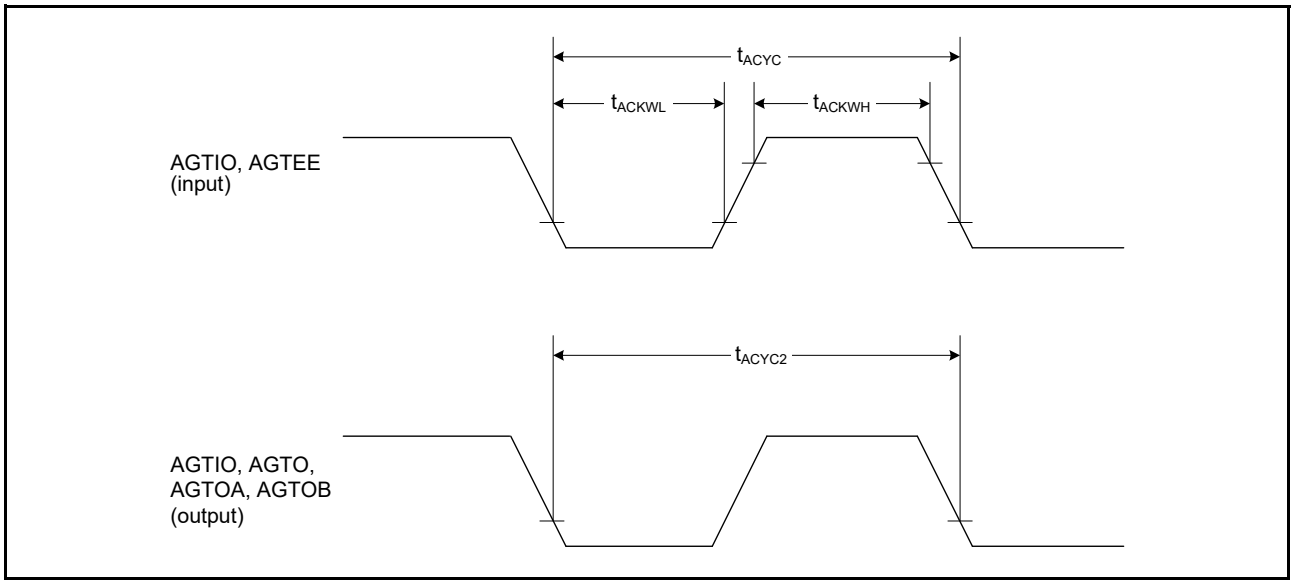



**Figure 2.33 AGT input/output timing**

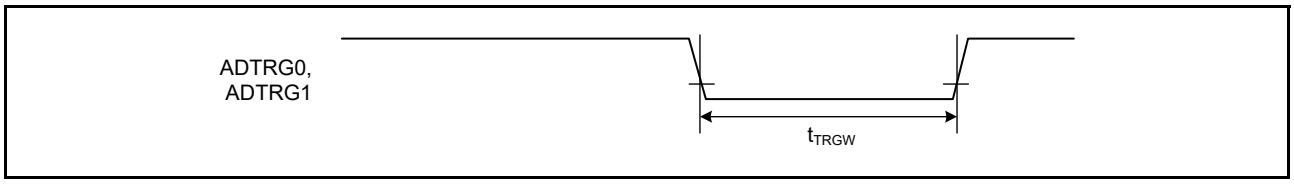



**Figure 2.34 ADC12 trigger input timing**

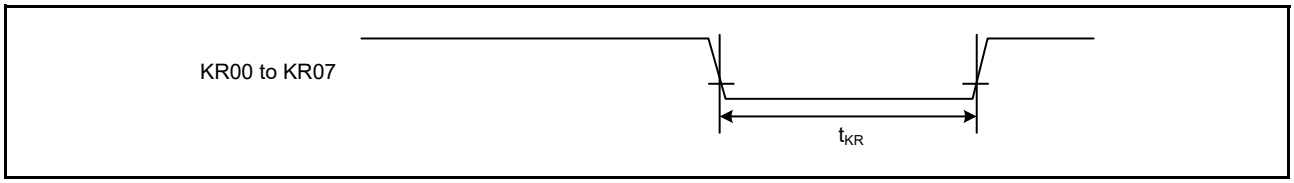



**Figure 2.35 Key interrupt input timing**

## 2.3.8 PWM Delay Generation Circuit Timing

**Table 2.20 PWM Delay Generation Circuit timing**

| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Operation frequency | 80 | - | 120 | MHz | - |
| Resolution | - | 260 | - | ps | PCLKD = 120 MHz |
| DNL*1 | - | ±2.0 | - | LSB | - |

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

## 2.3.9 CAC Timing

**Table 2.21 CAC timing**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| CAC | CACREF input pulse width | $t_{PBcyc} \leq t_{cac}$*2 | $t_{CACREF}$ | $4.5 \times t_{cac} + 3 \times t_{PBcyc}$ | - | - | ns | - |
| | | $t_{PBcyc} > t_{cac}$*2 | | $5 \times t_{cac} + 6.5 \times t_{PBcyc}$ | - | - | ns | |

Note 1. $t_{PBcyc}$: PCLKB cycle.
Note 2. $t_{cac}$: CAC count clock source cycle.

## 2.3.10 SCI Timing

**Table 2.22 SCI timing (1)**
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SCK0 to SCK4, SCK8, SCK9.
For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | | Symbol | Min | Max | Unit*1 | Test conditions |
|---|---|---|---|---|---|---|---|
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | - | $t_{Pcyc}$ | Figure 2.36 |
| | | Clock synchronous | | 6 | - | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | - | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | - | 5 | ns | |
| | Output clock cycle | Asynchronous | $t_{Scyc}$ | 6 | - | $t_{Pcyc}$ | |
| | | Clock synchronous | | 4 | - | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | - | 5 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | - | 5 | ns | |
| | Transmit data delay | Clock synchronous | $t_{TXD}$ | - | 25 | ns | Figure 2.37 |
| | Receive data setup time | Clock synchronous | $t_{RXS}$ | 15 | - | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 5 | - | ns | |

Note 1. $t_{Pcyc}$: PCLKA cycle.

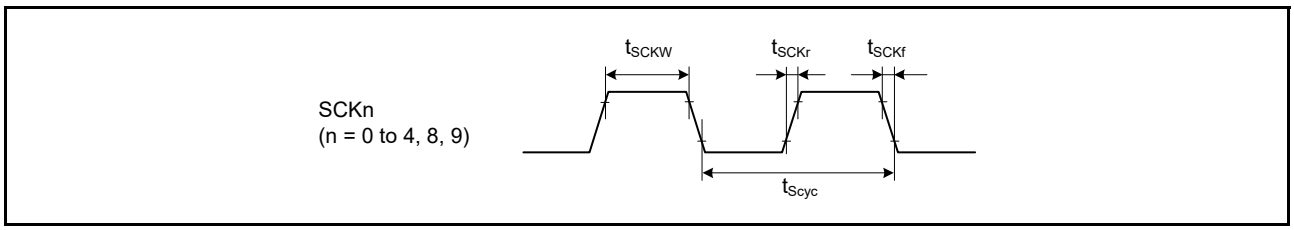



**Figure 2.36 SCK clock input/output timing**

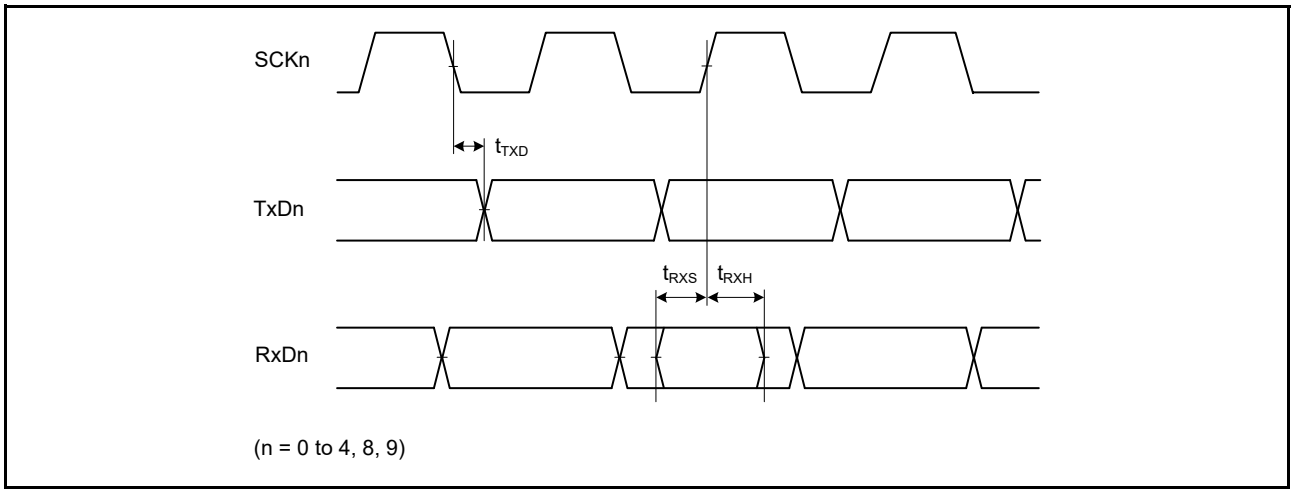



**Figure 2.37 SCI input/output timing in clock synchronous mode**

**Table 2.23 SCI timing (2)**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SCK0 to SCK4, SCK8, SCK9.
For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Simple SPI | SCK clock cycle output (master) | $t_{SPcyc}$ | 4 (PCLKA ≤ 60 MHz)<br>8 (PCLKA > 60 MHz) | 65536 | $t_{Pcyc}$ | Figure 2.38 |
| | SCK clock cycle input (slave) | - | 6 (PCLKA ≤ 60 MHz)<br>12 (PCLKA > 60 MHz) | 65536 | | |
| | SCK clock high pulse width | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise and fall time | $t_{SPCKr}$, $t_{SPCKf}$ | - | 20 | ns | |
| | Data input setup time | $t_{SU}$ | 33.3 | - | ns | Figure 2.39 to Figure 2.42 |
| | Data input hold time | $t_{H}$ | 33.3 | - | ns | |
| | SS input setup time | $t_{LEAD}$ | 1 | - | $t_{SPcyc}$ | |
| | SS input hold time | $t_{LAG}$ | 1 | - | $t_{SPcyc}$ | |
| | Data output delay | $t_{OD}$ | - | 33.3 | ns | |
| | Data output hold time | $t_{OH}$ | -10 | - | ns | |
| | Data rise and fall time | $t_{Dr}$, $t_{Df}$ | - | 16.6 | ns | |
| | SS input rise and fall time | $t_{SSLr}$, $t_{SSLf}$ | - | 16.6 | ns | |
| | Slave access time | $t_{SA}$ | - | 4 (PCLKA ≤ 60 MHz)<br>8 (PCLKA > 60 MHz) | $t_{Pcyc}$ | Figure 2.42 |
| | Slave output release time | $t_{REL}$ | - | 5 (PCLKA ≤ 60 MHz)<br>10 (PCLKA > 60 MHz) | $t_{Pcyc}$ | |

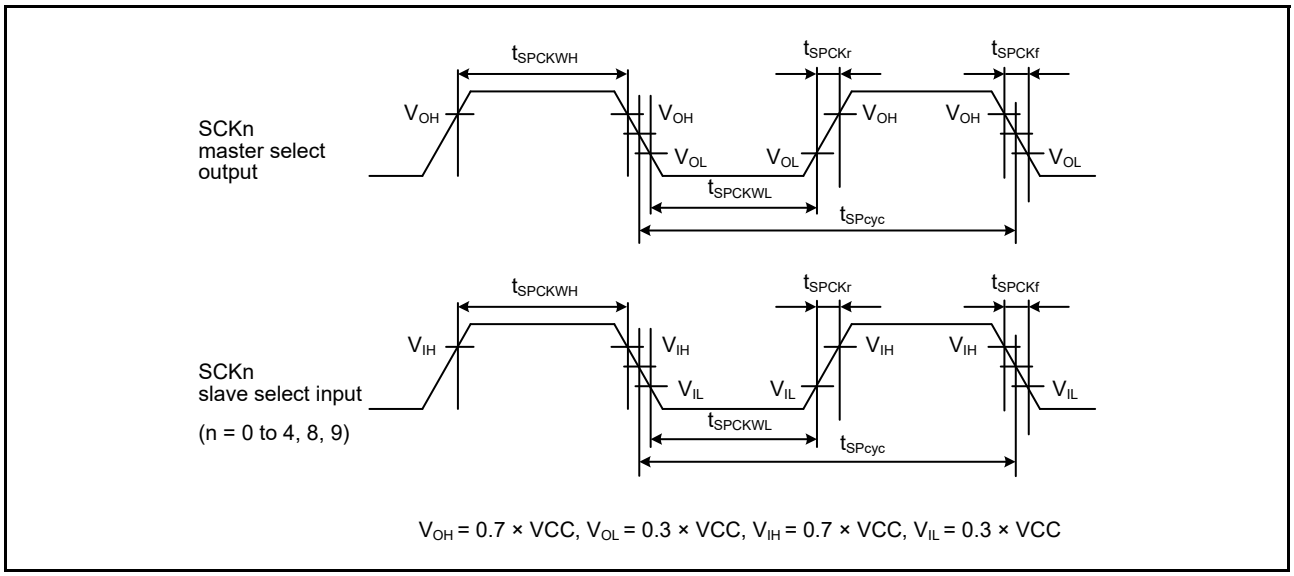



**Figure 2.38 SCI simple SPI mode clock timing**

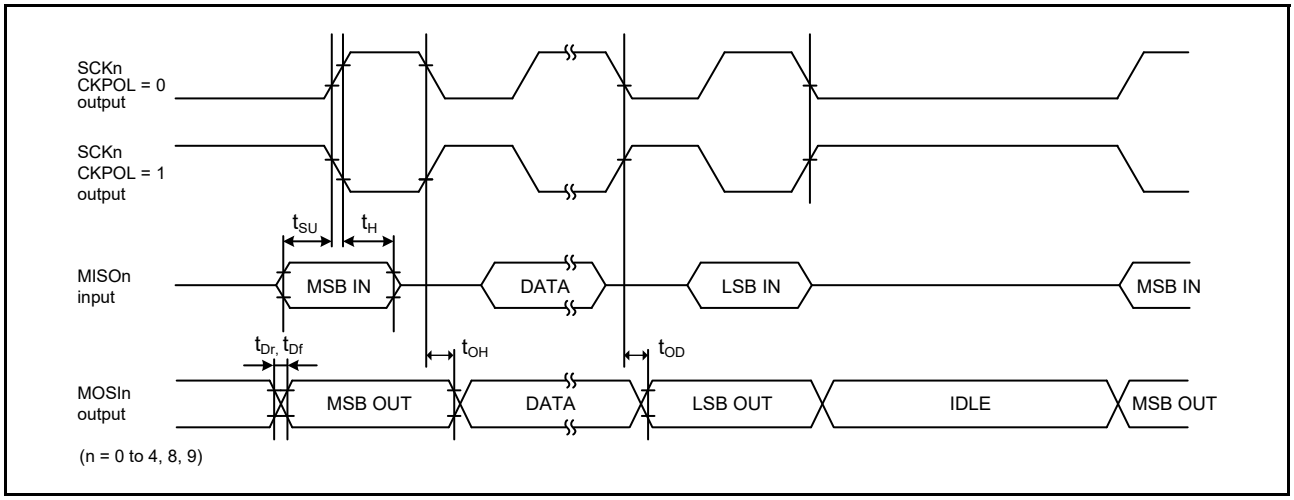



**Figure 2.39 SCI simple SPI mode timing for master when CKPH = 1**

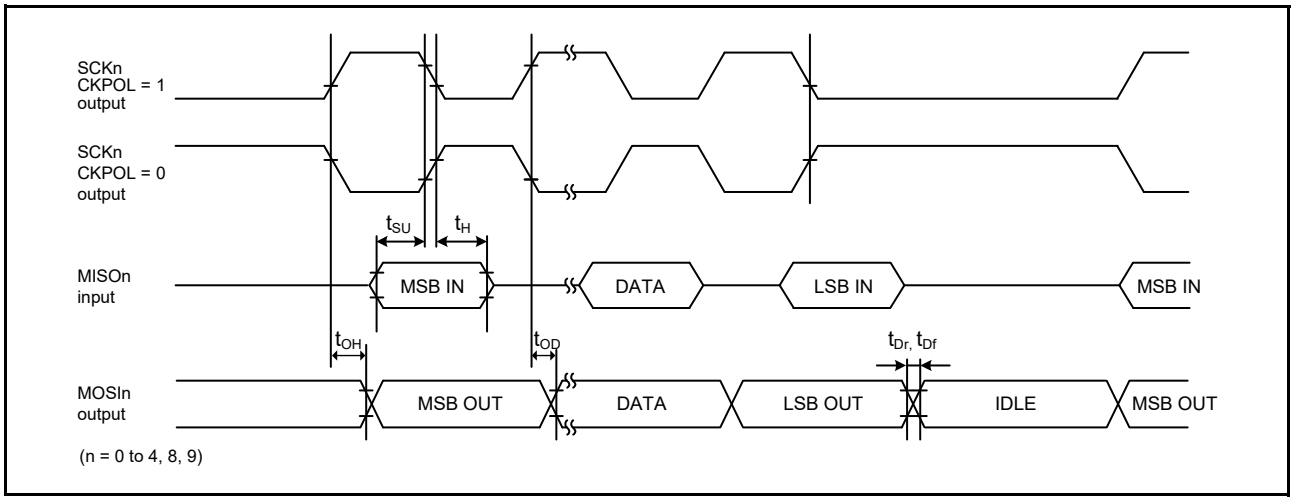



**Figure 2.40 SCI simple SPI mode timing for master when CKPH = 0**

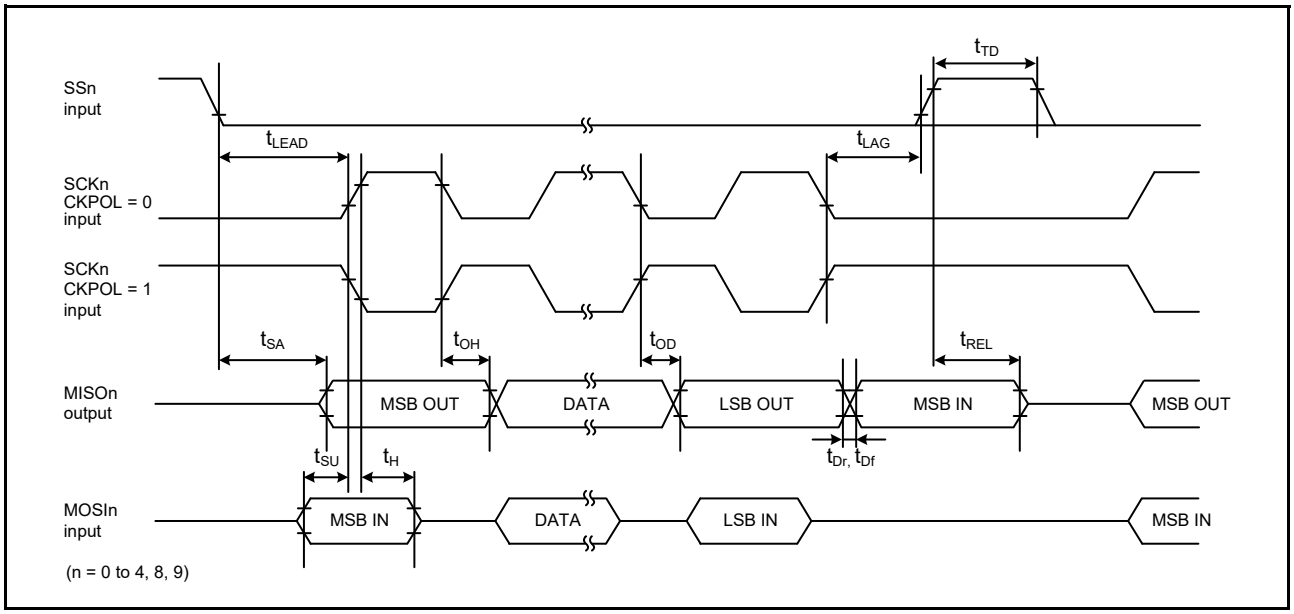



**Figure 2.41 SCI simple SPI mode timing for slave when CKPH = 1**

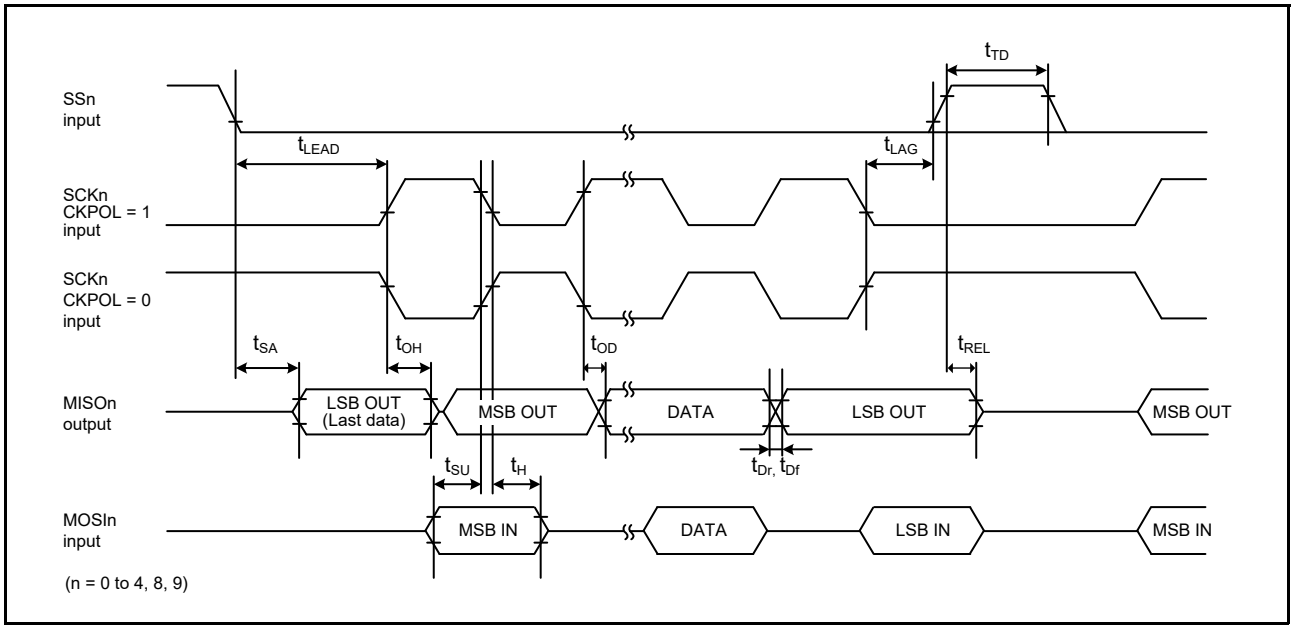



**Figure 2.42 SCI simple SPI mode timing for slave when CKPH = 0**

**Table 2.24 SCI timing (3) (1 of 2)**

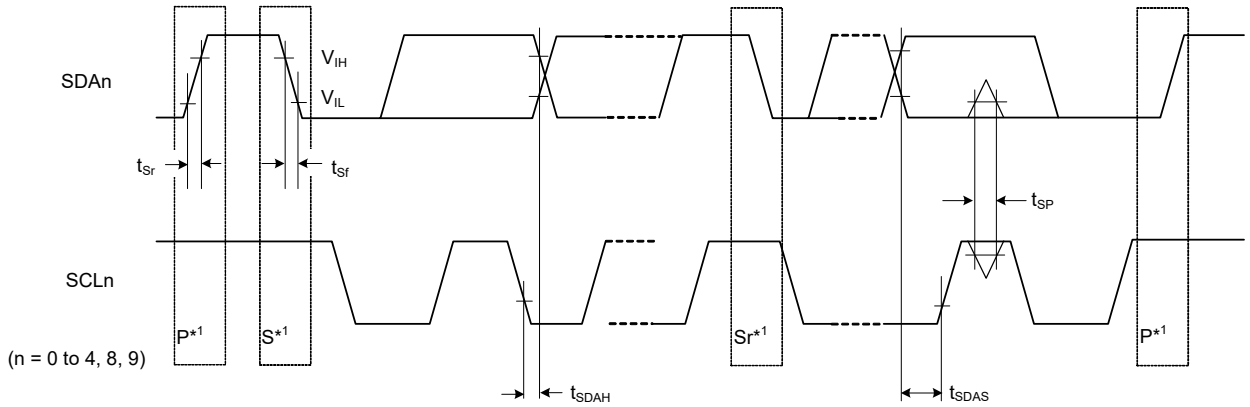
Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Simple IIC (Standard mode) | SDA input rise time | $t_{Sr}$ | - | 1000 | ns | Figure 2.43 |
| | SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 250 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$*1 | - | 400 | pF | |

**Table 2.24 SCI timing (3) (2 of 2)**
Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Simple IIC (Fast mode) | SDA input rise time | $t_{Sr}$ | - | 300 | ns | Figure 2.43 |
| | SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{IICcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 100 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$*1 | - | 400 | pF | |

Note: $t_{IICcyc}$: IIC internal reference clock (IICφ) cycle.
Note 1. Cb indicates the total capacity of the bus line.




Note 1. S, P, and Sr indicate the following:
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions:
$V_{IH}$ = VCC × 0.7, $V_{IL}$ = VCC × 0.3
$V_{OL}$ = 0.6 V, $I_{OL}$ = 6 mA

**Figure 2.43 SCI simple IIC mode timing**

## 2.3.11 SPI Timing

**Table 2.25 SPI timing**

Conditions:
For RSPCKA and RSPCKB pins, high drive output is selected with the Port Drive Capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | | Symbol | Min | Max | Unit*1 | Test conditions*2 |
|---|---|---|---|---|---|---|---|
| SPI | RSPCK clock cycle | Master | $t_{SPcyc}$ | 2 (PCLKA ≤ 60 MHz)<br>4 (PCLKA > 60 MHz) | 4096 | $t_{Pcyc}$ | Figure 2.44<br>C = 30 pF |
| | | Slave | | 4 | 4096 | | |
| | RSPCK clock high pulse width | Master | $t_{SPCKWH}$ | ($t_{SPcyc}$ - $t_{SPCKr}$ - $t_{SPCKf}$) / 2 - 3 | - | ns | |
| | | Slave | | 2 × $t_{Pcyc}$ | - | | |
| | RSPCK clock low pulse width | Master | $t_{SPCKWL}$ | ($t_{SPcyc}$ - $t_{SPCKr}$ - $t_{SPCKf}$) / 2 - 3 | - | ns | |
| | | Slave | | 2 × $t_{Pcyc}$ | - | | |
| | RSPCK clock rise and fall time | Master | $t_{SPCKr}$, $t_{SPCKf}$ | - | 5 | ns | |
| | | Slave | | - | 1 | μs | |
| | Data input setup time | Master | $t_{SU}$ | 4 | - | ns | Figure 2.45 to Figure 2.50<br>C = 30 pF |
| | | Slave | | 5 | - | | |
| | Data input hold time | Master (PCLKA division ratio set to 1/2) | $t_{HF}$ | 0 | - | ns | |
| | | Master (PCLKA division ratio set to a value other than 1/2) | $t_H$ | $t_{Pcyc}$ | - | | |
| | | Slave | $t_H$ | 20 | - | | |
| | SSL setup time | Master | $t_{LEAD}$ | N × $t_{SPcyc}$ - 10*3 | N × $t_{SPcyc}$ + 100*3 | ns | |
| | | Slave | | 6 x $t_{Pcyc}$ | - | ns | |
| | SSL hold time | Master | $t_{LAG}$ | N × $t_{SPcyc}$ - 10 *4 | N × $t_{SPcyc}$ + 100*4 | ns | |
| | | Slave | | 6 x $t_{Pcyc}$ | - | ns | |
| | Data output delay | Master | $t_{OD}$ | - | 6.3 | ns | |
| | | Slave | | - | 20 | | |
| | Data output hold time | Master | $t_{OH}$ | 0 | - | ns | |
| | | Slave | | 0 | - | | |
| | Successive transmission delay | Master | $t_{TD}$ | $t_{SPcyc}$ + 2 × $t_{Pcyc}$ | 8 × $t_{SPcyc}$ + 2 × $t_{Pcyc}$ | ns | |
| | | Slave | | 6 × $t_{Pcyc}$ | | | |
| | MOSI and MISO rise and fall time | Output | $t_{Dr}$, $t_{Df}$ | - | 5 | ns | |
| | | Input | | - | 1 | μs | |
| | SSL rise and fall time | Output | $t_{SSLr}$, $t_{SSLf}$ | - | 5 | ns | |
| | | Input | | - | 1 | μs | |
| | Slave access time | | $t_{SA}$ | - | 2 x $t_{Pcyc}$ + 28 | ns | Figure 2.49 and Figure 2.50<br>C = 30pF |
| | Slave output release time | | $t_{REL}$ | - | 2 x $t_{Pcyc}$ + 28 | | |

Note 1. $t_{Pcyc}$: PCLKA cycle.

Note 2. Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. N is set to an integer from 1 to 8 by the SPCKD register.
Note 4. N is set to an integer from 1 to 8 by the SSLND register.

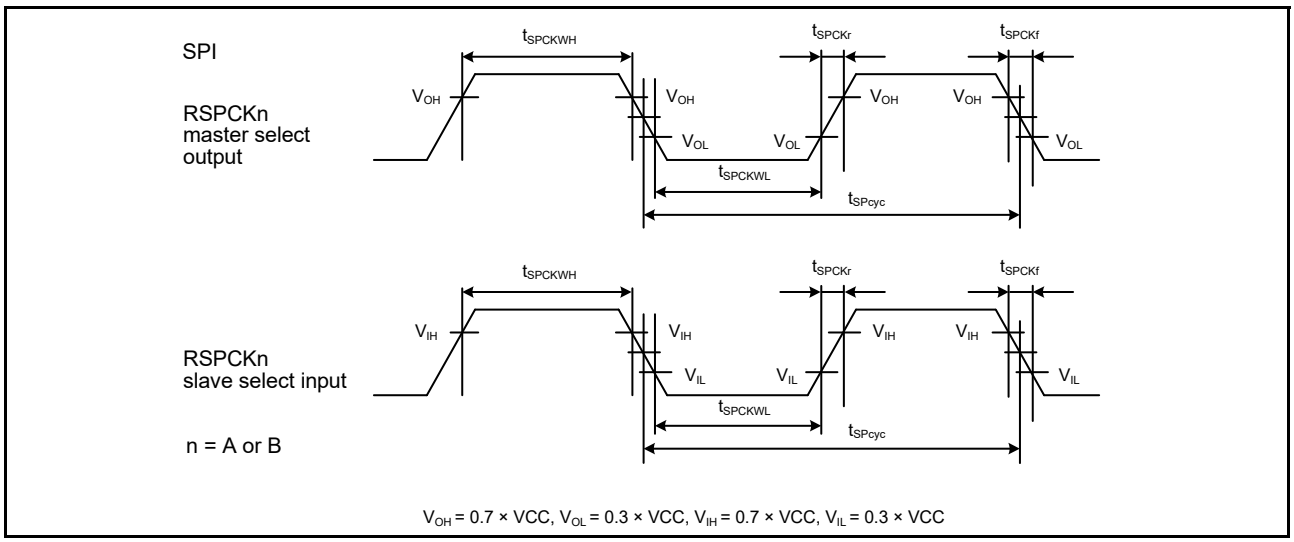



**Figure 2.44 SPI clock timing**

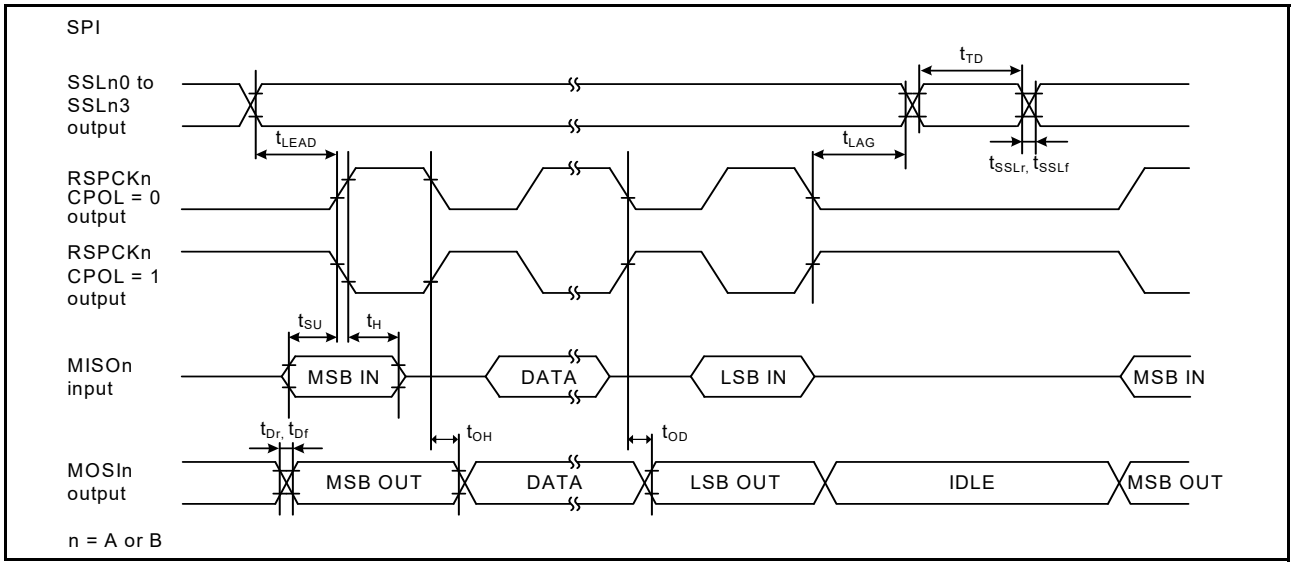



**Figure 2.45 SPI timing for master when CPHA = 0**

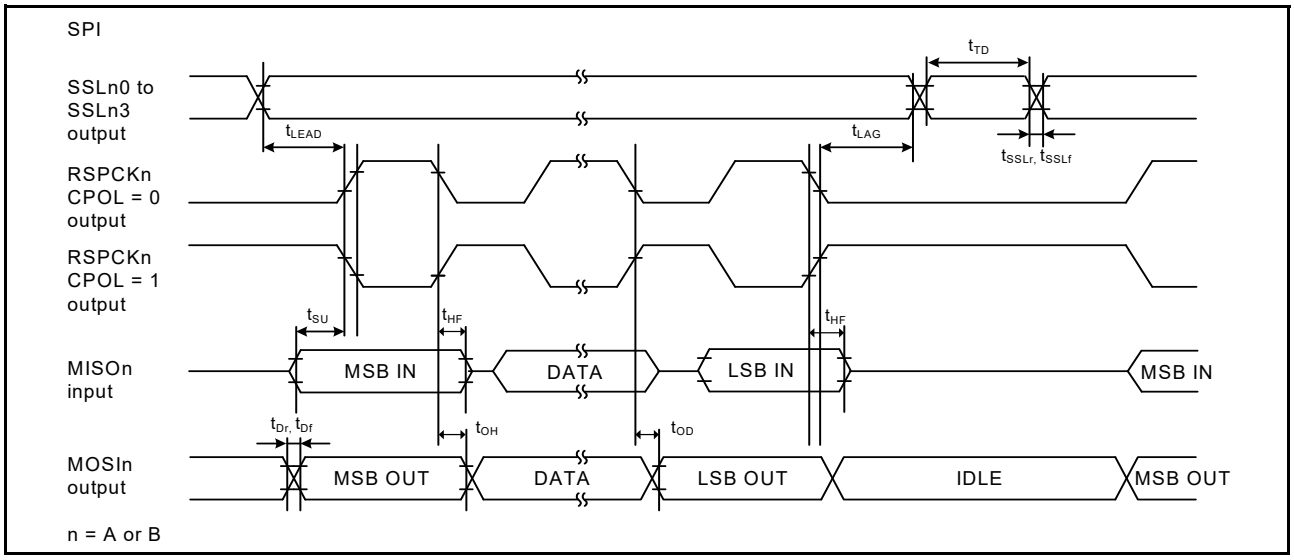



**Figure 2.46 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2**

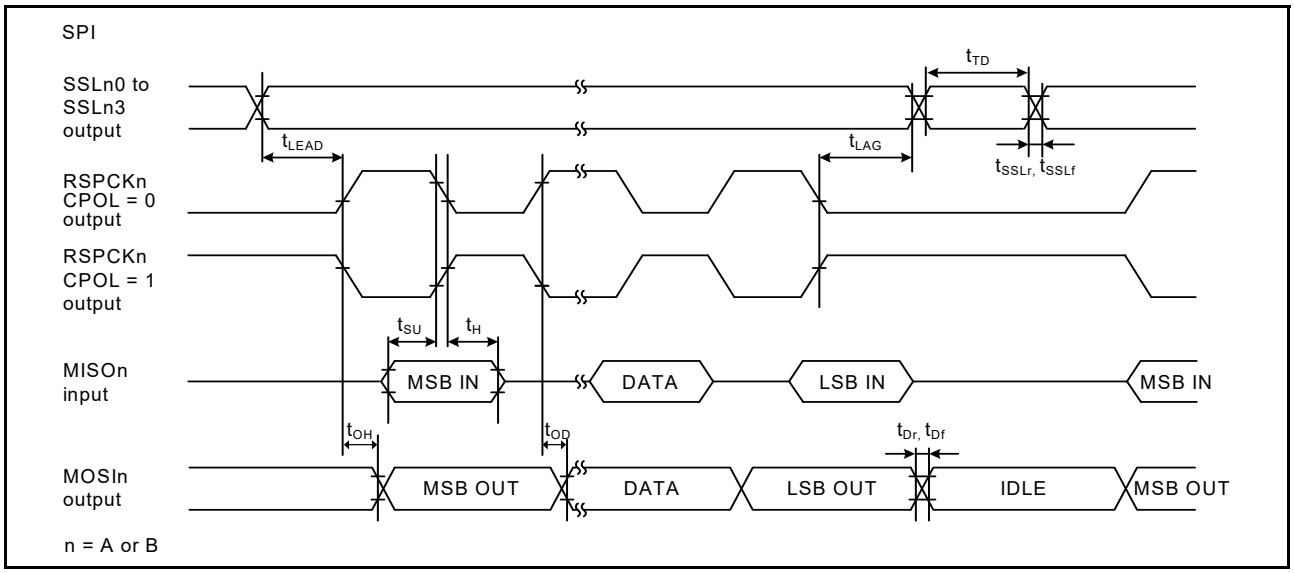



**Figure 2.47 SPI timing for master when CPHA = 1**

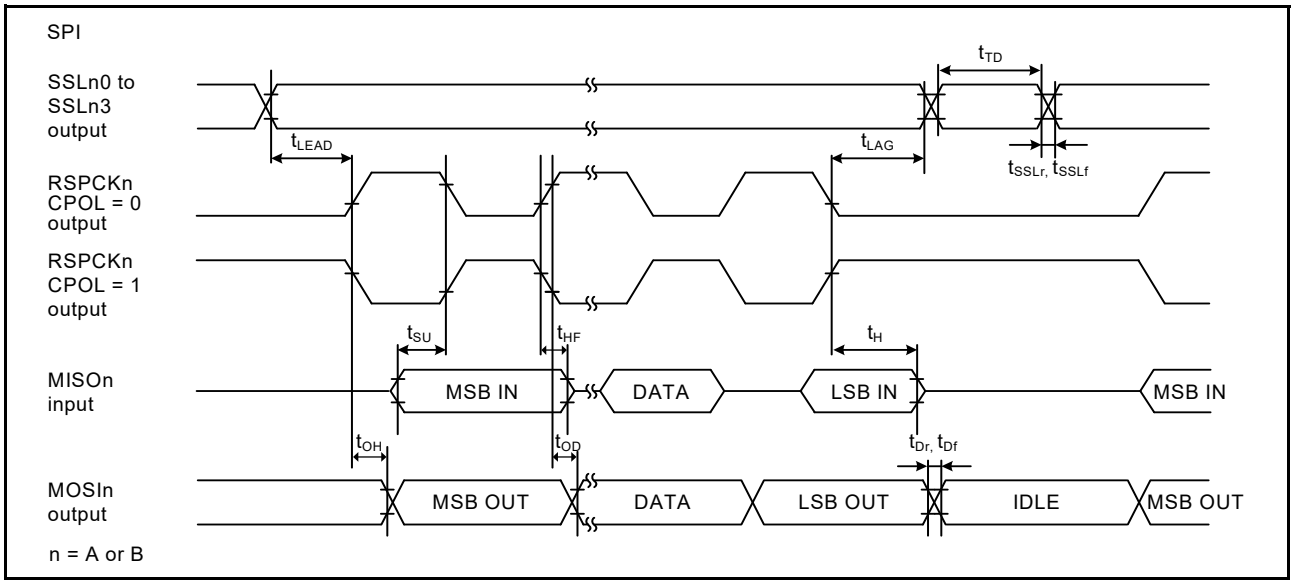



**Figure 2.48 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2**

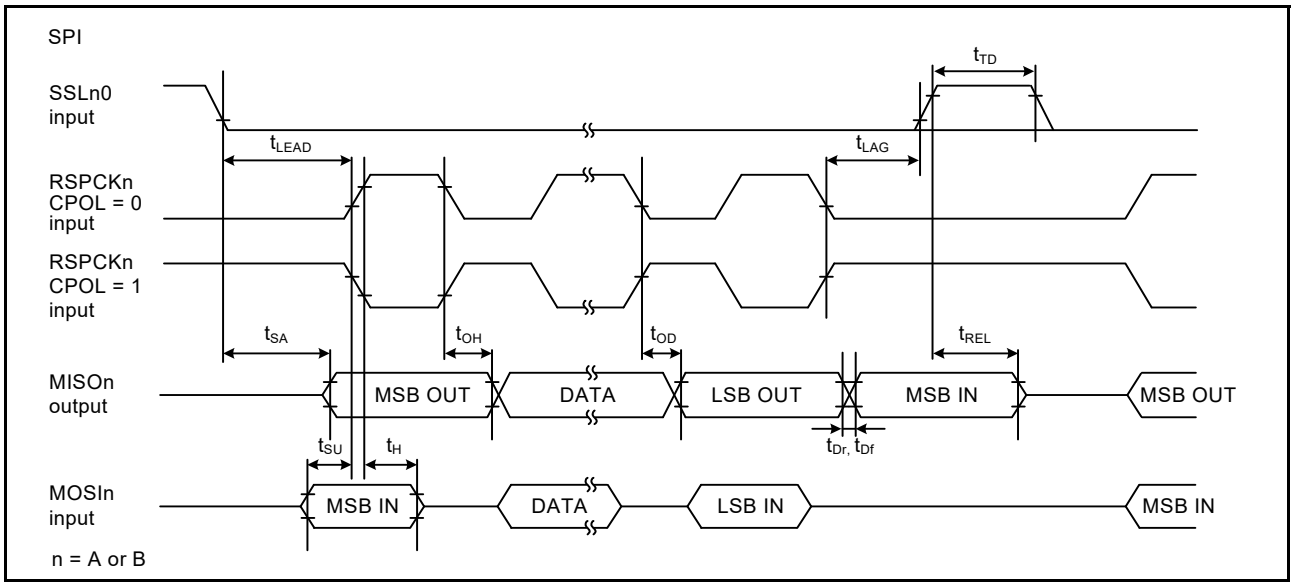



**Figure 2.49 SPI timing for slave when CPHA = 0**

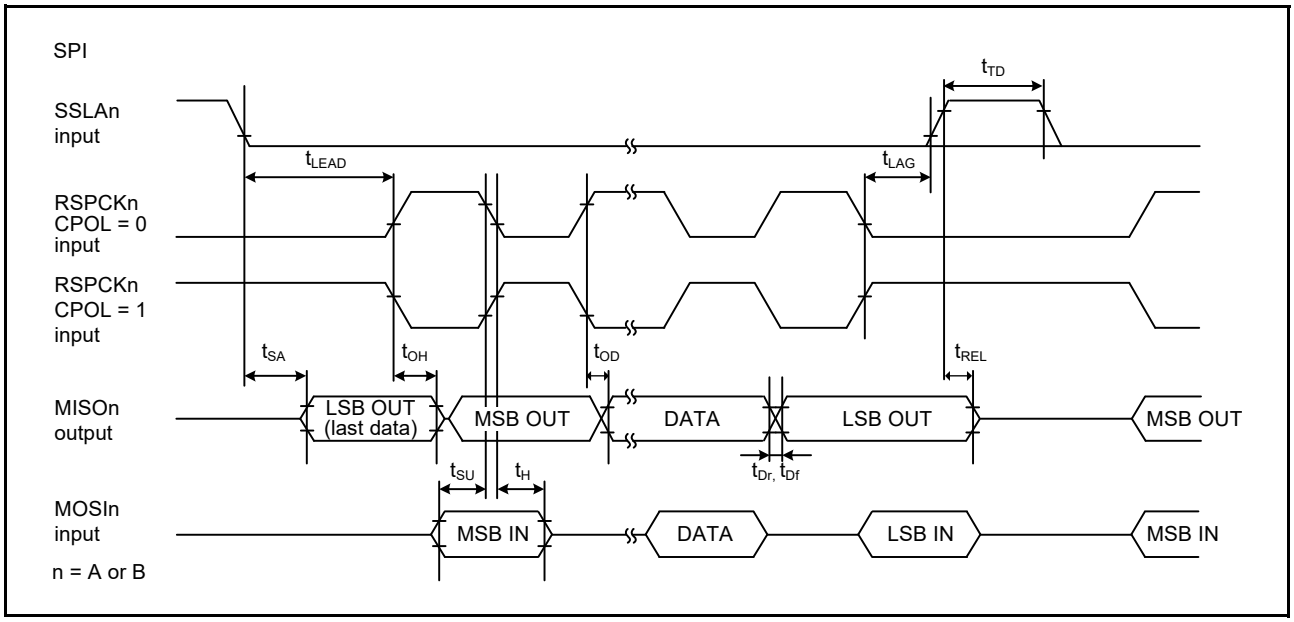



**Figure 2.50 SPI timing for slave when CPHA = 1**

## 2.3.12 QSPI Timing

**Table 2.26 QSPI timing**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min | Max | Unit*1 | Test conditions |
|---|---|---|---|---|---|---|
| QSPI | QSPCK clock cycle | $t_{QScyc}$ | 2 | 48 | $t_{Pcyc}$ | Figure 2.51 |
| | QSPCK clock high pulse width | $t_{QSWH}$ | $t_{QScyc}$ × 0.4 | - | ns | |
| | QSPCK clock low pulse width | $t_{QSWL}$ | $t_{QScyc}$ × 0.4 | - | ns | |
| | Data input setup time | $t_{Su}$ | 8 | - | ns | Figure 2.52 |
| | Data input hold time | $t_{IH}$ | 0 | - | ns | |
| | QSSL setup time | $t_{LEAD}$ | (N+0.5) x $t_{Qscyc}$ - 5 *2 | (N+0.5) x $t_{Qscyc}$ +100 *2 | ns | |
| | QSSL hold time | $t_{LAG}$ | (N+0.5) x $t_{Qscyc}$ - 5 *3 | (N+0.5) x $t_{Qscyc}$ +100 *3 | ns | |
| | Data output delay | $t_{OD}$ | - | 4 | ns | |
| | Data output hold time | $t_{OH}$ | -3.3 | - | ns | |
| | Successive transmission delay | $t_{TD}$ | 1 | 16 | $t_{QScyc}$ | |

Note 1. $t_{Pcyc}$: PCLKA cycle.
Note 2. N is set to 0 or 1 in SFMSLD.
Note 3. N is set to 0 or 1 in SFMSHD.

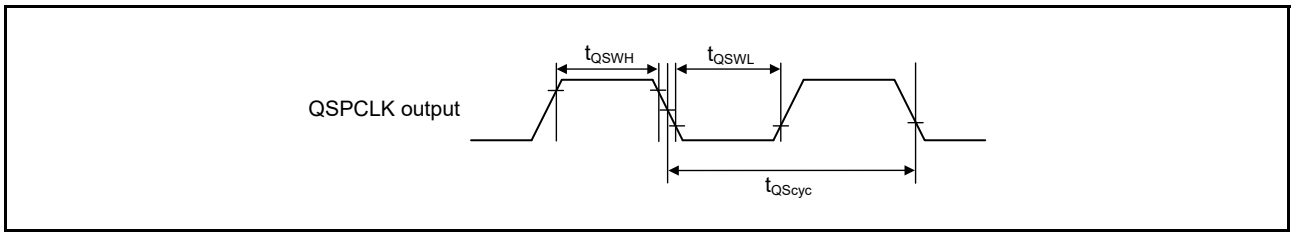



**Figure 2.51 QSPI clock timing**

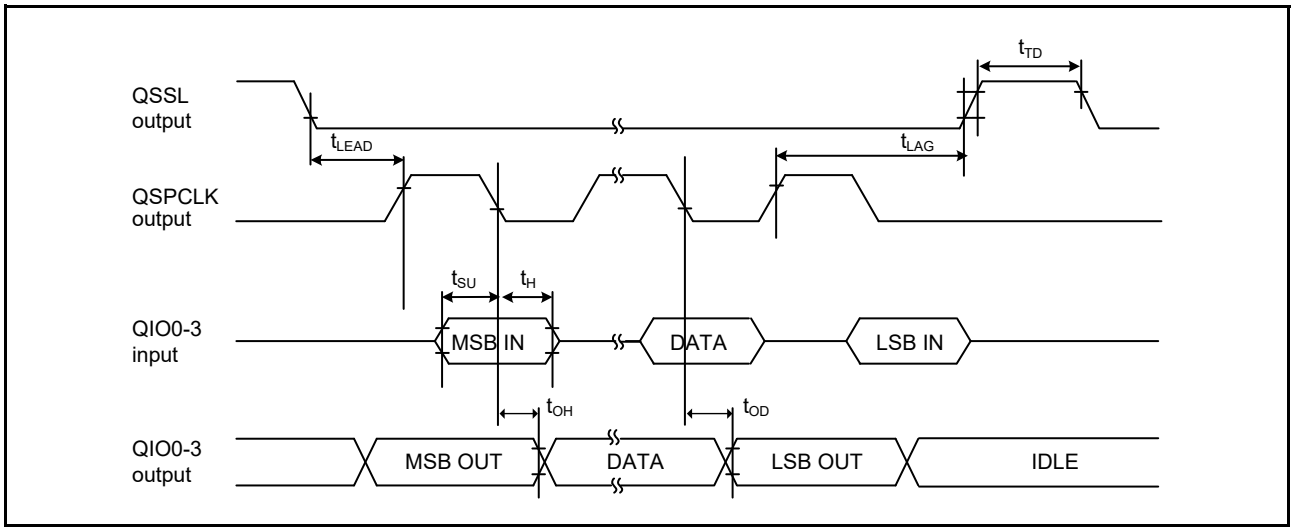



**Figure 2.52 Transmit and receive timing**

## 2.3.13 IIC Timing

**Table 2.27 IIC timing (1) (1 of 2)**

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter | | Symbol | Min*1 | Max | Unit | Test conditions*3 |
|---|---|---|---|---|---|---|
| IIC (Standard mode, SMBus) ICFER.FMPE = 0 | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 1300 | - | ns | Figure 2.53 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | - | 1000 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | - | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SDA input bus free time when wakeup function is enabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 4 × $t_{Pcyc}$ + 300 | - | ns | |
| | START condition input hold time when wakeup function is disabled | $t_{STAH}$ | $t_{IICcyc}$ + 300 | - | ns | |
| | START condition input hold time when wakeup function is enabled | $t_{STAH}$ | 1 (5) × $t_{IICcyc}$ + $t_{Pcyc}$ + 300 | - | ns | |
| | Repeated START condition input setup time | $t_{STAS}$ | 1000 | - | ns | |
| | STOP condition input setup time | $t_{STOS}$ | 1000 | - | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$ | - | 400 | pF | |

**Table 2.27 IIC timing (1) (2 of 2)**

(1) Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

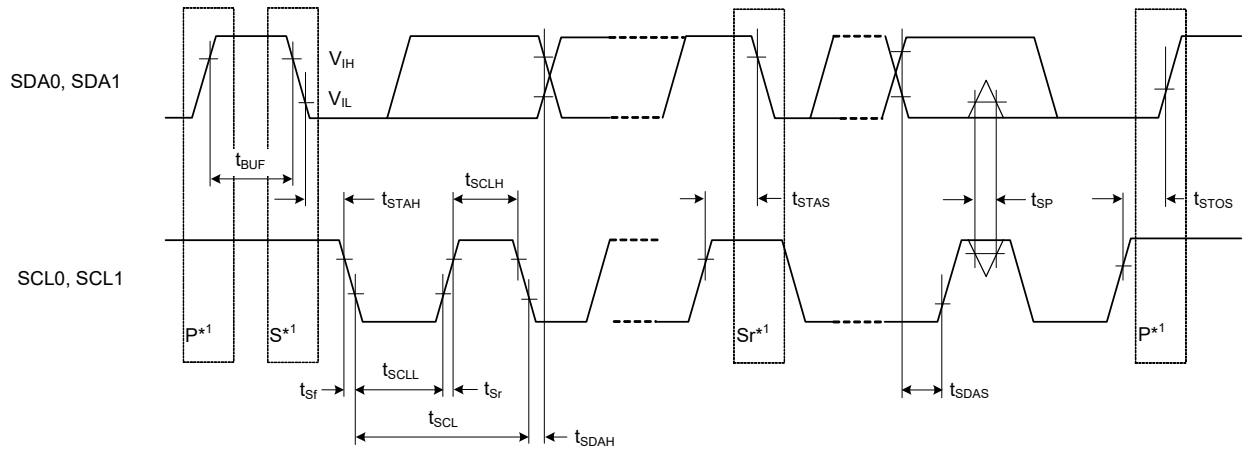
| Parameter | | Symbol | Min*1 | Max | Unit | Test conditions*3 |
|---|---|---|---|---|---|---|
| IIC (Fast mode) | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 600 | - | ns | Figure 2.53 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | 20 × (external pullup voltage/5.5V)*2 | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | 20 × (external pullup voltage/5.5V)*2 | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SDA input bus free time when wakeup function is enabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 4 × $t_{Pcyc}$ + 300 | - | ns | |
| | START condition input hold time when wakeup function is disabled | $t_{STAH}$ | $t_{IICcyc}$ + 300 | - | ns | |
| | START condition input hold time when wakeup function is enabled | $t_{STAH}$ | 1 (5) × $t_{IICcyc}$ + $t_{Pcyc}$ + 300 | - | ns | |
| | Repeated START condition input setup time | $t_{STAS}$ | 300 | - | ns | |
| | STOP condition input setup time | $t_{STOS}$ | 300 | - | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$ | - | 400 | pF | |

Note: $t_{IICcyc}$: IIC internal reference clock (IICφ) cycle, $t_{Pcyc}$: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Only supported for SCL0_A, SDA0_A.
Note 3. Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

**Table 2.28 IIC timing (2)**
Setting of the SCL0_A, SDA0_A pins is not required with the Port Drive Capability bit in the PmnPFS register.

| Parameter | | Symbol | Min*1,*2 | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| IIC (Fast mode+) ICFER.FMPE = 1 | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 240 | - | ns | Figure 2.53 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 120 | - | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 120 | - | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | - | 120 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | - | 120 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 120 | - | ns | |
| | SDA input bus free time when wakeup function is enabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 4 × $t_{Pcyc}$ + 120 | - | ns | |
| | Start condition input hold time when wakeup function is disabled | $t_{STAH}$ | $t_{IICcyc}$ + 120 | - | ns | |
| | START condition input hold time when wakeup function is enabled | $t_{STAH}$ | 1 (5) × $t_{IICcyc}$ + $t_{Pcyc}$ + 120 | - | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 120 | - | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 120 | - | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 30 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$ | - | 550 | pF | |

Note: $t_{IICcyc}$: IIC internal reference clock (IICφ) cycle, $t_{Pcyc}$: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Cb indicates the total capacity of the bus line.




Note 1. S, P, and Sr indicate the following:
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions:
$V_{IH}$ = VCC × 0.7, $V_{IL}$ = VCC × 0.3
$V_{OL}$ = 0.6 V, $I_{OL}$ = 6 mA (ICFER.FMPE = 0)
$V_{OL}$ = 0.4 V, $I_{OL}$ = 15 mA (ICFER.FMPE = 1)

**Figure 2.53 I²C bus interface input/output timing**

## 2.3.14 SSIE Timing

**Table 2.29 SSIE timing**

(1) High drive output is selected with the Port Drive Capability bit in the PmnPFS register.

(2) Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

| Parameter | | | Symbol | Target specification Min. | Target specification Max. | Unit | Comments |
|---|---|---|---|---|---|---|---|
| SSIBCK0 | Cycle | Master | $t_O$ | 80 | - | ns | Figure 2.54 |
| | | Slave | $t_I$ | 80 | - | ns | |
| | High level/low level | Master | $t_{HC}/t_{LC}$ | 0.35 | - | $t_O$ | |
| | | Slave | | 0.35 | - | $t_I$ | |
| | Rising time/falling time | Master | $t_{RC}/t_{FC}$ | - | 0.15 | $t_O$ / $t_I$ | |
| | | Slave | | - | 0.15 | $t_O$ / $t_I$ | |
| SSILRCK0/SSIFS0, SSITXD0, SSIRXD0 | Input set up time | Master | $t_{SR}$ | 12 | - | ns | Figure 2.56, Figure 2.57 |
| | | Slave | | 12 | - | ns | |
| | Input hold time | Master | $t_{HR}$ | 8 | - | ns | |
| | | Slave | | 15 | - | ns | |
| | Output delay time | Master | $t_{DTR}$ | -10 | 5 | ns | |
| | | Slave | | 0 | 20 | ns | Figure 2.56, Figure 2.57 |
| | Output delay time from SSILRCK0/SSIFS0 change | Slave | $t_{DTRW}$ | - | 20 | ns | Figure 2.58*1 |
| GTIOC1A, AUDIO_CLK | Cycle | | $t_{EXcyc}$ | 20 | - | ns | Figure 2.55 |
| | High level/low level | | $t_{EXL}$/ $t_{EXH}$ | 0.4 | 0.6 | $t_{EXcyc}$ | |

Note 1. For slave-mode transmission, SSIE has a path through which the signal input from the SSILRCK0/SSIFS0 pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 pin.

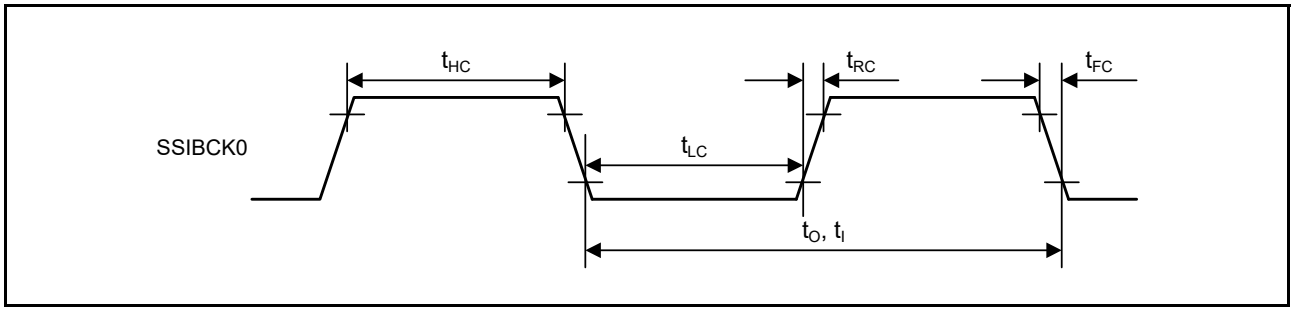



**Figure 2.54 SSIE clock input/output timing**

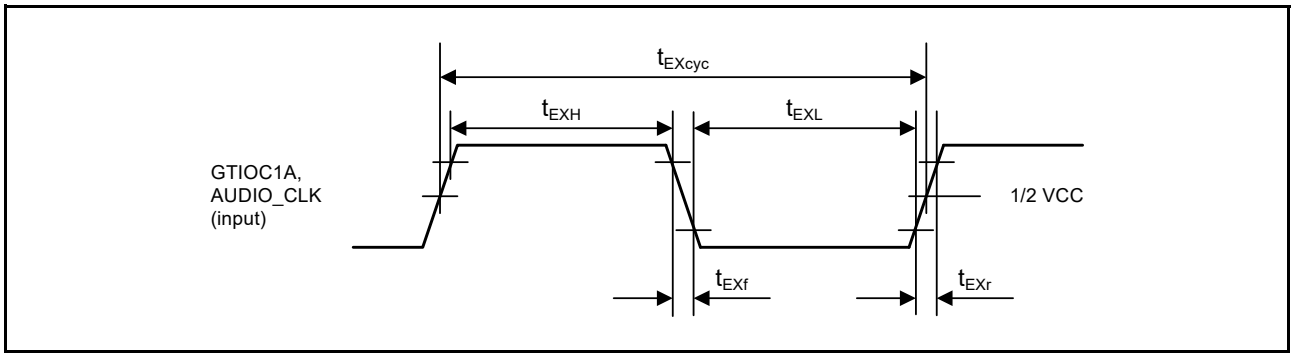



**Figure 2.55 Clock input timing**

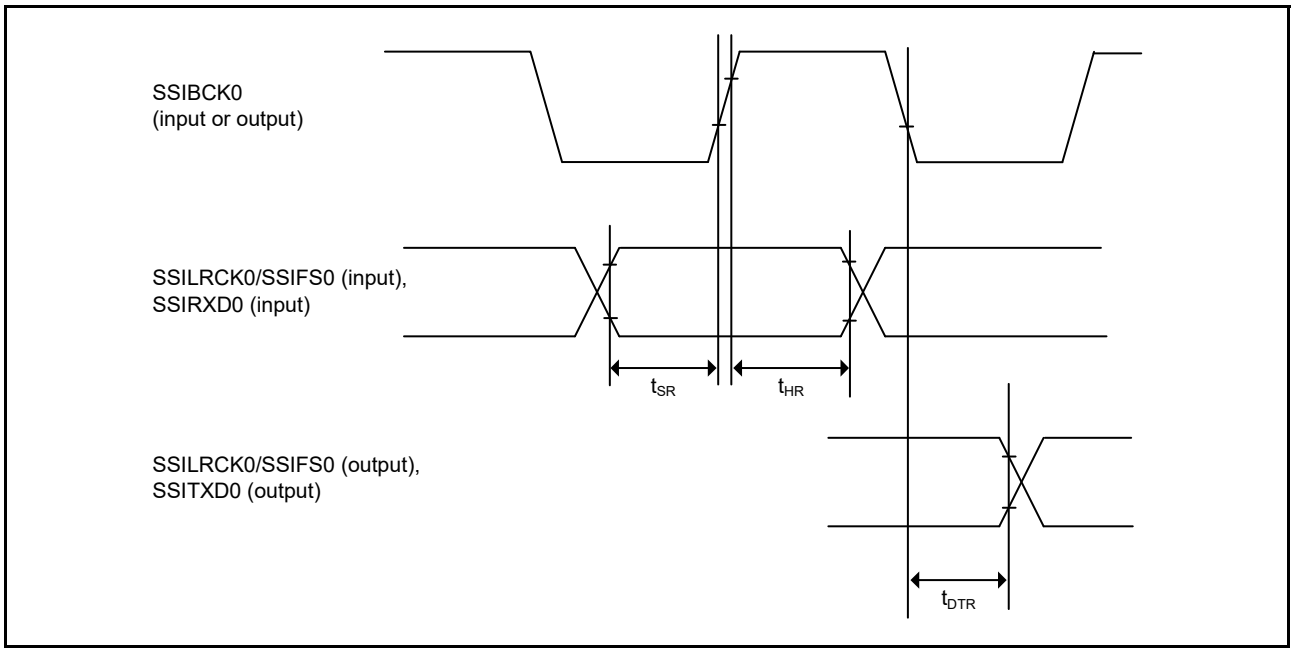



**Figure 2.56 SSIE data transmit and receive timing when SSICR.BCKP = 0**

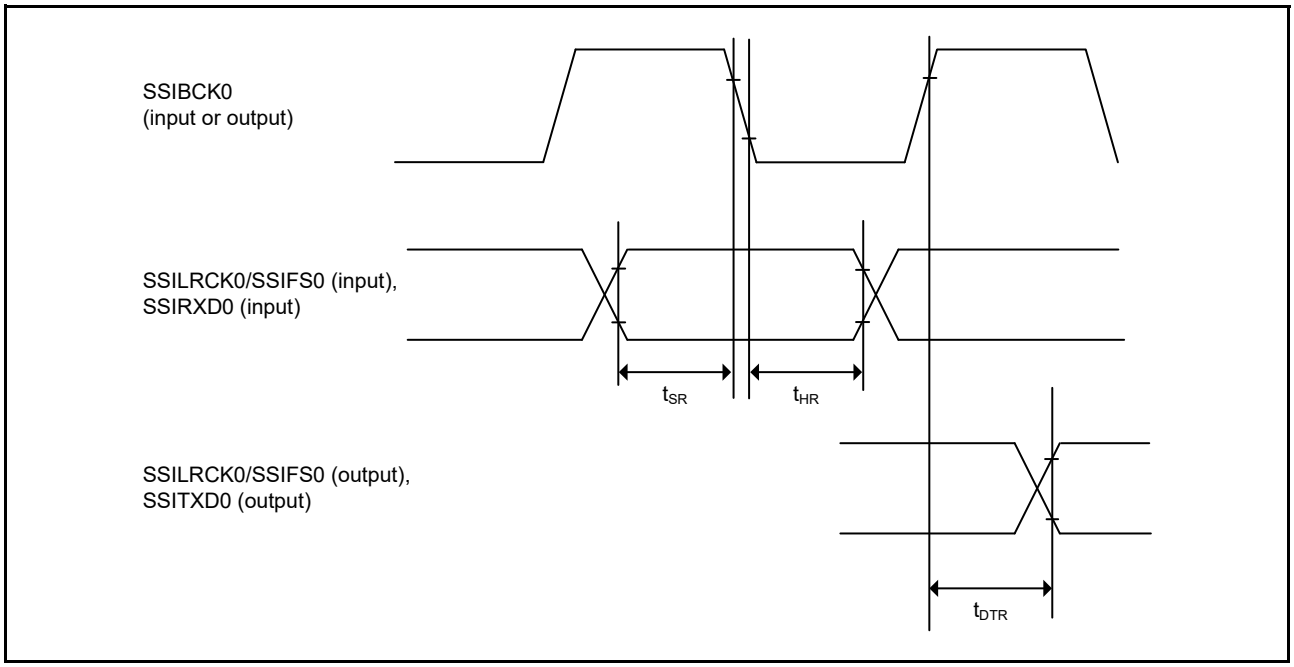



**Figure 2.57 SSIE data transmit and receive timing when SSICR.BCKP = 1**

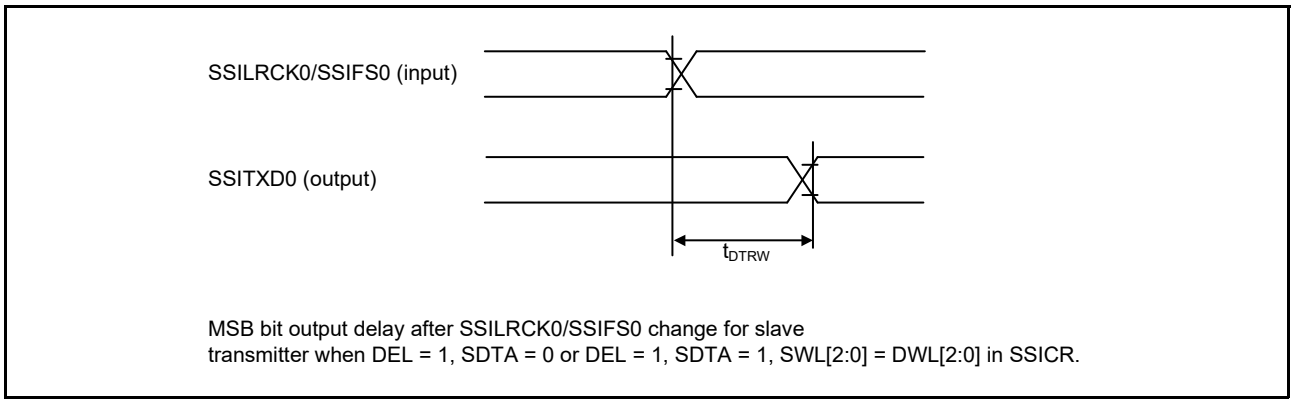



**Figure 2.58 SSIE data output delay after SSILRCK0/SSIFS0 change**

### 2.3.15 SD/MMC Host Interface Timing

**Table 2.30 SD/MMC Host Interface signal timing**

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
Clock duty ratio is 50%.

| Parameter | Symbol | Min | Max | Unit | Test conditions*1 |
|---|---|---|---|---|---|
| SDnCLK clock cycle | $T_{SDCYC}$ | 20 | - | ns | Figure 2.59 |
| SDnCLK clock high pulse width | $T_{SDWH}$ | 6.5 | - | ns | |
| SDnCLK clock low pulse width | $T_{SDWL}$ | 6.5 | - | ns | |
| SDnCLK clock rise time | $T_{SDLH}$ | - | 3 | ns | |
| SDnCLK clock fall time | $T_{SDHL}$ | - | 3 | ns | |
| SDnCMD/SDnDATm output data delay | $T_{SDODLY}$ | -6 | 5 | ns | |
| SDnCMD/SDnDATm input data setup | $T_{SDIS}$ | 4 | - | ns | |
| SDnCMD/SDnDATm input data hold | $T_{SDIH}$ | 2 | - | ns | |

Note 1. Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the SD/MMC Host interface, the AC portion of the electrical characteristics is measured for each group.

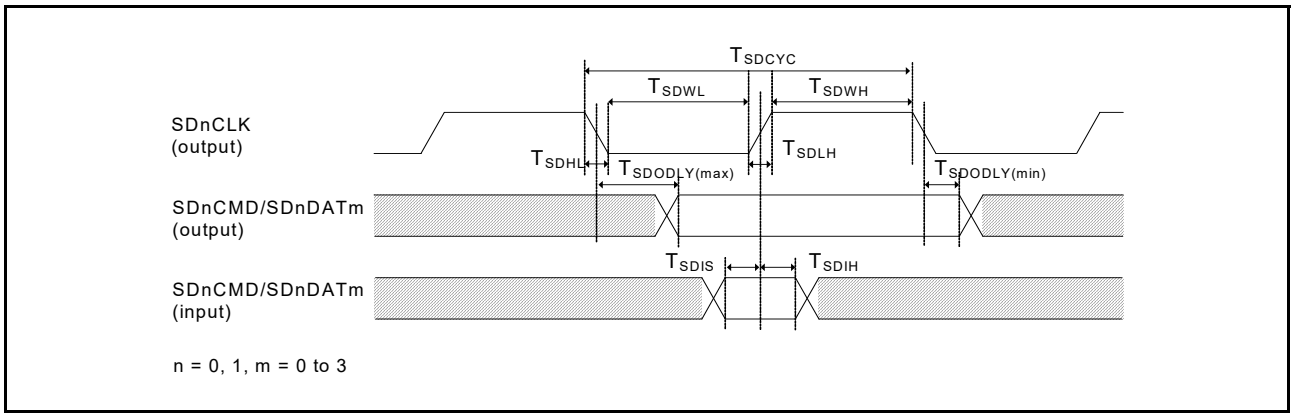



**Figure 2.59 SD/MMC Host Interface signal timing**

## 2.4 USB Characteristics

### 2.4.1 USBFS Timing

**Table 2.31 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics)**
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, UCLK = 48 MHz

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high voltage | $V_{IH}$ | 2.0 | - | - | V | - |
| | Input low voltage | $V_{IL}$ | - | - | 0.8 | V | - |
| | Differential input sensitivity | $V_{DI}$ | 0.2 | - | - | V | \| USB_DP - USB_DM \| |
| | Differential common-mode range | $V_{CM}$ | 0.8 | - | 2.5 | V | - |
| Output characteristics | Output high voltage | $V_{OH}$ | 2.8 | - | 3.6 | V | $I_{OH}$ = -200 μA |
| | Output low voltage | $V_{OL}$ | 0.0 | - | 0.3 | V | $I_{OL}$= 2 mA |
| | Cross-over voltage | $V_{CRS}$ | 1.3 | - | 2.0 | V | Figure 2.60 |
| | Rise time | $t_{LR}$ | 75 | - | 300 | ns | |
| | Fall time | $t_{LF}$ | 75 | - | 300 | ns | |
| | Rise/fall time ratio | $t_{LR}$ / $t_{LF}$ | 80 | - | 125 | % | $t_{LR}$/ $t_{LF}$ |
| Pull-up and pull-down characteristics | USB_DP and USB_DM pull-down resistance in host controller mode | $R_{pd}$ | 14.25 | - | 24.80 | kΩ | - |

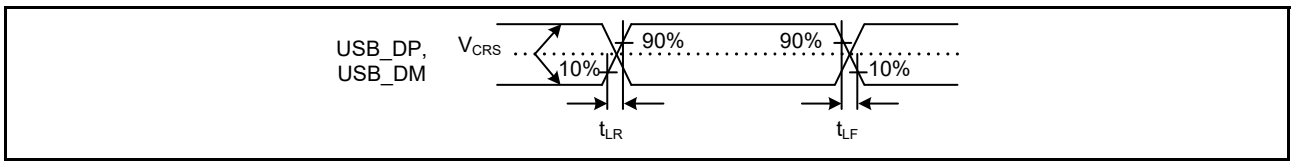



**Figure 2.60 USB_DP and USB_DM output timing in low-speed mode**

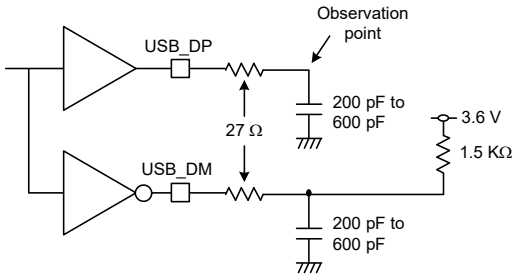



**Figure 2.61 Test circuit in low-speed mode**

**Table 2.32 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)**
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, UCLK = 48 MHz

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high voltage | $V_{IH}$ | 2.0 | - | - | V | - |
| | Input low voltage | $V_{IL}$ | - | - | 0.8 | V | - |
| | Differential input sensitivity | $V_{DI}$ | 0.2 | - | - | V | \| USB_DP - USB_DM \| |
| | Differential common-mode range | $V_{CM}$ | 0.8 | - | 2.5 | V | - |
| Output characteristics | Output high voltage | $V_{OH}$ | 2.8 | - | 3.6 | V | $I_{OH}$ = -200 μA |
| | Output low voltage | $V_{OL}$ | 0.0 | - | 0.3 | V | $I_{OL}$= 2 mA |
| | Cross-over voltage | $V_{CRS}$ | 1.3 | - | 2.0 | V | Figure 2.62 |
| | Rise time | $t_{LR}$ | 4 | - | 20 | ns | |
| | Fall time | $t_{LF}$ | 4 | - | 20 | ns | |
| | Rise/fall time ratio | $t_{LR}$ / $t_{LF}$ | 90 | - | 111.11 | % | $t_{FR}$/ $t_{FF}$ |
| | Output resistance | $Z_{DRV}$ | 28 | - | 44 | Ω | USBFS: Rs = 27 Ω included |
| Pull-up and pull-down characteristics | DM pull-up resistance in device controller mode | $R_{pu}$ | 0.900 | - | 1.575 | kΩ | During idle state |
| | | | 1.425 | - | 3.090 | kΩ | During transmission and reception |
| | USB_DP and USB_DM pull-down resistance in host controller mode | $R_{pd}$ | 14.25 | - | 24.80 | kΩ | - |

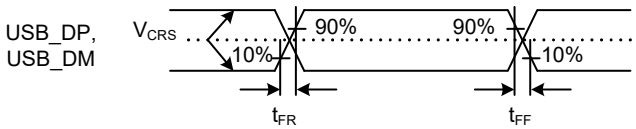



**Figure 2.62 USB_DP and USB_DM output timing in full-speed mode**

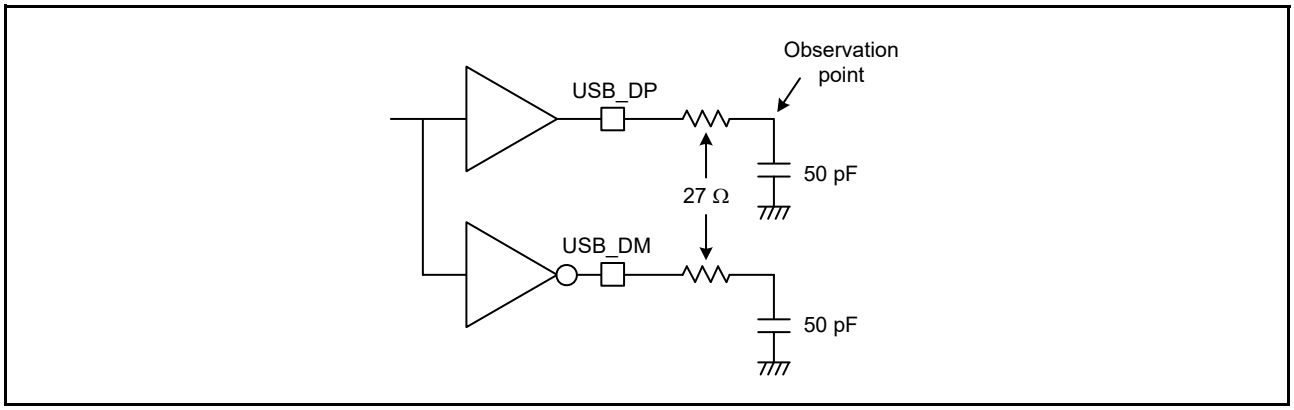



**Figure 2.63 Test circuit in full-speed mode**

## 2.5 ADC12 Characteristics

**Table 2.33 A/D conversion characteristics for unit 0 (1 of 2)**
Conditions: PCLKC = 1 to 60 MHz

| Parameter | | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Frequency | | | 1 | - | 60 | MHz | - |
| Analog input capacitance | | | - | - | 30 | pF | - |
| Quantization error | | | - | ±0.5 | - | LSB | - |
| Resolution | | | - | - | 12 | Bits | - |
| Channel-dedicated sample-and-hold circuits in use*3 (AN000 to AN002) | Conversion time*1 (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 1.06 (0.4 + 0.25)*2 | - | - | μs | • Sampling of channel-dedicated sample-and-hold circuits in 24 states<br>• Sampling in 15 states |
| | Offset error | | - | ±1.5 | ±3.5 | LSB | AN000 to AN002 = 0.25 V |
| | Full-scale error | | - | ±1.5 | ±3.5 | LSB | AN000 to AN002 = VREFH0- 0.25 V |
| | Absolute accuracy | | - | ±2.5 | ±5.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±1.0 | ±2.0 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.5 | ±3.0 | LSB | - |
| | Holding characteristics of sample-and hold circuits | | - | - | 20 | μs | - |
| | Dynamic range | | 0.25 | - | VREFH0 - 0.25 | V | - |
| Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002) | Conversion time*1 (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.48 (0.267)*2 | - | - | μs | Sampling in 16 states |
| | Offset error | | - | ±1.0 | ±2.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±2.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±4.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±1.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±2.5 | LSB | - |
| High-precision channels (AN003, AN005, AN006) | Conversion time*1 (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.48 (0.267)*2 | - | - | μs | Sampling in 16 states |
| | | Max. = 400 Ω | 0.40 (0.183)*2 | - | - | μs | Sampling in 11 states<br>VCC = AVCC0 = 3.0 to 3.6 V<br>3.0 V ≤ VREFH0 ≤ AVCC0 |
| | Offset error | | - | ±1.0 | ±2.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±2.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±4.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±1.5 | LSB | - |

**Table 2.33 A/D conversion characteristics for unit 0 (2 of 2)**
Conditions: PCLKC = 1 to 60 MHz

| Parameter | | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| High-precision channels (AN003, AN005, AN006) | INL integral nonlinearity error | | - | ±1.0 | ±2.5 | LSB | - |
| High-precision channels (AN007) | Conversion time*1 (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.75 (0.533)*2 | - | - | μs | Sampling in 32 states |
| | Offset error | | - | ±1.0 | ±2.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±2.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±4.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±1.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±2.5 | LSB | - |
| Normal-precision channels (AN016 to AN018, AN020) | Conversion time*1 (Operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.88 (0.667)*2 | - | - | μs | Sampling in 40 states |
| | Offset error | | - | ±1.0 | ±5.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±5.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±7.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±4.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±5.5 | LSB | - |

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, the values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Note 3. When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, see Table 2.35.

**Table 2.34 A/D conversion characteristics for unit 1 (1 of 2)**
Conditions: PCLKC = 1 to 60 MHz

| Parameter | | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Frequency | | | 1 | - | 60 | MHz | - |
| Analog input capacitance | | | - | - | 30 | pF | - |
| Quantization error | | | - | ±0.5 | - | LSB | - |
| Resolution | | | - | - | 12 | Bits | - |
| Channel-dedicated sample-and-hold circuits in use*3 (AN100 to AN102) | Conversion time*1 (operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 1.06 (0.4 + 0.25)*2 | - | - | μs | • Sampling of channel-dedicated sample-and-hold circuits in 24 states<br>• Sampling in 15 states |
| | Offset error | | - | ±1.5 | ±3.5 | LSB | AN100 to AN102 = 0.25 V |
| | Full-scale error | | - | ±1.5 | ±3.5 | LSB | AN100 to AN102 = VREFH - 0.25 V |
| | Absolute accuracy | | - | ±2.5 | ±5.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±1.0 | ±2.0 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.5 | ±3.0 | LSB | - |
| | Holding characteristics of sample-and hold circuits | | - | - | 20 | μs | - |
| | Dynamic range | | 0.25 | - | VREFH - 0.25 | V | - |

**Table 2.34 A/D conversion characteristics for unit 1 (2 of 2)**
Conditions: PCLKC = 1 to 60 MHz

| Parameter | | | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Channel-dedicated sample-and-hold circuits not in use (AN100 to AN102) | Conversion time*1 (Operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.48 (0.267)*2 | - | - | μs | Sampling in 16 states |
| | Offset error | | - | ±1.0 | ±2.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±2.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±4.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±1.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±2.5 | LSB | - |
| High-precision channels (AN105, AN106) | Conversion time*1 (Operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.48 (0.267)*2 | - | - | μs | Sampling in 16 states |
| | | Max. = 400 Ω | 0.40 (0.183)*2 | - | - | μs | Sampling in 11 states<br>VCC = AVCC0 = 3.0 to 3.6 V<br>3.0 V ≤ VREFH ≤ AVCC0 |
| | Offset error | | - | ±1.0 | ±2.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±2.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±4.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±1.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±2.5 | LSB | - |
| High-precision channels (AN107) | Conversion time*1 (Operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.75 (0.533)*2 | - | - | μs | Sampling in 32 states |
| | Offset error | | - | ±1.0 | ±2.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±2.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±4.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±1.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±2.5 | LSB | - |
| Normal-precision channels (AN116, AN117) | Conversion time*1 (Operation at PCLKC = 60 MHz) | Permissible signal source impedance Max. = 1 kΩ | 0.88 (0.667)*2 | - | - | μs | Sampling in 40 states |
| | Offset error | | - | ±1.0 | ±5.5 | LSB | - |
| | Full-scale error | | - | ±1.0 | ±5.5 | LSB | - |
| | Absolute accuracy | | - | ±2.0 | ±7.5 | LSB | - |
| | DNL differential nonlinearity error | | - | ±0.5 | ±4.5 | LSB | - |
| | INL integral nonlinearity error | | - | ±1.0 | ±5.5 | LSB | - |

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, the values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Note 3. When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, see Table 2.35.

**Table 2.35 A/D conversion characteristics for simultaneous use of channel-dedicated sample-and-hold circuits in unit 0 and unit 1**

Conditions: PCLKC = 30/60 MHz

| Parameter | | Min | Typ | Max | Test conditions |
|---|---|---|---|---|---|
| Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002) | Offset error | - | ±1.5 | ±5.0 | • PCLKC = 60 MHz<br>• Sampling in 15 states |
| | Full-scale error | - | ±2.5 | ±5.0 | |
| | Absolute accuracy | - | ±4.0 | ±8.0 | |
| Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102) | Offset error | - | ±1.5 | ±5.0 | |
| | Full-scale error | - | ±2.5 | ±5.0 | |
| | Absolute accuracy | - | ±4.0 | ±8.0 | |
| Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002) | Offset error | - | ±1.5 | ±3.5 | • PCLKC = 30 MHz<br>• Sampling in 7 states |
| | Full-scale error | - | ±1.5 | ±3.5 | |
| | Absolute accuracy | - | ±3.0 | +4.5/-6.5 | |
| Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102) | Offset error | - | ±1.5 | ±3.5 | |
| | Full-scale error | - | ±1.5 | ±3.5 | |
| | Absolute accuracy | - | ±3.0 | +4.5/-6.5 | |

Note: When simultaneously using channel-dedicated sample-and-hold circuits in unit 0 and unit 1, setting the ADSHMSR.SHMD bit to 1 is recommended.

**Table 2.36 A/D internal reference voltage characteristics**

| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| A/D internal reference voltage | 1.13 | 1.18 | 1.23 | V | - |
| Sampling time | 4.15 | - | - | μs | - |

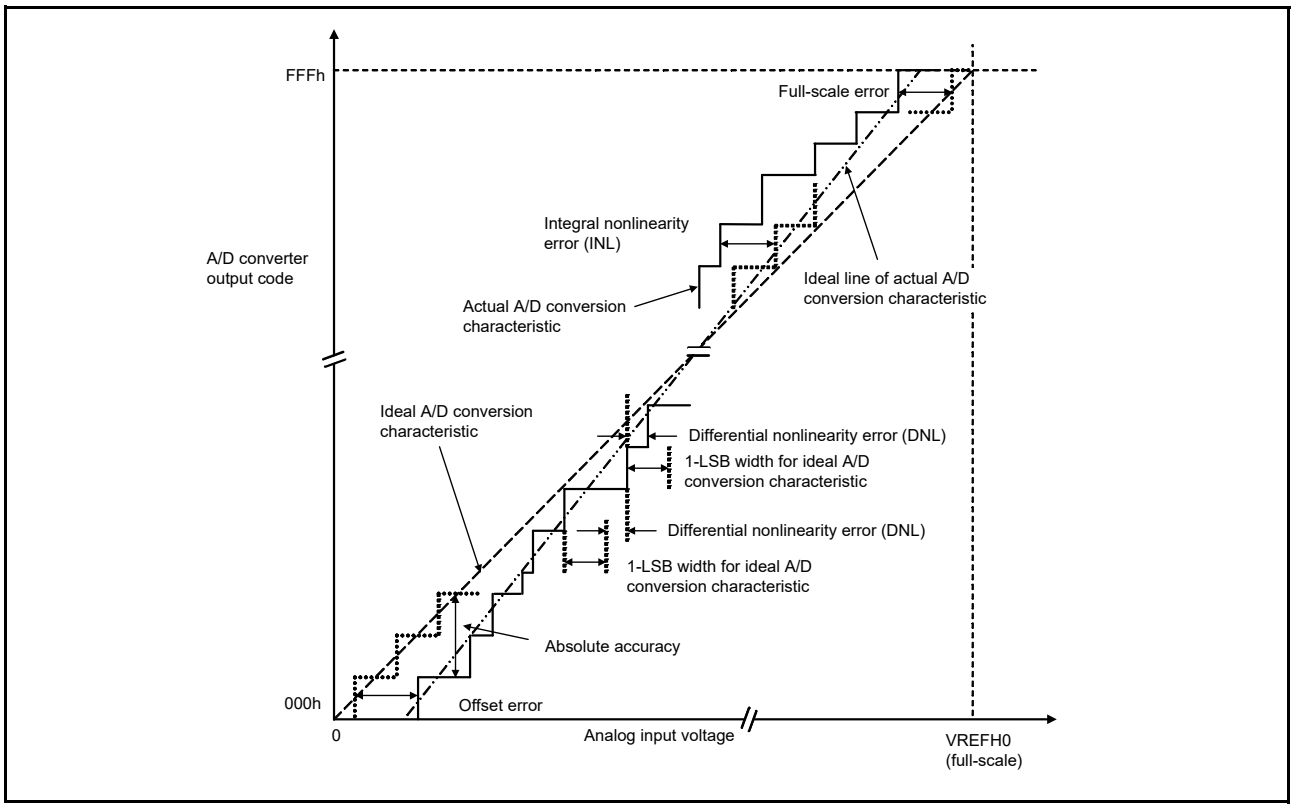



**Figure 2.64 Illustration of ADC12 characteristic terms**

### Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 is 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

### Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

### Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

### Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

### Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

## 2.6 DAC12 Characteristics

**Table 2.37 D/A conversion characteristics**

| Parameter | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Resolution | - | - | 12 | Bits | - |
| Without output amplifier | | | | | |
| Absolute accuracy | - | - | ±24 | LSB | Resistive load 2 MΩ |
| INL | - | ±2.0 | ±8.0 | LSB | Resistive load 2 MΩ |
| DNL | - | ±1.0 | ±2.0 | LSB | - |
| Output impedance | - | 8.5 | - | kΩ | - |
| Conversion time | - | - | 3.0 | μs | Resistive load 2 MΩ, Capacitive load 20 pF |
| Output voltage range | 0 | - | VREFH | V | - |
| With output amplifier | | | | | |
| INL | - | ±2.0 | ±4.0 | LSB | - |
| DNL | - | ±1.0 | ±2.0 | LSB | - |
| Conversion time | - | - | 4.0 | μs | - |
| Resistive load | 5 | - | - | kΩ | - |
| Capacitive load | - | - | 50 | pF | - |
| Output voltage range | 0.2 | - | VREFH - 0.2 | V | - |

## 2.7 TSN Characteristics

**Table 2.38 TSN characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Relative accuracy | - | - | ±1.0 | - | °C | - |
| Temperature slope | - | - | 4.0 | - | mV/°C | - |
| Output voltage (at 25°C) | - | - | 1.24 | - | V | - |
| Temperature sensor start time | $t_{START}$ | - | - | 30 | μs | - |
| Sampling time | - | 4.15 | - | - | μs | - |

## 2.8 OSC Stop Detect Characteristics

**Table 2.39 Oscillation stop detection circuit characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Detection time | $t_{dr}$ | - | - | 1 | ms | Figure 2.65 |

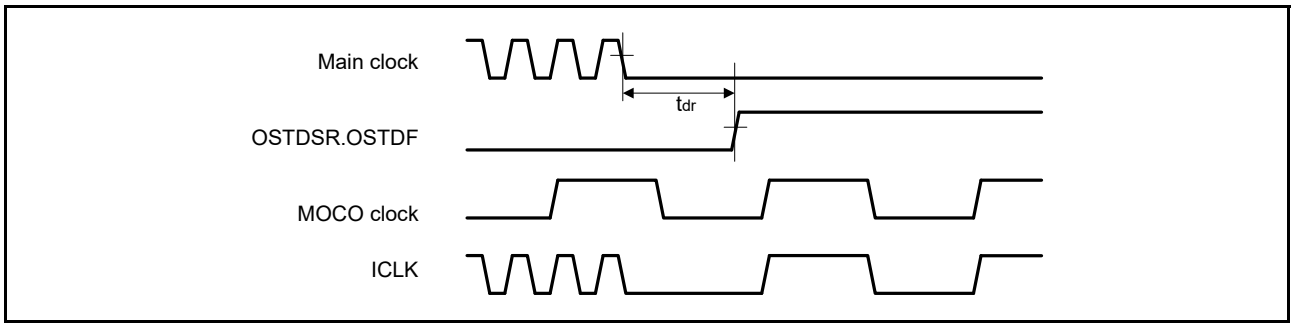



**Figure 2.65 Oscillation stop detection timing**

## 2.9 POR and LVD Characteristics

**Table 2.40 Power-on reset circuit and voltage detection circuit characteristics (1 of 2)**

| Parameter | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| Voltage detection level | Power-on reset (POR) | DPSBYCR.DEEPCUT[1:0] = 00b or 01b | $V_{POR}$ | 2.5 | 2.6 | 2.7 | V | Figure 2.66 |
| | | DPSBYCR.DEEPCUT[1:0] = 11b | | 1.8 | 2.25 | 2.7 | | |
| | Voltage detection circuit (LVD0) | | $V_{det0_1}$ | 2.84 | 2.94 | 3.04 | | Figure 2.67 |
| | | | $V_{det0_2}$ | 2.77 | 2.87 | 2.97 | | |
| | | | $V_{det0_3}$ | 2.70 | 2.80 | 2.90 | | |
| | Voltage detection circuit (LVD1) | | $V_{det1_1}$ | 2.89 | 2.99 | 3.09 | | Figure 2.68 |
| | | | $V_{det1_2}$ | 2.82 | 2.92 | 3.02 | | |
| | | | $V_{det1_3}$ | 2.75 | 2.85 | 2.95 | | |
| | Voltage detection circuit (LVD2) | | $V_{det2_1}$ | 2.89 | 2.99 | 3.09 | | Figure 2.69 |
| | | | $V_{det2_2}$ | 2.82 | 2.92 | 3.02 | | |
| | | | $V_{det2_3}$ | 2.75 | 2.85 | 2.95 | | |

**Table 2.40 Power-on reset circuit and voltage detection circuit characteristics (2 of 2)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| Internal reset time | Power-on reset time | $t_{POR}$ | - | 4.5 | - | ms | Figure 2.66 |
| | LVD0 reset time | $t_{LVD0}$ | - | 0.51 | - | | Figure 2.67 |
| | LVD1 reset time | $t_{LVD1}$ | - | 0.38 | - | | Figure 2.68 |
| | LVD2 reset time | $t_{LVD2}$ | - | 0.38 | - | | Figure 2.69 |
| Minimum VCC down time*1 | | $t_{VOFF}$ | 200 | - | - | μs | Figure 2.66, Figure 2.67 |
| Response delay | | $t_{det}$ | - | - | 200 | μs | Figure 2.66 to Figure 2.69 |
| LVD operation stabilization time (after LVD is enabled) | | $t_{d(E-A)}$ | - | - | 10 | μs | Figure 2.68, Figure 2.69 |
| Hysteresis width (LVD1 and LVD2) | | $V_{LVH}$ | - | 70 | - | mV | |

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels $V_{POR}$, $V_{det1}$, and $V_{det2}$ for POR and LVD.

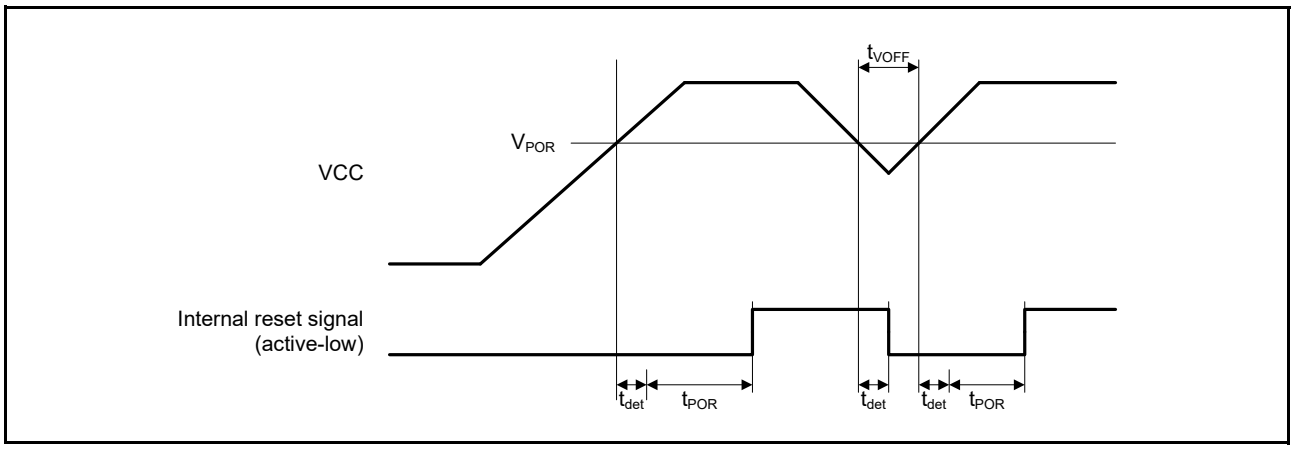



**Figure 2.66 Power-on reset timing**

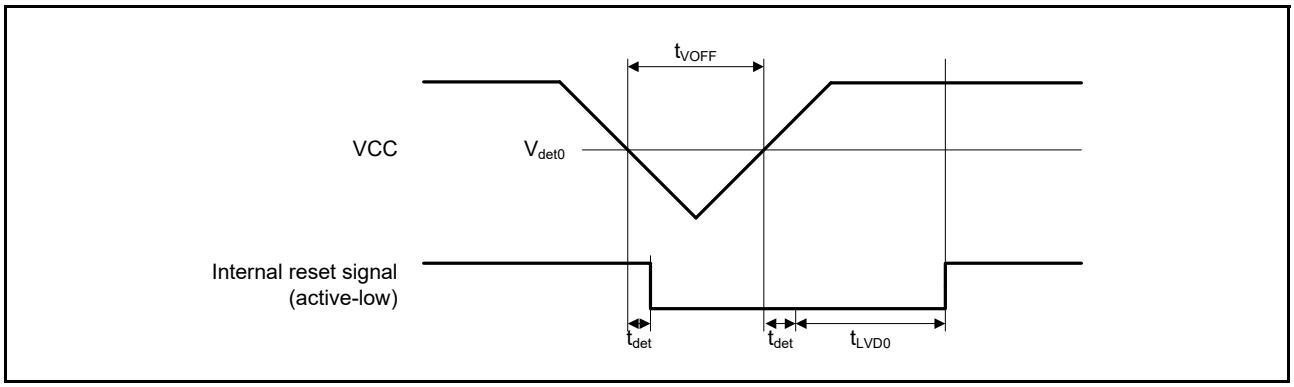



**Figure 2.67 Voltage detection circuit timing ($V_{det0}$)**

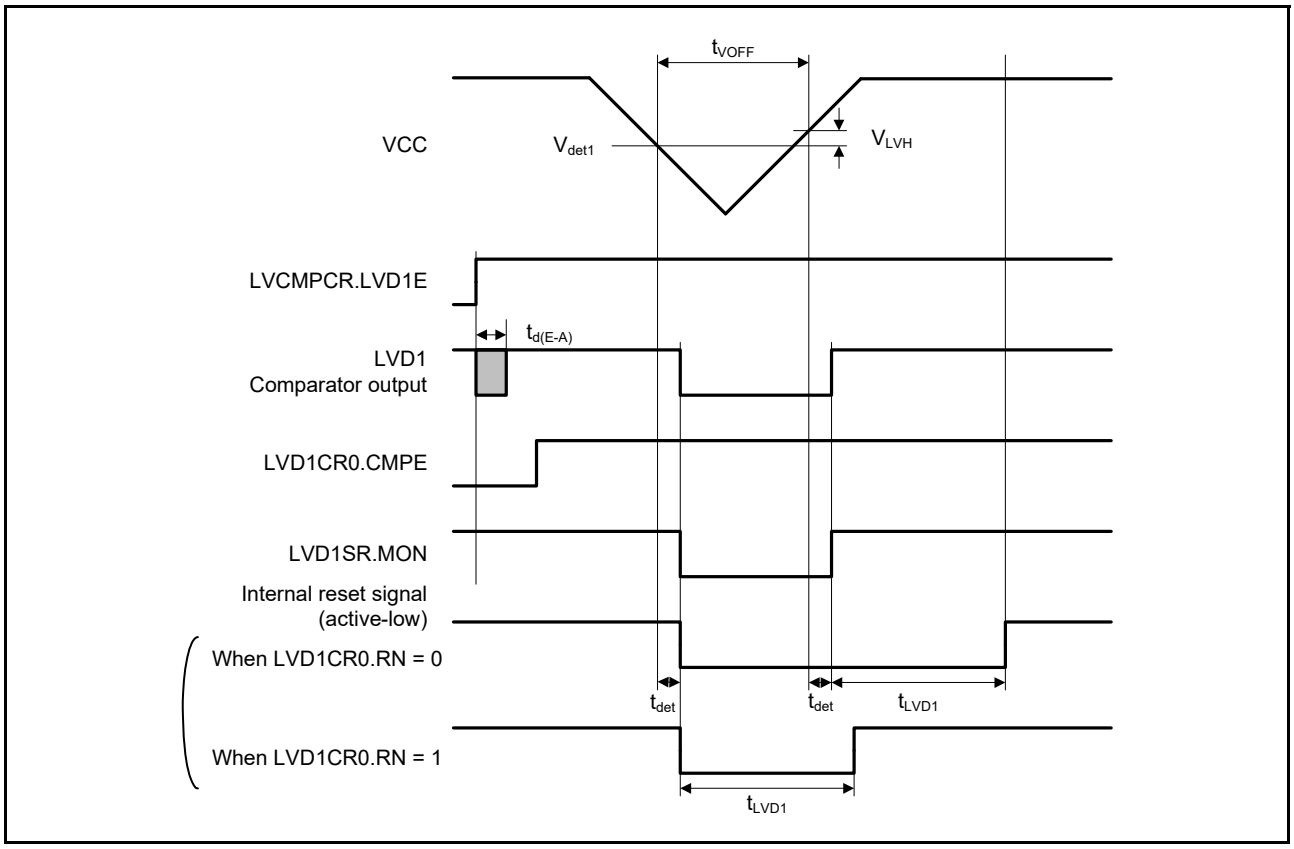



**Figure 2.68 Voltage detection circuit timing ($V_{det1}$)**

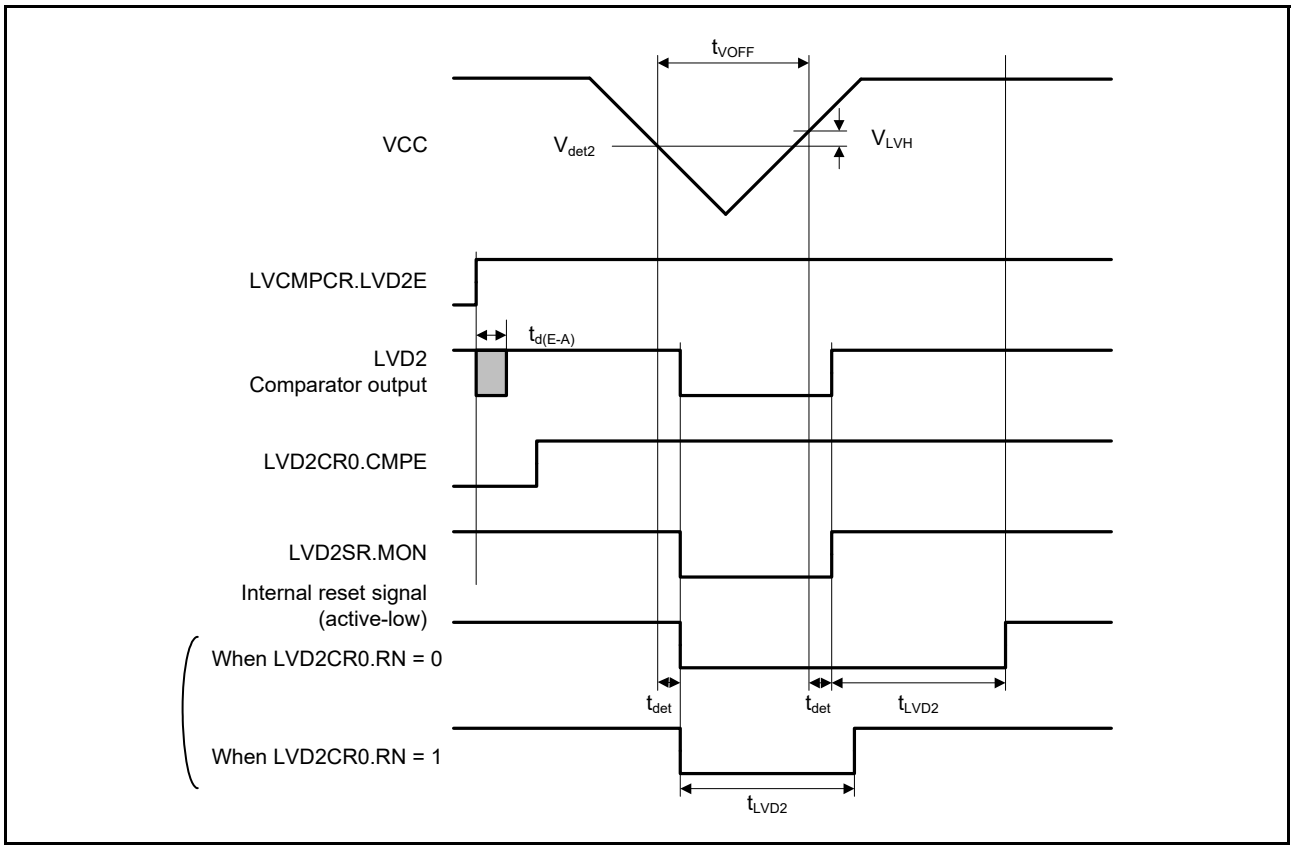



**Figure 2.69 Voltage detection circuit timing ($V_{det2}$)**

## 2.10 VBATT Characteristics

**Table 2.41 Battery backup function characteristics**

Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.65 to 3.6 V*1

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Voltage level for switching to battery backup | $V_{DETBATT}$ | 2.50 | 2.60 | 2.70 | V | Figure 2.70 |
| Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop | $V_{BATTSW}$ | 2.70 | - | - | V | |
| VCC-off period for starting power supply switching | $t_{VOFFBATT}$ | 200 | - | - | μs | |

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

Note 1. Low CL crystal cannot be used below VBATT = 1.8 V.

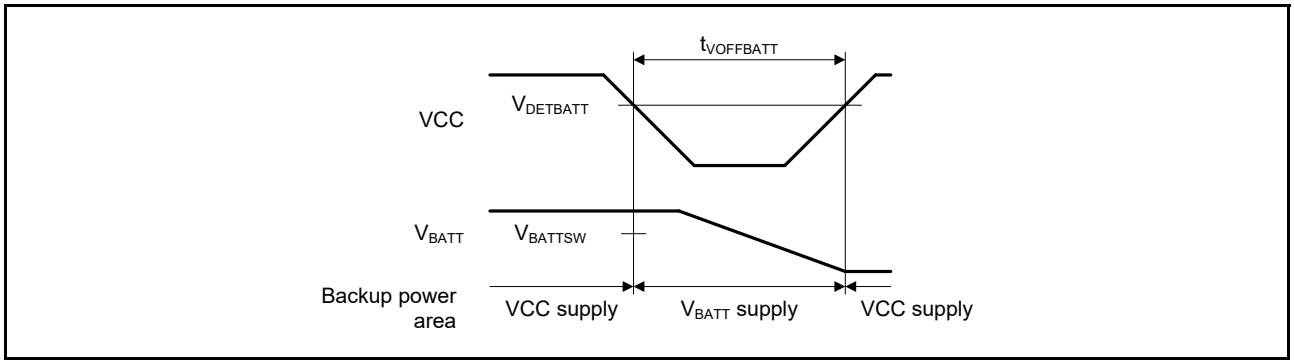



**Figure 2.70 Battery backup function characteristics**

## 2.11 CTSU Characteristics

**Table 2.42 CTSU characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| External capacitance connected to TSCAP pin | $C_{tscap}$ | 9 | 10 | 11 | nF | - |
| TS pin capacitive load | $C_{base}$ | - | - | 50 | pF | - |
| Permissible output high current | $\Sigma_{IoH}$ | - | - | -40 | mA | When the mutual capacitance method is applied |

## 2.12 ACMPHS Characteristics

**Table 2.43 ACMPHS characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Reference voltage range | VREF | 0 | - | AVCC0 | V | - |
| Input voltage range | VI | 0 | - | AVCC0 | V | - |
| Output delay*1 | Td | - | 50 | 100 | ns | VI = VREF ± 100 mV |
| Internal reference voltage | Vref | 1.13 | 1.18 | 1.23 | V | - |

Note 1. This value is the internal propagation delay.

## 2.13 PGA Characteristics

**Table 2.44 PGA characteristics in single mode**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| PGAVSS input voltage range | PGAVSS | 0 | - | 0 | V |
| | AIN0 (G = 2.000) | 0.050 × AVCC0 | - | 0.45 × AVCC0 | V |
| | AIN1 (G = 2.500) | 0.047 × AVCC0 | - | 0.360 × AVCC0 | V |
| | AIN2 (G = 2.667) | 0.046 × AVCC0 | - | 0.337 × AVCC0 | V |
| | AIN3 (G = 2.857) | 0.046 × AVCC0 | - | 0.32 × AVCC0 | V |
| | AIN4 (G = 3.077) | 0.045 × AVCC0 | - | 0.292 × AVCC0 | V |
| | AIN5 (G = 3.333) | 0.044 × AVCC0 | - | 0.265 × AVCC0 | V |
| | AIN6 (G = 3.636) | 0.042 × AVCC0 | - | 0.247 × AVCC0 | V |
| | AIN7 (G = 4.000) | 0.040 × AVCC0 | - | 0.212 × AVCC0 | V |
| | AIN8 (G = 4.444) | 0.036 × AVCC0 | - | 0.191 × AVCC0 | V |
| | AIN9 (G = 5.000) | 0.033 × AVCC0 | - | 0.17 × AVCC0 | V |
| | AIN10 (G = 5.714) | 0.031 × AVCC0 | - | 0.148 × AVCC0 | V |
| | AIN11 (G = 6.667) | 0.029 × AVCC0 | - | 0.127 × AVCC0 | V |
| | AIN12 (G = 8.000) | 0.027 × AVCC0 | - | 0.09 × AVCC0 | V |
| | AIN13 (G = 10.000) | 0.025 × AVCC0 | - | 0.08 × AVCC0 | V |
| | AIN14 (G = 13.333) | 0.023 × AVCC0 | - | 0.06 × AVCC0 | V |
| Gain error | Gerr0 (G = 2.000) | -1.0 | - | 1.0 | % |
| | Gerr1 (G = 2.500) | -1.0 | - | 1.0 | % |
| | Gerr2 (G = 2.667) | -1.0 | - | 1.0 | % |
| | Gerr3 (G = 2.857) | -1.0 | - | 1.0 | % |
| | Gerr4 (G = 3.077) | -1.0 | - | 1.0 | % |
| | Gerr5 (G = 3.333) | -1.5 | - | 1.5 | % |
| | Gerr6 (G = 3.636) | -1.5 | - | 1.5 | % |
| | Gerr7 (G = 4.000) | -1.5 | - | 1.5 | % |
| | Gerr8 (G = 4.444) | -2.0 | - | 2.0 | % |
| | Gerr9 (G = 5.000) | -2.0 | - | 2.0 | % |
| | Gerr10 (G = 5.714) | -2.0 | - | 2.0 | % |
| | Gerr11 (G = 6.667) | -2.0 | - | 2.0 | % |
| | Gerr12 (G = 8.000) | -2.0 | - | 2.0 | % |
| | Gerr13 (G = 10.000) | -2.0 | - | 2.0 | % |
| | Gerr14 (G = 13.333) | -2.0 | - | 2.0 | % |
| Offset error | Voff | -8 | - | 8 | mV |

**Table 2.45 PGA characteristics in differential mode (1 of 2)**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PGAVSS input voltage range | | PGAVSS | -0.5 | - | 0.3 | V |
| Differential input voltage range | G = 1.500 | AIN-PGAVSS | -0.5 | - | 0.5 | V |
| | G = 2.333 | | -0.4 | - | 0.4 | V |
| | G = 4.000 | | -0.2 | - | 0.2 | V |
| | G = 5.667 | | -0.15 | - | 0.15 | V |

**Table 2.45 PGA characteristics in differential mode (2 of 2)**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Gain error | G = 1.500 | Gerr | -1.0 | - | 1.0 | % |
| | G = 2.333 | | -1.0 | - | 1.0 | |
| | G = 4.000 | | -1.0 | - | 1.0 | |
| | G = 5.667 | | -1.0 | - | 1.0 | |

## 2.14 Flash Memory Characteristics

### 2.14.1 Code Flash Memory Characteristics

**Table 2.46 Code flash memory characteristics**

Conditions: Program or erase: FCLK = 4 to 60 MHz

Read: FCLK ≤ 60 MHz

| Parameter | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | | |
| Programming time $N_{PEC}$ ≤ 100 times | 128-byte | $t_{P128}$ | - | 0.75 | 13.2 | - | 0.34 | 6.0 | ms | |
| | 8-KB | $t_{P8K}$ | - | 49 | 176 | - | 22 | 80 | ms | |
| | 32-KB | $t_{P32K}$ | - | 194 | 704 | - | 88 | 320 | ms | |
| Programming time $N_{PEC}$ > 100 times | 128-byte | $t_{P128}$ | - | 0.91 | 15.8 | - | 0.41 | 7.2 | ms | |
| | 8-KB | $t_{P8K}$ | - | 60 | 212 | - | 27 | 96 | ms | |
| | 32-KB | $t_{P32K}$ | - | 234 | 848 | - | 106 | 384 | ms | |
| Erasure time $N_{PEC}$ ≤ 100 times | 8-KB | $t_{E8K}$ | - | 78 | 216 | - | 43 | 120 | ms | |
| | 32-KB | $t_{E32K}$ | - | 283 | 864 | - | 157 | 480 | ms | |
| Erasure time $N_{PEC}$ > 100 times | 8-KB | $t_{E8K}$ | - | 94 | 260 | - | 52 | 144 | ms | |
| | 32-KB | $t_{E32K}$ | - | 341 | 1040 | - | 189 | 576 | ms | |
| Reprogramming/erasure cycle*4 | | $N_{PEC}$ | 10000*1 | - | - | 10000*1 | - | - | Times | |
| Suspend delay during programming | | $t_{SPD}$ | - | - | 264 | - | - | 120 | μs | |
| First suspend delay during erasure in suspend priority mode | | $t_{SESD1}$ | - | - | 216 | - | - | 120 | μs | |
| Second suspend delay during erasure in suspend priority mode | | $t_{SESD2}$ | - | - | 1.7 | - | - | 1.7 | ms | |
| Suspend delay during erasure in erasure priority mode | | $t_{SEED}$ | - | - | 1.7 | - | - | 1.7 | ms | |
| Forced stop command | | $t_{FD}$ | - | - | 32 | - | - | 20 | μs | |
| Data hold time*2 | | $t_{DRP}$ | 10*2, *3 | - | - | 10*2, *3 | - | - | Years | |
| | | | 30*2, *3 | - | - | 30*2, *3 | - | - | | Ta = +85°C |

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.

Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.

Note 3. This result is obtained from reliability testing.

Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.

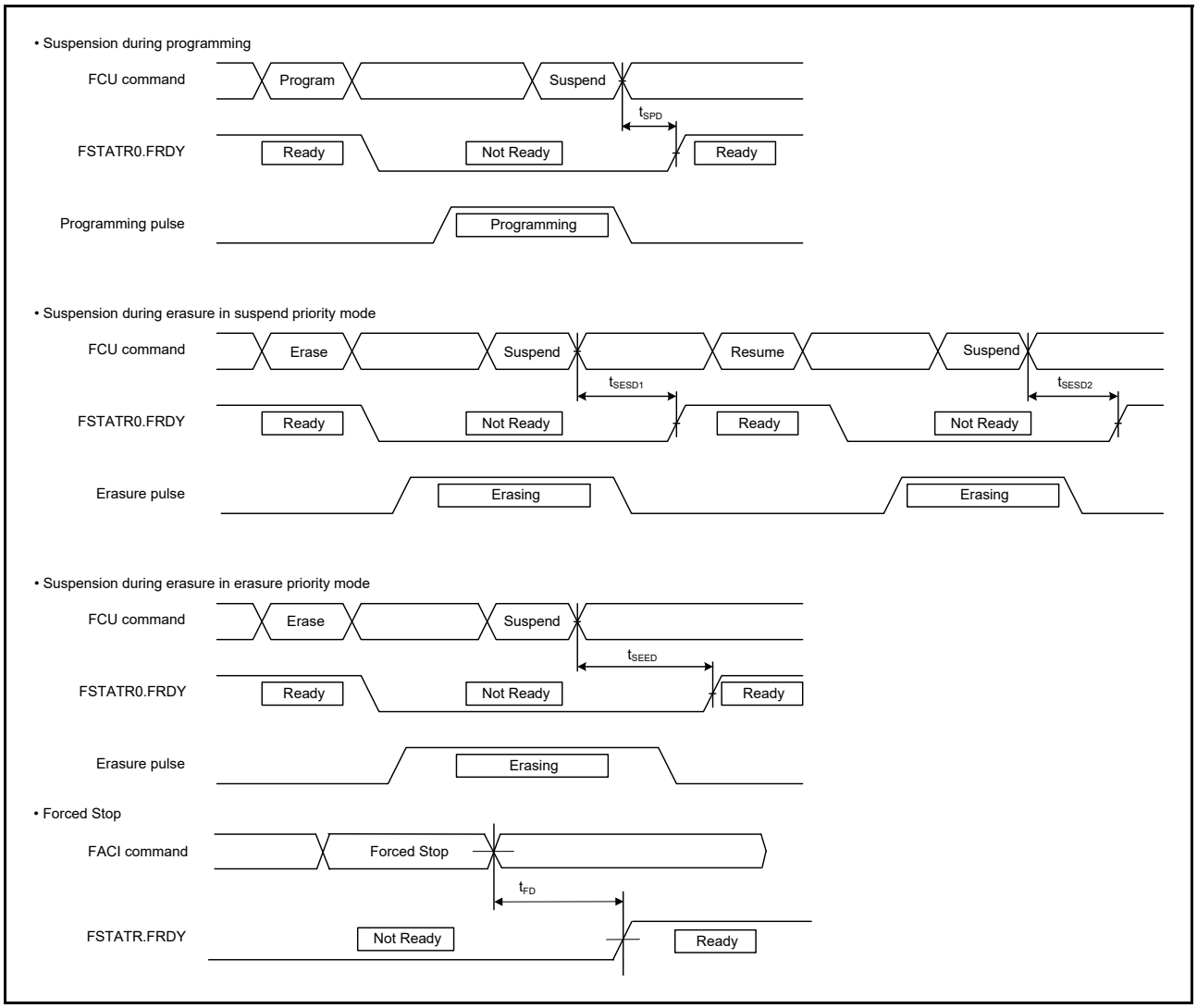



**Figure 2.71 Suspension and forced stop timing for flash memory programming and erasure**

### 2.14.2 Data Flash Memory Characteristics

**Table 2.47 Data flash memory characteristics**
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

| Parameter | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | | |
| Programming time | 4-byte | $t_{DP4}$ | - | 0.36 | 3.8 | - | 0.16 | 1.7 | ms | |
| | 8-byte | $t_{DP8}$ | - | 0.38 | 4.0 | - | 0.17 | 1.8 | | |
| | 16-byte | $t_{DP16}$ | - | 0.42 | 4.5 | - | 0.19 | 2.0 | | |
| Erasure time | 64-byte | $t_{DE64}$ | - | 3.1 | 18 | - | 1.7 | 10 | ms | |
| | 128-byte | $t_{DE128}$ | - | 4.7 | 27 | - | 2.6 | 15 | | |
| | 256-byte | $t_{DE256}$ | - | 8.9 | 50 | - | 4.9 | 28 | | |
| Blank check time | 4-byte | $t_{DBC4}$ | - | - | 84 | - | - | 30 | μs | |
| Reprogramming/erasure cycle*1 | | $N_{DPEC}$ | 125000*2 | - | - | 125000*2 | - | - | - | |
| Suspend delay during programming | 4-byte | $t_{DSPD}$ | - | - | 264 | - | - | 120 | μs | |
| | 8-byte | | - | - | 264 | - | - | 120 | | |
| | 16-byte | | - | - | 264 | - | - | 120 | | |
| First suspend delay during erasure in suspend priority mode | 64-byte | $t_{DSESD1}$ | - | - | 216 | - | - | 120 | μs | |
| | 128-byte | | - | - | 216 | - | - | 120 | | |
| | 256-byte | | - | - | 216 | - | - | 120 | | |
| Second suspend delay during erasure in suspend priority mode | 64-byte | $t_{DSESD2}$ | - | - | 300 | - | - | 300 | μs | |
| | 128-byte | | - | - | 390 | - | - | 390 | | |
| | 256-byte | | - | - | 570 | - | - | 570 | | |
| Suspend delay during erasing in erasure priority mode | 64-byte | $t_{DSEED}$ | - | - | 300 | - | - | 300 | μs | |
| | 128-byte | | - | - | 390 | - | - | 390 | | |
| | 256-byte | | - | - | 570 | - | - | 570 | | |
| Forced stop command | | $t_{FD}$ | - | - | 32 | - | - | 20 | μs | |
| Data hold time*3 | | $t_{DRP}$ | 10*3,*4 | - | - | 10*3,*4 | - | - | Year | |
| | | | 30*3,*4 | - | - | 30*3,*4 | - | - | | Ta = +85°C |

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.

## 2.15 Boundary Scan

**Table 2.48 Boundary scan characteristics (1 of 2)**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 100 | - | - | ns | Figure 2.72 |
| TCK clock high pulse width | $t_{TCKH}$ | 45 | - | - | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 45 | - | - | ns | |
| TCK clock rise time | $t_{TCKr}$ | - | - | 5 | ns | |
| TCK clock fall time | $t_{TCKf}$ | - | - | 5 | ns | |

**Table 2.48 Boundary scan characteristics (2 of 2)**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| TMS setup time | $t_{TMSS}$ | 20 | - | - | ns | Figure 2.73 |
| TMS hold time | $t_{TMSH}$ | 20 | - | - | ns | |
| TDI setup time | $t_{TDIS}$ | 20 | - | - | ns | |
| TDI hold time | $t_{TDIH}$ | 20 | - | - | ns | |
| TDO data delay | $t_{TDOD}$ | - | - | 40 | ns | |
| Boundary scan circuit startup time*1 | $T_{BSSTUP}$ | $t_{RESWP}$ | - | - | - | Figure 2.74 |

Note 1. Boundary scan does not function until the power-on reset becomes negative.

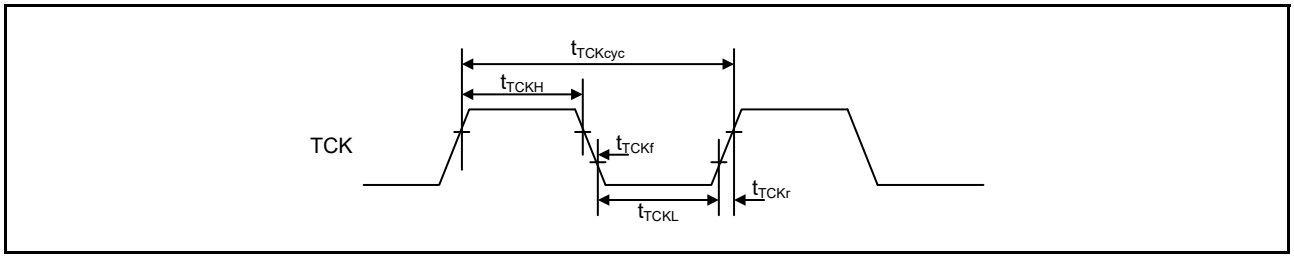



**Figure 2.72 Boundary scan TCK timing**

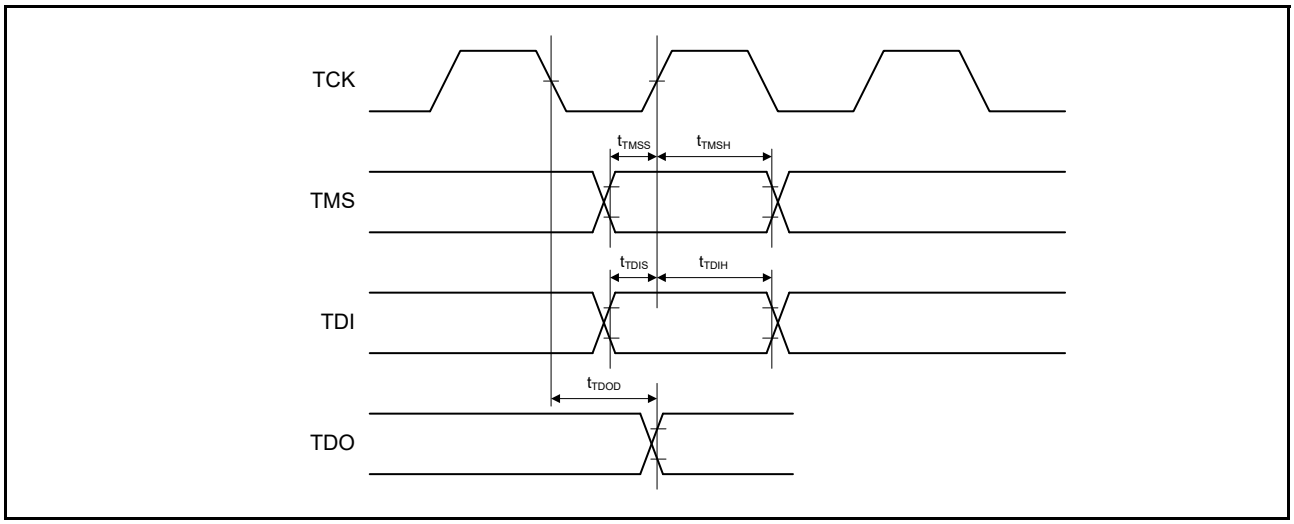



**Figure 2.73 Boundary scan input/output timing**

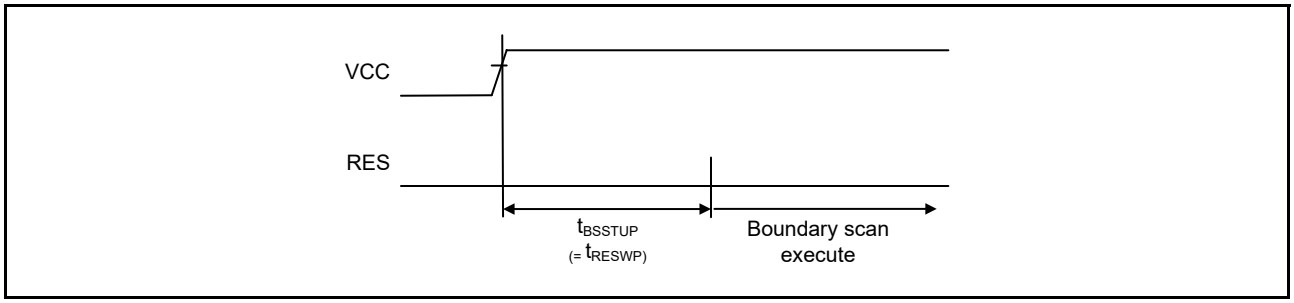



**Figure 2.74 Boundary scan circuit startup timing**

## 2.16 Joint Test Action Group (JTAG)

**Table 2.49 JTAG**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 40 | - | - | ns | Figure 2.72 |
| TCK clock high pulse width | $t_{TCKH}$ | 15 | - | - | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 15 | - | - | ns | |
| TCK clock rise time | $t_{TCKr}$ | - | - | 5 | ns | |
| TCK clock fall time | $t_{TCKf}$ | - | - | 5 | ns | |
| TMS setup time | $t_{TMSS}$ | 8 | - | - | ns | Figure 2.73 |
| TMS hold time | $t_{TMSH}$ | 8 | - | - | ns | |
| TDI setup time | $t_{TDIS}$ | 8 | - | - | ns | |
| TDI hold time | $t_{TDIH}$ | 8 | - | - | ns | |
| TDO data delay time | $t_{TDOD}$ | - | - | 20 | ns | |

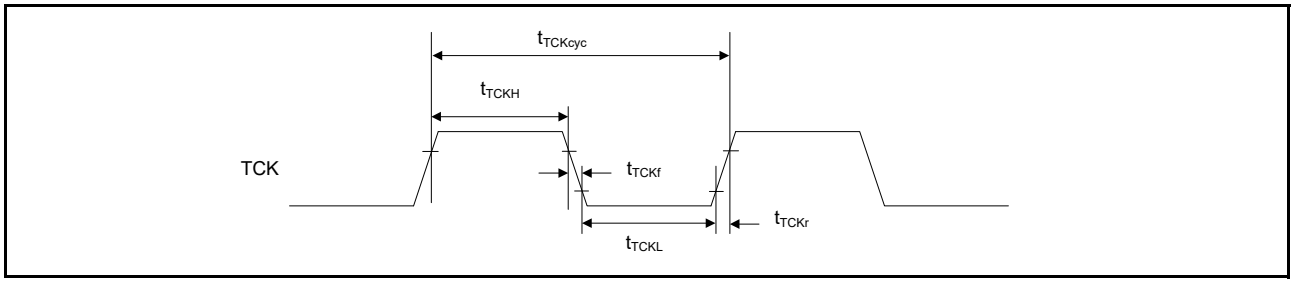



**Figure 2.75 JTAG TCK timing**

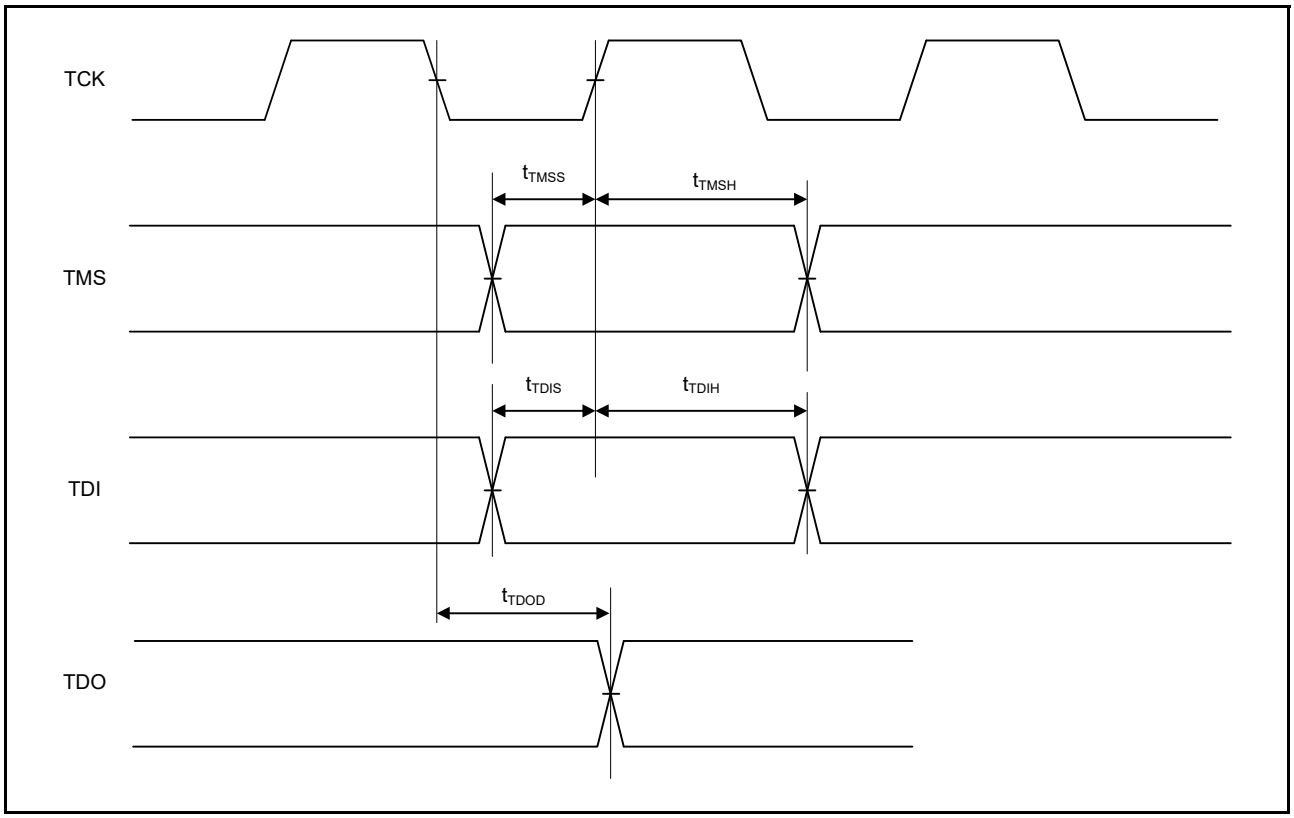



**Figure 2.76 JTAG input/output timing**

## 2.17 Serial Wire Debug (SWD)

**Table 2.50 SWD**

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| SWCLK clock cycle time | $t_{SWCKcyc}$ | 40 | - | - | ns | Figure 2.77 |
| SWCLK clock high pulse width | $t_{SWCKH}$ | 15 | - | - | ns | |
| SWCLK clock low pulse width | $t_{SWCKL}$ | 15 | - | - | ns | |
| SWCLK clock rise time | $t_{SWCKr}$ | - | - | 5 | ns | |
| SWCLK clock fall time | $t_{SWCKf}$ | - | - | 5 | ns | |
| SWDIO setup time | $t_{SWDS}$ | 8 | - | - | ns | Figure 2.78 |
| SWDIO hold time | $t_{SWDH}$ | 8 | - | - | ns | |
| SWDIO data delay time | $t_{SWDD}$ | 2 | - | 28 | ns | |

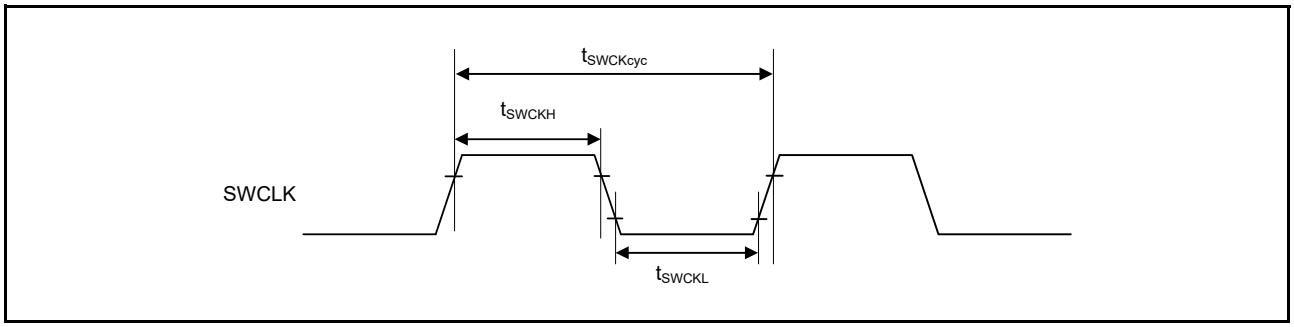



**Figure 2.77 SWD SWCLK timing**

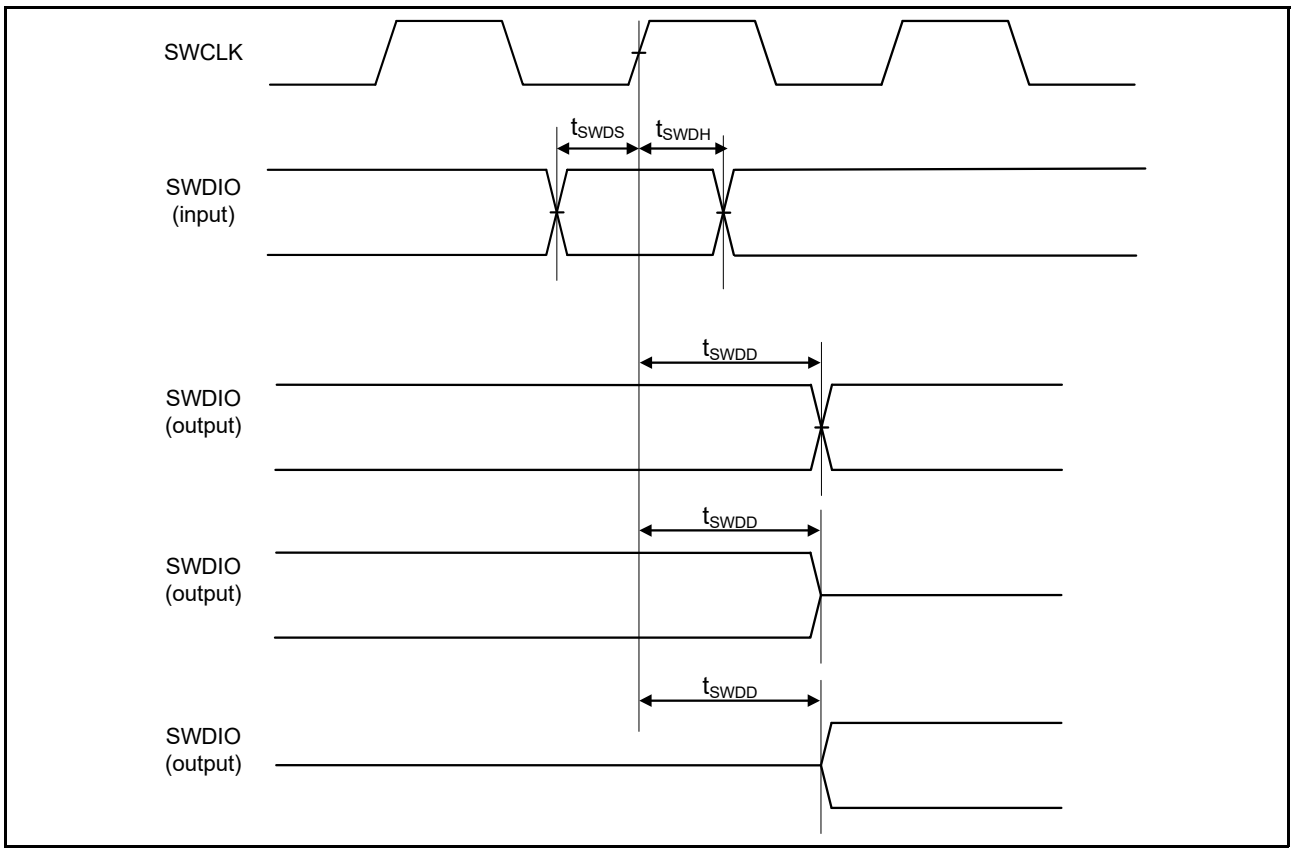



**Figure 2.78 SWD input/output timing**

## 2.18 Embedded Trace Macro Interface (ETM)

**Table 2.51 ETM**
Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| TCLK clock cycle time | $t_{TCLKcyc}$ | 33.3 | - | - | ns | Figure 2.79 |
| TCLK clock high pulse width | $t_{TCLKH}$ | 13.6 | - | - | ns | |
| TCLK clock low pulse width | $t_{TCLKL}$ | 13.6 | - | - | ns | |
| TCLK clock rise time | $t_{TCLKr}$ | - | - | 3 | ns | |
| TCLK clock fall time | $t_{TCLKf}$ | - | - | 3 | ns | |
| TDATA[3:0] output setup time | $t_{TRDS}$ | 3.5 | - | - | ns | Figure 2.80 |
| TDATA[3:0] output hold time | $t_{TRDH}$ | 2.5 | - | - | ns | |

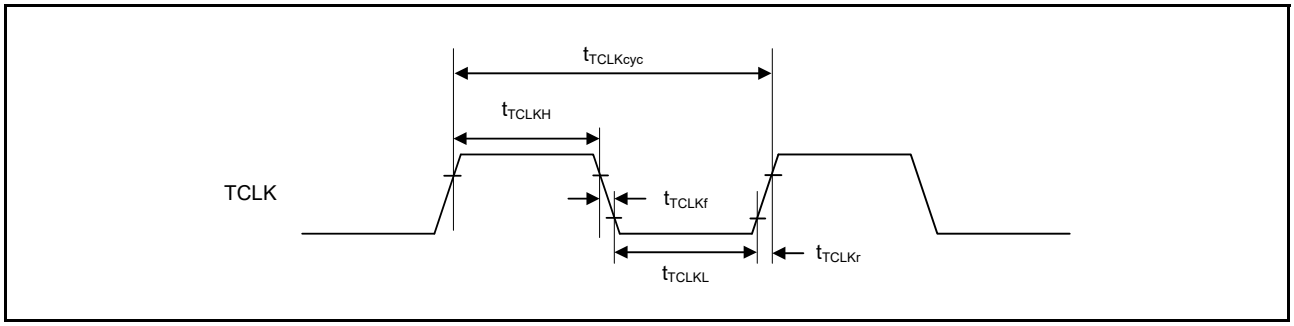



**Figure 2.79 ETM TCLK timing**

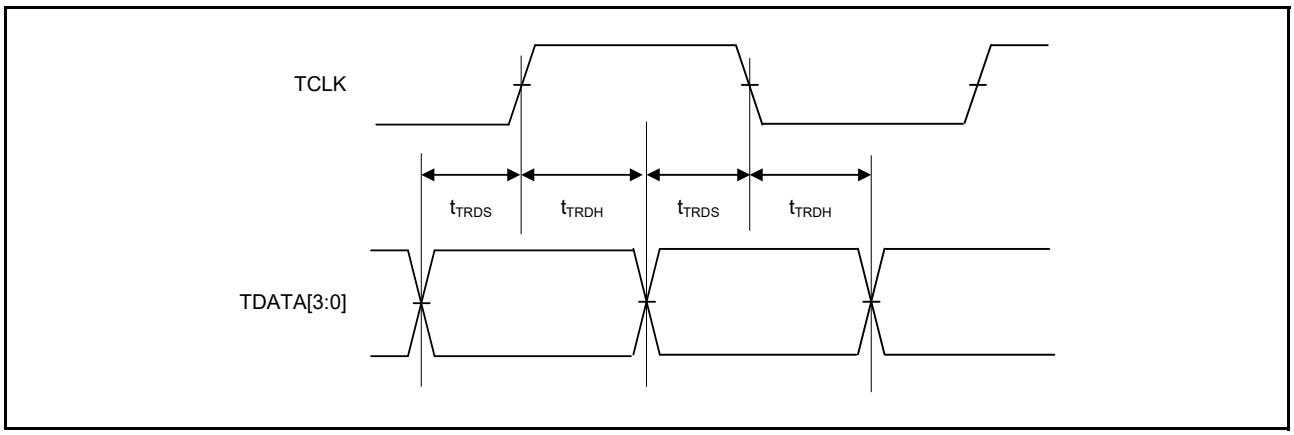
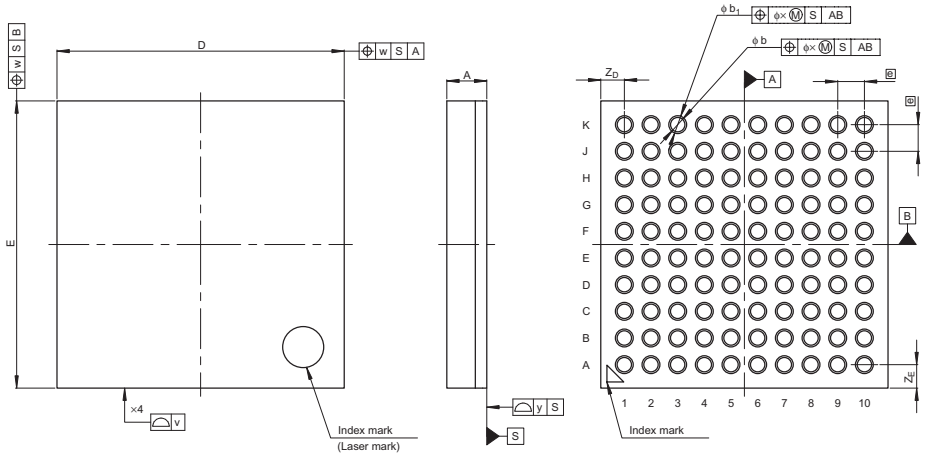



**Figure 2.80 ETM output timing**

# Appendix 1.Package Dimensions

Information on the latest version of the package dimensions or mountings is shown in “Packages” on the Renesas Electronics Corporation website.

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA100-7x7-0.65 | PTLG0100JA-A | 100F0G | 0.1g |

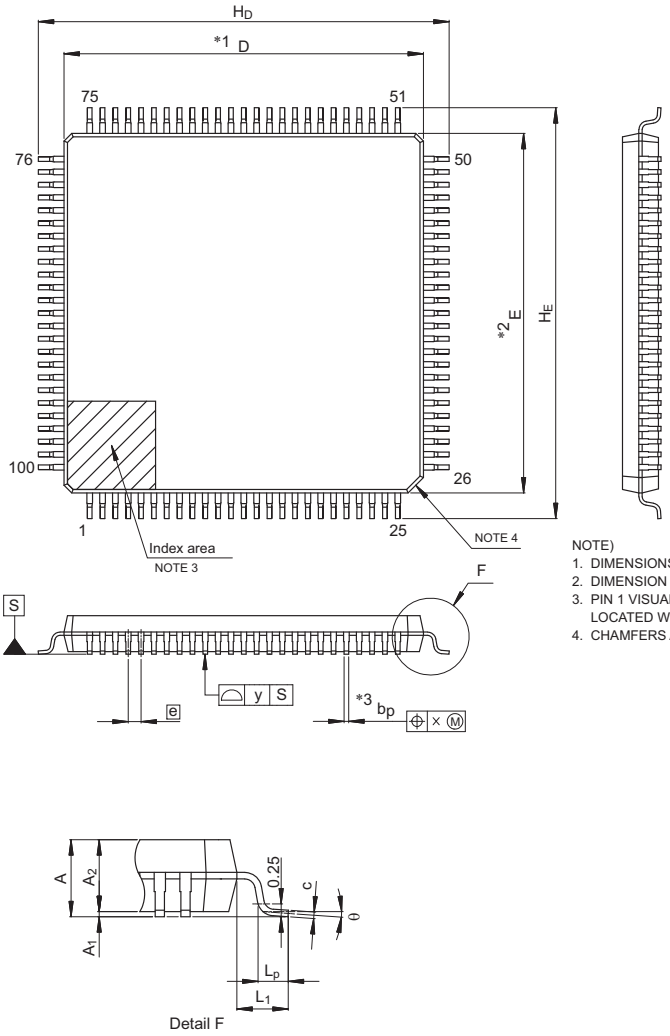



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 7.0 | — |
| E | — | 7.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.65 | — |
| b | 0.31 | 0.35 | 0.39 |
| $b_1$ | 0.385 | 0.435 | 0.485 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 0.575 | — |
| $Z_E$ | — | 0.575 | — |

**Figure 1.1 100-pin LGA**

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | — | 0.6 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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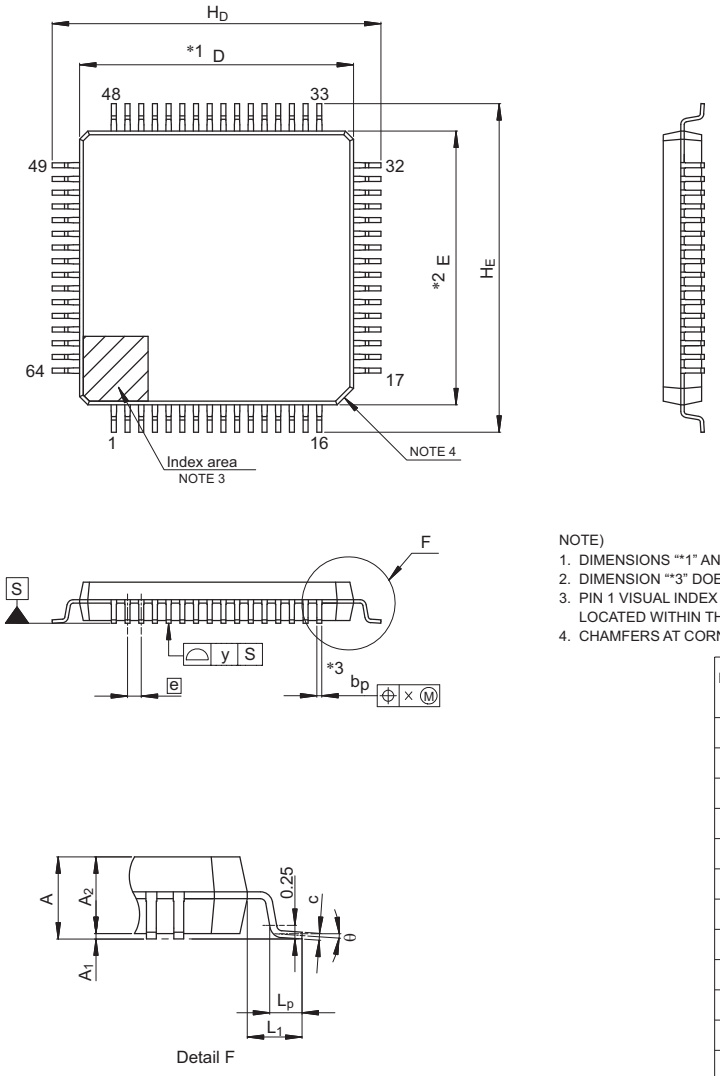
**Figure 1.2 100-pin LQFP**

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-C | — | 0.3 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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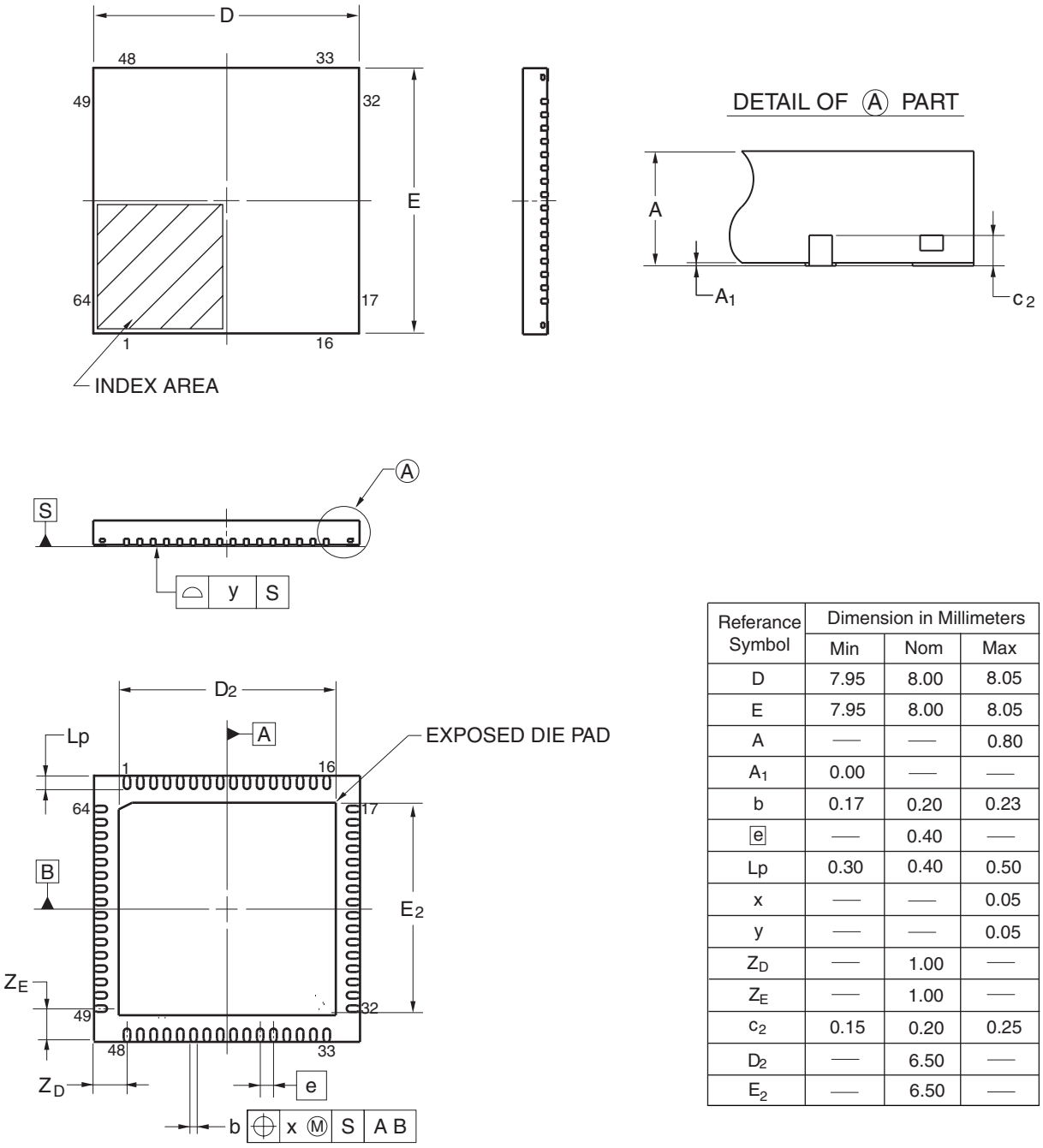
**Figure 1.3 64-pin LQFP**

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-HWQFN64-8x8-0.40 | PWQN0064LA-A | P64K8-40-9B5-3 | 0.16 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 7.95 | 8.00 | 8.05 |
| E | 7.95 | 8.00 | 8.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.17 | 0.20 | 0.23 |
| e | — | 0.40 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 1.00 | — |
| $Z_E$ | — | 1.00 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 6.50 | — |
| $E_2$ | — | 6.50 | — |

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**Figure 1.4 64-pin QFN**

| Revision History | RA6M1 Group Datasheet |
|---|---|

| Rev. | Date | Chapter | Summary |
|---|---|---|---|
| 1.00 | Oct 8, 2019 | - | First Edition issued |
| 1.10 | Dec 17, 2021 | - | Second Edition issued |
| 1.20 | Dec 2, 2022 | - | Third Edition issued |

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RA6M1 Group Datasheet

Publication Date: Rev.1.20 Dec 2, 2022

Published by: Renesas Electronics Corporation

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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