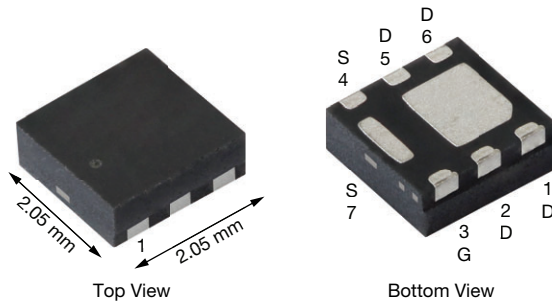




**THE DATASHEET OF
SQA470CEJW-T1_GE3**



Automotive N-Channel 20 V (D-S) 175 °C MOSFET

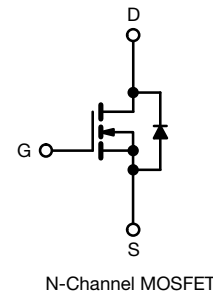
PowerPAK® SC-70W-6L Single

Marking Code: Q7XXXX

PRODUCT SUMMARY	
V_{DS} (V)	20
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.0280
$R_{DS(on)}$ (Ω) at $V_{GS} = 2.5$ V	0.0340
$R_{DS(on)}$ (Ω) at $V_{GS} = 1.8$ V	0.0380
I_D (A)	7.8
Configuration	Single

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- Wettable flank terminals
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912

 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


ORDERING INFORMATION	
Package	PowerPAK SC-70W-6L
Lead (Pb)-free and halogen-free	SQA410CEJW (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	20	V
Gate-source voltage		V_{GS}	± 8	
Continuous drain current ^a	$T_C = 25$ °C	I_D	7.8	A
	$T_C = 125$ °C		7.8	
Continuous source current (diode conduction) ^a		I_S	7.8	
Pulsed drain current ^a		I_{DM}	30	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	10	
Single pulse avalanche energy		E_{AS}	5	
Maximum power dissipation	$T_C = 25$ °C	P_D	13.6	W
	$T_C = 125$ °C		4.5	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount ^c	R_{thJA}	90	°C/W
Junction-to-case (drain)		R_{thJC}	11	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70W-6L is a leadless package and features wettable flank terminals. The end of the lead terminal is plated with tin.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		20	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		0.4	0.6	1.1	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 20 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 20 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 20 V, T _J = 175 °C	-	-	300	
On-state drain current ^a	I _{D(on)}	V _{GS} = 4.5 V	V _{DS} ≥ 5 V	10	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V	I _D = 5 A	-	0.0210	0.0280	Ω
		V _{GS} = 4.5 V	I _D = 5 A, T _J = 125 °C	-	-	0.0400	
		V _{GS} = 4.5 V	I _D = 5 A, T _J = 175 °C	-	-	0.0454	
		V _{GS} = 2.5 V	I _D = 4 A	-	0.0240	0.0340	
		V _{GS} = 1.8 V	I _D = 3 A	-	0.0280	0.0380	
Forward transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 5 A		-	29	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 10 V, f = 1 MHz	-	402	525	pF
Output capacitance	C _{oss}			-	96	125	
Reverse transfer capacitance	C _{rss}			-	44	58	
Total gate charge ^c	Q _g	V _{GS} = 4.5 V	V _{DS} = 10 V, I _D = 5.1 A	-	5.1	8	nC
Gate-source charge ^c	Q _{gs}			-	0.67	-	
Gate-drain charge ^c	Q _{gd}			-	0.95	-	
Gate resistance	R _g	f = 1 MHz		4.1	8.2	12.5	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _g = 1 Ω		-	7	12	ns
Rise time ^c	t _r			-	13	20	
Turn-off delay time ^c	t _{d(off)}			-	35	55	
Fall time ^c	t _f			-	10	15	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}			-	-	30	A
Forward voltage	V _{SD}	I _F = 4.5 A, V _{GS} = 0 V		-	0.79	1.2	V
Body diode reverse recovery time	t _{rr}	I _F = 1 A, di/dt = 100 A/μs		-	7.2	14.4	ns
Body diode reverse recovery charge	Q _{rr}			-	1.8	3.6	nC
Reverse recovery fall time	t _a			-	3.6	-	ns
Reverse recovery rise time	t _b			-	3.6	-	
Body diode peak reverse recovery current	I _{RM(REC)}					-	-0.45

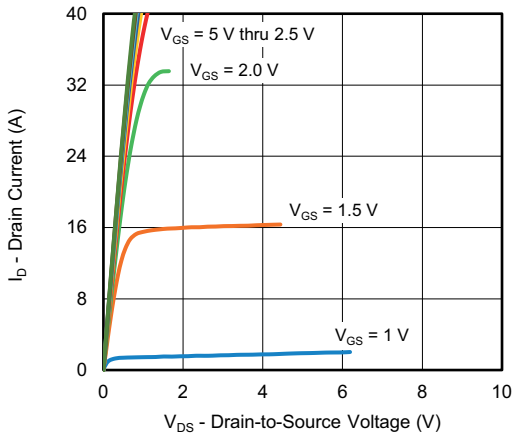
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

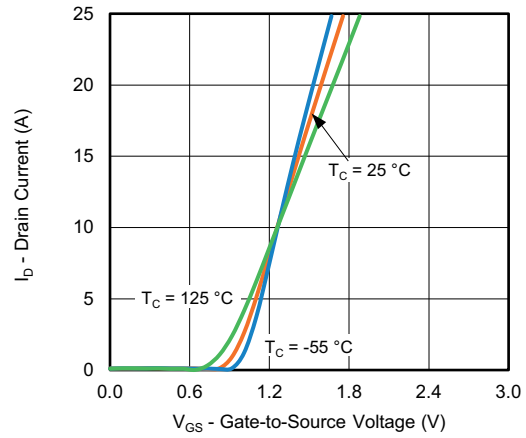
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



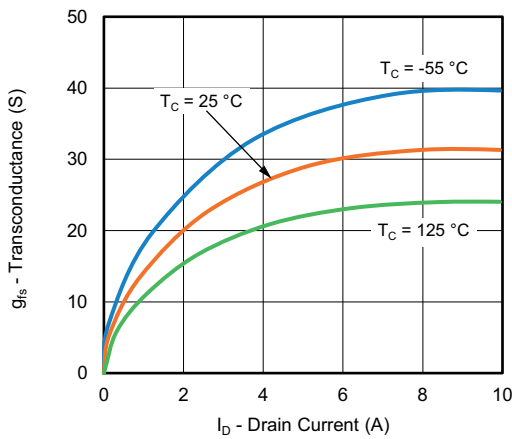
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



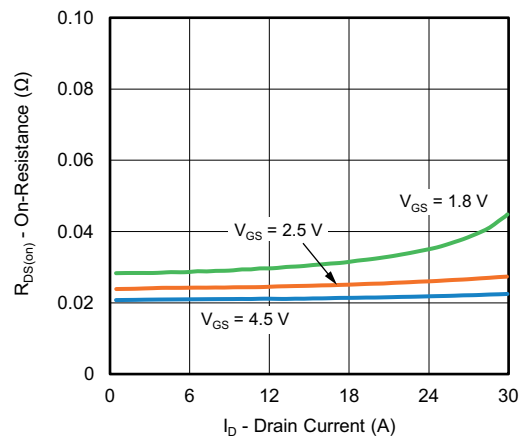
Output Characteristics



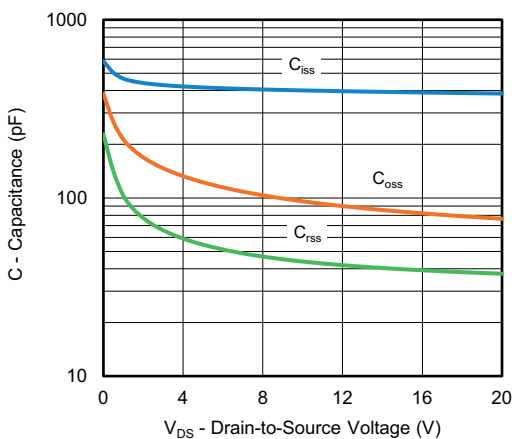
Transfer Characteristics



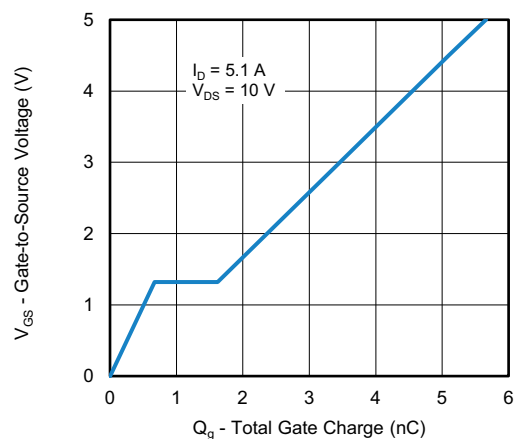
Transconductance



On-Resistance vs. Drain Current



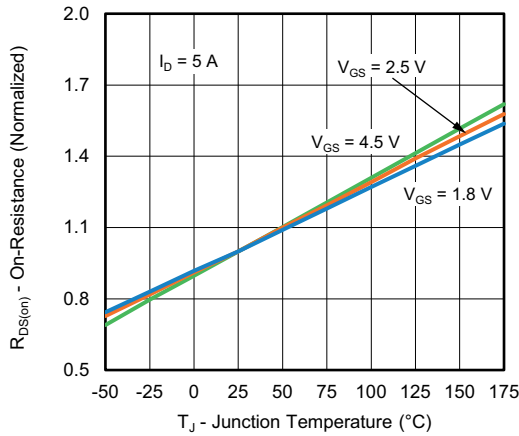
Capacitance



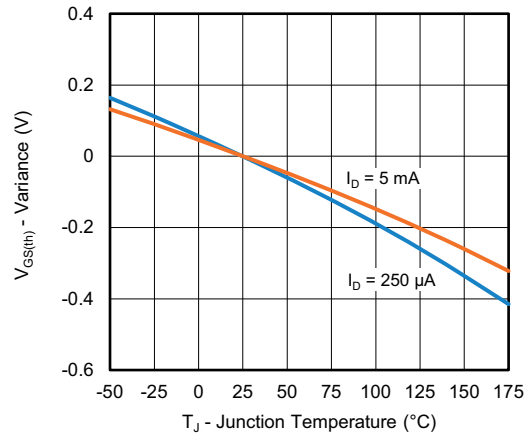
Gate Charge



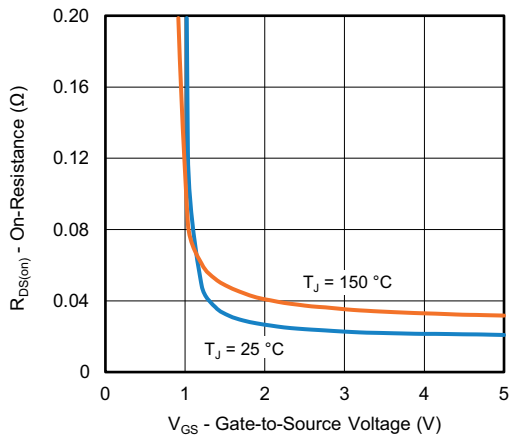
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



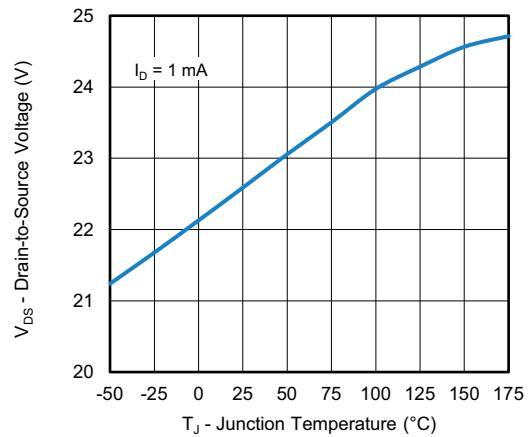
On-Resistance vs. Junction Temperature



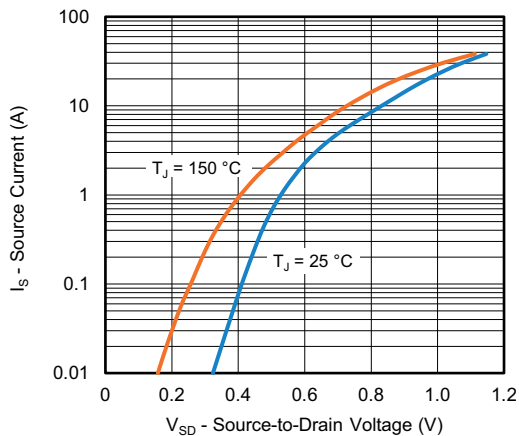
Threshold Voltage



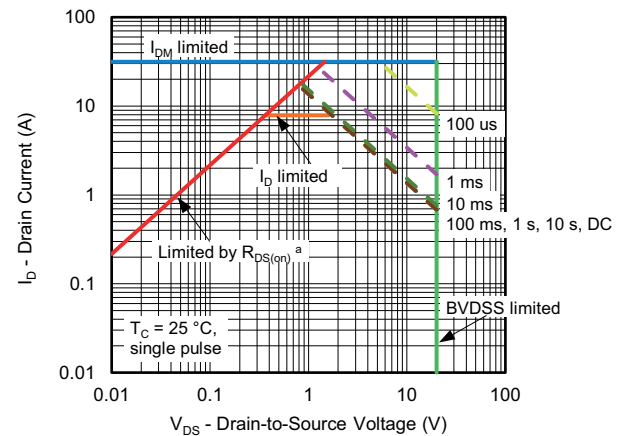
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



Source Drain Diode Forward Voltage



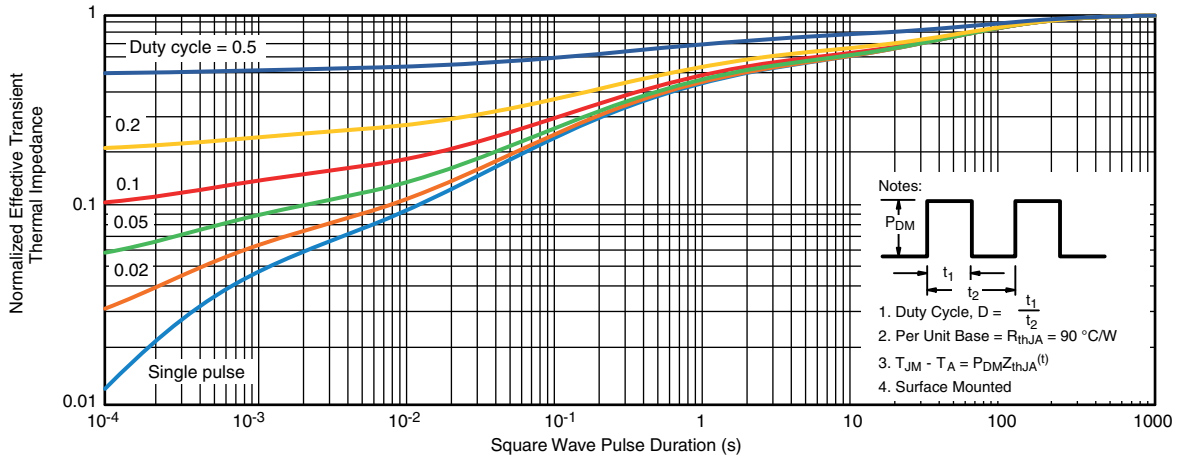
Safe Operating Area

Note

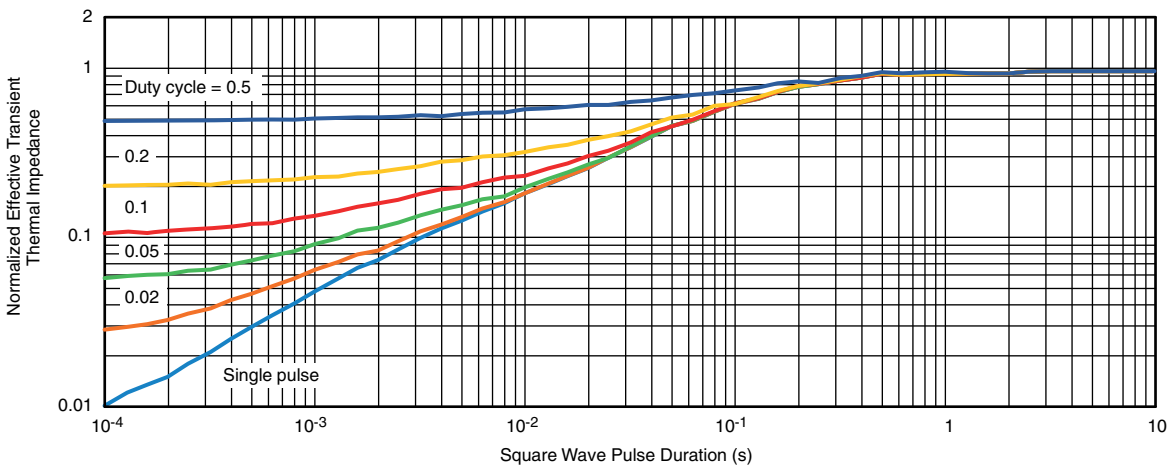
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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