

Introduction [\(Ask a Question\)](#)

Microchip military-grade SmartFusion[®] 2 SoC FPGA and IGLOO[®] 2 FPGA families integrate an industry standard 4-input Look-up Table (LUT)-based FPGA fabric with integrated mathblocks, multiple embedded memory blocks, and high-performance SerDes communications interfaces on a single chip. Both families benefit from low power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to 5 MB of embedded RAM, up to 16 SerDes lanes, and up to four PCI Express[®] Gen 1 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion 2 military grade devices integrate an entire low power real time Microcontroller Subsystem with a rich set of Industry standard peripherals including Ethernet, USB, and CAN, while the IGLOO 2 military devices integrate a high-performance memory subsystem with on-chip flash, 32 kB embedded SRAM, and multiple DMA controllers.

Device Status [\(Ask a Question\)](#)

Table 1. IGLOO[®] 2 FPGA and SmartFusion[®] 2 SoC FPGA Device Status

| Design Security Device Densities | Status |
|----------------------------------|------------|
| 010T | Production |
| 025T | Production |
| 050T | Production |
| 060T | Production |
| 090T | Production |
| 150T | Production |
| Data Security Device Densities | Status |
| 010TS | Production |
| 025TS | Production |
| 050TS | Production |
| 060TS | Production |
| 090TS | Production |
| 150TS | Production |

Product Briefs and Pin Descriptions [\(Ask a Question\)](#)

The product brief and pin descriptions are published separately:

- [PB0121: IGLOO 2 Product Brief](#)
- [DS0124: IGLOO 2 Pin Descriptions](#)
- [PB0115: SmartFusion 2 SoC FPGA Product Brief](#)
- [DS0115: SmartFusion 2 Pin Descriptions](#)

Ordering Information [\(Ask a Question\)](#)

The following figure shows the IGLOO 2 Ordering Information for the M2GL060 device, which explains the various parts and their purposes.

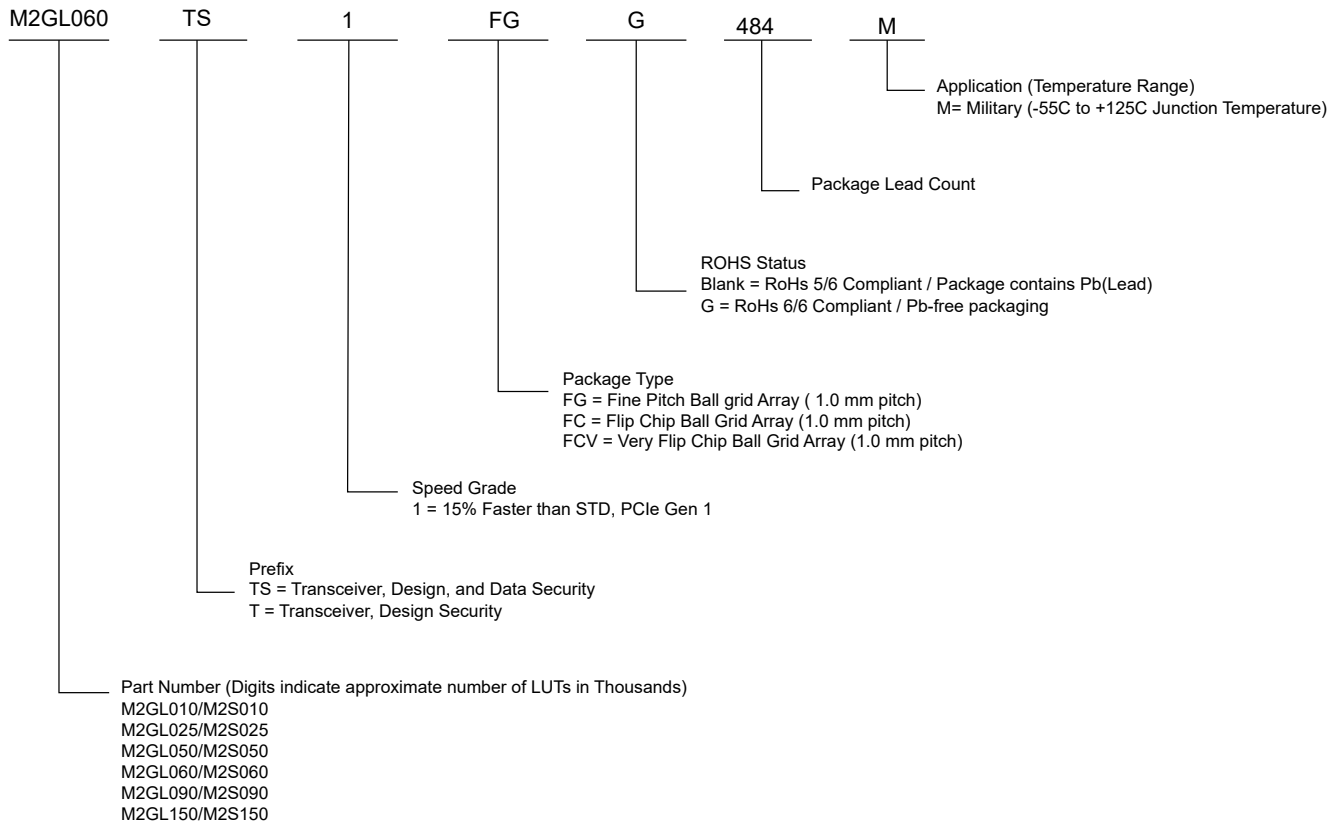


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1. General Specifications [\(Ask a Question\)](#)

This section describes the general specifications of SmartFusion 2 and IGLOO 2 military datasheet.

1.1 Operating Conditions [\(Ask a Question\)](#)

Stresses beyond those listed in the following table may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in the following table is not implied.

Table 1-1. Absolute Maximum Ratings

| Symbol | Parameter | Limits | | Units |
|-------------------------------|---|--------|------|-------|
| | | Min | Max | |
| VDD | DC core supply voltage. Must always power this pin | -0.3 | 1.32 | V |
| VPP | Power supply for charge pumps (for normal operation and programming). Must always power this pin | -0.3 | 3.63 | V |
| MSS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | -0.3 | 3.63 | V |
| HPMS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | -0.3 | 3.63 | V |
| FDDR_PLL_VDDA | Analog power pad for FDDR PLL | -0.3 | 3.63 | V |
| PLL0_PLL1_MSS_MDDR_VDDA | Analog power pad for MDDR PLL | -0.3 | 3.63 | V |
| PLL0_PLL1_HPMS_MDDR_VDDA | Analog power pad for MDDR PLL | -0.3 | 3.63 | V |
| CCC_XX[01]_PLL_VDDA | Analog power pad for PLL0-5 | -0.3 | 3.63 | V |
| SERDES_[01]_PLL_VDDA | High supply voltage for PLL SERDES[01] | -0.3 | 3.63 | V |
| SERDES_[01]_L[0123]_VDDAPLL | Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5V SerDes internal PLL supply | -0.3 | 2.75 | V |
| SERDES_[01]_L[0123]_VDDAIO | TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2V SerDes PMA supply | -0.3 | 1.32 | V |
| SERDES_[01]_VDD | PCIe [®] /PCS power supply | -0.3 | 1.32 | V |
| VDDix | DC FPGA I/O buffer supply voltage for MSIO I/O Bank | -0.3 | 3.63 | V |
| | DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O Banks | -0.3 | 2.75 | V |
| VI | I/O Input voltage for MSIO I/O Bank | -0.3 | 3.63 | V |
| | I/O Input voltage for MSIOD/DDRIO I/O Bank | -0.3 | 2.75 | V |
| VPPNVM | Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP | -0.3 | 3.63 | V |
| T _{STG} ¹ | Storage temperature | -65 | 150 | °C |
| T _J | Junction temperature | — | 145 | °C |

Note:

- For flash programming and retention maximum limits, see [Table 1-3](#). For recommended operating conditions, see [Table 1-2](#).

Table 1-2. Recommended Operating Conditions¹

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------|--|------------|------|-----|------|-------|
| T _J | Operating Junction Temperature | Military | - 55 | 25 | 125 | °C |
| | Programming Junction Temperature ² | — | 0 | 25 | 85 | °C |
| | | — | - 40 | 25 | 100 | °C |
| VDD | DC core supply voltage. Must always power this pin | — | 1.14 | 1.2 | 1.26 | V |

|continued | | | | | | |
|-----------------------------------|---|------------|--------------|-------------|--------------|-------|
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| VPP | Power Supply for Charge Pumps (for Normal Operation and Programming) for 010, 025, 050, and 060 Devices | 2.5V Range | 2.375 | 2.5 | 2.625 | V |
| | | 3.3V Range | 3.15 | 3.3 | 3.45 | V |
| | Power Supply for Charge Pumps (for Normal Operation and Programming) for 090, and 150 devices | 3.3V Range | 3.15 | 3.3 | 3.45 | V |
| MSS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | 2.5V Range | 2.375 | 2.5 | 2.625 | V |
| | | 3.3V Range | 3.15 | 3.3 | 3.45 | V |
| HPMS_MDDR_PLL_VDDA | Analog power pad for MDDR PLL | 2.5V Range | 2.375 | 2.5 | 2.625 | V |
| | | 3.3V Range | 3.15 | 3.3 | 3.45 | V |
| FDDR_PLL_VDDA | Analog power pad for FDDR PLL | 2.5V Range | 2.375 | 2.5 | 2.625 | V |
| | | 3.3V Range | 3.15 | 3.3 | 3.45 | V |
| PLL0_PLL1_MSS_MDDR_VDDA | Analog power pad for MDDR PLL | 2.5V Range | 2.375 | 2.5 | 2.625 | V |
| | | 3.3V Range | 3.15 | 3.3 | 3.45 | V |
| PLL0_PLL1_HPMS_MDDR_VDDA | Analog power pad for MDDR PLL | 2.5V Range | 2.375 | 2.5 | 2.625 | V |
| | | 3.3V Range | 3.15 | 3.3 | 3.45 | V |
| CCC_XX[01]_PLL_VDDA | Analog power pad for PLL0-5 | 2.5V Range | 2.375 | 2.5 | 2.625 | V |
| | | 3.3V Range | 3.15 | 3.3 | 3.45 | V |
| SERDES_[01]_PLL_VDDA ³ | High supply voltage for PLL SERDES[01] | 2.5V Range | 2.375 | 2.5 | 2.625 | V |
| | | 3.3V Range | 3.15 | 3.3 | 3.45 | V |
| SERDES_[01]_L[0123]_VDDAPLL | Analog power for SERDES[01] PLL lanes 0-3. It is a +2.5V SerDes internal PLL supply | — | 2.375 | 2.5 | 2.625 | V |
| SERDES_[01]_L[0123]_VDDAIO | TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. It is a +1.2V SerDes PMA supply | — | 1.14 | 1.2 | 1.26 | V |
| SERDES_[01]_VDD ⁴ | PCIe®/PCS Power supply | — | 1.14 | 1.2 | 1.26 | V |
| VDDIx | 1.2V DC supply voltage | — | 1.14 | 1.2 | 1.26 | V |
| | 1.5V DC supply voltage | — | 1.425 | 1.5 | 1.575 | V |
| | 1.8V DC supply voltage | — | 1.71 | 1.8 | 1.89 | V |
| | 2.5V DC supply voltage | — | 2.375 | 2.5 | 2.625 | V |
| | 3.3V DC supply voltage (MSIO only) | — | 3.15 | 3.3 | 3.45 | V |
| | LVDS differential I/O | — | 2.375 | 2.5 | 3.45 | V |
| | BLVDS, MLVDS, Mini-LVDS, RSDS differential I/O | — | 2.375 | 2.5 | 2.625 | V |
| LVPECL differential I/O | — | 3.15 | 3.3 | 3.45 | V | |
| | — | 3.15 | 3.3 | 3.45 | V | |
| VREFx | Reference Voltage Supply for FDDR and MDDR | — | 0.49 × VDDIx | 0.5 × VDDIx | 0.51 × VDDIx | V |
| VPPNVM | Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP | 2.5V Range | 2.375 | 2.5 | 2.625 | V |
| | | 3.3V Range | 3.15 | 3.3 | 3.45 | V |

Notes:

1. PLL supply voltages should be either 2.5V or 3.3V. Mixed voltages are not allowed.
2. Programming at this temperature range is available only with VPP in 3.3V range.
3. Power supply ramps must all be strictly monotonic, without plateaus.
4. The SERDES_[01]_VDD supply must be connected to VDD.
5. This product is designed and validated for operation within the junction temperature (T_J) range specified in the Recommended Operating Conditions in this datasheet. Device functionality and performance outside this recommended operating range are not supported. Customers should account for the temperature difference between ambient (T_A) and junction (T_J) in their thermal environment and specific use case, which may result in a different and typically narrower ambient (T_A) operating temperature range.

Table 1-3. FPGA Operating Limits

| Product Grade | Element | Programming Temperature | Operating Temperature | Programming Cycles | Digest Cycles per Programming Cycle | Retention (Biased/Unbiased) |
|-----------------------|---------|--|--|--------------------|-------------------------------------|-----------------------------|
| Military ¹ | FPGA | Min T_J = 0 °C Max T_J = 85 °C | Min T_J = -55 °C Max T_J = 100 °C | 500 | 2000 | 20 years |
| | | Min T_J = -40 °C Max T_J = 100 °C | Min T_J = -55 °C Max T_J = 125 °C | 500 | 2000 | 10 years |

Note:

1. Programming at these temperature ranges is available only with VPP = 3.3V.

Table 1-4. Embedded Flash Limits

| Product Grade | Element | Programming Temperature | Maximum Operating Temperature | Programming Cycles | Retention (Biased/Unbiased) |
|---------------|----------------|--|--|--|-----------------------------|
| Military | Embedded flash | Min T_J = -55 °C Max T_J = 125 °C | Min T_J = -55 °C Max T_J = 125 °C | < 10,000 cycles per pages, up to one million cycles per eNVM array | 10 years |
| | | Min T_J = -55 °C Max T_J = 100 °C | Min T_J = -55 °C Max T_J = 100 °C | < 10,000 cycles per pages, up to one million cycles per eNVM array | 20 years |

Table 1-5. Device Storage Temperature and Retention

| Product Grade | Storage Temperature (T_{stg}) | Retention |
|---------------|--|-----------|
| Military | Min T_J = -55 °C Max T_J = 125 °C | 10 years |
| | Min T_J = -55 °C Max T_J = 100 °C | 20 years |

Figure 1-1. High Temperature Data Retention (HTR)

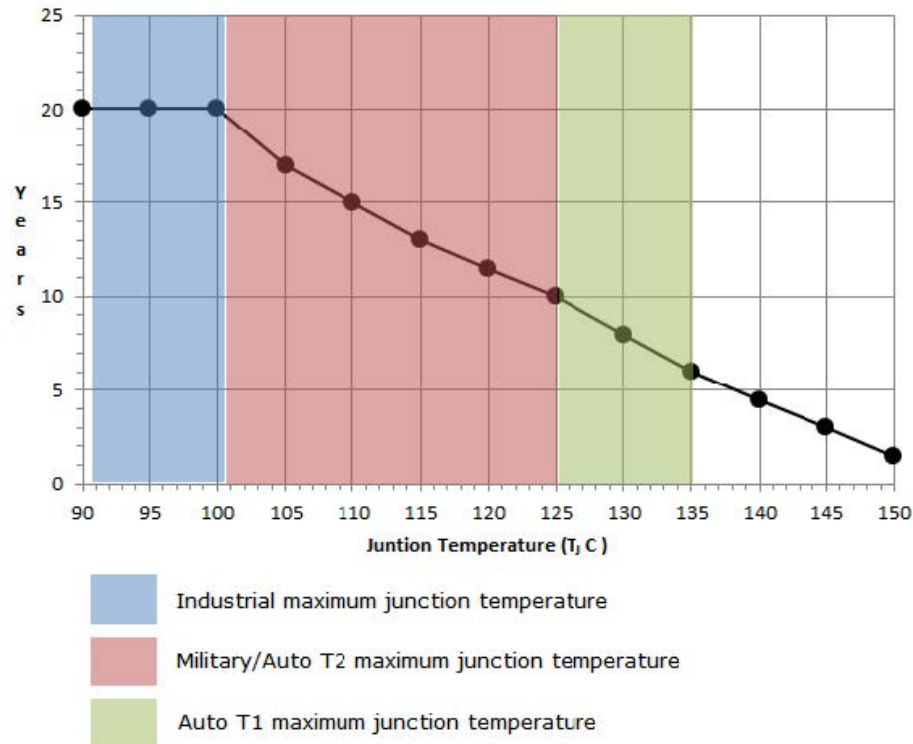


Table 1-6. High Temperature Data Retention (HTR)

| T_j (°C) | HTR Lifetime ^{1, 2} (years) |
|------------|--------------------------------------|
| 90 | 20.0 |
| 95 | 20.0 |
| 100 | 20.0 |
| 105 | 17.0 |
| 110 | 15.0 |
| 115 | 13.0 |
| 120 | 11.5 |
| 125 | 10.0 |
| 130 | 8.0 |
| 135 | 6.0 |
| 140 | 4.5 |
| 145 | 3.0 |
| 150 | 1.5 |

Notes:

- HTR lifetime is the period during which a verify failure is not expected due to flash leakage.
- The IGLOO 2 and SmartFusion 2 Military Grade maximum operational junction temperature specification is 125 °C.

1.2 Overshoot/Undershoot Limits [\(Ask a Question\)](#)

For AC signals, the input signal may undershoot during transitions to -1.0V for no longer than 10% or the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal may overshoot during transitions to VCCI +1.0V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

Note: The above specification does not apply to the PCI standard. The IGLOO® 2 and SmartFusion® 2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

1.3 Thermal Characteristics [\(Ask a Question\)](#)

The temperature variable in the Microchip Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures.

The following equations give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

where,

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JB} = Junction-to-board thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_B = Board temperature (measured 1.0 mm away from the package edge)
- T_C = Case temperature
- P = Total power dissipated by the device

Table 1-7. Package Thermal Resistance

| Product M2GL/M2S | θ_{JA} | | | θ_{JB} | θ_{JC} | Units |
|------------------|---------------|---------|---------|---------------|---------------|-------|
| | Still Air | 1.0 m/s | 2.5 m/s | | | |
| 010 | | | | | | |
| FG484 | 18.22 | 14.83 | 13.62 | 8.83 | 4.92 | °C/W |
| 025 | | | | | | |
| FG484 | 17.03 | 13.66 | 12.45 | 7.66 | 4.18 | °C/W |
| 050 | | | | | | |
| FG484 | 15.29 | 12.19 | 10.99 | 6.27 | 3.24 | °C/W |
| 060 | | | | | | |
| FG484 | 15.40 | 12.06 | 10.85 | 6.14 | 3.15 | °C/W |
| 090 | | | | | | |
| FG484 | 14.64 | 11.37 | 10.16 | 5.43 | 2.77 | °C/W |
| 150 | | | | | | |
| FC1152 | 9.08 | 6.81 | 5.87 | 2.56 | 0.38 | °C/W |

1.3.1 Theta-JA [\(Ask a Question\)](#)

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It must be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using the following equation.

$$\text{Maximum Power Allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

The absolute maximum junction temperature is 100 °C. The following equation shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050-FG484 package at military temperature and in still air, where:

$$\theta_{JA} = 15.29 \text{ °C/W (taken from Table 1-7).}$$

$$T_A = 85 \text{ °C}$$

$$\text{Maximum Power Allowed} = \frac{100\text{°C} - 85\text{°C}}{15.29\text{°C/W}} = 0.981 \text{ W}$$

The power consumption of a device can be calculated using the Microchip power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

1.3.2 Theta-JB [\(Ask a Question\)](#)

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

1.3.3 Theta-JC [\(Ask a Question\)](#)

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

2. Power Consumption [\(Ask a Question\)](#)

2.1 Quiescent Supply Current [\(Ask a Question\)](#)

Table 2-1. Quiescent Supply Current Characteristics

| Power Supplies/Blocks | Modes and Configurations | |
|--|--------------------------|-------------------|
| | Non-Flash*Freeze Mode | Flash*Freeze Mode |
| FPGA Core | ON | OFF |
| VDD / SERDES_[01]_VDD ¹ | ON | ON |
| VPP / VPPNVM | ON | ON |
| MDDR_PLL_VDDA CCC_XX[01]_PLL_VDDA PLL0_PLL1_MDDR_VDDA FDDR_PLL_VDDA | 0V | 0V |
| SERDES_[01]_PLL_VDDA ² | 0V | 0V |
| SERDES_[01]_L[0123]_VDDAPLL / VDD_2V5 ² | ON | ON |
| SERDES_[01]_L[0123]_VDDAIIO ² | ON | ON |
| VDDIx ^{3, 4} | ON | ON |
| VREFx | ON | ON |
| MSSDDR CLK | 32 kHz | 32 kHz |
| RAM | ON | Sleep state |
| HPMS Controller | 50 MHz | 50 MHz |
| 50 MHz Oscillator (enable/disable) | Enabled | Disabled |
| 1 MHz Oscillator (enable/disable) | Disabled | Disabled |
| Crystal Oscillator (enable/disable) | Disabled | Disabled |

Notes:

- SERDES_[01]_VDD Power Supply is shorted to VDD.
- SERDES and DDR blocks to be unused.
- VDDIx has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI Bank supplies. For details on bank power supplies, refer to the “Recommendation for Unused Bank Supplies” table in the [AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note](#).
- No differential (that is to say, LVDS) I/O's or ODT attributes to be used.

Table 2-2. SmartFusion[®] 2 and IGLOO[®] 2 Quiescent Supply Current—Typical Process

| Parameter | Modes | Conditions | 010 | 025 | 050 | 060 | 090 | 150 | Units |
|-----------|------------------|------------------------------------|------------|------------|------------|------------|------------|------------|-------|
| | | | VDD = 1.2V | VDD = 1.2V | VDD = 1.2V | VDD = 1.2V | VDD = 1.2V | VDD = 1.2V | |
| IDC1 | Non-Flash*Freeze | Typical (T _J = 25 °C) | 6.9 | 8.9 | 13.1 | 15.3 | 15.4 | 27.5 | mA |
| | | Military (T _J = 125 °C) | 73.0 | 106.4 | 180.9 | 215.4 | 217.5 | 390.5 | mA |
| IDC2 | Flash*Freeze | Typical (T _J = 25 °C) | 2.6 | 3.7 | 5.1 | 5.0 | 5.1 | 8.9 | mA |
| | | Military (T _J = 125 °C) | 55.6 | 74.2 | 98.5 | 98.5 | 99.5 | 161.0 | mA |

Table 2-3. SmartFusion® 2 and IGLOO® 2 Quiescent Supply Current–Worst-Case Process

| Parameter | Modes | Conditions | 010 | 025 | 050 | 060 | 090 | 150 | Units |
|-----------|------------------|------------------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------|
| | | | VDD = 1.26V | VDD = 1.26V | VDD = 1.26V | VDD = 1.26V | VDD = 1.26V | VDD = 1.26V | |
| IDC1 | Non-Flash*Freeze | Military (T _J = 125 °C) | 151.5 | 227.4 | 358.9 | 438.8 | 443.1 | 660.4 | mA |
| IDC2 | Flash*Freeze | Military (T _J = 125 °C) | 127.2 | 144.2 | 174.6 | 193.1 | 195.0 | 236.3 | mA |

2.2 Programming Currents [\(Ask a Question\)](#)

The following tables represent programming, verify and Inrush currents for SmartFusion 2 SoC and IGLOO 2 FPGA devices.

Table 2-4. Currents During Program Cycle, 0 °C ≤ T_J ≤ 85 °C, Typical Process

| Power Supplies | Voltage (V) | 010 | 025 | 050 | 060 | 090 | 150 | Units |
|---------------------|-------------------|-----|-----|-----|-----|-----|-----|-------|
| VDD | 1.26 | 53 | 55 | 58 | 30 | 42 | 52 | mA |
| VPP ¹ | 3.46 | 11 | 6 | 10 | 9 | 12 | 12 | mA |
| VPPNVM ¹ | 3.46 | 2 | 2 | 3 | 3 | 3 | — | mA |
| VDDI | 2.62 ² | 16 | 17 | 1 | 12 | 12 | 81 | mA |
| | 3.46 ² | 31 | 36 | 1 | 12 | 17 | 84 | mA |
| Number of banks | | 8 | 8 | 10 | 10 | 9 | 19 | — |

Notes:

- VPP and VPPNVM are internally shorted for the 150 device.
- The current for 050 device represents JTAG I/O bank only.

Table 2-5. Currents During Verify Cycle, 0 °C ≤ T_J ≤ 85 °C, Typical Process

| Power Supplies | Voltage (V) | 010 | 025 | 050 | 060 | 090 | 150 | Units |
|---------------------|-------------------|-----|-----|-----|-----|-----|-----|-------|
| VDD | 1.26 | 53 | 55 | 58 | 33 | 41 | 51 | mA |
| VPP ¹ | 3.46 | 5 | 3 | 15 | 8 | 11 | 12 | mA |
| VPPNVM ¹ | 3.46 | 0 | 0 | 1 | 0 | 1 | — | mA |
| VDDI | 2.62 ² | 16 | 17 | 1 | 12 | 11 | 81 | mA |
| | 3.46 ² | 32 | 36 | 1 | 12 | 17 | 84 | mA |
| Number of banks | | 8 | 8 | 10 | 10 | 9 | 19 | — |

Notes:

- VPP and VPPNVM are internally shorted for the 150 device.
- The current for 050 device represents JTAG I/O bank only.

Table 2-6. Inrush Currents at Power up, –55 °C ≤ T_J ≤ 125 °C, Typical Process

| Power Supplies | Voltage (V) | 010 | 025 | 050 | 060 | 090 | 150 | Units |
|-----------------|-------------|-----|-----|-----|-----|-----|-----|-------|
| VDD | 1.26 | 53 | 78 | 57 | 54 | 98 | 140 | mA |
| VPP | 3.46 | 57 | 50 | 180 | 14 | 36 | 51 | mA |
| VDDI | 2.62 | 141 | 161 | 187 | 106 | 283 | 404 | mA |
| Number of banks | | 8 | 8 | 10 | 10 | 9 | 19 | — |

3. Average Fabric Temperature and Voltage Derating Factors [\(Ask a Question\)](#)

Table 3-1. Average Temperature and Voltage Derating Factors for Fabric Timing Delays—(Normalized to $T_j = 125\text{ }^\circ\text{C}$, Worst-Case VDD = 1.14V)

| Core Voltage VDD (V) | Junction Temperature ($^\circ\text{C}$) | | | | | | | |
|----------------------|---|----------------------|--------------------|---------------------|---------------------|---------------------|----------------------|----------------------|
| | -55 $^\circ\text{C}$ | -40 $^\circ\text{C}$ | 0 $^\circ\text{C}$ | 25 $^\circ\text{C}$ | 70 $^\circ\text{C}$ | 85 $^\circ\text{C}$ | 100 $^\circ\text{C}$ | 125 $^\circ\text{C}$ |
| 1.14 | 0.91 | 0.91 | 0.93 | 0.94 | 0.96 | 0.97 | 0.98 | 1.00 |
| 1.2 | 0.82 | 0.83 | 0.84 | 0.85 | 0.87 | 0.87 | 0.88 | 0.90 |
| 1.26 | 0.75 | 0.75 | 0.77 | 0.77 | 0.79 | 0.80 | 0.81 | 0.75 |

4. Timing Model (Ask a Question)

Figure 4-1. Timing Model

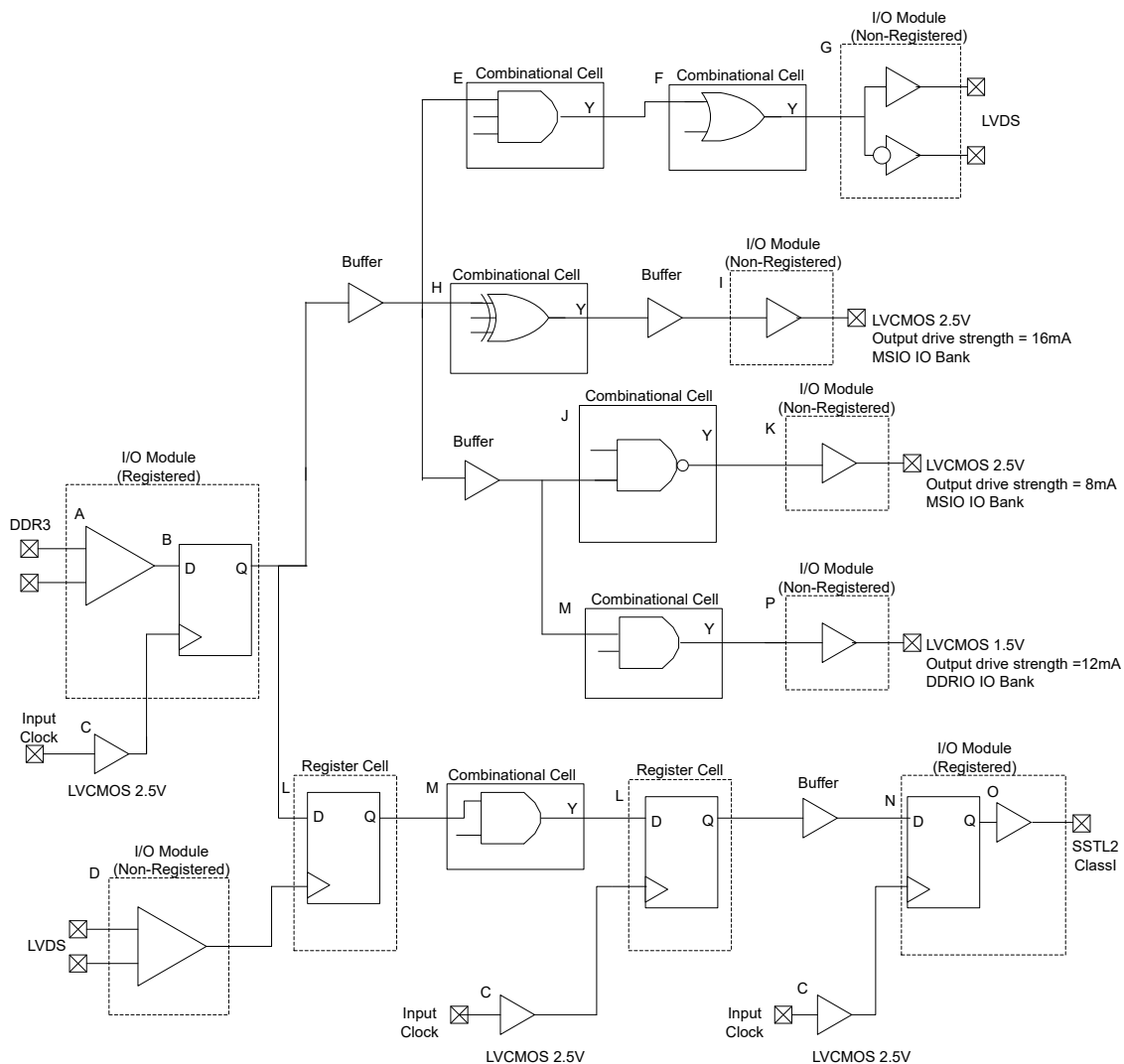


Table 4-1. Timing Model Parameters

| Index | Parameter | Description | Speed Grade -1 (ns) | Notes |
|-------|------------|---------------------------------------|---------------------|--|
| A | t_{PY} | Propagation Delay of DDR3 Receiver | 1.672 | Refer to Table 5-55 for more information |
| B | t_{CLKQ} | Clock-to-Q of the Input Data Register | 0.165 | Refer to Table 5-93 for more information |
| | t_{ISUD} | Setup Time of the Input Data Register | 0.369 | Refer to Table 5-93 for more information |

.....continued

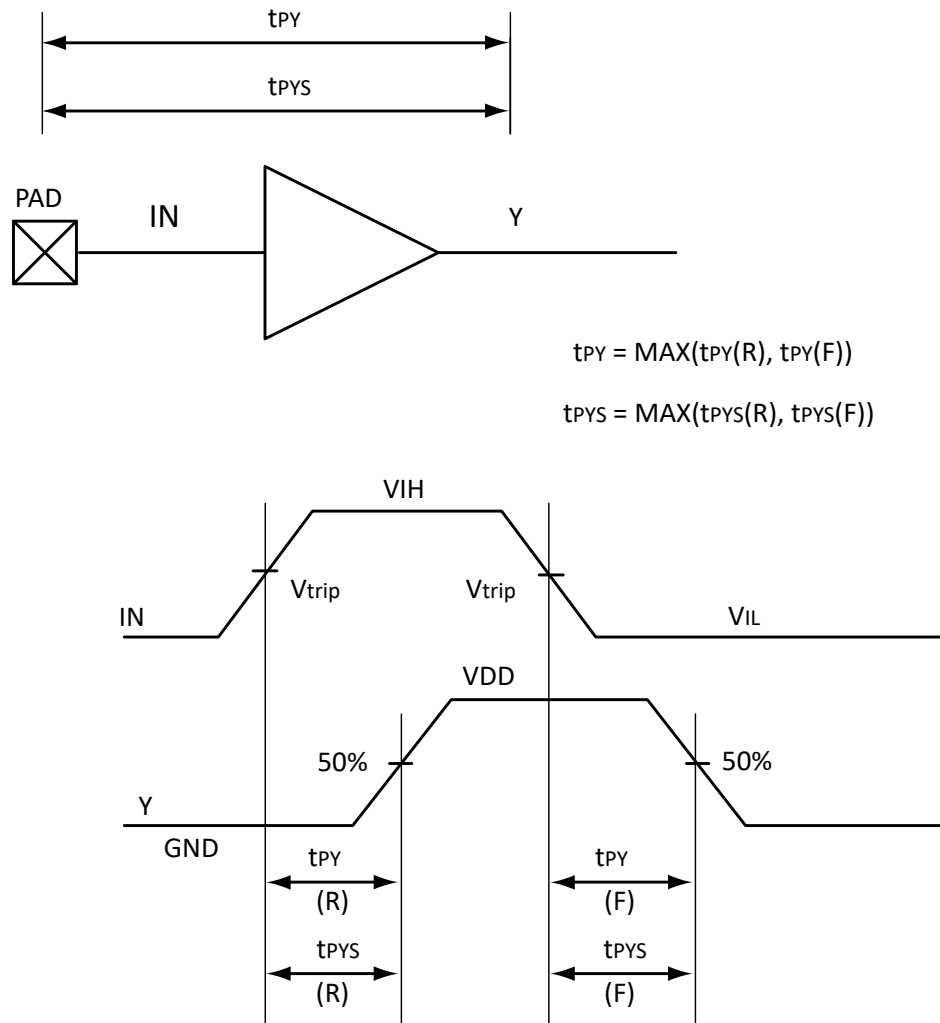
| Index | Parameter | Description | Speed Grade -1 (ns) | Notes |
|-------|-------------|--|---------------------|--|
| C | t_{RCKH} | Input High Delay for Global Clock | 1.55 | Refer to Table 7-1 for more information |
| | t_{RCKL} | Input Low Delay for Global Clock | 0.861 | Refer to Table 7-1 for more information |
| D | t_{PY} | Input Propagation Delay of LVDS Receiver | 3.061 | Refer to Table 5-70 for more information |
| E | t_{DP} | Propagation Delay of a three input AND Gate | 0.217 | Refer to Table 6-1 for more information |
| F | t_{DP} | Propagation Delay of a OR Gate | 0.17 | Refer to Table 6-1 for more information |
| G | t_{DP} | Propagation Delay of a LVDS Transmitter | 2.299 | Refer to Table 5-70 for more information |
| H | t_{DP} | Propagation Delay of a three input XOR Gate | 0.236 | Refer to Table 6-1 for more information |
| I | t_{DP} | Propagation Delay of LVCMOS 2.5V Transmitter, Drive strength of 16 mA on the MSIO Bank | 2.717 | Refer to Table 5-17 for more information |
| J | t_{DP} | Propagation Delay of a two input NAND Gate | 0.17 | Refer to Table 6-1 for more information |
| K | t_{DP} | Propagation Delay of LVCMOS 2.5V Transmitter, Drive strength of 8mA on the MSIO Bank | 2.594 | Refer to Table 5-17 for more information |
| L | t_{CLKQ} | Clock-to-Q of the Data Register | 0.112 | Refer to Table 5-93 for more information |
| | t_{SUD} | Setup Time of the Data Register | 0.262 | Refer to Table 5-93 for more information |
| M | t_{DP} | Propagation Delay of a two input AND gate | 0.17 | Refer to Table 6-1 for more information |
| N | t_{OCLKQ} | Clock-to-Q of the Output Data Register | 0.272 | Refer to Table 5-94 for more information |
| | t_{OSUD} | Setup Time of the Output Data Register | 0.196 | Refer to Table 5-94 for more information |
| O | t_{DP} | Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank | 2.283 | Refer to Table 5-48 for more information |
| P | t_{DP} | Propagation Delay of LVCMOS 1.5V Transmitter, Drive strength of 12 mA, fast slew on the DDRIO Bank | 3.703 | Refer to Table 5-17 for more information |

5. User I/O Characteristics [\(Ask a Question\)](#)

There are three types of I/Os supported in the IGLOO 2 FPGA and SmartFusion 2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the "I/Os" section of the [UG0445: IGLOO 2 FPGA and SmartFusion 2 SoC FPGA Fabric User Guide](#).

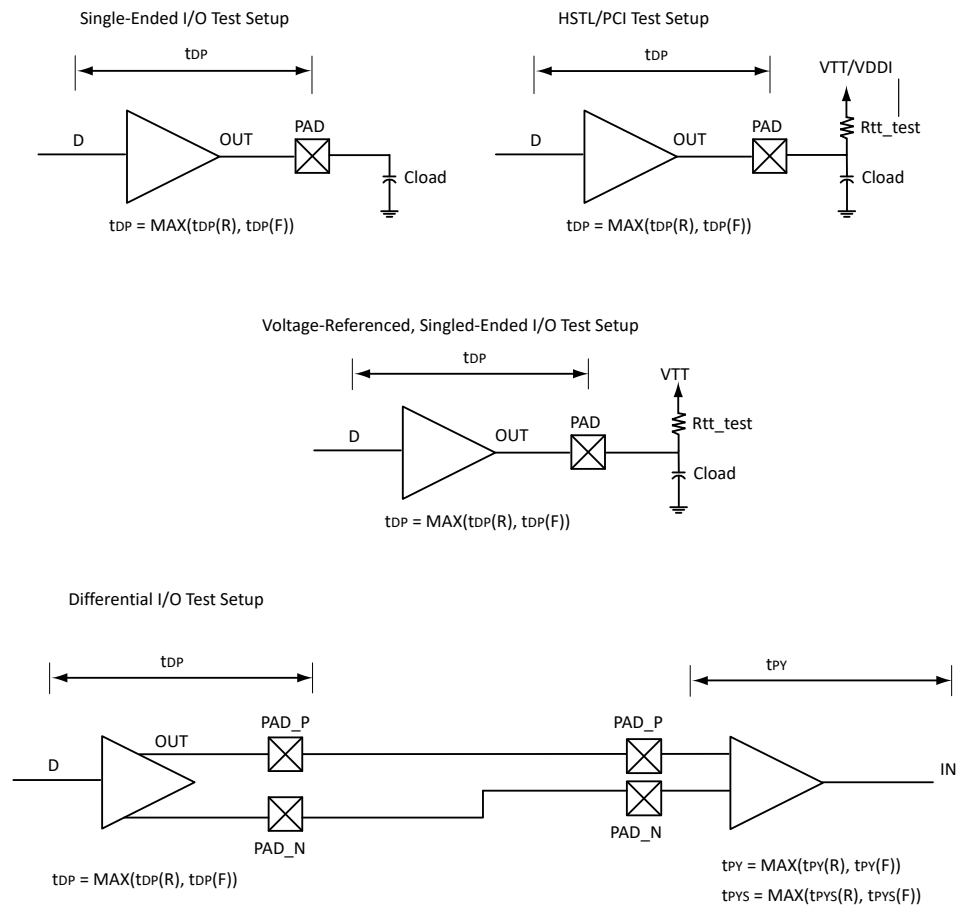
5.1 Input Buffer and AC Loading [\(Ask a Question\)](#)

Figure 5-1. Input Buffer AC Loading



5.2 Output Buffer and AC Loading [\(Ask a Question\)](#)

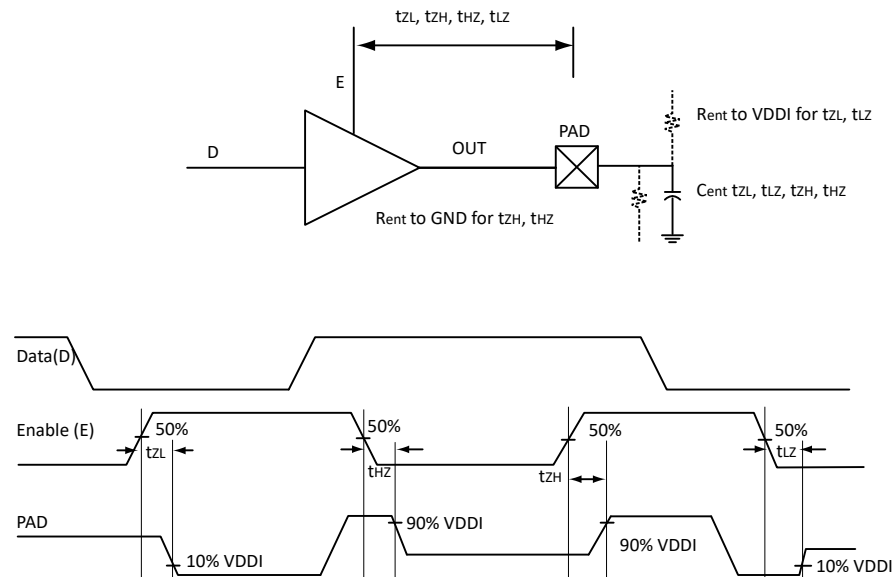
Figure 5-2. Output Buffer AC Loading



5.3 Tristate Buffer and AC Loading [\(Ask a Question\)](#)

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in the following figure.

Figure 5-3. Tristate Buffer for Enable Path Test Point



5.4 I/O Speeds [\(Ask a Question\)](#)

Table 5-1. Maximum Data Rate Summary for Worst-Case Military Conditions

| Single-Ended I/O | MSIO | MSIOD | DDRIO | Units |
|---------------------------|------|-------|-------|-------|
| PCI 3.3V | 560 | — | — | Mbps |
| LVTTTL 3.3V | 540 | — | — | Mbps |
| LVC MOS 3.3V | 540 | — | — | Mbps |
| LVC MOS 2.5V | 360 | 370 | 360 | Mbps |
| LVC MOS 1.8V | 260 | 360 | 360 | Mbps |
| LVC MOS 1.5V | 140 | 190 | 210 | Mbps |
| LVC MOS 1.2V | 100 | 140 | 180 | Mbps |
| LPDDR - LVC MOS 1.8V Mode | — | — | 360 | Mbps |
| Voltage-Referenced I/O | MSIO | MSIOD | DDRIO | Units |
| LPDDR | — | — | 360 | Mbps |
| HSTL1.5V | — | — | 360 | Mbps |
| SSTL 2.5V | 450 | 480 | 360 | Mbps |
| SSTL 1.8V | — | — | 600 | Mbps |
| SSTL 1.5V | — | — | 600 | Mbps |
| Differential I/O | MSIO | MSIOD | DDRIO | Units |
| LVPECL (input only) | 810 | — | — | Mbps |
| LVDS 3.3V | 480 | 480 | — | Mbps |
| LVDS 2.5V | 480 | 480 | — | Mbps |
| RS DS | 460 | 480 | — | Mbps |
| BLVDS | 450 | — | — | Mbps |
| MLVDS | 450 | — | — | Mbps |
| Mini-LVDS | 460 | 480 | — | Mbps |

Table 5-2. Maximum Frequency Summary for Worst-Case Military Conditions

| Single-Ended I/O | MSIO | MSIOD | DDRIO | Units |
|---------------------------|------|-------|-------|-------|
| PCI 3.3V | 280 | — | — | MHz |
| LVTTTL 3.3V | 270 | — | — | MHz |
| LVC MOS 3.3V | 270 | — | — | MHz |
| LVC MOS 2.5V | 180 | 185 | 180 | MHz |
| LVC MOS 1.8V | 130 | 180 | 180 | MHz |
| LVC MOS 1.5V | 70 | 95 | 105 | MHz |
| LVC MOS 1.2V | 50 | 70 | 90 | MHz |
| LPDDR - LVC MOS 1.8V mode | | — | 180 | MHz |
| Voltage-Referenced I/O | MSIO | MSIOD | DDRIO | Units |
| LPDDR | — | — | 180 | MHz |
| HSTL1.5V | — | — | 180 | MHz |
| SSTL 2.5V | 225 | 240 | 180 | MHz |
| SSTL 1.8V | — | — | 300 | MHz |
| SSTL 1.5V | — | — | 300 | MHz |
| Differential I/O | MSIO | MSIOD | DDRIO | Units |
| LVPECL (Input only) | 405 | — | — | MHz |
| LVDS 3.3V | 240 | 240 | — | MHz |
| LVDS 2.5V | 240 | 240 | — | MHz |
| RS DS | 230 | 240 | — | MHz |
| BLVDS | 225 | — | — | MHz |
| MLVDS | 225 | — | — | MHz |
| Mini-LVDS | 230 | 240 | — | MHz |

5.5 Detailed I/O Characteristics [\(Ask a Question\)](#)

Table 5-3. Input Capacitance

| Symbol | Definition | Condition | Min | Max | Units |
|----------------------|---|--------------------------|-----|-----|-------|
| C _{IN} | Input Capacitance | — | — | 10 | pF |
| I _{IL} (DC) | Input current LOW (applicable to HSTL/SSTL inputs only) ¹ | V _{DDI} = 2.5V | — | 400 | μA |
| | | V _{DDI} = 1.8V | — | 500 | μA |
| | | V _{DDI} = 1.5 V | — | 600 | μA |
| | Input current LOW (applicable to all other digital inputs) | — | — | 10 | μA |
| I _{IH} (DC) | Input current HIGH (applicable to HSTL/SSTL inputs only) ¹ | V _{DDI} = 2.5V | — | 400 | μA |
| | | V _{DDI} = 1.8V | — | 500 | μA |
| | | V _{DDI} = 1.5V | — | 600 | μA |
| | Input current HIGH (applicable to all other digital inputs) | — | — | 10 | μA |
| T _{RAMPIN} | Input ramp time (applicable to all digital inputs) ² | — | — | 50 | ns |

Notes:

1. Applicable when an I/O pair is programmed with an HSTL or SSTL I/O type on the IOP pad and an un-terminated I/O type (such as LVC MOS) on the ION pad.
2. The voltage ramp must be monotonic.
3. Device inputs on MSIO, M SIOD, and DEVRST pins are verified to function up to 1 ms ramp rate with no reliability issues. Timing is only characterized to 50 ns.

Table 5-4. I/O Weak Pull-Up/Pull-Down Resistance Values for DDRIO, MSIO, and MSIOD Banks—Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

| VDDI Domain | DDRIO I/O Bank | | | | MSIO I/O Bank | | | | MSIOD I/O Bank | | | |
|----------------------|---|-------|---|-------|---|-------|---|-------|---|-------|---|-------|
| | $R_{(WEAK\ PULL-UP)}$ at VOH (Ω) | | $R_{(WEAK\ PULL-DOWN)}$ at VOL (Ω) | | $R_{(WEAK\ PULL-UP)}$ at VOH (Ω) | | $R_{(WEAK\ PULL-DOWN)}$ at VOL (Ω) | | $R_{(WEAK\ PULL-UP)}$ at VOH (Ω) | | $R_{(WEAK\ PULL-DOWN)}$ at VOL (Ω) | |
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| 3.3V | N/A | N/A | N/A | N/A | 9.9k | 17.1k | 9.98k | 17.5k | N/A | N/A | N/A | N/A |
| 2.5V ^{1, 2} | 10k | 17.8k | 9.98k | 18k | 10k | 17.6k | 10.1k | 18.4k | 9.6k | 16.6k | 9.5k | 16.4k |
| 1.8V ^{1, 2} | 10.3k | 19.1k | 10.3k | 19.5k | 10.4k | 19.1k | 10.4k | 20.4k | 9.7k | 17.3k | 9.7k | 17.1k |
| 1.5V ^{1, 2} | 10.6k | 20.2k | 10.6k | 21.1k | 10.7k | 20.4k | 10.8k | 22.2k | 9.9k | 18k | 9.8k | 17.6k |
| 1.2V ^{1, 2} | 11.1k | 22.7k | 11.2k | 24.6k | 11.3k | 23.2k | 11.5k | 26.7k | 10.3k | 19.6k | 10k | 19.1k |

Notes:

- $R_{(WEAK\ PULL-DOWN)} = (VOL_{spec})/I_{(WEAK\ PULL-DOWN\ MAX)}$
- $R_{(WEAK\ PULL-UP)} = (VDDI_{max} - VOH_{spec})/I_{(WEAK\ PULL-UP\ MIN)}$

Table 5-5. Schmitt Trigger Input Hysteresis—Hysteresis Voltage Value for Schmitt Trigger Mode Input Buffers

| Input Buffer Configuration | Hysteresis Value (Typical, unless otherwise noted) |
|------------------------------|--|
| 3.3V LVTTTL/LVCMOS/PCI/PCI-X | $0.05 \times VDDI$ (Worst-case) |
| 2.5V LVCMOS | $0.05 \times VDDI$ (Worst-case) |
| 1.8V LVCMOS | $0.1 \times VDDI$ (Worst-case) |
| 1.5V LVCMOS | 60 mV |
| 1.2V LVCMOS | 20 mV |

5.6 Single-Ended I/O Standards [\(Ask a Question\)](#)**5.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)** [\(Ask a Question\)](#)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO 2 FPGAs and SmartFusion 2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

5.6.2 3.3V LVCMOS/LVTTTL [\(Ask a Question\)](#)

LVCMOS 3.3V or Low-Voltage Transistor-Transistor Logic (LVTTTL) is a general standard for 3.3V applications.

5.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification [\(Ask a Question\)](#)**Table 5-6.** LVTTTL/LVCMOS 3.3V DC Voltage Specification (Applicable to MSIO I/O Bank Only)

| Symbol | Parameters | Conditions | Min | Typ | Max | Units |
|---|----------------------|------------|------|-----|-------------------------------|-------|
| LVTTTL/LVCMOS 3.3V Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 3.15 | 3.3 | 3.45 | V |
| LVTTTL/LVCMOS 3.3V DC Input Voltage Specification | | | | | | |
| VIH (DC) | DC input logic High | | 2.0 | — | 3.45 | V |
| VIL (DC) | DC input logic Low | | -0.3 | — | 0.8 | V |
| IIH (DC) | Input current High | | — | — | See Table 5-3 | — |
| IIL (DC) | Input current Low | | — | — | See Table 5-3 | — |
| LVCMOS 3.3V DC Output Voltage Specification | | | | | | |
| VOH ¹ | DC output logic High | | 2.4 | — | — | V |
| VOL ¹ | DC output logic Low | | — | — | 0.4 | V |

.....continued

| Symbol | Parameters | Conditions | Min | Typ | Max | Units |
|---|----------------------|------------|-----|-----|-----|-------|
| LVTTL 3.3V DC Output Voltage Specification | | | | | | |
| VOH | DC output logic High | | 2.4 | — | — | V |
| VOL | DC output logic Low | | — | — | 0.4 | V |

Note:

1. The VOH/VOL test points selected ensure compliance with LVCMOS 3.3V JESD8-B requirements.

Table 5-7. LVTTL/LVCMOS 3.3V Maximum Switching Speeds (Applicable to MSIO I/O Bank Only)

| Symbol | Parameters | Conditions | Min | Typ | Max | Units |
|--|---------------------------------------|--|-----|-----|-----|-------|
| LVTTL/LVCMOS 3.3V Maximum Switching Speed | | | | | | |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 540 | Mbps |

Table 5-8. LVTTL/LVCMOS 3.3V AC Test Parameter Specifications (Applicable to MSIO Bank Only)

| Symbol | Parameters | Conditions | Min | Typ | Max | Units |
|---|--|------------|-----|-----|-----|----------|
| LVTTL/LVCMOS 3.3V AC Test Parameter Specifications | | | | | | |
| Vtrip | Measuring/trip point for data path | | — | 1.4 | — | V |
| Rent | Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 2k | — | Ω |
| Cent | Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 5 | — | pF |
| Cload | Capacitive loading for data path (t_{DP}) | | — | 5 | — | pF |

Table 5-9. LVTTL/LVCMOS 3.3V Transmitter Drive Strength Specifications (Applicable to MSIO Bank Only)

| Output Drive Selection | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|------------------------|---------|---------|-----------------|-----------------|
| 2 mA | 2.4 | 0.4 | 2 | 2 |
| 4 mA | 2.4 | 0.4 | 4 | 4 |
| 8 mA | 2.4 | 0.4 | 8 | 8 |
| 12 mA | 2.4 | 0.4 | 12 | 12 |
| 16 mA | 2.4 | 0.4 | 16 | 16 |
| 20 mA | 2.4 | 0.4 | 18 | 18 |

Note: Software Configurator GUI displays the Commercial/Industrial numeric values. The actual drive capability at temperature is defined in the preceding table.

5.6.2.2 AC Switching Characteristics ([Ask a Question](#))**AC Switching Characteristics for Receiver (Input Buffers)****Table 5-10.** LVTTL/LVCMOS 3.3V Receiver Characteristics for MSIO I/O Banks (Input Buffers)—Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, VDD = 1.14V, VDDI = 3.15V

| | On-Die Termination (ODT) | Speed Grade -1 (ns) | |
|---------------------------------------|--------------------------|---------------------|-----------|
| | | t_{PV} | t_{PVS} |
| LVTTL/LVCMOS 3.3V (for MSIO I/O Bank) | None | 2.416 | 2.443 |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**Table 5-11.** LVTTL/LVCMOS 3.3V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)—Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, VDD = 1.14V, VDDI = 3.15V

| Output Drive Selection | Slew Control | Speed Grade -1 (ns) | | | | |
|------------------------|--------------|---------------------|----------|----------|----------|----------|
| | | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} |
| 2 mA | slow | 3.515 | 3.826 | 3.242 | 2.024 | 3.636 |
| 4 mA | slow | 2.565 | 2.948 | 2.774 | 3.339 | 4.896 |

.....continued

| Output Drive Selection | Slew Control | Speed Grade -1 (ns) | | | | |
|------------------------|--------------|---------------------|-----------------|-----------------|-----------------|-----------------|
| | | t _{DP} | t _{ZL} | t _{ZH} | t _{HZ} | t _{LZ} |
| 8 mA | slow | 2.349 | 2.568 | 2.528 | 5.013 | 5.329 |
| 12 mA | slow | 2.261 | 2.324 | 2.386 | 6.389 | 6.05 |
| 16 mA | slow | 2.274 | 2.287 | 2.369 | 6.671 | 6.256 |
| 20 mA | slow | 2.372 | 2.206 | 2.306 | 6.976 | 6.541 |

5.6.3 2.5V LVCMOS [\(Ask a Question\)](#)

LVCMOS 2.5V is a general standard for 2.5V applications and is supported in IGLOO 2 FPGA and SmartFusion 2 SoC FPGAs in compliance to the JEDEC specification JESD8-5A.

5.6.3.1 Minimum and Maximum AC/DC Input and Output Levels Specification [\(Ask a Question\)](#)

Table 5-12. LVCMOS 2.5V DC Voltage Specification

| Symbol | Parameters | Conditions | Min | Typ | Max | Units |
|--|--|------------|-------|-----|-------------------------------|-------|
| LVCMOS 2.5V Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V |
| LVCMOS 2.5V DC Input Voltage Specification | | | | | | |
| VIH (DC) | DC input logic High (for MSIOD and DDRIO I/O Bank) | | 1.7 | — | 2.625 | V |
| VIH (DC) | DC input logic High (for MSIO I/O Bank) | | 1.7 | — | 2.75 | V |
| VIL (DC) | DC input logic Low | | -0.3 | — | 0.7 | V |
| IIH (DC) | Input current High | | — | — | See Table 5-3 | — |
| IIL (DC) | Input current Low | | — | — | See Table 5-3 | — |
| LVCMOS 2.5V DC Output Voltage Specification | | | | | | |
| VOH | DC output logic High ¹ | VDDI-0.4 | — | — | — | V |
| VOL | DC output logic Low ¹ | — | — | — | 0.4 | V |

Note:

1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5V JEDEC8-5A requirements.

Table 5-13. LVCMOS 2.5V Maximum AC Switching Speeds

| Symbol | Parameters | Conditions | Min | Typ | Max | Units |
|--------|--|--|-----|-----|-----|-------|
| Dmax | Maximum data rate (for DDRIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 360 | Mbps |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 360 | Mbps |
| Dmax | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 370 | Mbps |

Table 5-14. LVCMOS 2.5V AC Test Parameters and Driver Impedance Specifications

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|---|------------|-----|------------------------|-----|-------|
| LVCMOS 2.5V Calibrated Impedance Option | | | | | | |
| Rodt_cal | Supported output driver calibrated impedance (for DDRIO I/O Bank) | — | — | 75, 60, 50, 33, 25, 20 | — | Ω |
| LVCMOS 2.5V AC Test Parameters Specifications | | | | | | |
| Vtrip | Measuring/trip point for data path | — | — | 1.2 | — | V |

.....continued

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---------|--|------------|-----|-----|-----|----------|
| Rent | Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | — | — | 2k | — | Ω |
| Cent | Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | — | — | 5 | — | pF |
| Cload | Capacitive loading for data path (t_{DP}) | — | — | 5 | — | pF |

Table 5-15. LVCMOS 2.5V Transmitter Drive Strength Specifications

| Output Drive Selection | | | VOH (V) Min | VOL (V) Max | IOH (at VOH) mA | IOL (at VOL) mA |
|------------------------|----------------|---|----------------|----------------|-----------------|-----------------|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank (With Software Default Fixed Code) | | | | |
| 2 mA | 2 mA | 2 mA | VDDI-0.4 | 0.7 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | VDDI-0.4 | 0.7 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | VDDI-0.4 | 0.7 | 6 | 6 |
| 8 mA | 8 mA | 8 mA | VDDI-0.4 | 0.7 | 8 | 8 |
| 12 mA | 12 mA | 12 mA | VDDI-0.4 | 0.7 | 12 | 12 |
| 16 mA | N/A | 16 mA | VDDI-0.4 | 0.7 | 16 | 16 |

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances and I/V Curve use the corresponding IBIS models located at: www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas#ibis.

5.6.3.2 AC Switching Characteristics [\(Ask a Question\)](#)

AC Switching Characteristics for Receiver (Input Buffers)

Table 5-16. LVCMOS 2.5V AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, VDD = 1.14V, VDDI = 2.375V

| | On-Die Termination (ODT) | Speed Grade -1 | | Units |
|----------------------------------|--------------------------|----------------|-----------|-------|
| | | t_{PY} | t_{PYS} | |
| LVCMOS 2.5V (for DDRIO I/O Bank) | None | 1.903 | 2.021 | ns |
| LVCMOS 2.5V (for MSIO I/O Bank) | None | 2.689 | 2.698 | ns |
| LVCMOS 2.5V (for MSIOD I/O Bank) | None | 2.447 | 2.46 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-17. LVCMOS 2.5V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, VDD = 1.14V, VDDI = 2.375V

| Output Drive Selection | Slew Control | Speed Grade -1 | | | | | Units |
|---|--------------|----------------|----------|----------|----------|----------|-------|
| | | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| LVCMOS 2.5V (for DDRIO I/O Bank with Fixed Code) | | | | | | | |
| 2 mA | slow | 3.967 | 3.664 | 3.986 | 4.172 | 3.811 | ns |
| | medium | 3.625 | 3.38 | 3.647 | 3.882 | 3.458 | ns |
| | medium_fast | 3.485 | 3.259 | 3.507 | 3.747 | 3.327 | ns |
| | fast | 3.458 | 3.253 | 3.48 | 3.74 | 3.31 | ns |
| 4 mA | slow | 3.371 | 2.942 | 3.362 | 5.148 | 4.71 | ns |
| | medium | 3.063 | 2.701 | 3.059 | 4.874 | 4.381 | ns |
| | medium_fast | 2.925 | 2.566 | 2.92 | 4.686 | 4.248 | ns |
| | fast | 2.91 | 2.559 | 2.905 | 4.683 | 4.238 | ns |

.....continued

| Output Drive Selection | Slew Control | Speed Grade -1 | | | | | Units |
|--|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------|
| | | t _{DP} | t _{ZL} | t _{ZH} | t _{HZ} | t _{LZ} | |
| 6 mA | slow | 3.189 | 2.716 | 3.169 | 5.56 | 5.092 | ns |
| | medium | 2.886 | 2.473 | 2.876 | 5.273 | 4.752 | ns |
| | medium_fast | 2.749 | 2.355 | 2.738 | 5.127 | 4.167 | ns |
| | fast | 2.731 | 2.345 | 2.72 | 5.115 | 4.6 | ns |
| 8 mA | slow | 3.132 | 2.646 | 3.109 | 5.686 | 5.207 | ns |
| | medium | 2.832 | 2.407 | 2.82 | 5.402 | 4.864 | ns |
| | medium_fast | 2.698 | 2.292 | 2.685 | 5.262 | 4.732 | ns |
| | fast | 2.684 | 2.282 | 2.671 | 5.252 | 4.724 | ns |
| 12 mA | slow | 3.013 | 2.504 | 2.984 | 5.918 | 5.416 | ns |
| | medium | 2.72 | 2.284 | 2.707 | 5.657 | 5.074 | ns |
| | medium_fast | 2.592 | 2.176 | 2.578 | 5.537 | 4.949 | ns |
| | fast | 2.58 | 2.166 | 2.566 | 5.529 | 4.946 | ns |
| 16 mA | slow | 2.936 | 2.415 | 2.902 | 6.136 | 5.577 | ns |
| | medium | 2.66 | 2.206 | 2.645 | 5.901 | 5.261 | ns |
| | medium_fast | 2.536 | 2.102 | 2.519 | 5.815 | 5.142 | ns |
| | fast | 2.523 | 2.093 | 2.506 | 5.81 | 5.137 | ns |
| LVC MOS 2.5V (for MSIO I/O Bank) | | | | | | | |
| 2 mA | slow | 3.933 | 4.352 | 4.22 | 2.358 | 3.838 | ns |
| 4 mA | slow | 2.905 | 3.423 | 3.508 | 4.681 | 5.262 | ns |
| 6 mA | slow | 2.687 | 2.995 | 3.155 | 5.561 | 5.73 | ns |
| 8 mA | slow | 2.594 | 2.877 | 3.07 | 6.602 | 6.248 | ns |
| 12 mA | slow | 2.623 | 2.732 | 2.944 | 6.974 | 6.478 | ns |
| 16 mA | slow | 2.717 | 2.617 | 2.84 | 7.455 | 6.824 | ns |
| LVC MOS 2.5V (for MSIOD I/O Bank) | | | | | | | |
| 2 mA | slow | 2.403 | 2.922 | 2.89 | 5.397 | 5.202 | ns |
| 4 mA | slow | 1.998 | 2.446 | 2.468 | 5.936 | 5.665 | ns |
| 6 mA | slow | 1.861 | 2.329 | 2.375 | 6.391 | 6.068 | ns |
| 8 mA | slow | 1.781 | 2.145 | 2.208 | 6.884 | 6.44 | ns |
| 12 mA | slow | 1.804 | 2.039 | 2.108 | 7.23 | 6.685 | ns |

5.6.4 1.8V LVC MOS [\(Ask a Question\)](#)

LVC MOS 1.8 is a general standard for 1.8V applications and is supported in IGLOO 2 FPGAs and SmartFusion 2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

5.6.4.1 Minimum and Maximum AC/DC Input and Output Levels [\(Ask a Question\)](#)

Table 5-18. LVC MOS 1.8V DC Voltage Specification

| Symbols | Parameters | Min | Typ | Max | Units |
|---|---|-------------|-----|---------------|-------|
| Recommended DC Operating Conditions | | | | | |
| VDDI | Supply Voltage | 1.710 | 1.8 | 1.89 | V |
| LVC MOS 1.8 V DC Input Voltage Specification | | | | | |
| V _{IH} (DC) | DC input Logic HIGH (for MSIOD and DDRIO I/O Banks) | 0.65 × VDDI | — | 1.89 | V |
| V _{IH} (DC) | DC input Logic HIGH (for MSIO I/O Bank) | 0.65 × VDDI | — | 2.75 | V |
| V _{IL} (DC) | DC input Logic LOW | -0.3 | — | 0.35 × VDDI | V |
| I _{IH} (DC) | Input Current HIGH | — | — | See Table 5-3 | — |

.....continued

| Symbols | Parameters | Min | Typ | Max | Units |
|--|----------------------|-------------|-----|-------------------------------|-------|
| IIL(DC) | Input Current LOW | — | — | See Table 5-3 | — |
| LVC MOS 1.8 V DC Output Voltage Specification | | | | | |
| VOH | DC output Logic HIGH | VDDI – 0.45 | — | — | V |
| VOL | DC output Logic LOW | — | — | 0.45 | V |

Table 5-19. LVC MOS 1.8V Maximum AC Switching Speeds

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|--|--|-----|-----|-----|-------|
| LVC MOS 18V Maximum AC Switching Speed | | | | | | |
| Dmax | Maximum data rate (for DDRIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 360 | Mbps |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 260 | Mbps |
| Dmax | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 360 | Mbps |

Table 5-20. LVC MOS 1.8V Transmitter Drive Strength Specifications

| Output Drive Selection | | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|------------------------|----------------|-------------|---------|-----------------|-----------------|
| MSIO I/O Bank | MSIOD I/O Bank | Min | Max | | |
| 2 mA | 2 mA | VDDI – 0.45 | 0.45 | 2 | 2 |
| 4 mA | 4 mA | VDDI – 0.45 | 0.45 | 4 | 4 |
| 6 mA | 6 mA | VDDI – 0.45 | 0.45 | 6 | 6 |
| 8 mA | 8 mA | VDDI – 0.45 | 0.45 | 8 | 8 |
| 10 mA | 10 mA | VDDI – 0.45 | 0.45 | 10 | 10 |
| 12 mA | N/A | VDDI – 0.45 | 0.45 | 12 | 12 |

Note: Maximum data rate applies for drive strength 8 mA and above, all slews.

Table 5-21. LVC MOS 1.8V Transmitter Drive Strength Specifications

| Output Drive Selection | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|-------------------------|-------------|---------|-----------------|-----------------|
| DDRIO Bank ¹ | Min | Max | | |
| 2 mA | VDDI – 0.45 | 0.45 | 2 | 2 |
| 4 mA | VDDI – 0.45 | 0.45 | 4 | 4 |
| 6 mA ² | VDDI – 0.45 | 0.45 | 6 | 6 |
| 8 mA ² | VDDI – 0.45 | 0.45 | 6 | 6 |
| 10 mA | VDDI – 0.45 | 0.45 | 8 | 8 |
| 12 mA | VDDI – 0.45 | 0.45 | 10 | 10 |
| 16 mA | VDDI – 0.45 | 0.45 | 12 | 12 |

Notes:

- Software Configurator GUI will display the Commercial/Industrial numeric values. The actual drive capability at temperature is defined in this table.
- DDRIO has two 6 mA drive strength settings. The setting that corresponds to Output Drive Selection value of 8 mA has a shorter propagation delay.

Table 5-22. LVCMOS 1.8V AC Test Parameters and Driver Impedance Specifications

| LVCMOS 1.8V AC Calibrated Impedance Option | | | | | |
|---|--|-----|------------------------|-----|----------|
| Symbols | Parameters | Min | Typ | Max | Units |
| Rodt_cal | Supported output driver calibrated impedance (for DDRIO I/O Bank) | — | 75, 60, 50, 33, 25, 20 | — | Ω |
| LVCMOS 1.8V AC Test Parameters Specifications | | | | | |
| Vtrip | Measuring/trip point for data path | — | 0.9 | — | V |
| Rent | Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | — | 2k | — | Ω |
| Cent | Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | — | 5 | — | pF |
| Clod | Capacitive loading for data path (t_{DP}) | — | 5 | — | pF |

5.6.4.2 AC Switching Characteristics [\(Ask a Question\)](#)

AC Switching Characteristics for Receiver (Input Buffers)

Table 5-23. LVCMOS 1.8V AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions:
 $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{V}$, $V_{DDI} = 1.71\text{V}$

| | ODT (On Die Termination) | Speed Grade -1 | | Units |
|--|-----------------------------|----------------|-----------|-------|
| | | t_{PY} | t_{PYS} | |
| LVCMOS 1.8V (for DDRIO I/O Bank with Fixed Codes) | None | 2.071 | 2.213 | ns |
| LVCMOS 1.8V (for MSIO I/O Bank) | None | 3.185 | 3.171 | ns |
| | 50 | 3.394 | 3.397 | ns |
| | 75 | 3.322 | 3.316 | ns |
| | 150 | 3.252 | 3.239 | ns |
| LVCMOS 1.8V (for MSIOD I/O Bank) | None | 2.827 | 2.813 | ns |
| | 50 | 3.043 | 3.053 | ns |
| | 75 | 2.968 | 2.963 | ns |
| | 150 | 2.898 | 2.886 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-24. LVCMOS 1.8V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions:
 $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{V}$, $V_{DDI} = 1.71\text{V}$

| Output Drive Selection | Slew Control | Speed Grade -1 | | | | | Units |
|---|--------------|----------------|----------|----------|----------|----------|-------|
| | | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| LVCMOS 1.8V (for DDRIO I/O Bank with Fixed Codes) | | | | | | | |
| 2 mA | slow | 4.681 | 4.017 | 4.69 | 5.388 | 4.852 | ns |
| | medium | 4.211 | 3.599 | 4.219 | 5.058 | 4.488 | ns |
| | medium_fast | 3.978 | 3.392 | 3.986 | 4.874 | 4.327 | ns |
| | fast | 3.953 | 3.373 | 3.961 | 4.858 | 4.316 | ns |
| 4 mA | slow | 4.355 | 3.657 | 4.346 | 5.967 | 5.399 | ns |
| | medium | 3.886 | 3.246 | 3.879 | 5.628 | 5.01 | ns |
| | medium_fast | 3.656 | 3.05 | 3.647 | 5.461 | 4.845 | ns |
| | fast | 3.635 | 3.033 | 3.626 | 5.447 | 4.838 | ns |
| 6 mA | slow | 4.105 | 3.422 | 4.092 | 6.221 | 5.599 | ns |
| | medium | 3.68 | 3.05 | 3.668 | 5.9 | 5.257 | ns |
| | medium_fast | 3.477 | 2.867 | 3.463 | 5.739 | 5.118 | ns |
| | fast | 3.451 | 2.849 | 3.437 | 5.72 | 5.104 | ns |

.....continued

| Output Drive Selection | Slew Control | Speed Grade -1 | | | | | Units |
|--|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------|
| | | t _{DP} | t _{ZL} | t _{ZH} | t _{HZ} | t _{LZ} | |
| 8 mA | slow | 4.015 | 3.32 | 3.998 | 6.458 | 5.808 | ns |
| | medium | 3.59 | 2.947 | 3.574 | 6.129 | 5.449 | ns |
| | medium_fast | 3.383 | 2.761 | 3.366 | 5.963 | 5.304 | ns |
| | fast | 3.357 | 2.746 | 3.34 | 5.954 | 5.289 | ns |
| 10 mA | slow | 3.888 | 3.18 | 3.864 | 6.739 | 6.045 | ns |
| | medium | 3.485 | 2.822 | 3.467 | 6.422 | 5.7 | ns |
| | medium_fast | 3.281 | 2.642 | 3.26 | 6.277 | 5.553 | ns |
| | fast | 3.258 | 2.627 | 3.238 | 6.27 | 5.546 | ns |
| 12 mA | slow | 3.795 | 3.096 | 3.773 | 6.773 | 6.067 | ns |
| | medium | 3.408 | 2.764 | 3.389 | 6.47 | 5.743 | ns |
| | medium_fast | 3.215 | 2.599 | 3.194 | 6.346 | 5.61 | ns |
| | fast | 3.196 | 2.584 | 3.175 | 6.335 | 5.604 | ns |
| 16 mA | slow | 3.744 | 3.035 | 3.719 | 6.944 | 6.207 | ns |
| | medium | 3.358 | 2.712 | 3.339 | 6.657 | 5.868 | ns |
| | medium_fast | 3.175 | 2.546 | 3.153 | 6.547 | 5.751 | ns |
| | fast | 3.156 | 2.531 | 3.133 | 6.541 | 5.747 | ns |
| LVC MOS 1.8V (for MSIO I/O Bank) | | | | | | | |
| 2 mA | slow | 3.957 | 4.784 | 5.023 | 5.643 | 5.866 | ns |
| 4 mA | slow | 3.668 | 4.162 | 4.485 | 6.543 | 6.382 | ns |
| 6 mA | slow | 3.586 | 3.994 | 4.358 | 7.622 | 6.941 | ns |
| 8 mA | slow | 3.616 | 3.782 | 4.162 | 7.988 | 7.161 | ns |
| 10 mA | slow | 3.662 | 3.732 | 4.121 | 8.396 | 7.423 | ns |
| 12 mA | slow | 3.75 | 3.615 | 4.006 | 8.576 | 7.543 | ns |
| LVC MOS 1.8V (for MSIOD I/O Bank) | | | | | | | |
| 2 mA | slow | 3.048 | 3.692 | 3.898 | 5.818 | 5.609 | ns |
| 4 mA | slow | 2.5 | 3.088 | 3.288 | 6.421 | 6.121 | ns |
| 6 mA | slow | 2.225 | 2.747 | 2.937 | 7.18 | 6.753 | ns |
| 8 mA | slow | 2.233 | 2.72 | 2.904 | 7.49 | 6.992 | ns |
| 10 mA | slow | 2.263 | 2.577 | 2.759 | 7.851 | 7.253 | ns |

5.6.5 1.5V LVC MOS [\(Ask a Question\)](#)

LVC MOS 1.5 is a general standard for 1.5V applications and is supported in IGLOO 2 FPGAs and SmartFusion 2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

5.6.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification [\(Ask a Question\)](#)

Table 5-25. LVC MOS 1.5V Minimum and Maximum DC Input and Output Levels

| Symbols | Parameters | Min | Typ | Max | Units |
|---|---|-------------|-----|-------------------------------|-------|
| LVC MOS 1.5V Recommended DC Operating Conditions | | | | | |
| VDDI | Supply voltage | 1.425 | 1.5 | 1.575 | V |
| LVC MOS 1.5V DC Input Voltage Specification | | | | | |
| V _{IH} (DC) | DC input logic High for (MSIOD and DDRIO I/O banks) | 0.65 × VDDI | — | 1.575 | V |
| V _{IH} (DC) | DC input logic High (for MSIO I/O Bank) | 0.65 × VDDI | — | 2.75 | V |
| V _{IL} (DC) | DC input logic Low | -0.3 | — | 0.35 × VDDI | V |
| I _{IH} (DC) | Input current High | — | — | See Table 5-3 | — |

.....continued

| Symbols | Parameters | Min | Typ | Max | Units |
|---|----------------------|-------------|-----|---------------|-------|
| IIL (DC) | Input current Low | — | — | See Table 5-3 | — |
| LVC MOS 1.5V DC Output Voltage Specification | | | | | |
| VOH | DC output logic High | VDDI × 0.75 | — | — | V |
| VOL | DC output logic Low | — | — | VDDI × 0.25 | V |

Table 5-26. LVC MOS 1.5V Maximum AC Switching Speeds

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|--|--|-----|-----|-----|-------|
| LVC MOS 1.5V Maximum AC Switching Speed | | | | | | |
| Dmax | Maximum data rate (for DDRIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 210 | Mbps |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 140 | Mbps |
| Dmax | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 190 | Mbps |

Table 5-27. LVC MOS 1.5V AC Test Parameters and Driver Impedance Specifications

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|------------|-----|----------------|-----|-------|
| LVC MOS 1.5V AC Calibrated Impedance Option | | | | | | |
| Rodt_cal | Supported output driver calibrated impedance (for DDRIO I/O Bank) | | — | 75, 60, 50, 40 | — | Ω |
| LVC MOS 1.5V AC Test Parameters Specifications | | | | | | |
| Vtrip | Measuring/trip point for data path | | — | 0.75 | — | V |
| Rent | Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 2k | — | Ω |
| Cent | Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 5 | — | pF |
| Cload | Capacitive loading for data path (t _{DP}) | | — | 5 | — | pF |

Table 5-28. LVC MOS 1.5V Transmitter Drive Strength Specifications

| Output Drive Selection | | | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|------------------------|----------------|-------------------------------------|-------------|-------------|--------------------|--------------------|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank (with Fixed Code) | Min | Max | | |
| 2 mA | 2 mA | 2 mA | VDDI × 0.75 | VDDI × 0.25 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | VDDI × 0.75 | VDDI × 0.25 | 4 | 4 |
| 6 mA | 6 mA | 6 mA | VDDI × 0.75 | VDDI × 0.25 | 6 | 6 |
| 8 mA | N/A | 8 mA | VDDI × 0.75 | VDDI × 0.25 | 8 | 8 |
| N/A | N/A | 10 mA | VDDI × 0.75 | VDDI × 0.25 | 10 | 10 |
| N/A | N/A | 12 mA | VDDI × 0.75 | VDDI × 0.25 | 12 | 12 |

5.6.5.2 AC Switching Characteristics ([Ask a Question](#))**AC Switching Characteristics for Receiver (Input Buffers)****Table 5-29.** LVC MOS 1.5V AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions: T_J = 125 °C, VDD = 1.14V, VDDI = 1.425V

| | ODT (On Die Termination) | Speed Grade -1 | | Units |
|--|--------------------------|-----------------|------------------|-------|
| | | t _{py} | t _{pys} | |
| LVC MOS 1.5V (for DDRIO I/O Bank with Fixed Codes) | none | 2.19 | 2.216 | ns |

.....continued

| | ODT (On Die Termination) | Speed Grade -1 | | Units |
|----------------------------------|--------------------------|-----------------|------------------|-------|
| | | t _{py} | t _{pys} | |
| LVCMOS 1.5V (for MSIO I/O Bank) | none | 3.679 | 3.652 | ns |
| | 50 | 4.151 | 4.126 | ns |
| | 75 | 3.984 | 3.953 | ns |
| | 150 | 3.823 | 3.791 | ns |
| LVCMOS 1.5V (for MSIOD I/O Bank) | none | 3.262 | 3.229 | ns |
| | 50 | 3.76 | 3.739 | ns |
| | 75 | 3.555 | 3.52 | ns |
| | 150 | 3.395 | 3.359 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-30. LVCMOS 1.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions: T_j = 125 °C, VDD = 1.14V, VDDI = 1.425V

| Output Drive Selection | Slew Control | Speed Grade -1 | | | | | Units |
|--|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------|
| | | t _{DP} | t _{ZL} | t _{ZH} | t _{HZ} | t _{LZ} | |
| LVCMOS 1.5V (for DDRIO I/O Bank with Fixed Codes) | | | | | | | |
| 2 mA | slow | 5.712 | 4.796 | 5.735 | 5.814 | 5.138 | ns |
| | medium | 5.094 | 4.274 | 5.114 | 5.484 | 4.779 | ns |
| | medium_fast | 4.793 | 4.013 | 4.81 | 5.288 | 4.625 | ns |
| | fast | 4.762 | 3.98 | 4.78 | 5.261 | 4.615 | ns |
| 4 mA | slow | 4.966 | 4.133 | 4.956 | 6.763 | 6.05 | ns |
| | medium | 4.412 | 3.62 | 4.401 | 6.433 | 5.664 | ns |
| | medium_fast | 4.145 | 3.358 | 4.131 | 6.249 | 5.507 | ns |
| | fast | 4.116 | 3.338 | 4.103 | 6.238 | 5.498 | ns |
| 6 mA | slow | 4.744 | 3.869 | 4.728 | 7.173 | 6.383 | ns |
| | medium | 4.212 | 3.382 | 4.195 | 6.837 | 6.004 | ns |
| | medium_fast | 3.951 | 3.135 | 3.93 | 6.668 | 5.861 | ns |
| | fast | 3.919 | 3.11 | 3.899 | 6.644 | 5.845 | ns |
| 8 mA | slow | 4.603 | 3.691 | 4.585 | 7.397 | 6.553 | ns |
| | medium | 4.081 | 3.242 | 4.062 | 7.064 | 6.189 | ns |
| | medium_fast | 3.827 | 3.015 | 3.804 | 6.912 | 6.051 | ns |
| | fast | 3.804 | 2.994 | 3.781 | 6.903 | 6.051 | ns |
| 10 mA | slow | 4.519 | 3.612 | 4.499 | 7.578 | 6.676 | ns |
| | medium | 4.026 | 3.177 | 4.005 | 7.264 | 6.335 | ns |
| | medium_fast | 3.775 | 2.948 | 3.75 | 7.11 | 6.198 | ns |
| | fast | 3.747 | 2.929 | 3.721 | 7.103 | 6.19 | ns |
| 12 mA | slow | 4.456 | 3.562 | 4.433 | 7.704 | 6.795 | ns |
| | medium | 3.965 | 3.13 | 3.943 | 7.388 | 6.425 | ns |
| | medium_fast | 3.731 | 2.912 | 3.704 | 7.278 | 6.303 | ns |
| | fast | 3.703 | 2.893 | 3.676 | 7.275 | 6.294 | ns |
| LVCMOS 1.5V (for MSIO I/O Bank) | | | | | | | |
| 2 mA | slow | 5.118 | 6.263 | 6.53 | 6.524 | 6.388 | ns |
| 4 mA | slow | 4.657 | 5.178 | 5.65 | 8.57 | 7.55 | ns |
| 6 mA | slow | 4.693 | 4.89 | 5.389 | 8.928 | 7.766 | ns |
| 8 mA | slow | 4.876 | 4.663 | 5.183 | 9.59 | 8.173 | ns |

.....continued

| Output Drive Selection | Slew Control | Speed Grade -1 | | | | | Units |
|--|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------|
| | | t _{DP} | t _{ZL} | t _{ZH} | t _{HZ} | t _{LZ} | |
| LVC MOS 1.5V (for MSIOD I/O Bank) | | | | | | | |
| 2 mA | slow | 3.085 | 3.795 | 4.086 | 6.838 | 6.477 | ns |
| 4 mA | slow | 2.731 | 3.365 | 3.631 | 7.663 | 7.165 | ns |
| 6 mA | slow | 2.742 | 3.162 | 3.417 | 8.126 | 7.52 | ns |

5.6.6 1.2V LVC MOS [\(Ask a Question\)](#)

LVC MOS 1.2 is a general standard for 1.2V applications and is supported in IGLOO 2 FPGAs and SmartFusion 2 SoC FPGAs in compliance to the JEDEC specification JESD8-12A.

5.6.6.1 Minimum and Maximum Input and Output Levels Specification [\(Ask a Question\)](#)

Table 5-31. LVC MOS 1.2V Minimum and Maximum DC Input and Output Levels

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|------------|-------------|-----|-------------------------------|-------|
| LVC MOS 1.2V Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 1.140 | 1.2 | 1.26 | V |
| LVC MOS 1.2V DC Input Voltage Specification | | | | | | |
| V _{IH} (DC) | DC input logic High (for MSIOD and DDRIO I/O Banks) | | 0.65 × VDDI | — | 1.26 | V |
| V _{IH} (DC) | DC input logic High (for MSIO I/O Bank) | | 0.65 × VDDI | — | 2.75 | V |
| V _{IL} (DC) | DC input logic Low | | -0.3 | — | 0.35 × VDDI | V |
| I _{IH} (DC) | Input current High | | — | — | See Table 5-3 | — |
| I _{IL} (DC) | Input current Low | | — | — | See Table 5-3 | — |
| LVC MOS 1.2V DC Output Voltage Specification | | | | | | |
| V _{OH} | DC output logic High | | VDDI × 0.75 | — | — | V |
| V _{OL} | DC output logic Low | | — | — | VDDI × 0.25 | V |

Table 5-32. LVC MOS 1.2V Maximum AC Switching Speeds

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|--|--|-----|-----|-----|-------|
| LVC MOS 1.2V Maximum AC Switching Speed | | | | | | |
| D _{max} | Maximum data rate (for DDRIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 180 | Mbps |
| D _{max} | Maximum data rate (for MSIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 100 | Mbps |
| D _{max} | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17 pF load, maximum drive/slew | — | — | 140 | Mbps |

Table 5-33. LVC MOS 1.2V AC Calibrated Impedance and Test Parameters Specifications

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|------------|-----|----------------|-----|-------|
| LVC MOS 1.2V AC Calibrated Impedance Option | | | | | | |
| R _{odt_cal} | Supported output driver calibrated impedance (for DDRIO I/O Bank) | | — | 75, 60, 50, 40 | — | Ω |
| LVC MOS 1.2V AC Test Parameters Specifications | | | | | | |
| V _{trip} | Measuring/trip point for data path | | — | 0.6 | — | V |
| R _{ent} | Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 2k | — | Ω |
| C _{ent} | Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 5 | — | pF |
| C _{load} | Capacitive loading for data path (t _{DP}) | | — | 5 | — | pF |

Table 5-34. LVCMOS 1.2V Transmitter Drive Strength Specifications

| Output Drive Selection | | | VOH (V) | VOL (V) | IOH (at VOH) mA | IOL (at VOL) mA |
|------------------------|----------------|-------------------------------------|-------------|-------------|--------------------|-----------------|
| MSIO I/O Bank | MSIOD I/O Bank | DDRIO I/O Bank (with Fixed Code) | Min | Max | | |
| 2 mA | 2 mA | 2 mA | VDDI × 0.75 | VDDI × 0.25 | 2 | 2 |
| 4 mA | 4 mA | 4 mA | VDDI × 0.75 | VDDI × 0.25 | 4 | 4 |
| N/A | N/A | 6 mA | VDDI × 0.75 | VDDI × 0.25 | 6 | 6 |

5.6.6.2 AC Switching Characteristics [\(Ask a Question\)](#)**AC Switching Characteristics for Receiver (Input Buffers)****Table 5-35. LVCMOS 1.2V AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions:**
 $T_j = 125\text{ }^\circ\text{C}$, VDD = 1.14V, VDDI = 1.14V

| | ODT (On Die Termination) | Speed Grade -1 | | Units |
|---|--------------------------|----------------|-----------|-------|
| | | t_{PY} | t_{PYS} | |
| LVCMOS 1.2V (for DDRIO I/O Bank with Fixed Codes) | none | 2.539 | 2.556 | ns |
| LVCMOS 1.2V (for MSIO I/O Bank) | none | 4.888 | 4.845 | ns |
| | 50 | 6.683 | 6.605 | ns |
| | 75 | 5.923 | 5.847 | ns |
| | 150 | 5.29 | 5.235 | ns |
| LVCMOS 1.2V (for MSIOD I/O Bank) | none | 4.281 | 4.235 | ns |
| | 50 | 6.806 | 6.721 | ns |
| | 75 | 5.643 | 5.564 | ns |
| | 150 | 4.813 | 4.753 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**Table 5-36. LVCMOS 1.2V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions:** $T_j = 125\text{ }^\circ\text{C}$, VDD = 1.14V, VDDI = 1.14V

| Output Drive Selection | Slew Control | Speed Grade -1 | | | | | Units |
|---|--------------|----------------|----------|----------|----------|----------|-------|
| | | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| LVCMOS 1.2V (for DDRIO I/O Bank with Fixed Code) | | | | | | | |
| 2 mA | slow | 6.938 | 5.599 | 6.948 | 7.568 | 6.612 | ns |
| | medium | 6.11 | 4.814 | 6.114 | 7.201 | 6.234 | ns |
| | medium_fast | 5.675 | 4.409 | 5.676 | 6.971 | 6.048 | ns |
| | fast | 5.633 | 4.379 | 5.634 | 6.958 | 6.037 | ns |
| 4 mA | slow | 6.328 | 4.892 | 6.316 | 8.339 | 7.306 | ns |
| | medium | 5.538 | 4.192 | 5.521 | 7.961 | 6.923 | ns |
| | medium_fast | 5.119 | 3.832 | 5.097 | 7.76 | 6.741 | ns |
| | fast | 5.072 | 3.085 | 5.051 | 7.752 | 6.725 | ns |
| 6 mA | slow | 6.092 | 4.681 | 6.075 | 8.685 | 7.589 | ns |
| | medium | 5.342 | 4.016 | 5.32 | 8.33 | 7.19 | ns |
| | medium_fast | 4.949 | 3.66 | 4.922 | 8.139 | 7.022 | ns |
| | fast | 4.903 | 3.622 | 4.876 | 8.107 | 7.006 | ns |
| LVCMOS 1.2V (for MSIO I/O Bank) | | | | | | | |
| 2 mA | slow | 7.051 | 7.856 | 8.541 | 10.387 | 8.768 | ns |
| 4 mA | slow | 7.385 | 7.027 | 7.815 | 11.547 | 9.444 | ns |
| LVCMOS 1.2V (for MSIOD I/O Bank) | | | | | | | |

.....continued

| Output Drive Selection | Slew Control | Speed Grade -1 | | | | | Units |
|------------------------|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------|
| | | t _{DP} | t _{ZL} | t _{ZH} | t _{HZ} | t _{LZ} | |
| 2 mA | slow | 4.048 | 5.123 | 5.552 | 8.401 | 7.824 | ns |
| 4 mA | slow | 3.941 | 4.406 | 4.814 | 9.422 | 8.656 | ns |

5.6.7 3.3V PCI/PCIX [\(Ask a Question\)](#)

Peripheral Component Interface (PCI) for 3.3V standards specify support for 33 MHz and 66 MHz PCI bus applications.

5.6.7.1 Minimum and Maximum Input and Output Levels Specification [\(Ask a Question\)](#)

Table 5-37. PCI/PCI-X DC Voltage Specification (Applicable to MSIO Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|----------------------|------------|-----------------------|-----|-------------------------------|-------|
| PCI/PCIX Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 3.15 | 3.3 | 3.45 | V |
| PCI/PCIX DC Input Voltage Specification | | | | | | |
| V _I | DC input voltage | | 0 | — | 3.45 | V |
| I _{IH} (DC) | Input current High | | — | — | See Table 5-3 | — |
| I _{IL} (DC) | Input current Low | | — | — | See Table 5-3 | — |
| PCI/PCIX DC Output Voltage Specification | | | | | | |
| V _{OH} | DC output logic High | | Per PCI Specification | | | V |
| V _{OL} | DC output logic Low | | Per PCI Specification | | | V |

Table 5-38. PCI/PCI-X AC Specifications (Applicable to MSIO Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|---|--------------------------------------|-----|--------------|-----|-------|
| PCI/PCI-X AC Specifications | | | | | | |
| D _{max} | Maximum data rate (MSIO I/O Bank) | AC Loading: per JEDEC specifications | — | — | 560 | Mbps |
| PCI/PCI-X AC Test Parameters Specifications | | | | | | |
| V _{trip} | Measuring/trip point for data path (falling edge) | | — | 0.615 × VDDI | — | V |
| V _{trip} | Measuring/trip point for data path (rising edge) | | — | 0.285 × VDDI | — | V |
| R _{tt_test} | Resistance for data test path | | — | 25 | — | Ω |
| R _{ent} | Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 2k | — | Ω |
| C _{ent} | Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 5 | — | pF |
| C _{load} | Capacitive loading for data path (t _{DP}) | | — | 10 | — | pF |

5.6.7.2 AC Switching Characteristics [\(Ask a Question\)](#)

AC Switching Characteristics for Receiver (Input Buffers)

Table 5-39. PCI/PCIX AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions: T_J = 125 °C, VDD = 1.14V, VDDI = 3.15V

| | ODT (On Die Termination) | Speed Grade -1 | | Units |
|------------------------------|--------------------------|-----------------|------------------|-------|
| | | t _{PV} | t _{PYS} | |
| PCI/PCIX (for MSIO I/O Bank) | None | 2.379 | 2.387 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-40. PCI/PCIX AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$, $V_{DDI} = 3.15\text{V}$

| | Speed Grade -1 | | | | | Units |
|---------------------------------|----------------|----------|----------|----------|----------|-------|
| | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| PCI/PCIX (for MSIO I/O Bank) | 2.394 | 2.274 | 2.316 | 6.876 | 6.242 | ns |

5.7 Memory Interface and Voltage Referenced I/O Standards [\(Ask a Question\)](#)

5.7.1 High-Speed Transceiver Logic (HSTL) [\(Ask a Question\)](#)

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO 2 FPGA and SmartFusion 2 SoC FPGA devices support two classes of the 1.5V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

5.7.1.1 Minimum and Maximum Input and Output Levels Specification [\(Ask a Question\)](#)

Table 5-41. HSTL DC Voltage Specification (Applicable to DDRIO I/O Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|----------------------------------|------------|-----------------|-------|-------------------------------|-------|
| HSTL Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 1.425 | 1.5 | 1.575 | V |
| VTT | Termination voltage | | 0.698 | 0.750 | 0.803 | V |
| VREF | Input reference voltage | | 0.698 | 0.750 | 0.803 | V |
| HSTL DC Input Voltage Specification | | | | | | |
| VIH (DC) | DC input logic High | | $V_{REF} + 0.1$ | — | 1.575 | V |
| VIL (DC) | DC input logic Low | | -0.3 | — | $V_{REF} - 0.1$ | V |
| IIH (DC) | Input current High | | — | — | See Table 5-3 | — |
| IIL (DC) | Input current Low | | — | — | See Table 5-3 | — |
| HSTL DC Output Voltage Specification | | | | | | |
| HSTL Class I | | | | | | |
| VOH | DC output logic High | | $V_{DDI} - 0.4$ | — | — | V |
| VOL | DC output logic Low | | — | — | 0.4 | V |
| IOH at VOH | Output minimum source DC current | | -7.0 | — | — | mA |
| IOL at VOL | Output minimum sink current | | 7.0 | — | — | mA |
| HSTL Class II | | | | | | |
| VOH | DC output logic High | | $V_{DDI} - 0.4$ | — | — | V |
| VOL | DC output logic Low | | — | — | 0.4 | V |
| IOH at VOH | Output minimum source DC current | | -15.0 | — | — | mA |
| IOL at VOL | Output minimum sink current | | 15.0 | — | — | mA |
| HSTL DC Differential Voltage Specifications | | | | | | |
| VID (DC) | DC input differential voltage | | 0.2 | — | — | V |

Table 5-42. HSTL AC Specifications (Applicable to DDRIO Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|-------------------------------------|--------------------------------------|------|-----|-----|-------|
| HSTL AC Differential Voltage Specifications | | | | | | |
| VDIFF | AC input differential voltage | | 0.4 | — | — | V |
| Vx | AC differential cross point voltage | | 0.68 | — | 0.9 | V |
| HSTL Maximum AC Switching Speed | | | | | | |
| Dmax | Maximum data rate | AC loading: per JEDEC specifications | — | — | 360 | Mbps |

.....continued

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|--|-----------------------------|-----|---------------|-----|-------|
| HSTL Impedance Specification | | | | | | |
| Rref | Supported output driver calibrated impedance (for DDRIO I/O Bank) | Reference resistance = 191Ω | — | 25.5, 47.8 | — | Ω |
| RTT | Effective impedance value (ODT for DDRIO I/O Bank only) | Reference resistance = 191Ω | — | 47.8 | — | Ω |
| HSTL AC Test Parameters Specification | | | | | | |
| Vtrip | Measuring/trip point for data path | | — | 0.75 | — | V |
| Rent | Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 2k | — | Ω |
| Cent | Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 5 | — | pF |
| Rtt_test | Reference resistance for data test path for HSTL15 Class I (t_{DP}) | | — | 50 | — | Ω |
| Rtt_test | Reference resistance for data test path for HSTL15 Class II (t_{DP}) | | — | 25 | — | Ω |
| Cload | Capacitive loading for data path (t_{DP}) | | — | 5 | — | pF |

5.7.1.2 AC Switching Characteristics [\(Ask a Question\)](#)

AC Switching Characteristics for Receiver (Input Buffers)

Table 5-43. HSTL15 AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $VDD = 1.14\text{V}$, $VDDI = 1.425\text{V}$

| | ODT (On Die Termination) | t_{PY} | Units |
|--|--------------------------|----------------|-------|
| | | Speed Grade -1 | |
| HSTL (for DDRIO I/O Bank with Fixed Code) | | | |
| Pseudo-Differential | None | 1.673 | ns |
| True-Differential | None | 1.693 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-44. HSTL 15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $VDD = 1.14\text{V}$, $VDDI = 1.425\text{V}$

| | Speed Grade -1 | | | | | Units |
|---|----------------|----------|----------|----------|----------|-------|
| | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| HSTL Class I (for DDRIO I/O Bank) | | | | | | |
| Single Ended | 2.922 | 2.91 | 2.904 | 3.225 | 3.218 | ns |
| Differential | 2.907 | 2.757 | 2.755 | 2.662 | 2.66 | ns |
| HSTL Class II (for DDRIO I/O Bank) | | | | | | |
| Single Ended | 2.817 | 2.735 | 2.735 | 2.644 | 2.644 | ns |
| Differential | 2.827 | 2.81 | 2.803 | 3.205 | 3.197 | ns |

5.7.2 Stub-Series Terminated Logic [\(Ask a Question\)](#)

Stub-Series Terminated Logic (SSTL) for 2.5V (SSTL2), 1.8V (SSTL18), and 1.5V (SSTL15) is supported in IGLOO 2 and SmartFusion 2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO 2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

5.7.3 Stub-Series Terminated Logic 2.5V (SSTL2) [\(Ask a Question\)](#)

SSTL2 Class I and Class II are supported in IGLOO 2 and SmartFusion 2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO 2 and SmartFusion 2 SoC

FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

5.7.3.1 Minimum and Maximum DC Input and Output Levels Specification [\(Ask a Question\)](#)

Table 5-45. DDR1/SSTL2 Minimum and Maximum DC Input and Output Levels

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|----------------------------------|------------|-------------|-------|---------------|-------|
| Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V |
| VTT | Termination voltage | | 1.164 | 1.250 | 1.339 | V |
| VREF | Input reference voltage | | 1.164 | 1.250 | 1.339 | V |
| SSTL2 DC Input Voltage Specification | | | | | | |
| VIH (DC) | DC input logic High | | VREF + 0.15 | — | 2.625 | V |
| VIL (DC) | DC input logic Low | | -0.3 | — | VREF - 0.15 | V |
| IIH (DC) | Input current High | | — | — | See Table 5-3 | — |
| IIL (DC) | Input current Low | | — | — | See Table 5-3 | — |
| SSTL2 DC Output Voltage Specification | | | | | | |
| SSTL2 Class I (DDR Reduced Drive) | | | | | | |
| VOH | DC output logic High | | VTT + 0.608 | — | — | V |
| VOL | DC output logic Low | | — | — | VTT - 0.608 | V |
| IOH at VOH | Output minimum source DC current | | 8.1 | — | — | mA |
| IOL at VOL | Output minimum sink current | | -8.1 | — | — | mA |
| SSTL2 Class II (DDR Full Drive) - Applicable to MSIO and DDRIO I/O Banks Only | | | | | | |
| VOH | DC output logic High | | VTT + 0.81 | — | — | V |
| VOL | DC output logic Low | | — | — | VTT - 0.81 | V |
| IOH at VOH | Output minimum source DC current | | 16.2 | — | — | mA |
| IOL at VOL | Output minimum sink current | | -16.2 | — | — | mA |
| SSTL2 DC Differential Voltage Specification | | | | | | |
| VID (DC) | DC input differential voltage | | 0.3 | — | — | V |

Table 5-46. DDR1/SSTL2 AC Specifications

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|--|--------------------------------------|-------------------------|--------|-------------------------|-------|
| SSTL2 Maximum AC Switching Speeds | | | | | | |
| Dmax | Maximum data rate (for DDRIO I/O Bank) | AC loading: per JEDEC specifications | — | — | 360 | Mbps |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 17 pF load | — | — | 450 | Mbps |
| Dmax | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17 pF load | — | — | 480 | Mbps |
| SSTL2 AC Differential Voltage Specifications | | | | | | |
| VDIFF | AC Input Differential Voltage | | 0.7 | — | — | V |
| Vx | AC Differential Cross Point Voltage | | $0.5 \times VDDI - 0.2$ | — | $0.5 \times VDDI + 0.2$ | V |
| SSTL2 Impedance Specifications | | | | | | |
| | Supported output driver calibrated impedance (for DDRIO I/O Bank) | Reference resistor = 150Ω | — | 20, 42 | — | Ω |
| SSTL2 AC Test Parameters Specifications | | | | | | |
| Vtrip | Measuring/trip point for data path | | — | 1.25 | — | V |
| Rent | Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 2k | — | Ω |

.....continued

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|----------|--|------------|-----|-----|-----|----------|
| Cent | Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 5 | — | pF |
| Rtt_test | Reference resistance for data test path for SSTL2 Class I (t_{DP}) | | — | 50 | — | Ω |
| Rtt_test | Reference resistance for data test path for SSTL2 Class II (t_{DP}) | | — | 25 | — | Ω |
| Clload | Capacitive loading for data path (t_{DP}) | | — | 5 | — | pF |

5.7.3.2 AC Switching Characteristics [\(Ask a Question\)](#)

AC Switching Characteristics for Receiver (Input Buffers)

Table 5-47. DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, VDD = 1.14V, VDDI = 2.375V

| | ODT (On Die Termination) | Speed Grade -1 | Units |
|-------------------------------|--------------------------|----------------|-------|
| | | tPY | |
| SSTL2 (DDRIO I/O Bank) | | | |
| Pseudo-Differential | None | 1.613 | ns |
| True-Differential | None | 1.647 | ns |
| SSTL2 (MSIO I/O Bank) | | | |
| Pseudo-Differential | None | 3.083 | ns |
| True-Differential | None | 3.028 | ns |
| SSTL2 (MSIOD I/O Bank) | | | |
| Pseudo-Differential | None | 2.721 | ns |
| True-Differential | None | 2.71 | ns |

Table 5-48. DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, VDD = 1.14V, VDDI = 2.375V

| | Speed Grade -1 | | | | | Units |
|-----------------------|----------------|-------|-------|-------|-------|-------|
| | tDP | tZL | tZH | tHZ | tLZ | |
| SSTL2 Class I | | | | | | |
| DDRIO I/O Bank | | | | | | |
| Single Ended | 2.457 | 2.145 | 2.137 | 2.302 | 2.293 | ns |
| Differential | 2.454 | 2.38 | 2.375 | 2.589 | 2.584 | ns |
| MSIO I/O Bank | | | | | | |
| Single Ended | 2.283 | 2.255 | 2.243 | 2.286 | 2.273 | ns |
| Differential | 2.434 | 2.702 | 2.691 | 2.39 | 2.381 | ns |
| MSIOD I/O Bank | | | | | | |
| Single Ended | 1.646 | 1.59 | 1.589 | 1.82 | 1.818 | ns |
| Differential | 1.774 | 1.93 | 1.926 | 2.012 | 2.007 | ns |
| SSTL2 Class II | | | | | | |
| DDRIO I/O Bank | | | | | | |
| Single Ended | 2.317 | 2.06 | 2.053 | 2.229 | 2.221 | ns |
| Differential | 2.32 | 2.213 | 2.21 | 2.57 | 2.565 | ns |
| MSIO I/O Bank | | | | | | |
| Single Ended | 2.563 | 2.208 | 2.19 | 2.205 | 2.187 | ns |
| Differential | 2.703 | 2.566 | 2.555 | 2.363 | 2.353 | ns |

5.7.4 Stub-Series Terminated Logic 1.8V (SSTL18) [\(Ask a Question\)](#)

SSTL18 Class I and Class II are supported in IGLOO 2 and SmartFusion 2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO 2 and SmartFusion 2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

5.7.4.1 Minimum and Maximum Input and Output Levels Specification [\(Ask a Question\)](#)

Table 5-49. DDR2/SSTL18 AC/DC Minimum and Maximum Input and Output Levels Specification

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|--|------------|--------------|-------|-------------------------------|-------|
| Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 1.71 | 1.8 | 1.89 | V |
| VTT | Termination voltage | | 0.838 | 0.900 | 0.964 | V |
| VREF | Input reference voltage | | 0.838 | 0.900 | 0.964 | V |
| SSTL18 DC Input Voltage Specification | | | | | | |
| VIH (DC) | DC input logic High | | VREF + 0.125 | — | 1.89 | V |
| VIL (DC) | DC input logic Low | | -0.3 | — | VREF - 0.125 | V |
| IIH (DC) | Input current High | | — | — | See Table 5-3 | — |
| IIL (DC) | Input current Low | | — | — | See Table 5-3 | — |
| SSTL18 DC Output Voltage Specification | | | | | | |
| SSTL18 Class I (DDR2 Reduced Drive) | | | | | | |
| VOH | DC output logic High | | VTT + 0.603 | — | — | V |
| VOL | DC output logic Low | | — | — | VTT - 0.603 | V |
| IOH at VOH | Output minimum source DC current (DDRIO I/O Bank only) | | 6.0 | — | — | mA |
| IOL at VOL | Output minimum sink current (DDRIO I/O Bank only) | | -6.0 | — | — | mA |
| SSTL18 Class II (DDR2 Full Drive)¹ | | | | | | |
| VOH | DC output logic High | | VTT + 0.603 | — | — | V |
| VOL | DC output logic Low | | — | — | VTT - 0.603 | V |
| IOH at VOH | Output minimum source DC current (DDRIO I/O Bank only) | | 12.0 | — | — | mA |
| IOL at VOL | Output minimum sink current (DDRIO I/O Bank only) | | -12.0 | — | — | mA |
| SSTL18 DC Differential Voltage Specification | | | | | | |
| VID (DC) | DC input differential voltage | | 0.3 | — | — | V |

Note:

- To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

Table 5-50. DDR2/SSTL18 AC Specifications (Applicable to DDRIO Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|--|-------------------------------------|---------------------------|-----|---------------------------|-------|
| SSTL18 AC Differential Voltage Specification | | | | | | |
| VDIFF (AC) | AC input differential voltage | | 0.5 | — | — | V |
| Vx (AC) | AC differential cross point voltage | | $0.5 \times VDDI - 0.175$ | — | $0.5 \times VDDI + 0.175$ | V |
| SSTL18 Maximum AC Switching Speed | | | | | | |
| Dmax | Maximum data rate (for DDRIO I/O Bank) | AC loading: per JEDEC specification | — | — | 600 | Mbps |
| SSTL18 Impedance Specifications | | | | | | |

.....continued

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---------------------------|-----|-------------|-----|-------|
| Rref | Supported output driver calibrated impedance (for DDRIO I/O Bank) | Reference resistor = 150Ω | — | 20, 42 | — | Ω |
| RTT | Effective impedance value (ODT) | Reference resistor = 150Ω | — | 50, 75, 150 | — | Ω |
| SSTL18 AC Test Parameters Specifications | | | | | | |
| Vtrip | Measuring/trip point for data path | | — | 0.9 | — | V |
| Rent | Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 2k | — | Ω |
| Cent | Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 5 | — | pF |
| Rtt_test | Reference resistance for data test path for SSTL18 Class I (t _{DP}) | | — | 50 | — | Ω |
| Rtt_test | Reference resistance for data test path for SSTL18 Class II (t _{DP}) | | — | 25 | — | Ω |
| Cload | Capacitive loading for data path (t _{DP}) | | — | 5 | — | pF |

5.7.4.2 AC Switching Characteristics [\(Ask a Question\)](#)

AC Switching Characteristics for Receiver (Input Buffers)

Table 5-51. DDR2/SSTL18 AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions: T_J = 125 °C, VDD = 1.14V, VDDI = 1.71V

| | On Die Termination (ODT) | Speed Grade -1 | Units |
|---|--------------------------|-----------------|-------|
| | | t _{py} | |
| SSTL18 (for DDRIO I/O Bank with Fixed Codes) | | | |
| Pseudo differential | None | 1.633 | ns |
| True differential | None | 1.65 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-52. DDR2/SSTL18 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions: T_J = 125 °C, VDD = 1.14V, VDDI = 1.71V

| | Speed Grade -1 | | | | | Units |
|---|-----------------|-----------------|-----------------|-----------------|-----------------|-------|
| | t _{DP} | t _{ZL} | t _{ZH} | t _{HZ} | t _{LZ} | |
| SSTL18 Class I (for DDRIO I/O Bank) | | | | | | |
| Single Ended | 2.67 | 3.078 | 3.072 | 2.489 | 2.484 | ns |
| Differential | 2.645 | 2.431 | 2.434 | 2.396 | 2.398 | ns |
| SSTL18 Class II (for DDRIO I/O Bank) | | | | | | |
| Single Ended | 2.564 | 2.973 | 2.965 | 2.45 | 2.444 | ns |
| Differential | 2.532 | 2.401 | 2.398 | 2.368 | 2.365 | ns |

5.7.5 Stub-Series Terminated Logic 1.5V (SSTL15) [\(Ask a Question\)](#)

SSTL15 Class I and Class II are supported in IGLOO 2 FPGAs and SmartFusion 2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO 2 FPGA and SmartFusion 2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

5.7.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification [\(Ask a Question\)](#)

Table 5-53. DDR3 SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|----------------------------------|------------|------------|-------|-------------------------------|-------|
| Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 1.425 | 1.5 | 1.575 | V |
| VTT | Termination voltage | | 0.698 | 0.750 | 0.803 | V |
| VREF | Input reference voltage | | 0.698 | 0.750 | 0.803 | V |
| SSTL15 DC Input Voltage Specification | | | | | | |
| VIH(DC) | DC input logic High | | VREF + 0.1 | — | 1.575 | V |
| VIL(DC) | DC input logic Low | | -0.3 | — | VREF - 0.1 | V |
| IIH (DC) | Input current High | | — | — | See Table 5-3 | — |
| IIL (DC) | Input current Low | | — | — | See Table 5-3 | — |
| SSTL15 DC Output Voltage Specification | | | | | | |
| DDR3/SSTL15 Class I (DDR3 Reduced Drive) | | | | | | |
| VOH | DC output logic High | | 0.8 x VDDI | — | — | V |
| VOL | DC output logic Low | | — | — | 0.2 x VDDI | V |
| IOH at VOH | Output minimum source DC current | | 6.5 | — | — | mA |
| IOL at VOL | Output minimum sink current | | -6.5 | — | — | mA |
| SSTL15 Class II (DDR3 Full Drive) | | | | | | |
| VOH | DC output logic High | | 0.8 x VDDI | — | — | V |
| VOL | DC output logic Low | | — | — | 0.2 x VDDI | V |
| IOH at VOH | Output minimum source DC current | | 7.6 | — | — | mA |
| IOL at VOL | Output minimum sink current | | -7.6 | — | — | mA |
| SSTL15 Differential Voltage Specification | | | | | | |
| VID | DC input differential voltage | | 0.2 | — | — | V |

Note: To meet JEDEC Electrical Compliance, use DDR3 Full Drive Transmitter.

Table 5-54. DDR3/SSTL15 AC Specifications

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|--|--------------------------------------|-----------------------|------------------------|-----------------------|-------|
| SSTL15 AC Differential Voltage Specification | | | | | | |
| VDIFF | AC input differential voltage | | 0.3 | — | — | V |
| Vx | AC differential cross point voltage | | 0.5 x VDDI - 0.150 | — | 0.5 x VDDI + 0.150 | V |
| SSTL15 Maximum AC Switching Speed (for DDRIO I/O Banks Only) | | | | | | |
| Dmax | Maximum data rate | AC loading: per JEDEC specifications | — | — | 600 | Mbps |
| SSTL15 AC Calibrated Impedance Option | | | | | | |
| Rref | Supported output driver calibrated impedance | Reference resistor = 240Ω | — | 34, 40 | — | Ω |
| RTT | Effective impedance value (ODT) | Reference resistor = 240Ω | — | 20, 30, 40, 60, 120 | — | Ω |
| SSTL15 AC Test Parameters Specifications | | | | | | |
| Vtrip | Measuring/trip point for data path | | — | 0.75 | — | V |
| Rent | Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 2k | — | Ω |
| Cent | Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 5 | — | pF |
| Rtt_test | Reference resistance for data test path for SSTL15 Class I (t_{DP}) | | — | 50 | — | Ω |

.....continued

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|----------|--|------------|-----|-----|-----|----------|
| Rtt_test | Reference resistance for data test path for SSTL15 Class II (t_{DP}) | | — | 25 | — | Ω |
| Cload | Capacitive loading for data path (t_{DP}) | | — | 5 | — | pF |

5.7.5.2 AC Switching Characteristics [\(Ask a Question\)](#)

AC Switching Characteristics for Receiver (Input Buffers)

Table 5-55. DDR3/SSTL15 AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, VDD = 1.14V, VDDI = 1.425V

| | ODT (On Die Termination) | Speed Grade -1 | | | Units |
|---|--------------------------|----------------|-------|--|-------|
| | | t_{PY} | | | |
| DDR3/SSTL15 (for DDRIO I/O Bank) – Calibration Mode Only | | | | | |
| Pseudo-Differential | None | | 1.672 | | ns |
| True-Differential | None | | 1.694 | | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-56. DDR3/SSTL15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, VDD = 1.14V, VDDI = 1.425V

| | Speed Grade -1 | | | | | Units |
|---|----------------|----------|----------|----------|----------|-------|
| | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank) | | | | | | |
| Single Ended | 2.832 | 2.766 | 2.767 | 2.658 | 2.659 | ns |
| Differential | 2.848 | 3.401 | 3.393 | 3.173 | 3.166 | ns |
| DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank) | | | | | | |
| Single Ended | 2.832 | 2.76 | 2.759 | 2.655 | 2.655 | ns |
| Differential | 2.845 | 3.397 | 3.387 | 3.179 | 3.171 | ns |

5.7.6 Low Power Double Data Rate (LPDDR) [\(Ask a Question\)](#)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO 2 FPGA and SmartFusion 2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer. This I/O standard is supported in DDRIO I/O Bank only.

5.7.6.1 Minimum and Maximum AC/DC Input and Output Levels Specification [\(Ask a Question\)](#)

Table 5-57. LPDDR AC/DC Specifications (for DDRIO IO Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|-------------------------|------------|-------------------|-------|-------------------------------|-------|
| Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 1.71 | 1.8 | 1.89 | V |
| VTT | Termination voltage | | 0.838 | 0.900 | 0.964 | V |
| VREF | Input reference voltage | | 0.838 | 0.900 | 0.964 | V |
| LPDDR DC Input Voltage Specification | | | | | | |
| VIH (DC) | DC input logic High | | $0.7 \times VDDI$ | — | 1.89 | V |
| VIL (DC) | DC input logic Low | | -0.3 | — | $0.3 \times VDDI$ | V |
| IIH (DC) | Input current High | | — | — | See Table 5-3 | — |
| IIL (DC) | Input current Low | | — | — | See Table 5-3 | — |
| LPDDR DC Output Voltage Specification | | | | | | |
| LPDDR Reduced Drive | | | | | | |
| VOH | DC output logic High | | $0.9 \times VDDI$ | — | — | V |

.....continued

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|----------------------------------|------------|-------------------|-----|-------------------|-------|
| VOL | DC output logic Low | | — | — | $0.1 \times VDDI$ | V |
| IOH at VOH | Output minimum source DC current | | 0.1 | — | — | mA |
| IOL at VOL | Output minimum sink current | | -0.1 | — | — | mA |
| LPDDR Full Drive¹ | | | | | | |
| VOH | DC output logic High | | $0.9 \times VDDI$ | — | — | V |
| VOL | DC output logic Low | | — | — | $0.1 \times VDDI$ | V |
| IOH at VOH | Output minimum source DC current | | 0.1 | — | — | mA |
| IOL at VOL | Output minimum sink current | | -0.1 | — | — | mA |
| LPDDR DC Differential Voltage Specification | | | | | | |
| VID (DC) | DC input differential voltage | | $0.4 \times VDDI$ | — | — | V |

Note:

- To meet JEDEC Electrical Compliance, use LPDDR Full Drive .

Table 5-58. LPDDR Maximum AC Switching Speeds (for DDRIO I/O Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---------|-------------------|--------------------------------------|-----|-----|-----|-------|
| Dmax | Maximum data rate | AC loading: per JEDEC specifications | — | — | 360 | Mbps |

Table 5-59. LPDDR AC Specifications (for DDRIO IO Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|--|---------------------------|-------------------|-------------|-------------------|-------|
| LPDDR AC Differential Voltage Specification | | | | | | |
| V _{DIFF} (AC) | AC Input differential voltage | — | $0.6 \times VDDI$ | — | — | V |
| V _x (AC) | AC Differential Cross Point Voltage | — | $0.4 \times VDDI$ | — | $0.6 \times VDDI$ | V |
| LPDDR Impedance Specifications | | | | | | |
| R _{ref} | Supported Output Driver Calibrated Impedance | Reference Resistor = 150Ω | — | 20,42 | — | Ω |
| R _{TT} | Effective impedance Value - ODT | Reference Resistor = 150Ω | — | 50, 75, 150 | — | Ω |
| LPDDR AC Test Parameters Specifications | | | | | | |
| V _{trip} | Measuring/Trip Point for Data Path | — | — | 0.9 | — | V |
| R _{ent} | Resistance for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | — | — | 2k | — | Ω |
| C _{ent} | Capacitive Loading for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | — | — | 5 | — | pF |
| R _{tt_test} | Reference resistance for Data Test Path for LPDDR (t_{DP}) | — | — | 50 | — | Ω |
| C _{load} | Capacitive Loading for Data Path (t_{DP}) | — | — | 5 | — | pF |

5.7.6.2 AC Switching Characteristics [\(Ask a Question\)](#)**Table 5-60.** LPDDR AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions: T_j = 125 °C, VDD = 1.14V, VDDI = 1.71V

| | ODT (On Die Termination) | Speed Grade -1 | | Units |
|--|--------------------------|-----------------|--|-------|
| | | t _{py} | | |
| LPDDR (for DDRIO I/O Bank with Fixed Codes) | | | | |
| Pseudo-Differential | None | 1.633 | | ns |
| True-Differential | None | 1.65 | | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-61. LPDDR AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$, $V_{DDI} = 1.71\text{V}$

| | Speed Grade -1 | | | | | Units |
|---|----------------|----------|----------|----------|----------|-------|
| | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| LPDDR Reduced Drive (for DDRIO I/O Bank) | | | | | | |
| Single Ended | 2.645 | 2.431 | 2.434 | 2.396 | 2.398 | ns |
| Differential | 2.652 | 3.044 | 3.038 | 2.46 | 2.455 | ns |
| LPDDR Full Drive (for DDRIO I/O Bank) | | | | | | |
| Single Ended | 2.532 | 2.401 | 2.398 | 2.368 | 2.365 | ns |
| Differential | 2.546 | 2.509 | 2.503 | 2.852 | 2.845 | ns |

5.7.6.3 Minimum and Maximum AC/DC Input and Output Levels Specification Using LPDDR-LVCMOS 1.8V Mode [\(Ask a Question\)](#)

Table 5-62. LPDDR-LVCMOS 1.8V Mode, Minimum and Maximum DC Input and Output Levels (Applicable to DDRIO I/O Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|------------|-----------------------|-----|-------------------------------|-------|
| LPDDR-LVCMOS 1.8V Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply Voltage | — | 1.710 | 1.8 | 1.89 | V |
| LPDDR-LVCMOS 1.8V Mode DC Input Voltage Specification | | | | | | |
| VIH(DC) | DC input Logic HIGH for (MSIOD and DDRIO I/O Banks) | — | $0.65 \times V_{DDI}$ | — | 1.89 | V |
| VIH(DC) | DC input Logic HIGH (for MSIO I/O Bank) | — | $0.65 \times V_{DDI}$ | — | 3.45 | V |
| VIL(DC) | DC input Logic LOW | — | -0.3 | — | $0.35 \times V_{DDI}$ | V |
| IIH(DC) | Input current HIGH | — | — | — | See Table 5-3 | — |
| IIL(DC) | Input current LOW | — | — | — | See Table 5-3 | — |
| LPDDR-LVCMOS 1.8V Mode DC Output Voltage Specification | | | | | | |
| VOH | DC output Logic HIGH | — | $V_{DDI} - 0.45$ | — | — | V |
| VOL | DC output Logic LOW | — | — | — | 0.45 | V |

Table 5-63. LPDDR-LVCMOS 1.8V Maximum AC Switching Speeds (Applicable to DDRIO I/O Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---------|--|---|-----|-----|-----|-------|
| Dmax | Maximum Data Rate (for DDRIO I/O Bank) | AC Loading: 17 pF Load, 8 mA Drive and Above/All Slew | — | — | 360 | Mbps |

Table 5-64. LPDDR-LVCMOS 1.8V AC Test Parameters and Driver Impedance Specifications (Applicable to DDRIO I/O Bank Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|--|------------|-----|------------------------|-----|----------|
| LPDDR - LVCMOS 1.8V Calibrated Impedance Option | | | | | | |
| Rodt_cal | Supported Output Driver Calibrated Impedance (for DDRIO I/O Bank) | — | — | 75, 60, 50, 33, 25, 20 | — | Ω |
| LPDDR- LVCMOS 1.8 V AC Test Parameters Specifications | | | | | | |
| Vtrip | Measuring/Trip Point for Data Path | — | — | 0.9 | — | V |
| Rent | Resistance for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | — | — | 2k | — | Ω |

.....continued

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---------|--|------------|-----|-----|-----|-------|
| Cent | Capacitive Loading for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | — | — | 5 | — | pF |
| Cload | Capacitive Loading for Data Path (t_{DP}) | — | — | 5 | — | pF |

Table 5-65. LPDDR-LVCMOS 1.8V Mode Transmitter Drive Strength Specification (Applicable to DDRIO I/O Bank Only)

| Output Drive Selection | VOH (V) | VOL (V) | IOH (at VOH) | IOL (at VOL) | Notes |
|------------------------|-------------|---------|--------------|--------------|-------|
| | Min | Max | mA | mA | |
| 2 mA | VDDI - 0.45 | 0.45 | 2 | 2 | — |
| 4 mA | VDDI - 0.45 | 0.45 | 4 | 4 | — |
| 6 mA | VDDI - 0.45 | 0.45 | 6 | 6 | — |
| 8 mA | VDDI - 0.45 | 0.45 | 8 | 8 | — |
| 10 mA | VDDI - 0.45 | 0.45 | 10 | 10 | — |
| 12 mA | VDDI - 0.45 | 0.45 | 12 | 12 | — |
| 16 mA ¹ | VDDI - 0.45 | 0.45 | 16 | 16 | — |

Note:

- 16 mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance.

5.7.6.4 AC Switching Characteristics [\(Ask a Question\)](#)

Table 5-66. LPDDR - LVCMOS 1.8 V AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, VDD = 1.14V, VDDI = 1.71V

| | ODT (On Die Termination) | Speed Grade -1 | | Units |
|---|--------------------------|----------------|-----------|-------|
| | | t_{PY} | t_{PYS} | |
| LPDDR-LVCMOS 1.8 mode (for DDRIO I/O Bank with Fixed Codes) | None | 2.071 | 2.213 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-67. LPDDR - LVCMOS 1.8V AC Switching Characteristics for Transmitter DDRIO I/O Bank (Output and Tristate Buffers)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, VDD = 1.14V, VDDI = 1.71V

| Output Drive Selection | Slew Control | Speed Grade -1 | | | | | Units |
|------------------------|--------------|----------------|----------|----------|----------|----------|-------|
| | | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| 2 mA | slow | 4.681 | 4.017 | 4.69 | 5.388 | 4.852 | ns |
| | medium | 4.211 | 3.599 | 4.219 | 5.058 | 4.488 | ns |
| | medium_fast | 3.978 | 3.392 | 3.986 | 4.874 | 4.327 | ns |
| | fast | 3.953 | 3.373 | 3.961 | 4.858 | 4.316 | ns |
| 4 mA | slow | 4.355 | 3.657 | 4.346 | 5.967 | 5.399 | ns |
| | medium | 3.886 | 3.246 | 3.879 | 5.628 | 5.01 | ns |
| | medium_fast | 3.656 | 3.05 | 3.647 | 5.461 | 4.845 | ns |
| | fast | 3.635 | 3.033 | 3.626 | 5.447 | 4.838 | ns |
| 6 mA | slow | 4.105 | 3.422 | 4.092 | 6.221 | 5.599 | ns |
| | medium | 3.68 | 3.05 | 3.668 | 5.9 | 5.257 | ns |
| | medium_fast | 3.477 | 2.867 | 3.463 | 5.739 | 5.118 | ns |
| | fast | 3.451 | 2.849 | 3.437 | 5.72 | 5.104 | ns |

.....continued

| Output Drive Selection | Slew Control | Speed Grade -1 | | | | | Units |
|------------------------|--------------|----------------|----------|----------|----------|----------|-------|
| | | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| 8 mA | slow | 4.015 | 3.32 | 3.998 | 6.458 | 5.808 | ns |
| | medium | 3.59 | 2.947 | 3.574 | 6.129 | 5.449 | ns |
| | medium_fast | 3.383 | 2.761 | 3.366 | 5.963 | 5.304 | ns |
| | fast | 3.357 | 2.746 | 3.34 | 5.954 | 5.289 | ns |
| 10 mA | slow | 3.888 | 3.18 | 3.864 | 6.739 | 6.045 | ns |
| | medium | 3.485 | 2.822 | 3.467 | 6.422 | 5.7 | ns |
| | medium_fast | 3.281 | 2.642 | 3.26 | 6.277 | 5.553 | ns |
| | fast | 3.258 | 2.627 | 3.238 | 6.27 | 5.546 | ns |
| 12 mA | slow | 3.795 | 3.096 | 3.773 | 6.773 | 6.067 | ns |
| | medium | 3.408 | 2.764 | 3.389 | 6.47 | 5.743 | ns |
| | medium_fast | 3.215 | 2.599 | 3.194 | 6.346 | 5.61 | ns |
| | fast | 3.196 | 2.584 | 3.175 | 6.335 | 5.604 | ns |
| 16 mA | slow | 3.744 | 3.035 | 3.719 | 6.944 | 6.207 | ns |
| | medium | 3.358 | 2.712 | 3.339 | 6.657 | 5.868 | ns |
| | medium_fast | 3.175 | 2.546 | 3.153 | 6.547 | 5.751 | ns |
| | fast | 3.156 | 2.531 | 3.133 | 6.541 | 5.747 | ns |

5.8 Differential I/O Standards [\(Ask a Question\)](#)

Configuration of the I/O modules as a differential pair is handled by Microchip's Libero[®] SoC software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

5.8.1 LVDS [\(Ask a Question\)](#)

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

5.8.1.1 Minimum and Maximum Input and Output Levels [\(Ask a Question\)](#)

Table 5-68. LVDS DC Voltage Specification

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|-----------------------------------|------------|-------|-------|-------------------------------|-------|
| LVDS Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | 2.5V range | 2.375 | 2.5 | 2.625 | V |
| VDDI | Supply voltage | 3.3V range | 3.15 | 3.3 | 3.45 | V |
| LVDS DC Input Voltage Specification | | | | | | |
| VI | DC Input voltage | 2.5V range | 0 | — | 2.925 | V |
| VI | DC input voltage | 3.3V range | 0 | — | 3.45 | V |
| I _{IH} (DC) | Input current High | | — | — | See Table 5-3 | — |
| I _{IL} (DC) | Input current Low | | — | — | See Table 5-3 | — |
| LVDS DC Output Voltage Specification | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V |
| LVDS Differential Voltage Specification | | | | | | |
| VOD | Differential output voltage swing | | 250 | 350 | 450 | mV |
| VOCM | Output common mode voltage | | 1.125 | 1.25 | 1.375 | V |
| VICM | Input common mode voltage | | 0.05 | 1.25 | 2.35 | V |
| VID ¹ | Input differential voltage | | 100 | 350 | 600 | mV |

Note:

- When VID is < 300 mV, the input signal is delayed by up to an additional 450 ps for LVDS25 and 280 ps for LVDS33. This delay is not accounted in the timing model. Clock insertion delays, propagation delays, and I/O to FF delays are marginally affected. Adding a parallel termination resistor of 200Ω +/- 5% across the receiver pins can mitigate this additional delay when VID is < 300 mV.

Table 5-69. LVDS AC Specifications

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|--|-----|-------------|-----|-------|
| LVDS Maximum AC Switching Speed | | | | | | |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 12 pF/100Ω differential load | — | — | 480 | Mbps |
| Dmax | Maximum data rate (for MSIOD I/O Bank) | AC loading: 10 pF/100Ω differential load | — | — | 480 | Mbps |
| LVDS Impedance Specification | | | | | | |
| Rt | Termination resistance | — | — | 100 | — | Ω |
| LVDS AC Test Parameters Specifications | | | | | | |
| Vtrip | Measuring/trip point for data path | | — | Cross point | — | V |
| Rent | Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 2k | — | Ω |
| Cent | Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 5 | — | pF |

5.8.1.2 LVDS25 AC Switching Characteristics [\(Ask a Question\)](#)**AC Switching Characteristics for Receiver (Input Buffers)****Table 5-70.** LVDS25 Receiver Characteristics—Worst-Case Military Conditions: T_J = 125 °C, VDD = 1.14V, VDDI = 2.375V

| | On Die Termination (ODT) | Speed Grade -1 | Units |
|---------------------------|--------------------------|-----------------|-------|
| | | t _{py} | |
| LVDS (for MSIO I/O Bank) | None | 3.061 | ns |
| | 100 | 3.057 | ns |
| LVDS (for MSIOD I/O Bank) | None | 2.792 | ns |
| | 100 | 2.787 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**Table 5-71.** LVDS25 Transmitter Characteristics—Worst-Case Military Conditions: T_J = 125 °C, VDD = 1.14V, VDDI = 2.375V

| | Speed Grade -1 | | | | | Units |
|----------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------|
| | t _{DP} | t _{ZL} | t _{ZH} | t _{HZ} | t _{LZ} | |
| LVDS (for MSIO I/O Bank) | 2.299 | 2.602 | 2.589 | 2.305 | 2.32 | ns |
| LVDS (for MSIOD I/O Bank) | | | | | | |
| No pre-emphasis | 1.656 | 1.845 | 1.838 | 1.992 | 1.969 | ns |
| Min pre-emphasis | 1.583 | 1.868 | 1.866 | 2.018 | 1.998 | ns |
| Med pre-emphasis | 1.559 | 1.893 | 1.886 | 2.045 | 2.021 | ns |

5.8.1.3 LVDS33 AC Switching Characteristics [\(Ask a Question\)](#)**AC Switching Characteristics for Receiver (Input Buffers)**

Table 5-72. LVDS33 Receiver Characteristics—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$, $V_{DDI} = 3.15\text{V}$

| | On Die Termination (ODT) | Speed Grade -1 | Units |
|----------------------------|--------------------------|----------------|-------|
| | | t_{PY} | |
| LVDS33 (for MSIO I/O Bank) | None | 2.763 | ns |
| | 100 | 2.76 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**Table 5-73.** LVDS33 Transmitter Characteristics—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$, $V_{DDI} = 3.15\text{V}$

| | Speed Grade -1 | | | | | Units |
|----------------------------|----------------|----------|----------|----------|----------|-------|
| | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| LVDS33 (for MSIO I/O Bank) | 2.069 | 2.112 | 2.106 | 2.078 | 2.09 | ns |

5.8.2 B-LVDS [\(Ask a Question\)](#)

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

5.8.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification [\(Ask a Question\)](#)**Table 5-74.** B-LVDS DC Voltage Specification

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|--|------------|-------|-------|---------------|-------|
| Bus-LVDS Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V |
| Bus-LVDS DC Input Voltage Specification | | | | | | |
| V_I | DC input voltage | | 0 | — | 2.925 | V |
| I_{IH} (DC) | Input current High | | — | — | See Table 5-3 | — |
| I_{IL} (DC) | Input current Low | | — | — | See Table 5-3 | — |
| Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank only) | | | | | | |
| V_{OH} | DC output logic High | | 1.25 | 1.425 | 1.6 | V |
| V_{OL} | DC output logic Low | | 0.9 | 1.075 | 1.25 | V |
| Bus-LVDS Differential Voltage Specification | | | | | | |
| VOD | Differential output voltage swing (for MSIO I/O Bank only) | | 65 | — | 460 | mV |
| VOCM | Output common mode voltage (for MSIO I/O Bank only) | | 1.1 | — | 1.5 | V |
| VICM | Input common mode voltage | | 0.05 | — | 2.4 | V |
| VID | Input differential voltage | | 0.1 | — | VDDI | V |

Table 5-75. B-LVDS AC Specifications

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|--|---|-----|-------------|-----|----------|
| Bus-LVDS Maximum AC Switching Speed | | | | | | |
| D_{max} | Maximum data rate (for MSIO I/O Bank) | AC loading: 2 pF/100 Ω differential load | — | — | 450 | Mbps |
| Bus-LVDS Impedance Specifications | | | | | | |
| R_t | Termination resistance | | — | 27 | — | Ω |
| Bus-LVDS AC Test Parameters Specifications | | | | | | |
| V_{trip} | Measuring/trip point for data path | | — | Cross point | — | V |
| R_{ent} | Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 2k | — | Ω |

.....continued

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---------|--|------------|-----|-----|-----|-------|
| Cent | Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 5 | — | pF |

5.8.2.2 AC Switching Characteristics [\(Ask a Question\)](#)

AC Switching Characteristics for Receiver (Input Buffers)

Table 5-76. B-LVDS AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$, $V_{DDI} = 2.375\text{V}$

| | On-Die Termination (ODT) | Speed Grade -1 | Units |
|-------------------------------|--------------------------|----------------|-------|
| | | t_{pV} | |
| Bus-LVDS (for MSIO I/O Bank) | None | 3.011 | ns |
| | 100 | 3.006 | ns |
| Bus-LVDS (for MSIOD I/O Bank) | None | 2.722 | ns |
| | 100 | 2.725 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-77. B-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$, $V_{DDI} = 2.375\text{V}$

| | Speed Grade -1 | | | | | Units |
|------------------------------|----------------|----------|----------|----------|----------|-------|
| | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| Bus-LVDS (for MSIO I/O Bank) | 2.78 | 2.632 | 2.617 | 2.448 | 2.436 | ns |

5.8.3 M-LVDS [\(Ask a Question\)](#)

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

5.8.3.1 Minimum and Maximum Input and Output Levels [\(Ask a Question\)](#)

Table 5-78. M-LVDS DC Voltage Specification

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|--|------------|-------|-------|-------------------------------|-------|
| M-LVDS Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage ¹ | | 2.375 | 2.5 | 2.625 | V |
| M-LVDS DC Input Voltage Specification | | | | | | |
| VI | DC input voltage | | 0 | — | 2.925 | V |
| I _{IH} (DC) | Input current High | | — | — | See Table 5-3 | — |
| I _{IL} (DC) | Input current Low | | — | — | See Table 5-3 | — |
| M-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only) | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V |
| M-LVDS Differential Voltage Specification | | | | | | |
| VOD | Differential output voltage Swing (for MSIO I/O Bank only) | | 300 | — | 650 | mV |
| VOCM | Output common mode voltage (for MSIO I/O Bank only) | | 0.3 | — | 2.1 | V |
| VICM | Input common mode voltage | | 0.3 | — | 1.2 | V |
| VID | Input differential voltage | | 50 | — | 2400 | mV |

Note:

1. Only M-LVDS TYPE I is supported.

Table 5-79. M-LVDS AC Specifications

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|---|---|-----|-------------|-----|-------|
| M-LVDS Maximum AC Switching Speeds | | | | | | |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 2 pF/100Ω differential load | — | — | 450 | Mbps |
| M-LVDS Impedance Specification | | | | | | |
| Rt | Termination resistance | — | — | 50 | — | Ω |
| M-LVDS AC Test Parameters Specifications | | | | | | |
| VTrip | Measuring/trip point for data path | | — | Cross point | — | V |
| Rent | Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 2k | — | Ω |
| Cent | Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ}) | | — | 5 | — | pF |

5.8.3.2 AC Switching Characteristics [\(Ask a Question\)](#)**AC Switching Characteristics for Receiver (Input Buffers)****Table 5-80.** M-LVDS AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military conditions: T_j = 125 °C, VDD = 1.14V, VDDI = 2.375V

| | On-Die Termination (ODT) | Speed Grade -1 | Units |
|-----------------------------|--------------------------|-----------------|-------|
| | | t _{py} | |
| M-LVDS (for MSIO I/O Bank) | None | 3.011 | ns |
| | 100 | 3.006 | ns |
| M-LVDS (for MSIOD I/O Bank) | None | 2.722 | ns |
| | 100 | 2.725 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**Table 5-81.** M-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military conditions: T_j = 125 °C, VDD = 1.14V, VDDI = 2.375V

| | Speed Grade -1 | | | | | Units |
|----------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------|
| | t _{DP} | t _{ZL} | t _{ZH} | t _{HZ} | t _{LZ} | |
| M-LVDS (for MSIO I/O Bank) | 2.78 | 2.632 | 2.616 | 2.447 | 2.436 | ns |

5.8.4 Mini-LVDS [\(Ask a Question\)](#)

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

5.8.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels [\(Ask a Question\)](#)**Table 5-82.** Mini-LVDS DC Voltage Specification

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|----------------------|------------|-------|-------|-------|-------|
| Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V |
| Mini-LVDS DC Input Voltage Specification | | | | | | |
| VI | DC Input voltage | | 0 | — | 2.925 | V |
| Mini-LVDS DC Output Voltage Specification | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V |

.....continued

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|-----------------------------------|------------|-----|-----|-----|-------|
| Mini-LVDS Differential Voltage Specification | | | | | | |
| VOD | Differential output voltage swing | | 300 | — | 600 | mV |
| VOCM | Output common mode voltage | | 1 | — | 1.4 | V |
| VICM | Input common mode voltage | | 0.3 | — | 1.2 | V |
| VID | Input differential voltage | | 100 | — | 600 | mV |

Table 5-83. Mini-LVDS AC Specifications

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|--|--|-----|-------------|-----|-------|
| Mini-LVDS Maximum AC Switching Speed | | | | | | |
| Dmax | Maximum data rate (MSIO I/O Bank) | AC loading: 2 pF/100Ω differential load | — | — | 460 | Mbps |
| Dmax | Maximum data rate (MSIOD I/O Bank) | AC loading: 10 pF/100Ω differential load | — | — | 480 | Mbps |
| Mini-LVDS Impedance Specification | | | | | | |
| Rt | Termination resistance | | — | 100 | — | Ω |
| Mini-LVDS AC Test Parameters Specifications | | | | | | |
| VTrip | Measuring/trip point for data path | | — | Cross point | — | V |
| Rent | Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 2k | — | Ω |
| Cent | Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 5 | — | pF |

5.8.4.2 AC Switching Characteristics [\(Ask a Question\)](#)

AC Switching Characteristics for Receiver (Input Buffers)

Table 5-84. Mini-LVDS AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, VDD = 1.14V, VDDI = 2.375V

| | On-Die Termination (ODT) | Speed Grade -1 | Units |
|--------------------------------|--------------------------|----------------|-------|
| | | t_{PY} | |
| Mini-LVDS (for MSIO I/O Bank) | None | 3.112 | ns |
| | 100 | 2.995 | ns |
| Mini-LVDS (for MSIOD I/O Bank) | None | 2.612 | ns |
| | 100 | 2.612 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-85. Mini-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, VDD = 1.14V, VDDI = 2.375V

| | Speed Grade -1 | | | | | Units |
|---------------------------------------|----------------|----------|----------|----------|----------|-------|
| | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| Mini-LVDS (for MSIO I/O Bank) | 2.3 | 2.602 | 2.59 | 2.306 | 2.32 | ns |
| Mini-LVDS (for MSIOD I/O Bank) | | | | | | |
| No pre-emphasis | 1.652 | 1.84 | 1.833 | 1.988 | 1.965 | ns |
| Min pre-emphasis | 1.652 | 1.84 | 1.833 | 1.988 | 1.965 | ns |
| Med pre-emphasis | 1.577 | 1.868 | 1.86 | 2.02 | 1.994 | ns |
| Max pre-emphasis | 1.555 | 1.894 | 1.883 | 2.048 | 2.019 | ns |

5.8.5 RSDS [\(Ask a Question\)](#)

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

5.8.5.1 Minimum and Maximum Input and Output Levels [\(Ask a Question\)](#)

Table 5-86. RSDS DC Voltage Specification

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|-----------------------------------|------------|-------|-------|-------|-------|
| Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 2.375 | 2.5 | 2.625 | V |
| RSDS DC Input Voltage Specification | | | | | | |
| VI | DC input voltage | | 0 | — | 2.925 | V |
| RSDS DC Output Voltage Specification | | | | | | |
| VOH | DC output logic High | | 1.25 | 1.425 | 1.6 | V |
| VOL | DC output logic Low | | 0.9 | 1.075 | 1.25 | V |
| RSDS Differential Voltage Specification | | | | | | |
| VOD | Differential output voltage swing | | 100 | — | 600 | mV |
| VOCM | Output common mode voltage | | 0.5 | — | 1.5 | V |
| VICM | Input common mode voltage | | 0.3 | — | 1.5 | V |
| VID | Input differential voltage | | 100 | — | 600 | mV |

Table 5-87. RSDS AC Specifications

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---|--|--|-----|-------------|-----|-------|
| RSDS Maximum AC Switching Speed | | | | | | |
| Dmax | Maximum data rate (for MSIO I/O Bank) | AC loading: 2 pF/100Ω differential load | — | — | 460 | Mbps |
| Dmax | Maximum data rate (for MSIOD I/O Bank) | AC loading: 10 pF/100Ω differential load | — | — | 480 | Mbps |
| RSDS Impedance Specification | | | | | | |
| Rt | Termination resistance | | — | 100 | — | Ω |
| RSDS AC Test Parameters Specifications | | | | | | |
| VTrip | Measuring/trip point for data path | | — | Cross point | — | V |
| Rent | Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 2k | — | Ω |
| Cent | Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ}) | | — | 5 | — | pF |

5.8.5.2 AC Switching Characteristics [\(Ask a Question\)](#)

AC Switching Characteristics for Receiver (Input Buffers)

Table 5-88. RSDS AC Switching Characteristics for Receiver (Input Buffers)—Worst-Case Military conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{V}$, $V_{DDI} = 2.375\text{V}$

| | On-Die Termination (ODT) | Speed Grade -1 | Units |
|---------------------------|--------------------------|----------------|-------|
| | | t_{py} | |
| RSDS (for MSIO I/O Bank) | None | 3.112 | ns |
| | 100 | 3.108 | ns |
| RSDS (for MSIOD I/O Bank) | None | 2.832 | ns |
| | 100 | 2.821 | ns |

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 5-89. RSDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)—Worst-Case Military conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$, $V_{DDI} = 2.375\text{V}$

| | Speed Grade -1 | | | | | Units |
|----------------------------------|----------------|----------|----------|----------|----------|-------|
| | t_{DP} | t_{ZL} | t_{ZH} | t_{HZ} | t_{LZ} | |
| RSDS (for MSIO I/O Bank) | 2.256 | 2.484 | 2.472 | 2.111 | 2.096 | ns |
| RSDS (for MSIOD I/O Bank) | | | | | | |
| No pre-emphasis | 1.661 | 1.648 | 1.645 | 1.675 | 1.665 | ns |
| Min pre-emphasis | 1.651 | 1.84 | 1.833 | 1.988 | 1.964 | ns |
| Med pre-emphasis | 1.577 | 1.868 | 1.859 | 2.019 | 1.993 | ns |
| Max pre-emphasis | 1.555 | 1.894 | 1.883 | 2.047 | 2.018 | ns |

5.8.6 LVPECL [\(Ask a Question\)](#)

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO 2 and SmartFusion 2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

5.8.6.1 Minimum and Maximum Input and Output Levels [\(Ask a Question\)](#)

Table 5-90. LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|----------------------------|------------|------|-----|-------|-------|
| Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply voltage | | 3.15 | 3.3 | 3.45 | V |
| LVPECL DC Input Voltage Specification | | | | | | |
| VI | DC input voltage | | 0 | — | 3.45 | V |
| LVPECL Differential Voltage Specification | | | | | | |
| VICM | Input common mode voltage | | 0.3 | — | 2.8 | V |
| VIDIFF | Input differential voltage | | 100 | 300 | 1,000 | mV |

Table 5-91. LVPECL Maximum AC Switching Speeds (Applicable to MSIO I/O Banks Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|---------------------------------|---------------------------------------|------------|-----|-----|-----|-------|
| LVPECL AC Specifications | | | | | | |
| Fmax | Maximum data rate (for MSIO I/O Bank) | | — | — | 810 | Mbps |

5.8.6.2 AC Switching Characteristics [\(Ask a Question\)](#)

AC Switching Characteristics for Receiver (Input Buffers)

Table 5-92. LVPECL Receiver Characteristics—Worst-Case Military conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$, $V_{DDI} = 3.15\text{V}$

| | On-Die Termination (ODT) | t_{pY} | Units |
|-----------------------------------|--------------------------|----------------|-------|
| | | Speed Grade -1 | |
| LVPECL (for MSIO I/O Bank) | None | 2.71 | ns |
| | 100 | 2.71 | ns |

5.9 I/O Register Specifications [\(Ask a Question\)](#)

5.9.1 Input Register [\(Ask a Question\)](#)

Figure 5-4. Timing Model for Input Register

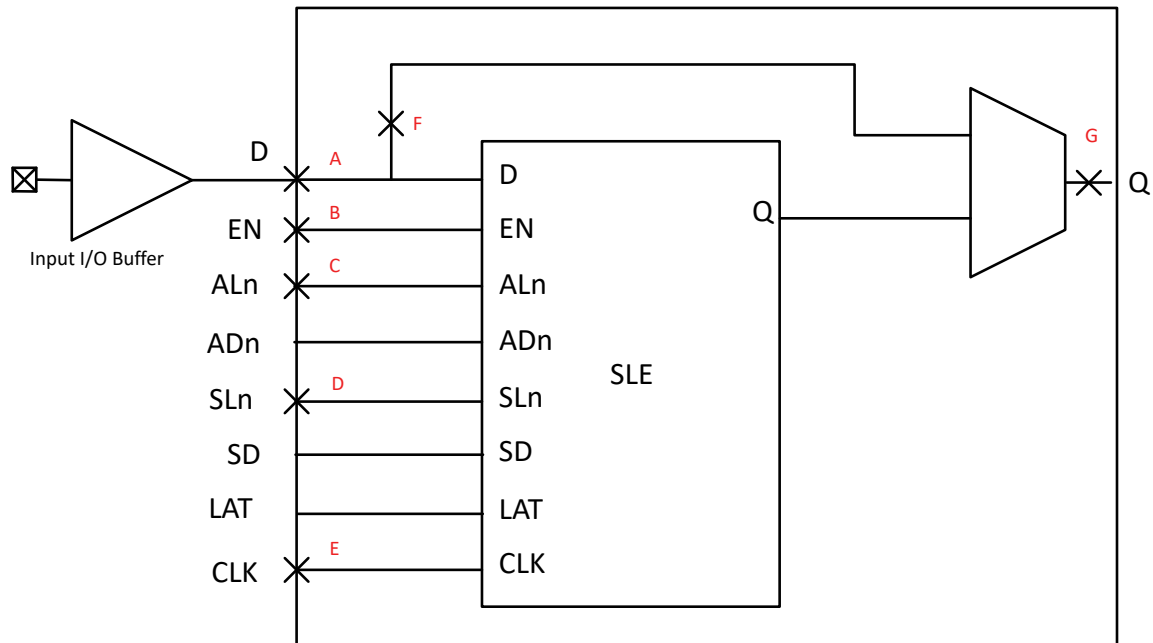
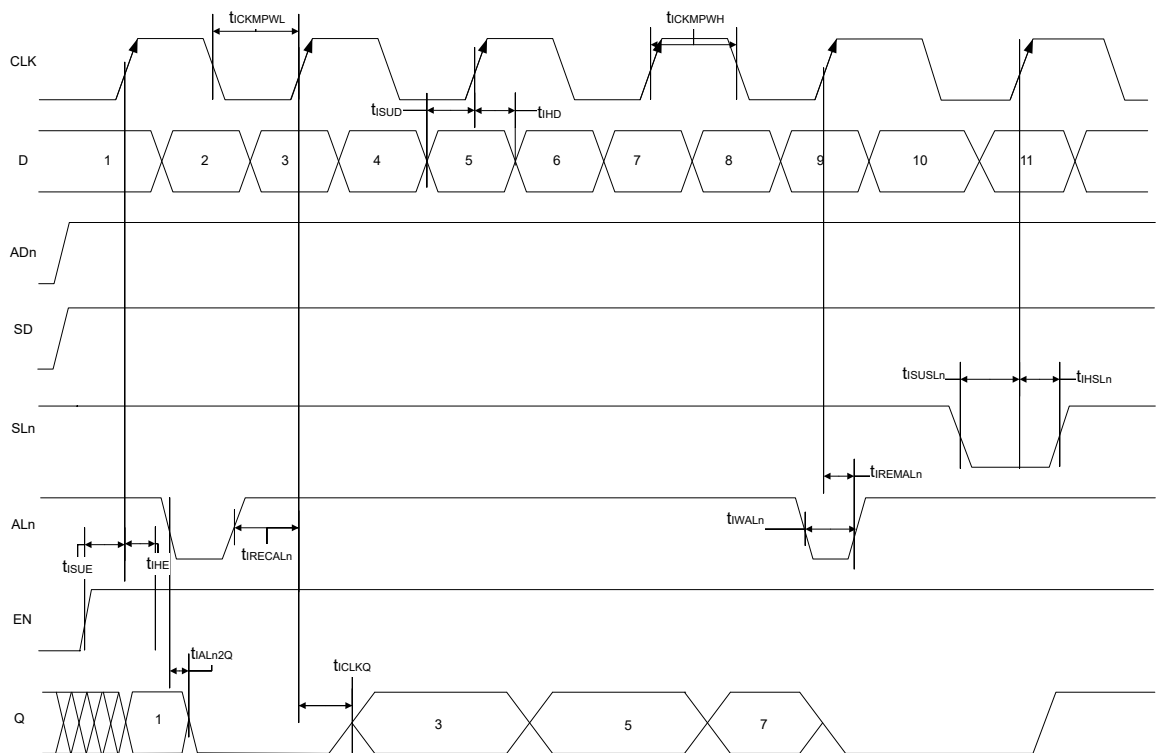


Figure 5-5. I/O Register Input Timing Diagram

Table 5-93. Input Data Register Propagation Delays—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Measuring Nodes (from, to)* | Speed Grade -1 | Units |
|---------------|--|-----------------------------|----------------------------|-------|
| t_{IBYP} | Bypass Delay of the Input Register | F,G | See SmartTime ¹ | ns |
| t_{iCLKQ} | Clock-to-Q of the Input Register | E,G | 0.13 | ns |
| t_{iSUD} | Data Setup Time for the Input Register | A,E | See SmartTime ¹ | ns |
| t_{iHD} | Data Hold Time for the Input Register | A,E | See SmartTime ¹ | ns |
| t_{iSUE} | Enable Setup Time for the Input Register | B,E | 0.821 | ns |
| t_{iHE} | Enable Hold Time for the Input Register | B,E | 0.016 | ns |
| t_{iSUSL} | Synchronous Load Setup Time for the Input Register | D,E | 1.726 | ns |
| t_{iHSL} | Synchronous Load Hold Time for the Input Register | D,E | 0.062 | ns |
| t_{iALn2Q} | Asynchronous Clear-to-Q of the Input Register ($ADn=1$) | C,G | 0.502 | ns |
| | Asynchronous Preset-to-Q of the Input Register ($ADn=0$) | C,G | 0.459 | ns |
| $t_{iREMAIn}$ | Asynchronous Load Removal Time for the Input Register | C,E | 0.127 | ns |
| $t_{iRECALn}$ | Asynchronous Load Recovery Time for the Input Register | C,E | 0.213 | ns |
| t_{iWALn} | Asynchronous Load Minimum Pulse Width for the Input Register | C,C | 0.444 | ns |
| $t_{iCKMPWH}$ | Clock Minimum Pulse Width High for the Input Register | E,E | 0.101 | ns |
| $t_{iCKMPWL}$ | Clock Minimum Pulse Width Low for the Input Register | E,E | 0.223 | ns |

Note:

1. Delay depends on the die and I/O location. Use the SmartTime tool in Libero for accurate timing data.

5.9.2 Output/Enable Register [\(Ask a Question\)](#)

Figure 5-6. Timing Model for Output/Enable Register

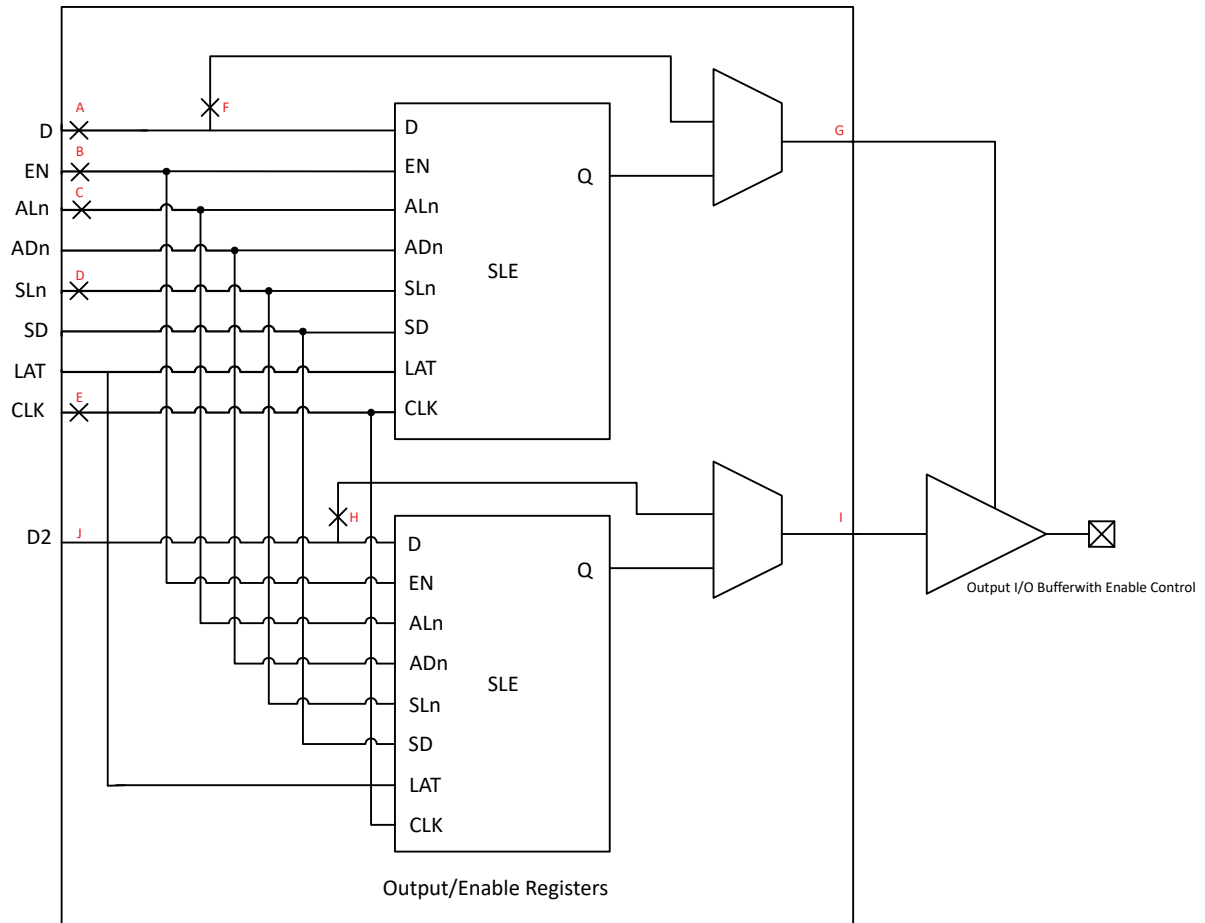


Figure 5-7. I/O Register Output Timing Diagram

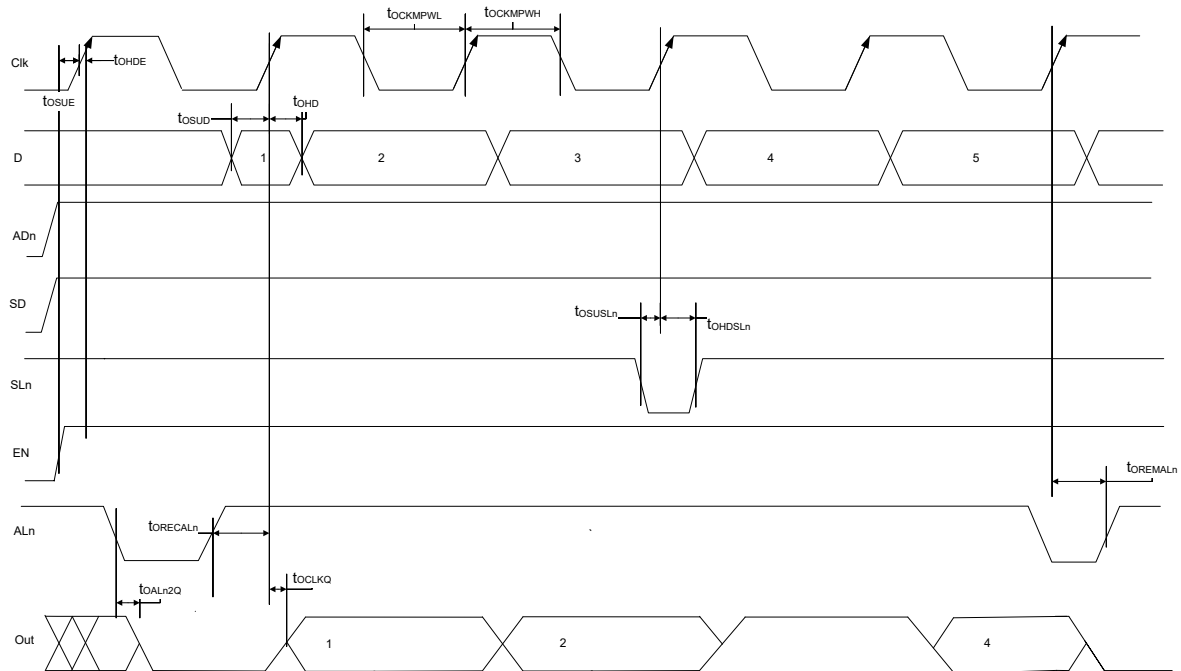


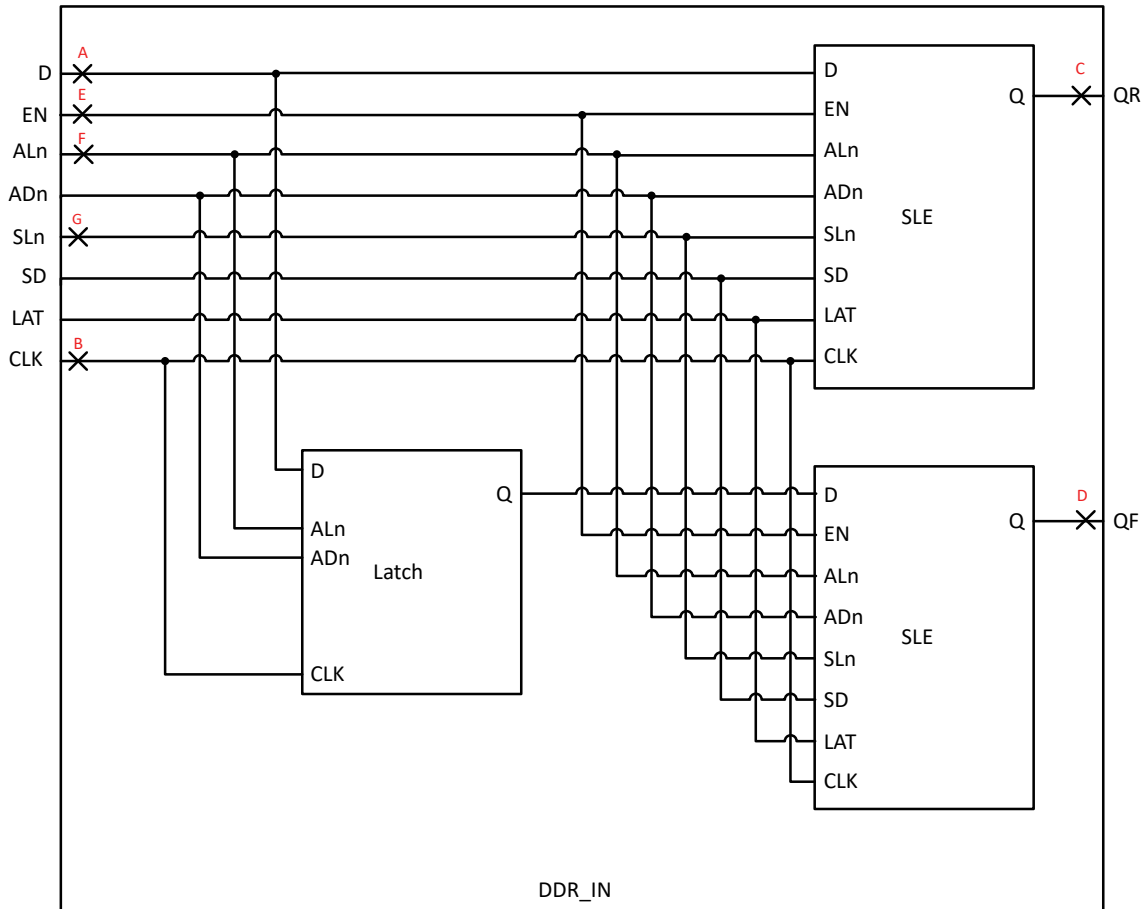
Table 5-94. Output/Enable Data Register Propagation Delays—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Measuring Nodes (from, to) | Speed Grade -1 | Units |
|---------------|--|----------------------------|----------------|-------|
| t_{OBYP} | Bypass Delay of the Output/Enable Register | F,G or H,I | 0.342 | ns |
| t_{OCLKQ} | Clock-to-Q of the Output/Enable Register | E,G or E,I | 0.254 | ns |
| t_{OSUD} | Data Setup Time for the Output/Enable Register | A,E or J,E | 0.268 | ns |
| t_{OHD} | Data Hold Time for the Output/Enable Register | A,E or J,E | 0.037 | ns |
| t_{OSUE} | Enable Setup Time for the Output/Enable Register | B,E | 0.821 | ns |
| t_{OHE} | Enable Hold Time for the Output/Enable Register | B,E | 0.029 | ns |
| t_{OSUSL} | Synchronous Load Setup Time for the Output/Enable Register | D,E | 1.824 | ns |
| t_{OHSL} | Synchronous Load Hold Time for the Output/Enable Register | D,E | 0.062 | ns |
| t_{OALn2Q} | Asynchronous Clear-to-Q of the Output/Enable Register ($ADn=1$) | C,G or C,I | 0.558 | ns |
| | Asynchronous Preset-to-Q of the Output/Enable Register ($ADn=0$) | C,G or C,I | 0.526 | ns |
| $t_{OREMALn}$ | Asynchronous Load Removal Time for the Output/Enable Register | C,E | 0.134 | ns |
| $t_{ORECALn}$ | Asynchronous Load Recovery Time for the Output/Enable Register | C,E | 0.236 | ns |
| t_{OWALn} | Asynchronous Load Minimum Pulse Width for the Output/Enable Register | C,C | 0.444 | ns |
| $t_{OCKMPWH}$ | Clock Minimum Pulse Width High for the Output/Enable Register | E,E | 0.101 | ns |
| $t_{OCKMPWL}$ | Clock Minimum Pulse Width Low for the Output/Enable Register | E,E | 0.223 | ns |

5.10 DDR Module Specification [\(Ask a Question\)](#)

5.10.1 Input DDR Module [\(Ask a Question\)](#)

Figure 5-8. Input DDR Module



.....continued

| Parameter | Description | Measuring Nodes (from, to) | Speed Grade -1 | Units |
|-------------------------|---|-------------------------------|----------------|-------|
| $t_{\text{DDRICKMPWL}}$ | Clock Minimum Pulse Width Low for Input DDR | B,B | 0.223 | ns |

Note:

1. Delay depends on the die and I/O location. Use the SmartTime tool in Libero for accurate timing data.

5.10.4 Output DDR Module [\(Ask a Question\)](#)

Figure 5-10. Output DDR Module

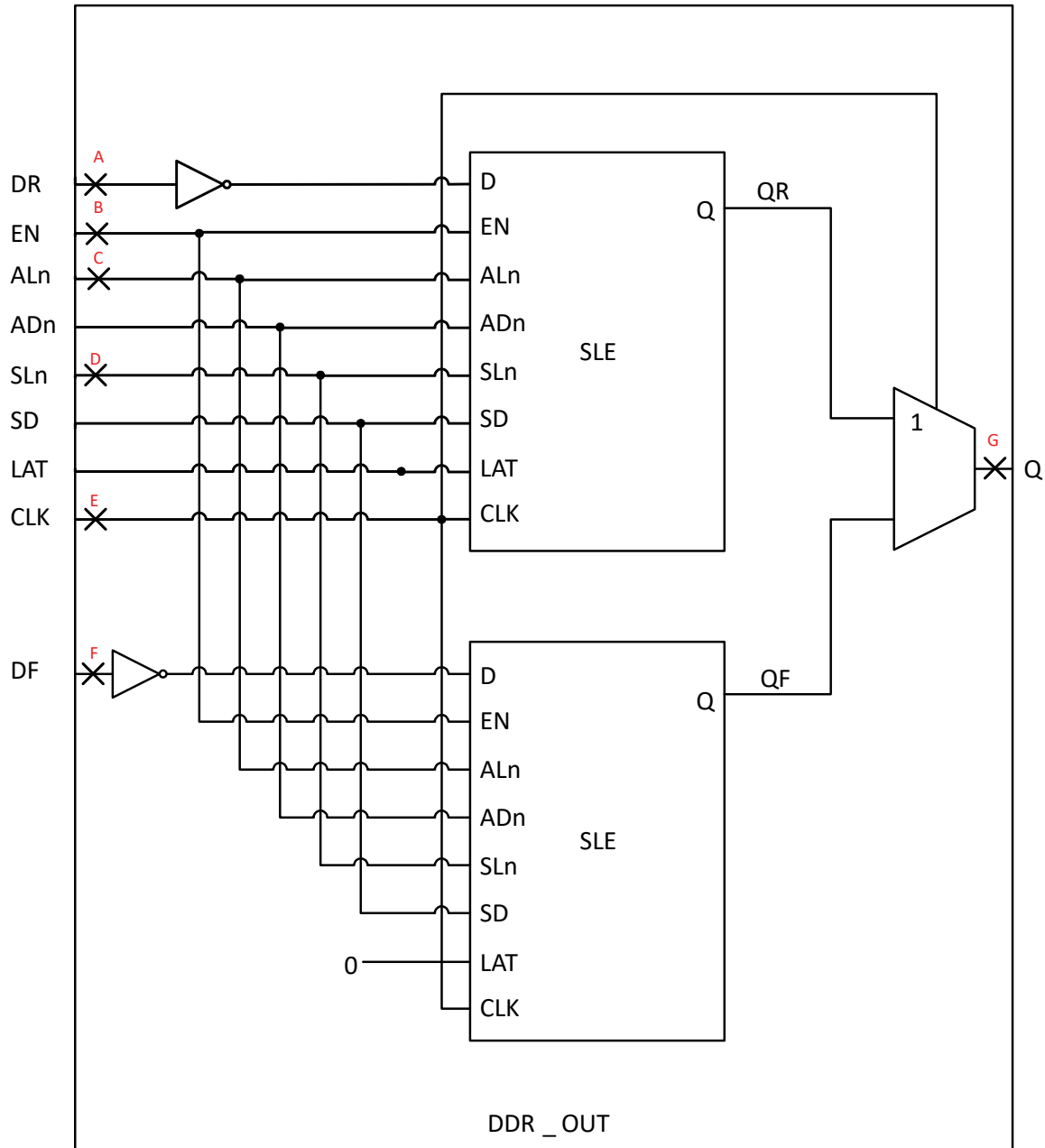
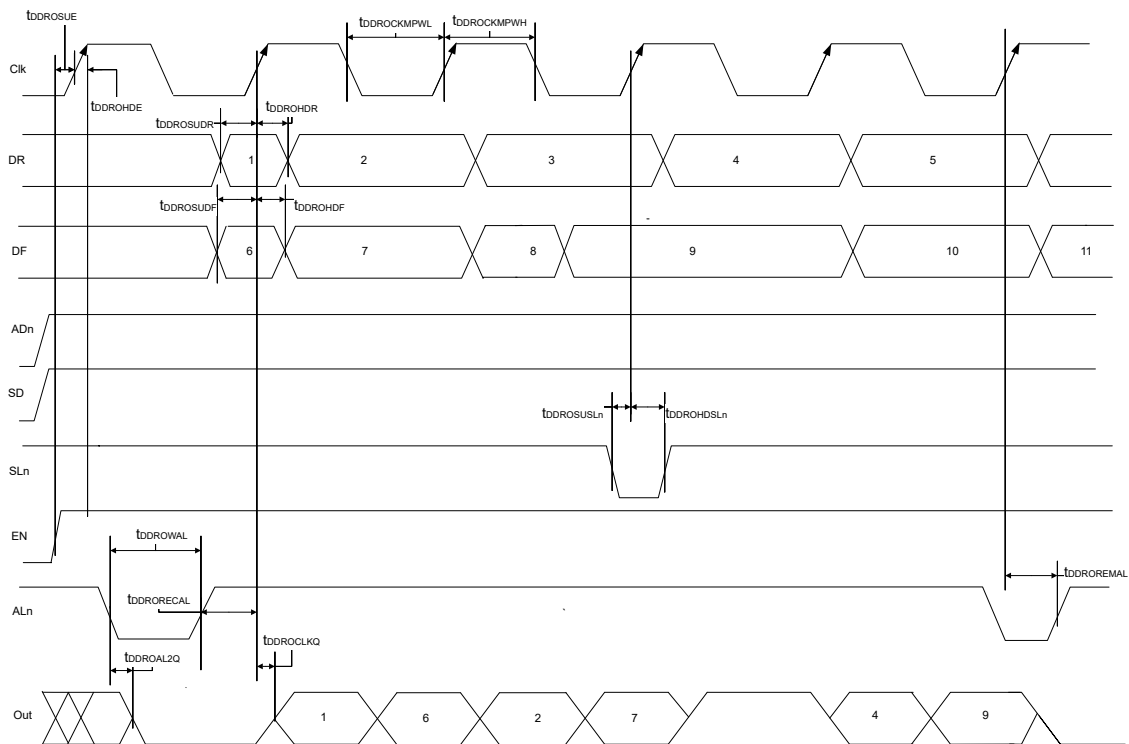


Figure 5-11. Output DDR Timing Diagram



5.10.5 Timing Characteristics [\(Ask a Question\)](#)

Table 5-96. Output DDR Propagation Delays—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Measuring Nodes (from, to) | Speed Grade -1 | Units |
|------------------|--|-------------------------------|----------------|-------|
| $t_{DDROCKQ}$ | Clock-to-Out of DDR for Output DDR | E,G | 0.258 | ns |
| $t_{DDROSUDF}$ | DF Data Setup for Output DDR | F,E | 0.278 | ns |
| $t_{DDROSUDR}$ | DR Data Setup for Output DDR | A,E | 0.288 | ns |
| $t_{DDROHDF}$ | DF Data Hold for Output DDR | F,E | 0.088 | ns |
| $t_{DDROHDR}$ | DR Data Hold for Output DDR | A,E | 0.077 | ns |
| $t_{DDROSUE}$ | Enable Setup for Output DDR | B,E | 0.829 | ns |
| t_{DDROHE} | Enable Hold for Output DDR | B,E | 0.031 | ns |
| $t_{DDROSUSLn}$ | Synchronous Load Setup for Output DDR | D,E | 1.831 | ns |
| $t_{DDROHSLn}$ | Synchronous Load Hold for Output DDR | D,E | 0.042 | ns |
| $t_{DDROAL2Q}$ | Asynchronous Load-to-Out for Output DDR | C,G | 0.549 | ns |
| $t_{DDROREMA}$ | Asynchronous Load Removal time for Output DDR | C,E | 0.134 | ns |
| $t_{DDRORECAL}$ | Asynchronous Load Recovery time for Output DDR | C,E | 0.238 | ns |
| $t_{DDROWAL}$ | Asynchronous Load Minimum Pulse Width for Output DDR | C,C | 0.377 | ns |
| $t_{DDROCKMPWH}$ | Clock Minimum Pulse Width High for the Output DDR | E,E | 0.101 | ns |

.....continued

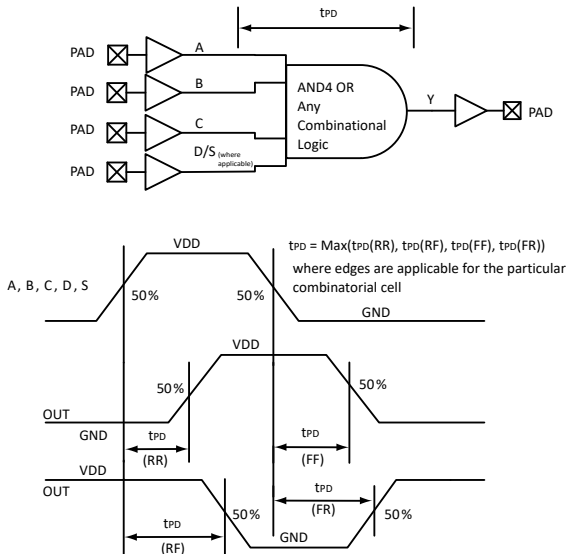
| Parameter | Description | Measuring Nodes (from, to) | Speed Grade -1 | Units |
|------------------|---|-------------------------------|----------------|-------|
| $t_{DDROCKMPWL}$ | Clock Minimum Pulse Width Low for the Output DDR | E,E | 0.223 | ns |

6. Logic Element Specifications [\(Ask a Question\)](#)

6.1 4-input LUT (LUT-4) [\(Ask a Question\)](#)

The IGLOO 2 and SmartFusion 2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the [SmartFusion2 and IGLOO2 Macro Library Guide](#).

Figure 6-1. LUT-4



6.1.1 Timing Characteristics [\(Ask a Question\)](#)

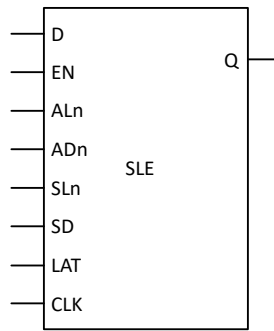
Table 6-1. Combinatorial Cell Propagation Delays—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Combinatorial Cell | Equation | Parameter | Speed Grade -1 | Units |
|--------------------|---------------------------------|-----------|----------------|-------|
| INV | $Y = !A$ | t_{PD} | 0.104 | ns |
| AND2 | $Y = A \cdot B$ | t_{PD} | 0.17 | ns |
| NAND2 | $Y = !(A \cdot B)$ | t_{PD} | 0.152 | ns |
| OR2 | $Y = A + B$ | t_{PD} | 0.17 | ns |
| NOR2 | $Y = !(A + B)$ | t_{PD} | 0.152 | ns |
| XOR2 | $Y = A \oplus B$ | t_{PD} | 0.17 | ns |
| XOR3 | $Y = A \oplus B \oplus C$ | t_{PD} | 0.233 | ns |
| AND3 | $Y = A \cdot B \cdot C$ | t_{PD} | 0.217 | ns |
| AND4 | $Y = A \cdot B \cdot C \cdot D$ | t_{PD} | 0.298 | ns |

6.2 Sequential Module [\(Ask a Question\)](#)

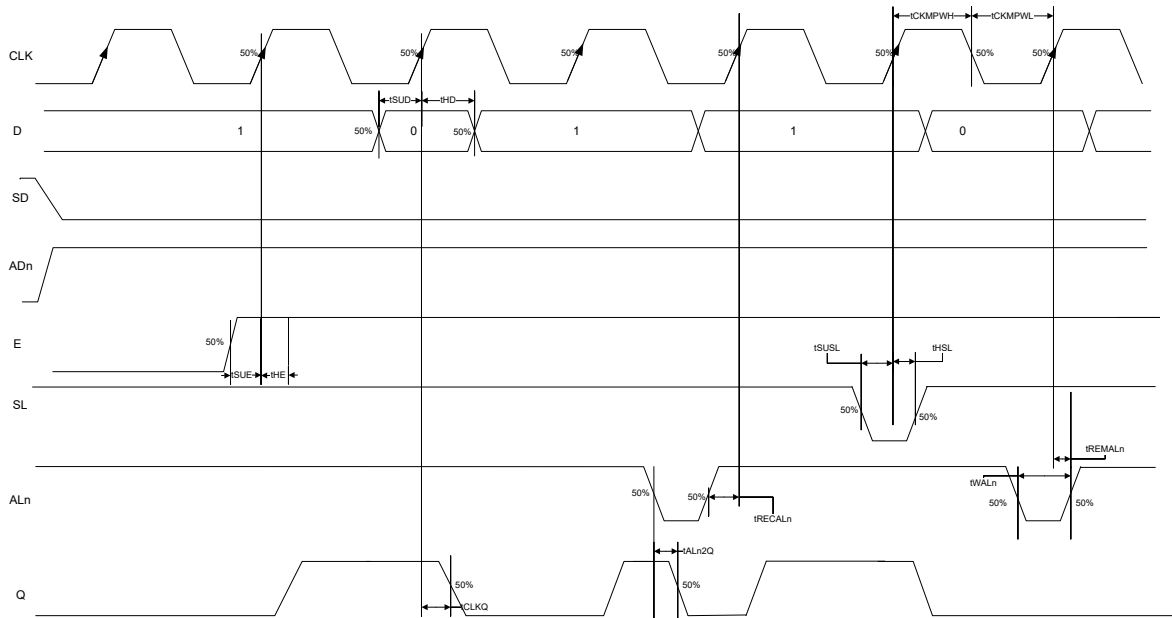
IGLOO 2 and SmartFusion 2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

Figure 6-2. Sequential Module



The following figure shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

Figure 6-3. Sequential Module Timing Diagram



6.2.1 Timing Characteristics [\(Ask a Question\)](#)

Table 6-2. Register Delays—Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | Units |
|-----------|---|----------------|-------|
| tCLKQ | Clock-to-Q of the Core Register | 0.114 | ns |
| tSUD | Data Setup Time for the Core Register | 0.262 | ns |
| tHD | Data Hold Time for the Core Register | 0 | ns |
| tSUE | Enable Setup Time for the Core Register | 0.318 | ns |
| tHE | Enable Hold Time for the Core Register | 0 | ns |
| tSUSL | Synchronous Load Setup Time for the Core Register | 0.565 | ns |
| tHSL | Synchronous Load Hold Time for the Core Register | 0 | ns |

.....continued

| Parameter | Description | Speed Grade -1 | Units |
|-----------|---|----------------|-------|
| tALn2Q | Asynchronous Clear-to-Q of the Core Register (ADn=1) | 0.495 | ns |
| | Asynchronous Preset-to-Q of the Core Register (ADn=0) | 0.47 | ns |
| tREMAIn | Asynchronous Load Removal Time for the Core Register | 0 | ns |
| tRECAIn | Asynchronous Load Recovery Time for the Core Register | 0.366 | ns |
| tWALn | Asynchronous Load Minimum Pulse Width for the Core Register | 0.266 | ns |
| tCKMPWH | Clock Minimum Pulse Width High for the Core Register | 0.065 | ns |
| tCKMPWL | Clock Minimum Pulse Width Low for the Core Register | 0.139 | ns |

7. Global Resource Characteristics (Ask a Question)

The IGLOO 2 and SmartFusion 2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. Refer to the [UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide](#) for the positions of various global routing resources.

Table 7-1. M2S150T Device Global Resource—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|-----------------------------------|----------------|-------|-------|
| | | Min | Max | |
| tRCKL | Input Low Delay for Global Clock | 0.788 | 0.868 | ns |
| tRCKH | Input High Delay for Global Clock | 1.46 | 1.594 | ns |
| tRCKSW | Maximum Skew for Global Clock | — | 0.134 | ns |

Table 7-2. M2S090T Device Global Resource —Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|-----------------------------------|----------------|-------|-------|
| | | Min | Max | |
| tRCKL | Input Low Delay for Global Clock | 0.793 | 0.847 | ns |
| tRCKH | Input High Delay for Global Clock | 1.412 | 1.498 | ns |
| tRCKSW | Maximum Skew for Global Clock | — | 0.086 | ns |

Table 7-3. M2S050T Device Global Resource—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|-----------------------------------|----------------|-------|-------|
| | | Min | Max | |
| tRCKL | Input Low Delay for Global Clock | 0.793 | 0.861 | ns |
| tRCKH | Input High Delay for Global Clock | 1.436 | 1.55 | ns |
| tRCKSW | Maximum Skew for Global Clock | — | 0.114 | ns |

Table 7-4. M2S025T Device Global Resource—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|-----------------------------------|----------------|-------|-------|
| | | Min | Max | |
| tRCKL | Input Low Delay for Global Clock | 0.713 | 0.762 | ns |
| tRCKH | Input High Delay for Global Clock | 1.306 | 1.391 | ns |
| tRCKSW | Maximum Skew for Global Clock | — | 0.085 | ns |

Table 7-5. M2S010T Device Global Resource—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|-----------------------------------|----------------|-------|-------|
| | | Min | Max | |
| tRCKL | Input Low Delay for Global Clock | 0.598 | 0.639 | ns |
| tRCKH | Input High Delay for Global Clock | 1.116 | 1.192 | ns |
| tRCKSW | Maximum Skew for Global Clock | — | 0.076 | ns |

8. FPGA Fabric SRAM [\(Ask a Question\)](#)

Refer to the [UG0445: IGL00 2 FPGA and SmartFusion 2 SoC FPGA Fabric User Guide](#) for more information.

8.1 FPGA Fabric Large SRAM (LSRAM) [\(Ask a Question\)](#)

Table 8-1. RAM1K18—Dual-Port Mode for Depth × Width Configuration 1Kx18—Worst-Case Military Conditions: T_j = 125 °C, VDD = 1.14V

| Parameter | Description | Speed Grade -1 | | Units |
|--------------------------------|---|----------------|-------|-------|
| | | Min | Max | |
| t _{cy} | Clock Period | 3.333 | — | ns |
| t _{clkmpwh} | Clock Minimum Pulse Width High | 1.5 | — | ns |
| t _{clkmpwl} | Clock Minimum pulse Width Low | 1.5 | — | ns |
| t _{plcy} | Pipelined Clock Period | 3.333 | — | ns |
| t _{plclkmpwh} | Pipelined Clock Minimum Pulse Width High | 1.5 | — | ns |
| t _{plclkmpwl} | Pipelined Clock Minimum pulse Width Low | 1.5 | — | ns |
| t _{clk2q} | Read Access Time with Pipeline Register | — | 0.346 | ns |
| | Read Access Time without Pipeline Register | — | 2.346 | ns |
| | Access Time with Feed-Through Write Timing | — | 2.346 | ns |
| t _{addr_{su}} | Address Setup Time | 0.455 | — | ns |
| t _{addr_{hd}} | Address Hold Time | 0.282 | — | ns |
| t _{dsu} | Data Setup Time | 0.352 | — | ns |
| t _{dhd} | Data Hold Time | 0.11 | — | ns |
| t _{blksu} | Block Select Setup Time | 0.214 | — | ns |
| t _{blkhd} | Block Select Hold Time | 0.223 | — | ns |
| t _{blk2q} | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 1.578 | ns |
| t _{blkmpw} | Block Select Minimum Pulse Width | 0.218 | — | ns |
| t _{rdesu} | Read Enable Setup Time | 0.463 | — | ns |
| t _{rdehd} | Read Enable Hold Time | 0.173 | — | ns |
| t _{rdplesu} | Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN) | 0.256 | — | ns |
| t _{rdplehd} | Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN) | 0.106 | — | ns |
| t _{r2q} | Asynchronous Reset to Output Propagation Delay | — | 1.561 | ns |
| t _{rstrem} | Asynchronous Reset Removal Time | 0.522 | — | ns |
| t _{rstrec} | Asynchronous Reset Recovery Time | 0.005 | — | ns |
| t _{rstmpw} | Asynchronous Reset Minimum Pulse Width | 0.352 | — | ns |
| t _{plrstrem} | Pipelined Register Asynchronous Reset Removal Time | -0.288 | — | ns |
| t _{plrstrec} | Pipelined Register Asynchronous Reset Recovery Time | 0.338 | — | ns |
| t _{plrstmpw} | Pipelined Register Asynchronous Reset Minimum Pulse Width | 0.33 | — | ns |
| t _{srtsu} | Synchronous Reset Setup Time | 0.233 | — | ns |
| t _{srsth} | Synchronous Reset Hold Time | 0.037 | — | ns |
| t _{wesu} | Write Enable Setup Time | 0.402 | — | ns |
| t _{wehd} | Write Enable Hold Time | 0.25 | — | ns |
| f _{max} | Maximum Frequency | — | 300 | MHz |

Table 8-2. RAM1K18—Dual-Port Mode for Depth × Width Configuration 2Kx9 — Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|------------|---|----------------|-------|-------|
| | | Min | Max | |
| tcy | Clock Period | 3.333 | — | ns |
| tclkmpwh | Clock Minimum Pulse Width High | 1.5 | — | ns |
| tclkmpwl | Clock Minimum pulse Width Low | 1.5 | — | ns |
| tplcy | Pipelined Clock Period | 3.333 | — | ns |
| tplclkmpwh | Pipelined Clock Minimum Pulse Width High | 1.5 | — | ns |
| tplclkmpwl | Pipelined Clock Minimum pulse Width Low | 1.5 | — | ns |
| tclk2q | Read Access Time with Pipeline Register | — | 0.346 | ns |
| | Read Access Time without Pipeline Register | — | 2.346 | ns |
| | Access Time with Feed-Through Write Timing | — | 2.346 | ns |
| taddrsu | Address Setup Time | 0.49 | — | ns |
| taddrhd | Address Hold Time | 0.282 | — | ns |
| tdsu | Data Setup Time | 0.346 | — | ns |
| tdhd | Data Hold Time | 0.084 | — | ns |
| tblkstu | Block Select Setup Time | 0.214 | — | ns |
| tblkhd | Block Select Hold Time | 0.223 | — | ns |
| tblk2q | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 1.578 | ns |
| tblkmpw | Block Select Minimum Pulse Width | 0.218 | — | ns |
| trdesu | Read Enable Setup Time | 0.5 | — | ns |
| trdehd | Read Enable Hold Time | 0.073 | — | ns |
| trdplestu | Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN) | 0.256 | — | ns |
| trdplehd | Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN) | 0.106 | — | ns |
| tr2q | Asynchronous Reset to Output Propagation Delay | — | 1.569 | ns |
| trstrem | Asynchronous Reset Removal Time | 0.522 | — | ns |
| trstrec | Asynchronous Reset Recovery Time | 0.005 | — | ns |
| trstmpw | Asynchronous Reset Minimum Pulse Width | 0.352 | — | ns |
| tplrstrem | Pipelined Register Asynchronous Reset Removal Time | -0.288 | — | ns |
| tplrstrec | Pipelined Register Asynchronous Reset Recovery Time | 0.338 | — | ns |
| tplrstmpw | Pipelined Register Asynchronous Reset Minimum Pulse Width | 0.33 | — | ns |
| tsrstsu | Synchronous Reset Setup Time | 0.233 | — | ns |
| tsrsthd | Synchronous Reset Hold Time | 0.037 | — | ns |
| twesu | Write Enable Setup Time | 0.428 | — | ns |
| twehd | Write Enable Hold Time | 0.05 | — | ns |
| Fmax | Maximum Frequency | — | 300 | MHz |

Table 8-3. RAM1K18—Dual-Port Mode for Depth × Width Configuration 4Kx4—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|------------|--|----------------|-----|-------|
| | | Min | Max | |
| tcy | Clock Period | 3.333 | — | ns |
| tclkmpwh | Clock Minimum Pulse Width High | 1.5 | — | ns |
| tclkmpwl | Clock Minimum pulse Width Low | 1.5 | — | ns |
| tplcy | Pipelined Clock Period | 3.333 | — | ns |
| tplclkmpwh | Pipelined Clock Minimum Pulse Width High | 1.5 | — | ns |

.....continued

| Parameter | Description | Speed Grade -1 | | |
|------------|---|----------------|-------|-------|
| | | Min | Max | Units |
| tplclkmpwl | Pipelined Clock Minimum pulse Width Low | 1.5 | — | ns |
| tclk2q | Read Access Time with Pipeline Register | — | 0.334 | ns |
| | Read Access Time without Pipeline Register | — | 2.346 | ns |
| | Access Time with Feed-Through Write Timing | — | 2.346 | ns |
| taddrsu | Address Setup Time | 0.56 | — | ns |
| taddrhd | Address Hold Time | 0.282 | — | ns |
| tdsu | Data Setup Time | 0.345 | — | ns |
| tdhd | Data Hold Time | 0.084 | — | ns |
| tblkstu | Block Select Setup Time | 0.214 | — | ns |
| tblkhd | Block Select Hold Time | 0.223 | — | ns |
| tblk2q | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 1.56 | ns |
| tblkmpw | Block Select Minimum Pulse Width | 0.218 | — | ns |
| trdesu | Read Enable Setup Time | 0.532 | — | ns |
| trdehd | Read Enable Hold Time | 0.073 | — | ns |
| trdplesu | Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN) | 0.256 | — | ns |
| trdpleshd | Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN) | 0.106 | — | ns |
| tr2q | Asynchronous Reset to Output Propagation Delay | — | 1.562 | ns |
| trstrem | Asynchronous Reset Removal Time | 0.522 | — | ns |
| trstrec | Asynchronous Reset Recovery Time | 0.005 | — | ns |
| trstmpw | Asynchronous Reset Minimum Pulse Width | 0.352 | — | ns |
| tplrstrem | Pipelined Register Asynchronous Reset Removal Time | -0.288 | — | ns |
| tplrstrec | Pipelined Register Asynchronous Reset Recovery Time | 0.338 | — | ns |
| tplrstmpw | Pipelined Register Asynchronous Reset Minimum Pulse Width | 0.33 | — | ns |
| tsrstsu | Synchronous Reset Setup Time | 0.233 | — | ns |
| tsrsthd | Synchronous Reset Hold Time | 0.037 | — | ns |
| twesu | Write Enable Setup Time | 0.473 | — | ns |
| twehd | Write Enable Hold Time | 0.05 | — | ns |
| Fmax | Maximum Frequency | — | 300 | MHz |

Table 8-4. RAM1K18—Dual-Port Mode for Depth × Width Configuration 8Kx2—Worst-Case Military Conditions: T_j = 125 °C, VDD = 1.14V

| Parameter | Description | Speed Grade -1 | | Units |
|------------|--|----------------|-------|-------|
| | | Min | Max | |
| tcy | Clock Period | 3.333 | — | ns |
| tclkmpwh | Clock Minimum Pulse Width High | 1.5 | — | ns |
| tclkmpwl | Clock Minimum pulse Width Low | 1.5 | — | ns |
| tplcy | Pipelined Clock Period | 3.333 | — | ns |
| tplclkmpwh | Pipelined Clock Minimum Pulse Width High | 1.5 | — | ns |
| tplclkmpwl | Pipelined Clock Minimum pulse Width Low | 1.5 | — | ns |
| tclk2q | Read Access Time with Pipeline Register | — | 0.332 | ns |
| | Read Access Time without Pipeline Register | — | 2.346 | ns |
| | Access Time with Feed-Through Write Timing | — | 2.346 | ns |
| taddrsu | Address Setup Time | 0.631 | — | ns |
| taddrhd | Address Hold Time | 0.282 | — | ns |

.....continued

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|---|----------------|-------|-------|
| | | Min | Max | |
| tdsu | Data Setup Time | 0.34 | — | ns |
| tdhd | Data Hold Time | 0.084 | — | ns |
| tblksu | Block Select Setup Time | 0.214 | — | ns |
| tblkhd | Block Select Hold Time | 0.223 | — | ns |
| tblk2q | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 1.56 | ns |
| tblkmpw | Block Select Minimum Pulse Width | 0.218 | — | ns |
| trdesu | Read Enable Setup Time | 0.546 | — | ns |
| trdehd | Read Enable Hold Time | 0.073 | — | ns |
| trdple su | Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN) | 0.256 | — | ns |
| trdplehd | Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN) | 0.106 | — | ns |
| tr2q | Asynchronous Reset to Output Propagation Delay | — | 1.583 | ns |
| trstrem | Asynchronous Reset Removal Time | 0.522 | — | ns |
| trstrec | Asynchronous Reset Recovery Time | 0.005 | — | ns |
| trstmpw | Asynchronous Reset Minimum Pulse Width | 0.352 | — | ns |
| tplrstrem | Pipelined Register Asynchronous Reset Removal Time | -0.288 | — | ns |
| tplrstrec | Pipelined Register Asynchronous Reset Recovery Time | 0.338 | — | ns |
| tplrstmpw | Pipelined Register Asynchronous Reset Minimum Pulse Width | 0.33 | — | ns |
| tsrstsu | Synchronous Reset Setup Time | 0.233 | — | ns |
| tsrsthd | Synchronous Reset Hold Time | 0.037 | — | ns |
| twesu | Write Enable Setup Time | 0.504 | — | ns |
| twehd | Write Enable Hold Time | 0.05 | — | ns |
| Fmax | Maximum Frequency | — | 300 | MHz |

Table 8-5. RAM1K18—Dual-Port Mode for Depth × Width Configuration 16Kx1—Worst-Case Military Conditions: T_j = 125 °C, VDD = 1.14V

| Parameter | Description | Speed Grade -1 | | Units |
|------------|---|----------------|-------|-------|
| | | Min | Max | |
| tcy | Clock Period | 3.333 | — | ns |
| tclkmpwh | Clock Minimum Pulse Width High | 1.5 | — | ns |
| tclkmpwl | Clock Minimum pulse Width Low | 1.5 | — | ns |
| tplcy | Pipelined Clock Period | 3.333 | — | ns |
| tplclkmpwh | Pipelined Clock Minimum Pulse Width High | 1.5 | — | ns |
| tplclkmpwl | Pipelined Clock Minimum pulse Width Low | 1.5 | — | ns |
| tclk2q | Read Access Time with Pipeline Register | — | 0.332 | ns |
| | Read Access Time without Pipeline Register | — | 2.342 | ns |
| | Access Time with Feed-Through Write Timing | — | 2.342 | ns |
| taddr su | Address Setup Time | 0.646 | — | ns |
| taddrhd | Address Hold Time | 0.282 | — | ns |
| tdsu | Data Setup Time | 0.332 | — | ns |
| tdhd | Data Hold Time | 0.084 | — | ns |
| tblksu | Block Select Setup Time | 0.214 | — | ns |
| tblkhd | Block Select Hold Time | 0.223 | — | ns |
| tblk2q | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 1.559 | ns |
| tblkmpw | Block Select Minimum Pulse Width | 0.218 | — | ns |

.....continued

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|---|----------------|-------|-------|
| | | Min | Max | |
| trdesu | Read Enable Setup Time | 0.547 | — | ns |
| trdehd | Read Enable Hold Time | 0.073 | — | ns |
| trdpleSU | Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN) | 0.256 | — | ns |
| trdplehd | Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN) | 0.106 | — | ns |
| tr2q | Asynchronous Reset to Output Propagation Delay | — | 1.603 | ns |
| trstrem | Asynchronous Reset Removal Time | 0.522 | — | ns |
| trstrec | Asynchronous Reset Recovery Time | 0.005 | — | ns |
| trstmpw | Asynchronous Reset Minimum Pulse Width | 0.352 | — | ns |
| tplrstrem | Pipelined Register Asynchronous Reset Removal Time | -0.288 | — | ns |
| tplrstrec | Pipelined Register Asynchronous Reset Recovery Time | 0.338 | — | ns |
| tplrstmpw | Pipelined Register Asynchronous Reset Minimum Pulse Width | 0.33 | — | ns |
| tsrstSU | Synchronous Reset Setup Time | 0.233 | — | ns |
| tsrsthd | Synchronous Reset Hold Time | 0.037 | — | ns |
| twesu | Write Enable Setup Time | 0.468 | — | ns |
| twehd | Write Enable Hold Time | 0.05 | — | ns |
| Fmax | Maximum Frequency | — | 300 | MHz |

Table 8-6. RAM1K18—Two-Port Mode for Depth × Width Configuration 512x36—Worst-Case Military Conditions: T_J = 125 °C, VDD = 1.14V

| Parameter | Description | Speed Grade -1 | | Units |
|------------|---|----------------|-------|-------|
| | | Min | Max | |
| tcy | Clock Period | 3.333 | — | ns |
| tclkmpwh | Clock Minimum Pulse Width High | 1.5 | — | ns |
| tclkmpwl | Clock Minimum pulse Width Low | 1.5 | — | ns |
| tplcy | Pipelined Clock Period | 3.333 | — | ns |
| tplclkmpwh | Pipelined Clock Minimum Pulse Width High | 1.5 | — | ns |
| tplclkmpwl | Pipelined Clock Minimum pulse Width Low | 1.5 | — | ns |
| tclk2q | Read Access Time with Pipeline Register | — | 0.346 | ns |
| | Read Access Time without Pipeline Register | — | 2.322 | ns |
| taddrSU | Address Setup Time | 0.323 | — | ns |
| taddrhd | Address Hold Time | 0.282 | — | ns |
| tdSU | Data Setup Time | 0.348 | — | ns |
| tdhd | Data Hold Time | 0.114 | — | ns |
| tblkSU | Block Select Setup Time | 0.214 | — | ns |
| tblkhd | Block Select Hold Time | 0.208 | — | ns |
| tblk2q | Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 2.322 | ns |
| tblkmpw | Block Select Minimum Pulse Width | 0.218 | — | ns |
| trdesu | Read Enable Setup Time | 0.463 | — | ns |
| trdehd | Read Enable Hold Time | 0.173 | — | ns |
| trdpleSU | Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN) | 0.256 | — | ns |
| trdplehd | Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN) | 0.106 | — | ns |
| tr2q | Asynchronous Reset to Output Propagation Delay | — | 1.561 | ns |
| trstrem | Asynchronous Reset Removal Time | 0.522 | — | ns |
| trstrec | Asynchronous Reset Recovery Time | 0.005 | — | ns |

.....continued

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|---|----------------|-----|-------|
| | | Min | Max | |
| trstmpw | Asynchronous Reset Minimum Pulse Width | 0.352 | — | ns |
| tplrstrem | Pipelined Register Asynchronous Reset Removal Time | -0.288 | — | ns |
| tplrstrec | Pipelined Register Asynchronous Reset Recovery Time | 0.338 | — | ns |
| tplrstmpw | Pipelined Register Asynchronous Reset Minimum Pulse Width | 0.33 | — | ns |
| tsrststu | Synchronous Reset Setup Time | 0.233 | — | ns |
| tsrsthd | Synchronous Reset Hold Time | 0.037 | — | ns |
| twesu | Write Enable Setup Time | 0.402 | — | ns |
| twehd | Write Enable Hold Time | 0.25 | — | ns |
| Fmax | Maximum Frequency | — | 300 | MHz |

8.2 FPGA Fabric Micro SRAM (μ SRAM) [\(Ask a Question\)](#)

Table 8-7. μ SRAM (RAM64x18) in 64x18 Mode—Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|------------|---|----------------|-------|-------|
| | | Min | Max | |
| tcy | Read Clock Period | 4 | — | ns |
| tclkmpwh | Read Clock Minimum Pulse Width High | 1.8 | — | ns |
| tclkmpwl | Read Clock Minimum pulse Width Low | 1.8 | — | ns |
| tplcy | Read Pipe-line clock period | 4 | — | ns |
| tplclkmpwh | Read Pipe-line clock Minimum Pulse Width High | 1.8 | — | ns |
| tplclkmpwl | Read Pipe-line clock Minimum Pulse Width Low | 1.8 | — | ns |
| tclk2q | Read Access Time with Pipeline Register | — | 0.276 | ns |
| | Read Access Time without Pipeline Register | — | 1.738 | ns |
| taddrsu | Read Address Setup Time in Synchronous Mode | 0.311 | — | ns |
| | Read Address Setup Time in Asynchronous Mode | 1.916 | — | ns |
| taddrhd | Read Address Hold Time in Synchronous Mode | 0.094 | — | ns |
| | Read Address Hold Time in Asynchronous Mode | -0.803 | — | ns |
| trdensu | Read Enable Setup Time | 0.287 | — | ns |
| trdenhd | Read Enable Hold Time | 0.059 | — | ns |
| tblkstu | Read Block Select Setup Time | 1.898 | — | ns |
| tblkhd | Read Block Select Hold Time | -0.671 | — | ns |
| tblk2q | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 2.102 | ns |
| trstrem | Read Asynchronous Reset Removal Time (Pipelined Clock) | -0.15 | — | ns |
| | Read Asynchronous Reset Removal Time (Non-Pipelined Clock) | 0.047 | — | ns |
| trstrec | Read Asynchronous Reset Recovery Time (Pipelined Clock) | 0.524 | — | ns |
| | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock) | 0.244 | — | ns |
| tr2q | Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled) | — | 0.869 | ns |
| tsrststu | Read Synchronous Reset Setup Time | 0.279 | — | ns |
| tsrsthd | Read Synchronous Reset Hold Time | 0.062 | — | ns |
| tccy | Write Clock Period | 4 | — | ns |
| tcclkmpwh | Write Clock Minimum Pulse Width High | 1.8 | — | ns |
| tcclkmpwl | Write Clock Minimum Pulse Width Low | 1.8 | — | ns |
| tblkcsu | Write Block Setup Time | 0.417 | — | ns |

.....continued

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|-----------------------------|----------------|-----|-------|
| | | Min | Max | |
| tblkchd | Write Block Hold Time | 0.007 | — | ns |
| tdincsu | Write Input Data setup Time | 0.119 | — | ns |
| tdinchd | Write Input Data hold Time | 0.155 | — | ns |
| taddrclu | Write Address Setup Time | 0.091 | — | ns |
| taddrchd | Write Address Hold Time | 0.132 | — | ns |
| twecsu | Write Enable Setup Time | 0.41 | — | ns |
| twechd | Write Enable Hold Time | -0.027 | — | ns |
| fmax | Maximum Frequency | — | 250 | MHz |

Table 8-8. μ SRAM (RAM64x16) in 64x16 Mode—Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|------------|---|----------------|-------|-------|
| | | Min | Max | |
| tcy | Read Clock Period | 4 | — | ns |
| tclkmpwh | Read Clock Minimum Pulse Width High | 1.8 | — | ns |
| tclkmpwl | Read Clock Minimum pulse Width Low | 1.8 | — | ns |
| tplcy | Read Pipe-line clock period | 4 | — | ns |
| tplclkmpwh | Read Pipe-line clock Minimum Pulse Width High | 1.8 | — | ns |
| tplclkmpwl | Read Pipe-line clock Minimum Pulse Width Low | 1.8 | — | ns |
| tclk2q | Read Access Time with Pipeline Register | — | 0.276 | ns |
| | Read Access Time without Pipeline Register | — | 1.738 | ns |
| taddrclu | Read Address Setup Time in Synchronous Mode | 0.311 | — | ns |
| | Read Address Setup Time in Asynchronous Mode | 1.916 | — | ns |
| taddrhd | Read Address Hold Time in Synchronous Mode | 0.094 | — | ns |
| | Read Address Hold Time in Asynchronous Mode | -0.803 | — | ns |
| trdensu | Read Enable Setup Time | 0.287 | — | ns |
| trdenhd | Read Enable Hold Time | 0.059 | — | ns |
| tblkclu | Read Block Select Setup Time | 1.898 | — | ns |
| tblkhd | Read Block Select Hold Time | -0.671 | — | ns |
| tclk2q | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 2.102 | ns |
| | | | | |
| trstrem | Read Asynchronous Reset Removal Time (Pipelined Clock) | -0.15 | — | ns |
| | Read Asynchronous Reset Removal Time (Non-Pipelined Clock) | 0.047 | — | ns |
| trstrec | Read Asynchronous Reset Recovery Time (Pipelined Clock) | 0.524 | — | ns |
| | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock) | 0.244 | — | ns |
| tr2q | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | — | 0.866 | ns |
| tsrstu | Read Synchronous Reset Setup Time | 0.279 | — | ns |
| tsrsth | Read Synchronous Reset Hold Time | 0.062 | — | ns |
| tccy | Write Clock Period | 4 | — | ns |
| tcclkmpwh | Write Clock Minimum Pulse Width High | 1.8 | — | ns |
| tcclkmpwl | Write Clock Minimum Pulse Width Low | 1.8 | — | ns |
| tblkclu | Write Block Setup Time | 0.417 | — | ns |
| tblkchd | Write Block Hold Time | 0.007 | — | ns |
| tdincsu | Write Input Data setup Time | 0.119 | — | ns |
| tdinchd | Write Input Data hold Time | 0.155 | — | ns |

.....continued

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|--------------------------|----------------|-----|-------|
| | | Min | Max | |
| taddrcsu | Write Address Setup Time | 0.091 | — | ns |
| taddrchd | Write Address Hold Time | 0.132 | — | ns |
| twecsu | Write Enable Setup Time | 0.41 | — | ns |
| twechd | Write Enable Hold Time | -0.027 | — | ns |
| fmax | Maximum Frequency | — | 250 | MHz |

Table 8-9. μ SRAM (RAM128x9) in 128x9 Mode—Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|------------|---|----------------|-------|-------|
| | | Min | Max | |
| tcy | Read Clock Period | 4 | — | ns |
| tclcmpwh | Read Clock Minimum Pulse Width High | 1.8 | — | ns |
| tclcmpwl | Read Clock Minimum pulse Width Low | 1.8 | — | ns |
| tplcy | Read Pipe-line clock period | 4 | — | ns |
| tplclcmpwh | Read Pipe-line clock Minimum Pulse Width High | 1.8 | — | ns |
| tplclcmpwl | Read Pipe-line clock Minimum Pulse Width Low | 1.8 | — | ns |
| tclk2q | Read Access Time with Pipeline Register | — | 0.276 | ns |
| | Read Access Time without Pipeline Register | — | 1.776 | ns |
| taddrsu | Read Address Setup Time in Synchronous Mode | 0.311 | — | ns |
| | Read Address Setup Time in Asynchronous Mode | 1.959 | — | ns |
| taddrhd | Read Address Hold Time in Synchronous Mode | 0.125 | — | ns |
| | Read Address Hold Time in Asynchronous Mode | -0.704 | — | ns |
| trdensu | Read Enable Setup Time | 0.287 | — | ns |
| trdenhd | Read Enable Hold Time | 0.059 | — | ns |
| tblksu | Read Block Select Setup Time | 1.898 | — | ns |
| tblkhd | Read Block Select Hold Time | -0.671 | — | ns |
| tblk2q | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 2.14 | ns |
| trstrem | Read Asynchronous Reset Removal Time (Pipelined Clock) | -0.15 | — | ns |
| | Read Asynchronous Reset Removal Time (Non-Pipelined Clock) | 0.047 | — | ns |
| trstrec | Read Asynchronous Reset Recovery Time (Pipelined Clock) | 0.524 | — | ns |
| | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock) | 0.244 | — | ns |
| tr2q | Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled) | — | 0.865 | ns |
| tsrstsu | Read Synchronous Reset Setup Time | 0.279 | — | ns |
| tsrsthd | Read Synchronous Reset Hold Time | 0.062 | — | ns |
| tccy | Write Clock Period | 4 | — | ns |
| tcclcmpwh | Write Clock Minimum Pulse Width High | 1.8 | — | ns |
| tcclcmpwl | Write Clock Minimum Pulse Width Low | 1.8 | — | ns |
| tblkcsu | Write Block Setup Time | 0.417 | — | ns |
| tblkchd | Write Block Hold Time | 0.007 | — | ns |
| tdincsu | Write Input Data setup Time | 0.104 | — | ns |
| tdinchd | Write Input Data hold Time | 0.142 | — | ns |
| taddrcsu | Write Address Setup Time | 0.091 | — | ns |
| taddrchd | Write Address Hold Time | 0.24 | — | ns |
| twecsu | Write Enable Setup Time | 0.41 | — | ns |

.....continued

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|------------------------|----------------|-----|-------|
| | | Min | Max | |
| twechd | Write Enable Hold Time | -0.027 | — | ns |
| fmax | Maximum Frequency | — | 250 | MHz |

Table 8-10. μ SRAM (RAM128x8) in 128x8 Mode—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|------------|---|----------------|-------|-------|
| | | Min | Max | |
| tcy | Read Clock Period | 4 | — | ns |
| tclkmpwh | Read Clock Minimum Pulse Width High | 1.8 | — | ns |
| tclkmpwl | Read Clock Minimum pulse Width Low | 1.8 | — | ns |
| tplcy | Read Pipe-line clock period | 4 | — | ns |
| tplclkmpwh | Read Pipe-line clock Minimum Pulse Width High | 1.8 | — | ns |
| tplclkmpwl | Read Pipe-line clock Minimum Pulse Width Low | 1.8 | — | ns |
| tclk2q | Read Access Time with Pipeline Register | — | 0.276 | ns |
| | Read Access Time without Pipeline Register | — | 1.776 | ns |
| taddrsu | Read Address Setup Time in Synchronous Mode | 0.311 | — | ns |
| | Read Address Setup Time in Asynchronous Mode | 1.959 | — | ns |
| taddrhd | Read Address Hold Time in Synchronous Mode | 0.125 | — | ns |
| | Read Address Hold Time in Asynchronous Mode | -0.704 | — | ns |
| trdensu | Read Enable Setup Time | 0.287 | — | ns |
| trdenhd | Read Enable Hold Time | 0.059 | — | ns |
| tblkcu | Read Block Select Setup Time | 1.898 | — | ns |
| tblkhd | Read Block Select Hold Time | -0.671 | — | ns |
| tblk2q | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 2.14 | ns |
| trstrem | Read Asynchronous Reset Removal Time (Pipelined Clock) | -0.15 | — | ns |
| | Read Asynchronous Reset Removal Time (Non-Pipelined Clock) | 0.047 | — | ns |
| trstrec | Read Asynchronous Reset Recovery Time (Pipelined Clock) | 0.524 | — | ns |
| | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock) | 0.244 | — | ns |
| tr2q | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | — | 0.865 | ns |
| tsrstcu | Read Synchronous Reset Setup Time | 0.279 | — | ns |
| tsrsthd | Read Synchronous Reset Hold Time | 0.062 | — | ns |
| tccy | Write Clock Period | 4 | — | ns |
| tcclkmpwh | Write Clock Minimum Pulse Width High | 1.8 | — | ns |
| tcclkmpwl | Write Clock Minimum Pulse Width Low | 1.8 | — | ns |
| tblkcsu | Write Block Setup Time | 0.417 | — | ns |
| tblkchd | Write Block Hold Time | 0.007 | — | ns |
| tdinccu | Write Input Data setup Time | 0.104 | — | ns |
| tdinchd | Write Input Data hold Time | 0.142 | — | ns |
| taddrccu | Write Address Setup Time | 0.091 | — | ns |
| taddrchd | Write Address Hold Time | 0.24 | — | ns |
| twccsu | Write Enable Setup Time | 0.41 | — | ns |
| twechd | Write Enable Hold Time | -0.027 | — | ns |
| fmax | Maximum Frequency | — | 250 | MHz |

Table 8-11. μ SRAM (RAM256x4) in 256x4 Mode—Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|------------|---|----------------|-------|-------|
| | | Min | Max | |
| tcy | Read Clock Period | 4 | — | ns |
| tclkmpwh | Read Clock Minimum Pulse Width High | 1.8 | — | ns |
| tclkmpwl | Read Clock Minimum pulse Width Low | 1.8 | — | ns |
| tplcy | Read Pipe-line clock period | 4 | — | ns |
| tplclkmpwh | Read Pipe-line clock Minimum Pulse Width High | 1.8 | — | ns |
| tplclkmpwl | Read Pipe-line clock Minimum Pulse Width Low | 1.8 | — | ns |
| tclk2q | Read Access Time with Pipeline Register | — | 0.276 | ns |
| | Read Access Time without Pipeline Register | — | 1.812 | ns |
| taddrsu | Read Address Setup Time in Synchronous Mode | 0.311 | — | ns |
| | Read Address Setup Time in Asynchronous Mode | 1.993 | — | ns |
| taddrhd | Read Address Hold Time in Synchronous Mode | 0.125 | — | ns |
| | Read Address Hold Time in Asynchronous Mode | -0.669 | — | ns |
| trdensu | Read Enable Setup Time | 0.287 | — | ns |
| trdenhd | Read Enable Hold Time | 0.059 | — | ns |
| tblksu | Read Block Select Setup Time | 1.898 | — | ns |
| tblkhd | Read Block Select Hold Time | -0.671 | — | ns |
| tblk2q | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 2.166 | ns |
| trstrem | Read Asynchronous Reset Removal Time (Pipelined Clock) | -0.15 | — | ns |
| | Read Asynchronous Reset Removal Time (Non-Pipelined Clock) | 0.047 | — | ns |
| trstrec | Read Asynchronous Reset Recovery Time (Pipelined Clock) | 0.524 | — | ns |
| | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock) | 0.244 | — | ns |
| tr2q | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | — | 0.863 | ns |
| tsrstsu | Read Synchronous Reset Setup Time | 0.279 | — | ns |
| tsrsthd | Read Synchronous Reset Hold Time | 0.062 | — | ns |
| tccy | Write Clock Period | 4 | — | ns |
| tcclkmpwh | Write Clock Minimum Pulse Width High | 1.8 | — | ns |
| tcclkmpwl | Write Clock Minimum Pulse Width Low | 1.8 | — | ns |
| tblkcsu | Write Block Setup Time | 0.417 | — | ns |
| tblkchd | Write Block Hold Time | 0.007 | — | ns |
| tdincsu | Write Input Data setup Time | 0.104 | — | ns |
| tdinchd | Write Input Data hold Time | 0.142 | — | ns |
| taddrcsu | Write Address Setup Time | 0.091 | — | ns |
| taddrchd | Write Address Hold Time | 0.253 | — | ns |
| twecsu | Write Enable Setup Time | 0.41 | — | ns |
| twechd | Write Enable Hold Time | -0.027 | — | ns |
| fmax | Maximum Frequency | — | 250 | MHz |

Table 8-12. μ SRAM (RAM512x2) in 512x2 Mode—Worst-Case Military Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|-----------|-------------------------------------|----------------|-----|-------|
| | | Min | Max | |
| tcy | Read Clock Period | 4 | — | ns |
| tclkmpwh | Read Clock Minimum Pulse Width High | 1.8 | — | ns |
| tclkmpwl | Read Clock Minimum pulse Width Low | 1.8 | — | ns |

.....continued

| Parameter | Description | Speed Grade -1 | | Units |
|------------|---|----------------|-------|-------|
| | | Min | Max | |
| tplcy | Read Pipe-line clock period | 4 | — | ns |
| tplclkmpwh | Read Pipe-line clock Minimum Pulse Width High | 1.8 | — | ns |
| tplclkmpwl | Read Pipe-line clock Minimum Pulse Width Low | 1.8 | — | ns |
| tclk2q | Read Access Time with Pipeline Register | — | 0.276 | ns |
| | Read Access Time without Pipeline Register | — | 1.824 | ns |
| taddrsu | Read Address Setup Time in Synchronous Mode | 0.311 | — | ns |
| | Read Address Setup Time in Asynchronous Mode | 2.023 | — | ns |
| taddrhd | Read Address Hold Time in Synchronous Mode | 0.141 | — | ns |
| | Read Address Hold Time in Asynchronous Mode | -0.599 | — | ns |
| trdensu | Read Enable Setup Time | 0.287 | — | ns |
| trdenhd | Read Enable Hold Time | 0.059 | — | ns |
| tblkusu | Read Block Select Setup Time | 1.898 | — | ns |
| tblkhd | Read Block Select Hold Time | -0.671 | — | ns |
| tblk2q | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 2.219 | ns |
| trstrem | Read Asynchronous Reset Removal Time (Pipelined Clock) | -0.15 | — | ns |
| | Read Asynchronous Reset Removal Time (Non-Pipelined Clock) | 0.047 | — | ns |
| trstrec | Read Asynchronous Reset Recovery Time (Pipelined Clock) | 0.524 | — | ns |
| | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock) | 0.244 | — | ns |
| tr2q | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | — | 0.862 | ns |
| tsrstsu | Read Synchronous Reset Setup Time | 0.279 | — | ns |
| tsrsthd | Read Synchronous Reset Hold Time | 0.062 | — | ns |
| tccy | Write Clock Period | 4 | — | ns |
| tcclkmpwh | Write Clock Minimum Pulse Width High | 1.8 | — | ns |
| tcclkmpwl | Write Clock Minimum Pulse Width Low | 1.8 | — | ns |
| tblkcsu | Write Block Setup Time | 0.417 | — | ns |
| tblkchd | Write Block Hold Time | 0.007 | — | ns |
| tdinusu | Write Input Data setup Time | 0.104 | — | ns |
| tdinchd | Write Input Data hold Time | 0.142 | — | ns |
| taddrusu | Write Address Setup Time | 0.091 | — | ns |
| taddrchd | Write Address Hold Time | 0.255 | — | ns |
| twecsu | Write Enable Setup Time | 0.41 | — | ns |
| twechd | Write Enable Hold Time | -0.027 | — | ns |
| fmax | Maximum Frequency | — | 250 | MHz |

Table 8-13. μ SRAM (RAM1024x1) in 1024x1 Mode—Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | Units |
|------------|---|----------------|-----|-------|
| | | Min | Max | |
| tcy | Read Clock Period | 4 | — | ns |
| tclkmpwh | Read Clock Minimum Pulse Width High | 1.8 | — | ns |
| tclkmpwl | Read Clock Minimum pulse Width Low | 1.8 | — | ns |
| tplcy | Read Pipe-line clock period | 4 | — | ns |
| tplclkmpwh | Read Pipe-line clock Minimum Pulse Width High | 1.8 | — | ns |
| tplclkmpwl | Read Pipe-line clock Minimum Pulse Width Low | 1.8 | — | ns |

|continued | | | | |
|----------------|---|----------------|-------|-------|
| Parameter | Description | Speed Grade -1 | | Units |
| | | Min | Max | |
| tclk2q | Read Access Time with Pipeline Register | — | 0.274 | ns |
| | Read Access Time without Pipeline Register | — | 1.839 | ns |
| taddrsu | Read Address Setup Time in Synchronous Mode | 0.311 | — | ns |
| | Read Address Setup Time in Asynchronous Mode | 2.041 | — | ns |
| taddrhd | Read Address Hold Time in Synchronous Mode | 0.141 | — | ns |
| | Read Address Hold Time in Asynchronous Mode | -0.623 | — | ns |
| trdensu | Read Enable Setup Time | 0.287 | — | ns |
| trdenhd | Read Enable Hold Time | 0.059 | — | ns |
| tblksu | Read Block Select Setup Time | 1.898 | — | ns |
| tblkhd | Read Block Select Hold Time | -0.671 | — | ns |
| tblk2q | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled) | — | 2.236 | ns |
| trstrem | Read Asynchronous Reset Removal Time (Pipelined Clock) | -0.15 | — | ns |
| | Read Asynchronous Reset Removal Time (Non-Pipelined Clock) | 0.047 | — | ns |
| trstrec | Read Asynchronous Reset Recovery Time (Pipelined Clock) | 0.524 | — | ns |
| | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock) | 0.244 | — | ns |
| tr2q | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | — | 0.862 | ns |
| tsrstsu | Read Synchronous Reset Setup Time | 0.279 | — | ns |
| tsrsthd | Read Synchronous Reset Hold Time | 0.062 | — | ns |
| tccy | Write Clock Period | 4 | — | ns |
| tcclkmpwh | Write Clock Minimum Pulse Width High | 1.8 | — | ns |
| tcclkmpwl | Write Clock Minimum Pulse Width Low | 1.8 | — | ns |
| tblkcsu | Write Block Setup Time | 0.417 | — | ns |
| tblkchd | Write Block Hold Time | 0.007 | — | ns |
| tdincsu | Write Input Data setup Time | 0.003 | — | ns |
| tdinchd | Write Input Data hold Time | 0.142 | — | ns |
| taddrcsu | Write Address Setup Time | 0.091 | — | ns |
| taddrchd | Write Address Hold Time | 0.255 | — | ns |
| twecsu | Write Enable Setup Time | 0.41 | — | ns |
| twechd | Write Enable Hold Time | -0.027 | — | ns |
| fmax | Maximum Frequency | — | 250 | MHz |

9. Programming Time [\(Ask a Question\)](#)

External SPI flash part # AT25DF641-s3H was used during these measurements. Typical Conditions:
 $T_j = 25\text{ }^\circ\text{C}$, $V_{DD} = 1.2\text{V}$.

Table 9-1. Programming Time of JTAG, 2 Step IAP, and MSS/Cortex®-M3 ISP—Typical Conditions

| | Device | Image size Bytes | JTAG | | 2 Step IAP | | | MSS/Cortex-M3 ISP (SmartFusion® 2 Only) | | | Auto Programming | Auto Update | Programming Recovery | Units |
|--------------------|--------|------------------|---------|--------|--------------|---------|--------|---|---------|--------|-------------------|--------------------|----------------------|-------|
| | | | PROGRAM | VERIFY | Authenticate | Program | VERIFY | Authenticate | Program | VERIFY | SPI CLK = 100 KHz | SPI CLK = 12.5 MHz | SPI CLK = 12.5 MHz | |
| Fabric Only | 010 | 568,784 | 28 | 18 | 7 | 23 | 12 | 10 | 26 | 14 | 77 | 35 | 35 | sec |
| | 025 | 1,223,504 | 51 | 26 | 14 | 33 | 23 | 21 | 39 | 29 | 150 | 41 | 41 | sec |
| | 050 | 2,424,832 | 66 | 54 | 29 | 52 | 40 | 39 | 60 | 50 | 33 ¹ | Not Supported | | sec |
| | 060 | 2,418,896 | 77 | 54 | 39 | 61 | 50 | 44 | 65 | 54 | 291 | 82 | 82 | sec |
| | 090 | 3,645,968 | 113 | 126 | 60 | 84 | 73 | 66 | 90 | 79 | 427 | 108 | 108 | sec |
| | 150 | 6,139,184 | 155 | 193 | 100 | 132 | 120 | 108 | 140 | 128 | 708 | 160 | 160 | sec |
| eNVM Only | 010 | 274,816 | 78 | 9 | 4 | 76 | 11 | 4 | 82 | 7 | 86 | 87 | 87 | sec |
| | 025 | 274,816 | 78 | 9 | 4 | 78 | 10 | 4 | 82 | 8 | 87 | 86 | 86 | sec |
| | 050 | 278,528 | 84 | 8 | 3 | 85 | 9 | 4 | 80 | 8 | 85 | Not Supported | | sec |
| | 060 | 268,480 | 76 | 8 | 5 | 76 | 22 | 6 | 80 | 8 | 78 | 86 | 86 | sec |
| | 090 | 544,496 | 154 | 15 | 10 | 152 | 43 | 10 | 157 | 15 | 154 | 162 | 162 | sec |
| | 150 | 544,496 | 155 | 15 | 10 | 153 | 44 | 10 | 158 | 15 | 161 | 161 | 161 | sec |
| Fabric+eNVM | 010 | 842,688 | 107 | 20 | 11 | 100 | 21 | 15 | 107 | 21 | 161 | 113 | 113 | sec |
| | 025 | 1,497,408 | 120 | 35 | 19 | 113 | 32 | 26 | 121 | 35 | 229 | 121 | 121 | sec |
| | 050 | 2,695,168 | 162 | 59 | 32 | 136 | 48 | 43 | 141 | 55 | 112 | Not Supported | | sec |
| | 060 | 2,686,464 | 158 | 70 | 43 | 137 | 70 | 48 | 143 | 60 | 368 | 158 | 158 | sec |
| | 090 | 4,190,208 | 266 | 147 | 68 | 236 | 115 | 75 | 244 | 91 | 582 | 260 | 260 | sec |
| | 150 | 6,682,768 | 316 | 231 | 109 | 286 | 162 | 117 | 296 | 141 | 867 | 310 | 310 | sec |

Note:

1. Auto programming in 050 device is done through SC_SPI and SPI CLK is set to 6.25 MHz.

Worst-case conditions: $T_j = 100\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$.

Table 9-2. Programming Time of JTAG, 2 Step IAP, and MSS/Cortex-M3 ISP—Worst-Case Conditions

| | Device | Image size Bytes | JTAG | | 2 Step IAP | | | MSS/Cortex-M3 ISP (SmartFusion® 2 Only) | | | Auto Programming | Auto Update | Programming Recovery | Units |
|--------------------|--------|------------------|---------|--------|--------------|---------|--------|---|---------|--------|-------------------|--------------------|----------------------|-------|
| | | | PROGRAM | VERIFY | Authenticate | Program | VERIFY | Authenticate | Program | VERIFY | SPI CLK = 100 KHz | SPI CLK = 12.5 MHz | SPI CLK = 12.5 MHz | |
| Fabric Only | 010 | 568,784 | 50 | 18 | 7 | 45 | 12 | 10 | 48 | 14 | 99 | 57 | 57 | sec |
| | 025 | 1,223,504 | 73 | 26 | 14 | 55 | 23 | 21 | 61 | 29 | 150 | 63 | 63 | sec |
| | 050 | 2,424,832 | 88 | 54 | 29 | 74 | 40 | 39 | 82 | 50 | 55 ¹ | Not Supported | | sec |
| | 060 | 2,418,896 | 99 | 54 | 39 | 83 | 50 | 44 | 87 | 54 | 313 | 104 | 104 | sec |
| | 090 | 3,645,968 | 135 | 126 | 60 | 106 | 73 | 66 | 112 | 79 | 449 | 130 | 130 | sec |
| | 150 | 6,139,184 | 177 | 193 | 100 | 154 | 120 | 108 | 162 | 128 | 730 | 183 | 183 | sec |

.....continued

| | Device | Image size Bytes | JTAG | | 2 Step IAP | | | MSS/Cortex-M3 ISP (SmartFusion® 2 Only) | | | Auto Programming | Auto Update | Programming Recovery | Units |
|--------------------|--------|------------------|---------|--------|--------------|---------|--------|---|---------|--------|-------------------|--------------------|----------------------|-------|
| | | | PROGRAM | VERIFY | Authenticate | Program | VERIFY | Authenticate | Program | VERIFY | SPI CLK = 100 KHz | SPI CLK = 12.5 MHz | SPI CLK = 12.5 MHz | |
| eNVM Only | 010 | 274,816 | 100 | 9 | 4 | 98 | 11 | 4 | 104 | 7 | 108 | 109 | 109 | sec |
| | 025 | 274,816 | 100 | 9 | 4 | 100 | 10 | 4 | 104 | 8 | 109 | 108 | 108 | sec |
| | 050 | 278,528 | 106 | 8 | 3 | 107 | 9 | 4 | 102 | 8 | 107 | Not Supported | | sec |
| | 060 | 268,480 | 98 | 8 | 5 | 98 | 22 | 6 | 102 | 8 | 100 | 108 | 108 | sec |
| | 090 | 544,496 | 176 | 15 | 10 | 174 | 43 | 10 | 179 | 15 | 176 | 184 | 184 | sec |
| | 150 | 544,496 | 177 | 15 | 10 | 175 | 44 | 10 | 180 | 15 | 183 | 183 | 183 | sec |
| Fabric+eNVM | 010 | 842,688 | 129 | 20 | 11 | 122 | 21 | 15 | 129 | 21 | 183 | 135 | 135 | sec |
| | 025 | 1,497,408 | 142 | 35 | 19 | 135 | 32 | 26 | 143 | 35 | 251 | 143 | 143 | sec |
| | 050 | 2,695,168 | 184 | 59 | 32 | 158 | 48 | 43 | 163 | 55 | 134 | Not Supported | | sec |
| | 060 | 2,686,464 | 180 | 70 | 43 | 159 | 70 | 48 | 165 | 60 | 390 | 180 | 180 | sec |
| | 090 | 4,190,208 | 288 | 147 | 68 | 258 | 115 | 75 | 266 | 91 | 604 | 282 | 282 | sec |
| | 150 | 6,682,768 | 338 | 231 | 109 | 308 | 162 | 117 | 318 | 141 | 889 | 332 | 332 | sec |

Note:

1. Auto programming in 050 device is done through SC_SPI and SPI CLK is set to 6.25 MHz.

10. Embedded NVM (eNVM) Characteristics [\(Ask a Question\)](#)

Table 10-1. eNVM Read Performance—Worst-Case Conditions: VDD = 1.14V, VPPNVM = VPP = 2.375V

| Symbol | Description | Operating Temperature Range | | | | | | Units |
|----------------------|-----------------------------|-----------------------------|------------------|---------------|-----|----|-----|-------|
| T _j | Junction Temperature Range | -55 °C to 125 °C | -40 °C to 100 °C | 0 °C to 85 °C | | | | °C |
| Speed grade | — | -1 | Std | -1 | Std | -1 | Std | — |
| F _{MAXREAD} | eNVM Maximum Read Frequency | 25 | 25 | 25 | 25 | 25 | 25 | MHz |

Table 10-2. eNVM Page Programming—Worst-Case Conditions: VDD = 1.14V, VPPNVM = VPP = 2.375V

| Symbol | Description | Operating Temperature Range | | | | | | Units |
|----------------------|----------------------------|-----------------------------|------------------|---------------|-----|----|-----|-------|
| T _j | Junction Temperature Range | -55 °C to 125 °C | -40 °C to 100 °C | 0 °C to 85 °C | | | | °C |
| Speed grade | — | -1 | Std | -1 | Std | -1 | Std | — |
| t _{PAGEPGM} | eNVM Page Programming Time | 40 | 40 | 40 | 40 | 40 | 40 | ms |

11. Crystal Oscillator [\(Ask a Question\)](#)

The following table describes the electrical characteristics of the crystal oscillator in the IGLOO 2 FPGA and SmartFusion 2 SoC FPGAs.

Table 11-1. Electrical Characteristics of the Crystal Oscillator—High Gain Mode (20 MHz)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Min | Typ | Max | Units |
|------------|--|---------------------|-------|---------------------|-------|
| FXTAL | Operating frequency | — | 20 | — | MHz |
| ACCXTAL | Accuracy | — | — | 0.006 | % |
| CYCXTAL | Output duty cycle | — | 49–51 | 47–53 | % |
| JITPERXTAL | Output Period Jitter (peak to peak) | — | 200 | 300 | ps |
| JITCYCXTAL | Output Cycle to Cycle Jitter (peak to peak) | — | 200 | 550 | ps |
| IDYNXTAL | Operating current | — | 1.5 | — | mA |
| VIHXTAL | Input logic level High | $0.9 \times V_{PP}$ | — | — | V |
| VILXTAL | Input logic level Low | — | — | $0.1 \times V_{PP}$ | V |
| SUXTAL | Startup time (with regard to stable oscillator output) | — | — | 1 | ms |

Table 11-2. Electrical Characteristics of the Crystal Oscillator—Medium Gain Mode (2 MHz)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Min | Typ | Max | Units |
|------------|--|---------------------|-------|---------------------|-------|
| FXTAL | Operating frequency | — | 2 | — | MHz |
| ACCXTAL | Accuracy | — | — | 0.003 | % |
| CYCXTAL | Output duty cycle | — | 49–51 | 47–53 | % |
| JITPERXTAL | Output Period Jitter (peak to peak) | — | 1 | 5 | ns |
| JITCYCXTAL | Output Cycle to Cycle Jitter (peak to peak) | — | 1 | 5 | ns |
| IDYNXTAL | Operating current | — | 0.3 | — | mA |
| VIHXTAL | Input logic level High | $0.9 \times V_{PP}$ | — | — | V |
| VILXTAL | Input logic level Low | — | — | $0.1 \times V_{PP}$ | V |
| SUXTAL | Startup time (with regard to stable oscillator output) | — | — | 4.5 | ms |

Table 11-3. Electrical Characteristics of the Crystal Oscillator—Low Gain Mode (32 kHz)—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Min | Typ | Max | Units |
|------------|--|---------------------|-------|---------------------|-------|
| FXTAL | Operating frequency | — | 32 | — | kHz |
| ACCXTAL | Accuracy | — | — | 0.006 | % |
| CYCXTAL | Output duty cycle | — | 49–51 | 45.5–54.5 | % |
| JITPERXTAL | Output Period Jitter (peak to peak) | — | 150 | 300 | ns |
| JITCYCXTAL | Output Cycle to Cycle Jitter (peak to peak) | — | 150 | 300 | ns |
| IDYNXTAL | Operating current | — | 0.044 | — | mA |
| VIHXTAL | Input logic level High | $0.9 \times V_{PP}$ | — | — | V |
| VILXTAL | Input logic level Low | — | — | $0.1 \times V_{PP}$ | V |
| SUXTAL | Startup time (with regard to stable oscillator output) | — | — | 120 | ms |

12. On-Chip Oscillator [\(Ask a Question\)](#)

The following tables describe the electrical characteristics of the available on-chip oscillators in the IGLOO 2 FPGAs and SmartFusion 2 SoC FPGAs.

Table 12-1. Electrical Characteristics of the 50 MHz RC Oscillator—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Condition | Min | Typ | Max | Units |
|-----------|------------------------------|-----------------------|-----|-------|-------|-------|
| F50RC | Operating frequency | — | — | 50 | — | MHz |
| ACC50RC | Accuracy | — | — | 1 | 8 | % |
| CYC50RC | Output duty cycle | — | — | 49-51 | 46-54 | % |
| JIT50RC | Output jitter (peak to peak) | Period Jitter | — | 200 | 500 | ps |
| | | Cycle-to-Cycle Jitter | — | 320 | 900 | ps |
| IDYN50RC | Operating current | — | — | 8.5 | — | mA |

Table 12-2. Electrical Characteristics of the 1 MHz RC Oscillator—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Condition | Min | Typ | Max | Units |
|-----------|------------------------------|-----------------------|-----|-------|-----------|---------------|
| F1RC | Operating frequency | — | — | 1 | — | MHz |
| ACC1RC | Accuracy | — | — | 1 | 6 | % |
| CYC1RC | Output duty cycle | — | — | 49-51 | 46.5-53.5 | % |
| JIT1RC | Output jitter (peak to peak) | Period Jitter | — | 10 | 36 | ps |
| | | Cycle-to-Cycle Jitter | — | 10 | 50 | ps |
| IDYN1RC | Operating current | — | — | 0.1 | — | mA |
| SU1RC | Startup time | — | — | — | 20 | μs |

13. Clock Conditioning Circuits (CCC) [\(Ask a Question\)](#)

Table 13-1. IGLOO® 2 and SmartFusion® 2 SoC FPGAs CCC/PLL Specification—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Conditions | Min | Typ | Max | Units |
|--|---|-------|-----|------|---------------|
| Clock conditioning circuitry input frequency f_{IN_CCC} | All CCC | 1 | — | 200 | MHz |
| | 32 kHz Capable CCC | 0.032 | — | 200 | MHz |
| Clock conditioning circuitry output frequency $f_{OUT_CCC}^1$ | — | 0.078 | — | 400 | MHz |
| PLL VCO frequency ² | — | 500 | — | 1000 | MHz |
| Delay increments in programmable delay blocks | — | — | 75 | 100 | ps |
| Number of programmable values in each programmable delay block | — | — | — | 64 | — |
| Acquisition time | $f_{IN} \geq 1\text{MHz}$ | — | 70 | 100 | μs |
| | $f_{IN} = 32\text{kHz}$ | — | 1 | 16 | ms |
| Input Duty Cycle (Reference Clock) | Internal Feedback | | | | |
| | $1\text{ MHz} \leq f_{IN_CCC} \leq 25\text{ MHz}$ | 10 | — | 90 | % |
| | $25\text{ MHz} \leq f_{IN_CCC} \leq 100\text{ MHz}$ | 25 | — | 75 | % |
| | $100\text{ MHz} \leq f_{IN_CCC} \leq 150\text{ MHz}$ | 35 | — | 65 | % |
| | $150\text{ MHz} \leq f_{IN_CCC} \leq 200\text{ MHz}$ | 45 | — | 55 | % |
| | External Feedback (CCC, FPGA, Off-chip) | | | | |
| | $1\text{ MHz} \leq f_{IN_CCC} \leq 25\text{ MHz}$ | 25 | — | 75 | % |
| | $25\text{ MHz} \leq f_{IN_CCC} \leq 35\text{ MHz}$ | 35 | — | 65 | % |
| Output duty cycle | 010, 025, and 050 Devices | 46 | — | 52 | % |
| | 060, 090, and 150 Devices | 44 | — | 52 | % |
| Spread Spectrum Characteristics | | | | | |
| Modulation frequency range | — | 25 | 35 | 50 | kHz |
| Modulation depth range | — | 0 | — | 1.5 | % |
| Modulation depth control | — | — | 0.5 | — | % |

Notes:

- The minimum output clock frequency is limited by the PLL. For more information, refer to the [UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide](#).
- The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output frequency.

Table 13-2. IGLOO® 2 and SmartFusion® 2 SoC FPGAs CCC/PLL Jitter Specifications—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Conditions/Package Combinations | Units |
|--|--|-------|
| CCC Output Peak-to-Peak Period Jitter f_{OUT_CCC} | | |
| 010, 050 FG484 Packages ¹ | SSO = 0 | — |
| 20 MHz to 100 MHz | $\text{Max}(110, \pm 1\% \times (1/f_{OUT_CCC}))$ | ps |
| 100 MHz to 400 MHz | 120 | ps |
| 025 FG484 Package ¹ | $0 < \text{SSO} \leq 16$ | — |
| 20 MHz to 74 MHz | $\pm 1\% \times (1/f_{OUT_CCC})$ | ps |

.....continued

| Parameter | Conditions/Package Combinations | Units |
|--|-----------------------------------|-------|
| 74 MHz to 400 MHz | 210 | ps |
| 090 FG484 and 150 FC1152 Packages ¹ | 0 < SSO <=16 | |
| 20 MHz to 100 MHz | $\pm 1\% \times (1/f_{OUT_CCC})$ | ps |
| 100 MHz to 400 MHz | 150 | ps |

Note:

1. SSO Data is based on LVCMOS 2.5V MSIO and/or MSIOD Bank I/Os.

14. JTAG [\(Ask a Question\)](#)

Table 14-1. JTAG 1532—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Speed Grade -1 | | | | | | Units |
|-----------|-----------------------------|----------------|-------|-------|-------|-------|-------|-------|
| | | 010 | 025 | 050 | 060 | 090 | 150 | |
| tTCK2Q | Clock to Q (data out) | 7.91 | 7.95 | 8.15 | 8.54 | 9.21 | 8.85 | ns |
| tRSTB2Q | Reset to Q (data out) | 6.54 | 6.27 | 7.54 | 8.70 | 7.94 | 8.99 | ns |
| tDISU | Test Data Input Setup Time | -0.70 | -0.70 | -0.31 | -1.20 | -1.33 | -1.02 | ns |
| tDIHD | Test Data Input Hold Time | 2.38 | 2.47 | 2.13 | 2.55 | 2.71 | 2.59 | ns |
| tTMSSU | Test Mode Select Setup Time | -0.86 | -1.13 | 0.26 | -0.99 | -1.03 | -0.56 | ns |
| tTMDHD | Test Mode Select Hold Time | 1.48 | 1.98 | 0.21 | 1.71 | 1.69 | 1.05 | ns |
| tTRSTREM | ResetB Removal Time | -1.1 | -1.38 | -0.49 | -1.24 | -0.8 | -1.07 | ns |
| tTRSTREC | ResetB Recovery Time | -1.1 | -1.38 | -0.47 | -1.23 | -0.8 | -1.07 | ns |
| FTCKMAX | TCK Maximum frequency | 25 | 25 | 25 | 25 | 25 | 25 | MHz |

Note: The JTAG IOs are LVCMOS/LVTTL IOs (TMS, TRSTB, TDI, TCK, and TDO). The JTAG IOs are powered by VDDI of the Bank they are located in.

15. Power-Up to Functional Time (Ask a Question)

Worst-Case Industrial Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$.

Figure 15-1. Power-Up to Functional Timing Diagram when MSS/HPMS is Used

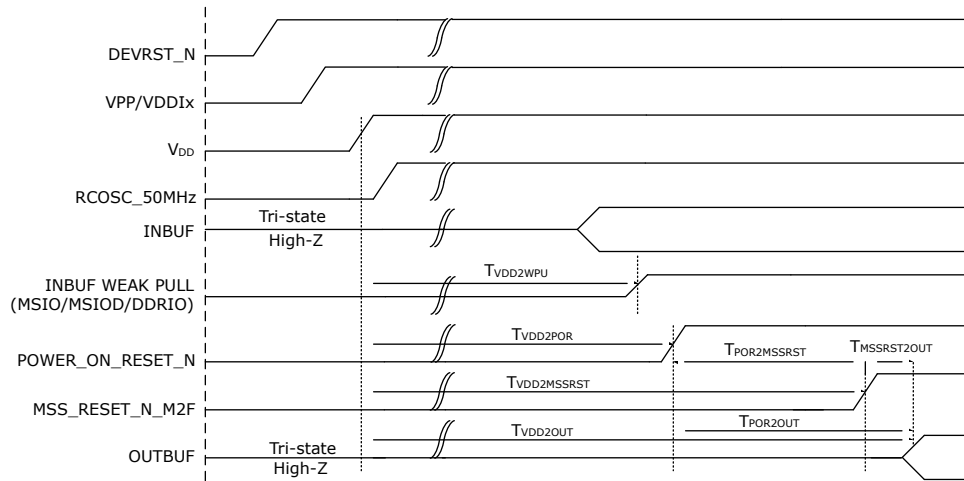
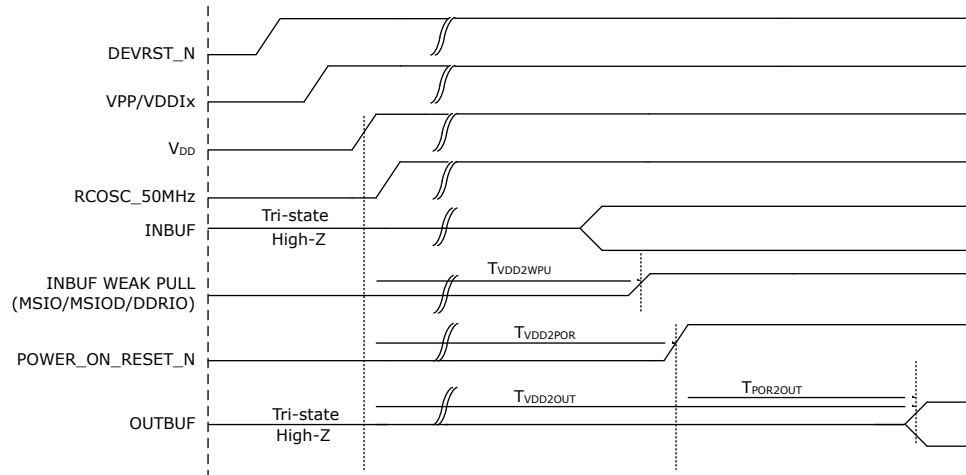


Table 15-1. Maximum Power-Up to Functional Time when MSS/HPMS is Used (μs)

| Parameter | From | To | Description | 010 | 025 | 050 | 060 | 090 | 150 |
|------------------|------------------------------------|-------------------------|--|------|------|------|------|------|------|
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 500 | 531 | 483 | 474 | 524 | 647 |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESET_N_M2F | Fabric to MSS | 497 | 528 | 480 | 468 | 518 | 641 |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F / HMPS_RESET_N_M2F | Output available at I/O | MSS to output | 3.6 | 3.6 | 3.4 | 4.9 | 4.8 | 4.8 |
| $T_{VDD2OUT}$ | VDD | Output available at I/O | VDD at its minimum threshold level to output | 2975 | 3012 | 2959 | 2869 | 2992 | 3225 |
| $T_{VDD2POR}$ | VDD | POWER_ON_RESET_N | VDD at its minimum threshold level to Fabric | 2487 | 2496 | 2486 | 2406 | 2563 | 2602 |
| $T_{VDD2MSSRST}$ | VDD | MSS_RESET_N_M2F | VDD at its minimum threshold level to MSS | 2972 | 3008 | 2956 | 2864 | 2987 | 3220 |
| $T_{VDD2WPU}$ | VDD | DDRIO Inbuf Weak Pull | VDD to Inbuf Weak Pull | 2487 | 2509 | 2475 | 2507 | 2519 | 2617 |
| | VDD | MSIO Inbuf Weak Pull | VDD to Inbuf Weak Pull | 2491 | 2510 | 2478 | 2517 | 2525 | 2620 |
| | VDD | MSIOD Inbuf Weak Pull | VDD to Inbuf Weak Pull | 2468 | 2493 | 2458 | 2486 | 2499 | 2595 |

Note: This table does not consider SUSPEND_MODE.

Figure 15-2. Power-Up to Functional Timing Diagram when MSS/HPMS is not Used

Table 15-2. Maximum Power-Up to Functional Time when MSS/HPMS is Not Used (μs)

| Parameter | From | To | Description | 010 | 025 | 050 | 060 | 090 | 150 |
|----------------------|------------------|-------------------------|--|------|------|------|------|------|------|
| T _{POR2OUT} | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 114 | 114 | 113 | 114 | 114 | 114 |
| T _{VDD2OUT} | VDD | Output available at I/O | VDD at its minimum threshold level to output | 2600 | 2607 | 2558 | 2591 | 2600 | 2699 |
| T _{VDD2POR} | VDD | POWER_ON_RESET_N | VDD at its minimum threshold level to Fabric | 2486 | 2493 | 2445 | 2477 | 2486 | 2585 |
| T _{VDD2WPU} | VDD | DDRIO Inbuf Weak Pull | DEVRST_N to Inbuf Weak Pull | 2487 | 2509 | 2475 | 2507 | 2519 | 2617 |
| | VDD | MSIO Inbuf Weak Pull | DEVRST_N to Inbuf Weak Pull | 2491 | 2510 | 2478 | 2517 | 2525 | 2620 |
| | VDD | MSIOD Inbuf Weak Pull | DEVRST_N to Inbuf Weak Pull | 2468 | 2493 | 2458 | 2486 | 2499 | 2595 |

Note: This table does not consider SUSPEND_MODE.

16. DEVRST_N Characteristics [\(Ask a Question\)](#)

Table 16-1. DEVRST_N Characteristics—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Symbol | Description | All Devices/Speed Grades | | | Units |
|---------------|----------------------|--------------------------|-----|-----|---------------|
| | | Min | Typ | Max | |
| TRAMPDEVRST_N | DEVRSTN ramp time | — | — | 1 | μs |
| FMAXPDEVRST_N | DEVRSTN cycling rate | — | — | 100 | kHZ |

17. DEVRST_N to Functional Time (Ask a Question)

Worst-case industrial conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$.

Figure 17-1. DEVRST_N to Functional Timing Diagram when MSS/HPMS is Used

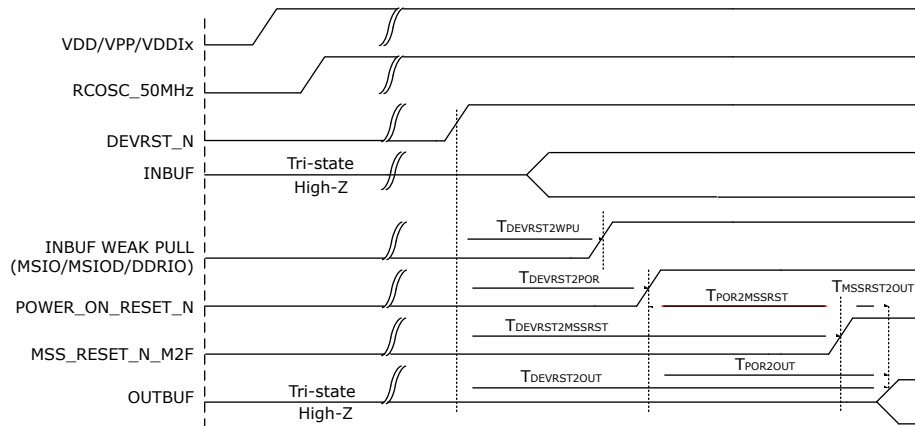


Table 17-1. Maximum DEVRST_N to Functional Time when MSS/HPMS is Used (μs)

| Parameter | From | To | Description | 010 | 025 | 050 | 060 | 090 | 150 |
|---------------------|-------------------------------------|-------------------------|--|-----|-----|-----|-----|-----|-----|
| $T_{POR2OUT}$ | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 501 | 527 | 521 | 422 | 419 | 694 |
| $T_{POR2MSSRST}$ | POWER_ON_RESET_N | MSS_RESET_N_M2F | Fabric to MSS | 497 | 524 | 518 | 417 | 414 | 689 |
| $T_{MSSRST2OUT}$ | MSS_RESET_N_M2F / HMPMS_RESET_N_M2F | Output available at I/O | MSS to output | 3.5 | 3.5 | 3.3 | 4.8 | 4.8 | 4.8 |
| $T_{DEVRST2OUT}$ | DEVRST_N | Output available at I/O | VDD at its minimum threshold level to output | 768 | 715 | 691 | 641 | 635 | 871 |
| $T_{DEVRST2POR}$ | DEVRST_N | POWER_ON_RESET_N | VDD at its minimum threshold level to Fabric | 289 | 216 | 213 | 237 | 234 | 219 |
| $T_{DEVRST2MSSRST}$ | DEVRST_N | MSS_RESET_N_M2F | VDD at its minimum threshold level to MSS | 765 | 712 | 688 | 636 | 630 | 866 |
| $T_{DEVRST2WPU}$ | DEVRST_N | DDRIO Inbuf Weak Pull | DEVRST_N to Inbuf Weak Pull | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf Weak Pull | DEVRST_N to Inbuf Weak Pull | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf Weak Pull | DEVRST_N to Inbuf Weak Pull | 202 | 197 | 193 | 216 | 215 | 215 |

Note: This table does not support SUSPEND_MODE.

Figure 17-2. DEVRST_N to Functional Timing Diagram when MSS/HPMS is not Used

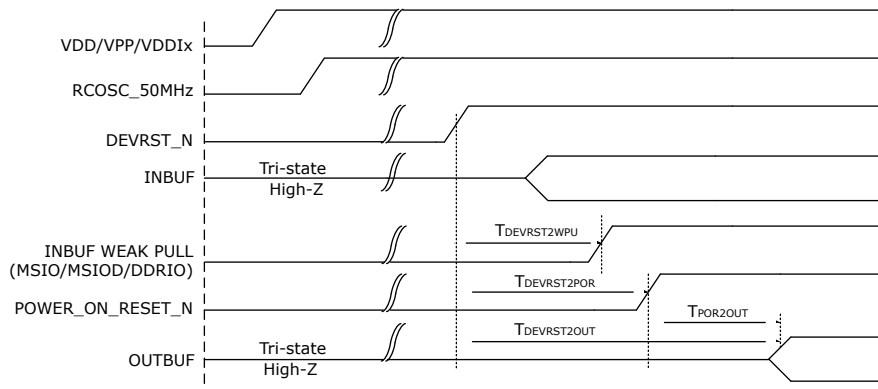


Table 17-2. Maximum DEVRST_N to Functional Time when MSS/HPMS is Not Used (µs)

| Parameter | From | To | Description | 010 | 025 | 050 | 060 | 090 | 150 |
|-------------------------|------------------|-------------------------|--|-----|-----|-----|-----|-----|-----|
| T _{POR2OUT} | POWER_ON_RESET_N | Output available at I/O | Fabric to output | 116 | 113 | 113 | 115 | 115 | 114 |
| T _{DEVRST2OUT} | DEVRST_N | Output available at I/O | VDD at its minimum threshold level to output | 353 | 314 | 307 | 343 | 341 | 341 |
| T _{DEVRST2POR} | DEVRST_N | POWER_ON_RESET_N | VDD at its minimum threshold level to Fabric | 238 | 201 | 195 | 230 | 229 | 227 |
| T _{DEVRST2WPU} | DEVRST_N | DDRIO Inbuf Weak Pull | DEVRST_N to Inbuf Weak Pull | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIO Inbuf Weak Pull | DEVRST_N to Inbuf Weak Pull | 202 | 197 | 193 | 216 | 215 | 215 |
| | DEVRST_N | MSIOD Inbuf Weak Pull | DEVRST_N to Inbuf Weak Pull | 202 | 197 | 193 | 216 | 215 | 215 |

Note: This table does not support SUSPEND_MODE.

18. System Controller SPI Characteristics [\(Ask a Question\)](#)

Table 18-1. System Controller SPI Characteristics—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Units |
|---|---|--|--------------------------|-------|-----|-------|
| | | | Min | Typ | Max | |
| sp1 | SC_SPI_SCK minimum period | — | 20 | — | — | ns |
| sp2 | SC_SPI_SCK minimum pulse width high | — | 10 | — | — | ns |
| sp3 | SC_SPI_SCK minimum pulse width low | — | 10 | — | — | ns |
| sp4 ¹ | SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%-90%) 1 | I/O Configuration: LVTTTL 3.3V-20 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C | — | 1.239 | — | ns |
| sp5 ¹ | SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%-90%) 1 | I/O Configuration: LVTTTL 3.3V-20 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C | — | 1.245 | — | ns |
| sp6 | SC_SPI_SDO setup time | — | 160 | — | — | ns |
| sp7 | SC_SPI_SDO hold time | — | 160 | — | — | ns |
| sp8 | SC_SPI_SDI setup time | — | 20 | — | — | ns |
| sp9 | SC_SPI_SDI hold time | — | 20 | — | — | ns |
| Delay on SC_SPI_SDO after SC_SPI_SS is de-asserted when using SPI slave programming. ² | | | — | — | 265 | ns |

Notes:

- For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website: www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas#ibis. Use the supported I/O Configurations for the System Controller SPI in [Table 18-2](#).
- SC_SPI_SDO becomes tri-stated after SC_SPI_SS is de-asserted.

Table 18-2. Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)

| Voltage Supply | I/O Drive Configuration | Units |
|----------------|-------------------------|-------|
| 3.3V | 20 | mA |
| 2.5V | 16 | mA |
| 1.8V | 12 | mA |
| 1.5V | 8 | mA |
| 1.2V | 4 | mA |

19. Mathblock Timing Characteristics [\(Ask a Question\)](#)

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO 2 and SmartFusion 2 SoC mathblock supports 18x18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

Table 19-1. Mathblocks With All Registers Used (Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$)

| Mathblock With All Registers Used | | Speed Grade -1 | | Units |
|-----------------------------------|-------------------------------------|----------------|-------|-------|
| Parameter | Description | Min | Max | |
| TMISU | Input, Control Register Setup time | 0.149 | — | ns |
| TMIHD | Input, Control Register Hold time | 0.08 | — | ns |
| TMOCDINSU | CDIN Input Setup time | 1.68 | — | ns |
| TMOCDINH | CDIN Input Hold time | -0.419 | — | ns |
| TMSRSTENSU | Synchronous Reset/Enable Setup time | 0.185 | — | ns |
| TMSRSTENHD | Synchronous Reset/Enable Hold time | 0.011 | — | ns |
| TMARSTREM | Asynchronous Reset Removal time | 0 | — | ns |
| TMARSTREC | Asynchronous Reset Recovery time | 0.088 | — | ns |
| TMOCQ | Output Register Clock to Out delay | — | 0.232 | ns |
| TMCLKMP | CLK Minimum period | 2.245 | — | ns |

Table 19-2. Mathblock With Input Bypassed and Output Registers Used—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Mathblock With Input Bypassed and Output Registers Used | | Speed Grade -1 | | Units |
|---|-------------------------------------|----------------|-------|-------|
| Parameter | Description | Min | Max | |
| TMOSU | Output Register Setup time | 2.294 | — | ns |
| TMOHD | Output Register Hold time | -0.444 | — | ns |
| TMOCDINSU | CDIN Input Setup time | 1.68 | — | ns |
| TMOCDINH | CDIN Input Hold time | -0.419 | — | ns |
| TMSRSTENSU | Synchronous Reset/Enable Setup time | 0.115 | — | ns |
| TMSRSTENHD | Synchronous Reset/Enable Hold time | 0.011 | — | ns |
| TMARSTREM | Asynchronous Reset Removal time | 0 | — | ns |
| TMARSTREC | Asynchronous Reset Recovery time | 0.014 | — | ns |
| TMOCQ | Output Register Clock to Out delay | — | 0.232 | ns |
| TMCLKMP | CLK Minimum period | 2.179 | — | ns |

Table 19-3. Mathblock With Input Register Used and Output in Bypass Mode—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Mathblock With Input Register Used and Output in Bypass Mode | | Speed Grade -1 | | Units |
|--|-------------------------------------|----------------|-----|-------|
| Parameter | Description | Min | Max | |
| TMISU | Input Register Setup time | 0.149 | — | ns |
| TMIHD | Input Register Hold time | 0.08 | — | ns |
| TMSRSTENSU | Synchronous Reset/Enable Setup time | 0.185 | — | ns |
| TMSRSTENHD | Synchronous Reset/Enable Hold time | -0.012 | — | ns |
| TMARSTREM | Asynchronous Reset Removal time | -0.005 | — | ns |

.....continued

| Mathblock With Input Register Used and Output in Bypass Mode | | Speed Grade -1 | | Units |
|--|--------------------------------------|----------------|-------|-------|
| Parameter | Description | Min | Max | |
| TMARSTREC | Asynchronous Reset Recovery time | 0.088 | — | ns |
| TMICQ | Input Register Clock to Output delay | — | 2.52 | ns |
| TMCDIN2Q | CDIN to Output delay | — | 1.951 | ns |

Table 19-4. Mathblock With Input and Output in Bypass Mode—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Mathblock With Input and Output in Bypass Mode | | Speed Grade -1 | | Units |
|--|-----------------------|----------------|-------|-------|
| Parameter | Description | Min | Max | |
| TMIQ | Input to Output delay | — | 2.568 | ns |
| TMCDIN2Q | CDIN to Output delay | — | 1.951 | ns |

20. Flash*Freeze Timing Characteristics [\(Ask a Question\)](#)

Table 20-1. Flash*Freeze Entry and Exit Times—Military Worst-Case conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Symbols | Parameters | Conditions | Entry/Exit Timing | | Units |
|-----------|--|--|-------------------|------------|---------------|
| | | | FCLK=100 MHz | FCLK=3 MHz | |
| TFF_ENTRY | Entry time | eNVM and MSS/HPMS PLL = ON | 160 | 320 | μs |
| | | eNVM and MSS/HPMS PLL = OFF | 215 | 430 | μs |
| TFF_EXIT | Exit time with respect to MSS PLL Lock | eNVM and MSS/HPMS PLL = ON during Flash*Freeze | 100 | 140 | μs |
| | | eNVM = ON and MSS/HPMS PLL = OFF during Flash*Freeze and MSS/HPMS PLL turned back on at exit | 136 | 190 | μs |
| | | eNVM and MSS PLL=OFF during Flash*Freeze and both are turned back on at exit | 200 | 285 | μs |
| | | eNVM = OFF and MSS PLL = ON during Flash*Freeze and eNVM turned back on at exit | 200 | 285 | μs |
| | Exit time with respect to Fabric PLL Lock ¹ | eNVM and MSS/HPMS PLL = ON during Flash*Freeze | 1.5 | 1.5 | ms |
| | | eNVM and MSS PLL=OFF during Flash*Freeze and both are turned back on at exit | 1.5 | 1.5 | ms |
| | Exit time with respect to Fabric buffer output | eNVM and MSS/HPMS PLL = ON during Flash*Freeze | 21 | 21 | μs |
| | | eNVM and MSS PLL=OFF during Flash*Freeze and both are turned back on at exit | 65 | 65 | μs |

Note:

1. PLL lock delay set to 1024 cycles (default).

21. DDR Memory Interface Characteristics [\(Ask a Question\)](#)

Table 21-1. DDR Memory Interface Characteristics—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Standard | Supported Data Rate | | | Unit |
|----------|---------------------|---|-----|------|
| DDR3 | — | — | 667 | Mbps |
| DDR2 | — | — | 667 | Mbps |
| LPDDR | 50 | — | 400 | Mbps |

22. SFP Transceiver Characteristics [\(Ask a Question\)](#)

IGLOO 2 and SmartFusion 2 SerDes complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. The following table provides the electrical characteristics.

Table 22-1. SFP Transceiver Electrical Characteristics—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Pin | Direction | Differential Peak-Peak Voltage | | Unit | |
|--------------------|-----------|--------------------------------|---|------|----|
| RD+/- ¹ | Output | 1600 | — | 2400 | mV |
| TD+/- ² | Input | 350 | — | 2400 | mV |

Notes:

1. Based on default SerDes transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0V. Requires AC Coupling.

23. SRAM PUF (Ask a Question)

Worst-case military conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$.

For more information about SRAM physical unclonable functions (PUF) services, see [AC434: Using SRAM PUF System Service in SmartFusion2 Application Note](#).

Table 23-1. SRAM PUF

| Service | PUF OFF | | PUF ON | | Units |
|--------------------------|---------|---------|--------|--------|-------|
| | Typ | Max | Typ | Max | |
| Create activation code | 709.1 | 770.8 | 796.0 | 865.3 | ms |
| Delete activation code | 1329.3 | 1444.9 | 1303.0 | 1416.3 | ms |
| Create intrinsic keycode | 656.6 | 713.7 | 643.6 | 699.5 | ms |
| Create extrinsic keycode | 656.6 | 713.7 | 643.6 | 699.5 | ms |
| Get number of keys | 1.3 | 1.5 | 1.3 | 1.4 | ms |
| Export (KC0, KC1) | 998.0 | 1084.8 | 978.2 | 1063.3 | ms |
| Export 2 keycodes | 2020.2 | 2195.9 | 1980.2 | 2152.4 | ms |
| Export 4 keycodes | 3065.7 | 3332.2 | 3005.0 | 3266.3 | ms |
| Export 8 keycodes | 5101.0 | 5544.6 | 5000.0 | 5434.8 | ms |
| Export 16 keycodes | 9212.1 | 10013.2 | 9029.7 | 9814.9 | ms |
| Import (KC0, KC1) | 39.7 | 43.1 | 38.9 | 42.3 | ms |
| Import 2 keycodes | 50.1 | 54.5 | 49.1 | 53.4 | ms |
| Import 4 keycodes | 60.6 | 65.9 | 59.4 | 64.6 | ms |
| Import 8 keycodes | 80.9 | 87.9 | 79.3 | 86.2 | ms |
| Import 16 keycodes | 123.8 | 134.6 | 121.4 | 131.9 | ms |
| Delete keycode | 552.5 | 600.6 | 541.6 | 588.7 | ms |
| Fetch key | 31.4 | 34.1 | 11.5 | 12.5 | ms |
| Fetch ECC key | 20.0 | 21.7 | 1.9 | 2.1 | ms |
| Get seed | 2.0 | 2.2 | 0.9 | 1.0 | ms |

24. Non-Deterministic Random Bit Generator (NRBG) Characteristics (Ask a

Question)

The following table lists the NRBG characteristics of military-grade SmartFusion 2 and IGLOO 2 devices. For detailed information about NRBG, see [AC407: Using NRBG Services in SmartFusion 2 and IGLOO 2 Devices Application Note](#).

Table 24-1. NRBG Characteristics—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

| Service | Conditions | | Timing | Units |
|---|---------------------------|------------------|---|-------|
| | Prediction Resistance | Additional Input | | |
| Instantiate | OFF | X | 85 | ms |
| Generate (after instantiate) ¹ | OFF | 0 | 4.5 ms + (7 $\mu\text{s}/\text{byte} \times$ No. of bytes) | — |
| | OFF | 64 | 6.0 ms + (7 $\mu\text{s}/\text{byte} \times$ No. of bytes) | — |
| | OFF | 128 | 7.0 ms + (7 $\mu\text{s}/\text{byte} \times$ No. of bytes) | — |
| | ON | X | 47 | ms |
| Generate (subsequent) ¹ | OFF | 0 | 0.5 ms + (7 $\mu\text{s}/\text{byte} \times$ No. of bytes) | — |
| | OFF | 64 | 2.0 ms + (7 $\mu\text{s}/\text{byte} \times$ No. of bytes) | — |
| | OFF | 128 | 3.0 ms + (7 $\mu\text{s}/\text{byte} \times$ No. of bytes) | — |
| | ON | X | 43 | ms |
| Reseed | — | — | 40 | ms |
| Uninstantiate | — | — | 0.16 | ms |
| Reset | — | — | 0.10 | ms |
| Self test | First time after power-up | — | 20 | ms |
| | Subsequent | — | 6 | ms |

Note:

1. If PUF is OFF, Generate incurs an additional PUF delay time for consecutive service calls.

25. Cryptographic Block Characteristics [\(Ask a Question\)](#)

The following table lists the cryptographic block characteristics of military-grade SmartFusion 2 and IGLOO 2 devices. For detailed information about cryptographic blocks, see the following documents:

- [AC410: Using AES System Services in SmartFusion 2 and IGLOO 2 Devices Application Note](#)
- [AC432: Using SHA-256 System Services in SmartFusion 2 and IGLOO 2 Devices Application Note](#)

Table 25-1. Cryptographic Block Characteristics—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Service | Conditions | Timing | Units |
|---|---|--------|-------|
| Any service | First certificate check penalty at boot | 11.5 | ms |
| AES128/256 (encoding/decoding) ¹ | Up to 100 blocks | 200 | kbps |
| | 100 blocks up to 64k blocks | 650 | kbps |
| SHA256 | 512 bits | 530 | kbps |
| | 1024 bits | 770 | kbps |
| | 2048 bits | 940 | kbps |
| | 24 kbits | 1130 | kbps |
| HMAC | 512 bytes | 810 | kbps |
| | 1024 bytes | 880 | kbps |
| | 2048 bytes | 920 | kbps |
| | 24 kbytes | 970 | kbps |
| KeyTree | — | 1.6 | ms |
| Challenge-response | PUF = OFF | 23 | ms |
| | PUF = ON | 6.6 | ms |
| ECC point multiplication | — | 590 | ms |
| ECC point addition | — | 8 | ms |

Note:

1. Applicable when using Cypher Block Chaining (CBC) mode.

26. SerDes Electrical and Timing AC and DC Characteristics [\(Ask a Question\)](#)

The IGLOO 2 and SmartFusion 2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block.

Table 26-1. Transmitter Parameters—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Min | Typ | Max | Units |
|---------------|---|-------|-----|---------------|---------------|
| VTX-DIFF-PP | Differential swing (2.5 Gbps) | 0.8 | — | 1.2 | V |
| VTX-CM-AC-P | Output common mode voltage (2.5 Gbps) | — | — | 20 | mV |
| VTX-RISE-FALL | Rise and fall time (20% to 80%, 2.5 Gbps) | 0.125 | — | — | UI |
| ZTX-DIFF-DC | Output impedance – differential | 80 | — | 120 | Ω |
| LTX-SKEW | Lane-to-lane TX skew within a SERDES block (2.5 Gbps) | — | — | 500 ps + 2 UI | ps |
| RLTX-DIFF | Return loss differential mode (2.5 Gbps) | -10 | — | — | dB |
| RLTX-CM | Return loss common mode (2.5 Gbps) | -6 | — | — | dB |
| TX-LOCK-RST | Transmit PLL lock time from reset | — | — | 10 | μs |
| VTX-AMP | 100 mV setting | 90 | — | 150 | mV |
| | 400 mV setting | 320 | — | 480 | mV |
| | 800 mV setting | 660 | — | 940 | mV |
| | 1200 mV setting | 950 | — | 1400 | mV |

Table 26-2. Receiver Parameters—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Min | Typ | Max | Units |
|----------------------|--|-------|-------|-------|---------------|
| VRX-IN-PP-CC | Differential input peak-to-peak sensitivity (2.5 Gbps) | 0.238 | — | 1.2 | V |
| | Differential input peak-to-peak sensitivity (2.5 Gbps, deemphasized) | 0.219 | — | 1.2 | V |
| VRX-CM-AC-P | Input common mode range (AC coupled) | — | — | 150 | mV |
| ZRX-DIFF-DC | Differential input termination | 80 | 100 | 120 | Ω |
| REXT | External calibration resistor | 1,188 | 1,200 | 1,212 | Ω |
| CDR-LOCK-RST | CDR relock time from reset | — | — | 15 | μs |
| RLRX-DIFF | Return loss differential mode (2.5 Gbps) | -10 | — | — | dB |
| RLRX-CM | Return loss common mode (2.5 Gbps) | -6 | — | — | dB |
| RX-CID ¹ | CID limit (set by 8B/10B coding, not the receiver PLL) | — | — | 200 | UI |
| VRX-IDLE-DET-DIFF-PP | Signal detect limit | 65 | — | 175 | mV |

Note:

1. AC-coupled, $\text{BER} = e^{-12}$.

Table 26-3. SERDES Reference Clock AC Specifications —Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Symbols | Description | Min | Typ | Max | Units |
|----------|---------------------------------|------|-----|------|-------|
| FREFCLK | Reference Clock Frequency | 100 | — | 160 | MHz |
| TRISE | Reference Clock Rise Time | 0.6 | — | 4 | V/ns |
| TFALL | Reference Clock Fall Time | 0.6 | — | 4 | V/ns |
| TCYC | Reference Clock Duty Cycle | 40 | — | 60 | % |
| Mmrefclk | Reference Clock Mismatch | -300 | — | 300 | ppm |
| SSCref | Reference Spread Spectrum Clock | 0 | — | 5000 | ppm |

Table 26-4. HCSL Minimum and Maximum DC Input Levels (Applicable to SERDES REFCLK Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--|----------------------------|------------|-------|-----|-------|-------|
| Recommended DC Operating Conditions | | | | | | |
| VDDI | Supply Voltage | — | 2.375 | 2.5 | 2.625 | V |
| HCSL DC Input Voltage Specification | | | | | | |
| VI | DC Input voltage | — | 0 | — | 2.625 | V |
| HCSL Differential Voltage Specification | | | | | | |
| VICM | Input common mode voltage | — | 0.05 | — | 2.4 | V |
| VIDIFF | Input differential voltage | — | 100 | — | 1100 | mV |

Table 26-5. HCSL Maximum AC Switching Speeds (Applicable to SERDES REFCLK Only)

| Symbols | Parameters | Conditions | Min | Typ | Max | Units |
|--------------------------------------|--------------------------------------|------------|-----|-----|-----|----------|
| HCSL AC Specifications | | | | | | |
| Fmax | Maximum Data Rate (for MSIO IO Bank) | — | — | — | 350 | Mbps |
| HCSL Impedance Specifications | | | | | | |
| Rt | Termination Resistance | — | — | 100 | — | Ω |

27. SERDES Protocol Compliance [\(Ask a Question\)](#)

Table 27-1. SERDES Protocol Compliance

| Protocol | Maximum Data Rate | -1 Speed Grade |
|-------------------|-------------------|----------------|
| PCIe® Gen 1 | 2.5 Gbps | Yes |
| XAUI ¹ | 3.125 Gbps | Yes |
| Generic EPCS | 2.5 Gbps | Yes |

Note:

1. XAUI protocol is not supported in Military temperature range.

28. MMUART Characteristics [\(Ask a Question\)](#)

Worst-case military conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$.

Table 28-1. MMUART Characteristics

| Parameter | Descriptions | -1 Speed Grade | Units |
|-----------------|---|----------------|-------|
| FMMUART_REF_CLK | Internally sourced MMUART reference clock frequency | 133 | MHz |
| BAUDMMUARTTx | Maximum transmit baud rate | 8.3125 | Mbps |
| BAUDMMUARTRx | Maximum receive baud rate | 8.3125 | Mbps |

29. CAN Controller Characteristics [\(Ask a Question\)](#)

Table 29-1. CAN Controller Characteristics—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Min | Typ | Max | Units |
|-------------------------|--|------|-----|-----|-------|
| FCANREFCLK ¹ | Internally Sourced CAN Reference Clock Frequency | — | — | 128 | MHz |
| BAUDCAN | CAN Performance Baud Rate | 0.05 | — | 1 | Mbps |

Note:

1. PCLK to CAN controller must be a multiple of 8 MHz.

29.1 USB Characteristics [\(Ask a Question\)](#)

Table 29-2. USB Characteristics—Worst-Case Military Conditions: $T_j = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Description | Min | Typ | Max | Units |
|------------|--|-----|-----|-------|-------|
| FUSBREFCLK | Internally Sourced USB Reference Clock Frequency | — | — | 133 | MHz |
| TUSBCLK | USB Clock Period | — | — | 16.66 | ns |
| TUSBPD | Clock to USB Data Propagation Delay | — | — | 9.0 | ns |
| TUSBSU | Setup Time for USB Data | — | — | 6.0 | ns |
| TUSBHD | Hold Time for USB Data | 0 | — | — | ns |

30. SmartFusion 2 Specifications [\(Ask a Question\)](#)

30.1 MSS Clock Frequency [\(Ask a Question\)](#)

Table 30-1. Maximum Frequency for MSS Main Clock—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Symbol | Description | Speed Grade -1 | Units |
|--------|---|----------------|-------|
| M3_CLK | Maximum frequency for the MSS Main Clock (FCLK) | 133 | MHz |

30.2 SmartFusion 2 Inter-Integrated Circuit (I²C) Characteristics [\(Ask a Question\)](#)

This section describes the DC and switching of the I2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins.

Table 30-2. I2C Characteristics—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Parameter | Definition | Conditions | Min | Typ | Max | Units |
|----------------------------|--|--|------------------|--------|--------|---------------|
| VIL | Input low voltage | Refer to the Single-Ended I/O Standards for more information. I/O standard used for illustration: MSIO bank- LVTTTL 8 mA low drive. | -0.3 | — | 0.8 | V |
| VIH | Input high voltage | Refer to the Single-Ended I/O Standards for more information. I/O standard used for illustration: MSIO bank - LVTTTL 8 mA low drive. | 2 | — | 3.45 | V |
| VHYS | Hysteresis of Schmitt triggered inputs for $V_{DDI} > 2\text{V}$ | Refer to Table 5-5 for more information. | 0.05 x V_{DDI} | — | — | V |
| IIL | Input current high | Refer to the Single-Ended I/O Standards for more information. | — | — | 10 | μA |
| IIH | Input current low | Refer to the Single-Ended I/O Standards for more information. | — | — | 10 | μA |
| Tir | Input rise time | Standard Mode | — | — | 1000 | ns |
| | | Fast Mode | — | — | 300 | ns |
| Tif | Input fall time | Standard Mode | — | — | 300 | ns |
| | | Fast Mode | — | — | 300 | ns |
| VOL | Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI} > 2\text{V}$ | Refer to the Single-Ended I/O Standards for more information. I/O standard used for illustration: MSIO bank - LVTTTL 8 mA low drive. | — | — | 0.4 | V |
| Cin | Pin capacitance | $V_{IN} = 0$, $f = 1.0\text{ MHz}$ | — | — | 10 | pF |
| tOF | Output fall time from V_{IHMin} to V_{ILMax} | V_{IHmin} to V_{ILMax} , $C_{load} = 400\text{ pF}$ ¹ | — | 21.04 | — | ns |
| | | V_{IHmin} to V_{ILMax} , $C_{load} = 100\text{ pF}$ | — | 5.556 | — | ns |
| tOR | Output rise time from V_{ILMax} to V_{IHMin} | V_{ILMax} to V_{IHmin} , $C_{load} = 400\text{ pF}$ ¹ | — | 19.887 | — | ns |
| | | V_{ILMax} to V_{IHmin} , $C_{load} = 100\text{ pF}$ | — | 5.218 | — | ns |
| Rpull-up ^{2, 3} | Output buffer maximum pull-down resistance | — | — | — | 50 | Ω |
| Rpull-down ^{2, 4} | Output buffer maximum pull-up resistance | — | — | — | 131.25 | Ω |
| Dmax | Maximum data rate | Fast mode | — | — | 400 | Kbps |
| | | Standard mode | — | — | 100 | Kbps |

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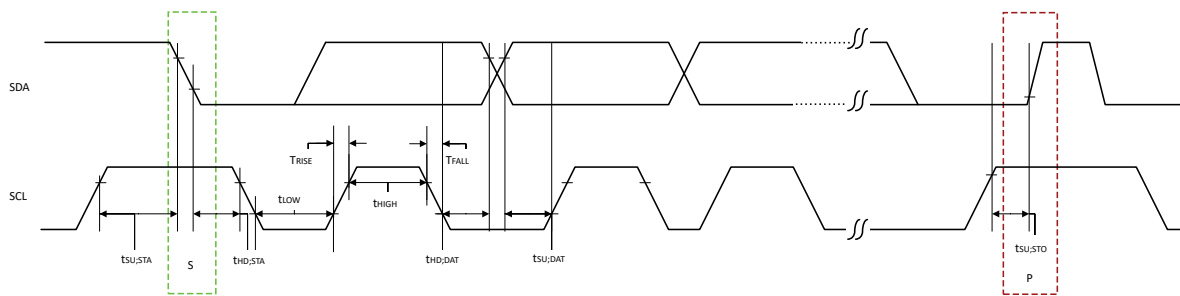
| Parameter | Definition | Conditions | Min | Typ | Max | Units |
|-----------|--|------------|-----|-----|-----|-------|
| tFILT | Pulse width of spikes which must be suppressed by the input filter | Fast mode | — | 50 | — | ns |

Notes:

1. These values are provided for MSIO Bank - LVTTTL 8 mA Low Drive at 25°C, typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website: www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas#ibis.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on VDDIx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website: www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas#ibis.
3. $R(\text{PULL-DOWN-MAX}) = (V_{\text{OLspec}}) / I_{\text{OLspec}}$.
4. $R(\text{PULL-UP-MAX}) = (V_{\text{DDI}max} - V_{\text{OHspec}}) / I_{\text{OHspec}}$.

Table 30-3. I2C Switching Characteristics—Worst-Case Military Conditions: $T_j = 125^\circ\text{C}$, $V_{\text{DD}} = 1.14\text{V}$

| Parameter | Definition | Conditions | Speed Grade -1 | | Units |
|---------------------|--------------------------|------------|----------------|-----|-------------|
| | | | Min | Max | |
| t _{LOW} | Low period of I2C_x_SCL | — | 1 | — | pclk cycles |
| t _{HIGH} | High period of I2C_x_SCL | — | 1 | — | pclk cycles |
| t _{HD;STA} | START hold time | — | 1 | — | pclk cycles |
| t _{SU;STA} | START setup time | — | 1 | — | pclk cycles |
| t _{HD;DAT} | DATA hold time | — | 1 | — | pclk cycles |
| t _{SU;DAT} | DATA setup time | — | 1 | — | pclk cycles |
| t _{SU;STO} | STOP setup time | — | 1 | — | pclk cycles |

Figure 30-1. I²C Timing Parameter Definition

30.3 Serial Peripheral Interface (SPI) Characteristics [\(Ask a Question\)](#)

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK.

Table 30-4. SPI Characteristics—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

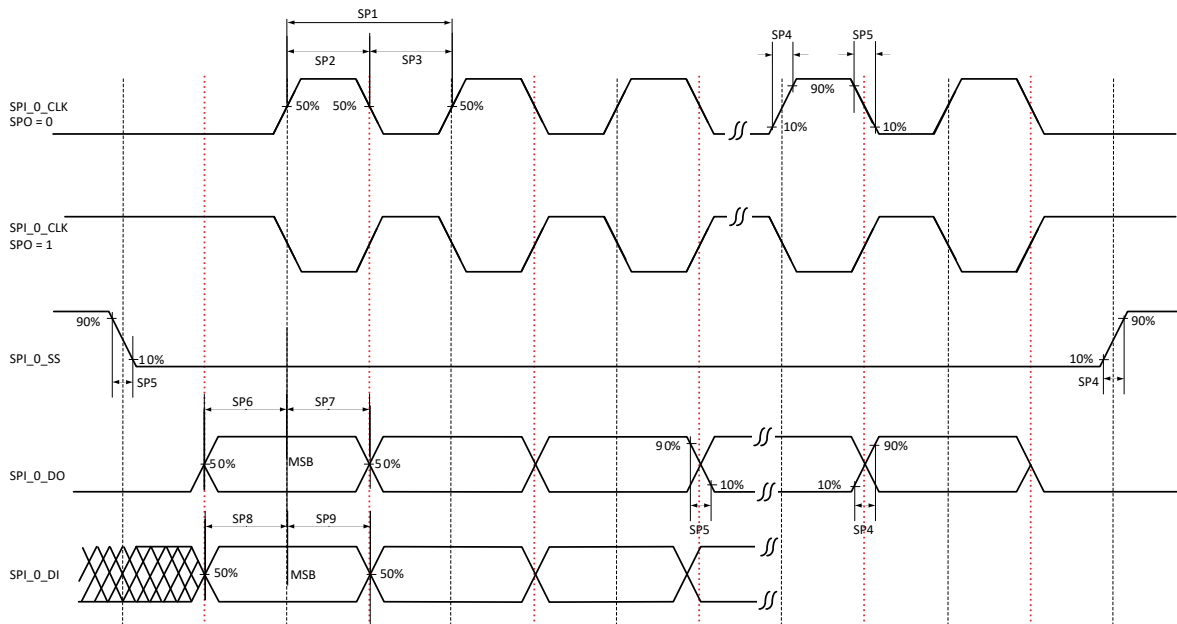
| Symbol | Description | Conditions | All Devices/Speed Grades | | | Unit |
|---|---|---|---|-------|-----|---------------|
| | | | Min | Typ | Max | |
| SPIFMAX | Maximum operating frequency of SPI interface | — | — | — | 20 | MHz |
| sp1 | SPI_[0 1]_CLK minimum period | | | | | |
| | SPI_[0 1]_CLK = PCLK/2 | — | 12 | — | — | ns |
| | SPI_[0 1]_CLK = PCLK/4 | — | 24.1 | — | — | ns |
| | SPI_[0 1]_CLK = PCLK/8 | — | 48.2 | — | — | ns |
| | SPI_[0 1]_CLK = PCLK/16 | — | 0.1 | — | — | μs |
| | SPI_[0 1]_CLK = PCLK/32 | — | 0.19 | — | — | μs |
| | SPI_[0 1]_CLK = PCLK/64 | — | 0.39 | — | — | μs |
| | SPI_[0 1]_CLK = PCLK/128 | — | 0.77 | — | — | μs |
| sp2 | SPI_[0 1]_CLK minimum pulse width high | | | | | |
| | SPI_[0 1]_CLK = PCLK/2 | — | 6 | — | — | ns |
| | SPI_[0 1]_CLK = PCLK/4 | — | 12.05 | — | — | ns |
| | SPI_[0 1]_CLK = PCLK/8 | — | 24.1 | — | — | ns |
| | SPI_[0 1]_CLK = PCLK/16 | — | 0.05 | — | — | μs |
| | SPI_[0 1]_CLK = PCLK/32 | — | 0.095 | — | — | μs |
| | SPI_[0 1]_CLK = PCLK/64 | — | 0.195 | — | — | μs |
| | SPI_[0 1]_CLK = PCLK/128 | — | 0.385 | — | — | μs |
| sp3 | SPI_[0 1]_CLK minimum pulse width low | | | | | |
| | SPI_[0 1]_CLK = PCLK/2 | — | 6 | — | — | ns |
| | SPI_[0 1]_CLK = PCLK/4 | — | 12.05 | — | — | ns |
| | SPI_[0 1]_CLK = PCLK/8 | — | 24.1 | — | — | ns |
| | SPI_[0 1]_CLK = PCLK/16 | — | 0.05 | — | — | μs |
| | SPI_[0 1]_CLK = PCLK/32 | — | 0.095 | — | — | μs |
| | SPI_[0 1]_CLK = PCLK/64 | — | 0.195 | — | — | μs |
| | SPI_[0 1]_CLK = PCLK/128 | — | 0.385 | — | — | μs |
| sp4 ¹ | SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%–90%) | IO Configuration: LVCMOS 2.5V - 8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C | — | 2.77 | — | ns |
| sp5 ¹ | SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%–90%) | IO Configuration: LVCMOS 2.5V - 8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C | — | 2.906 | — | ns |
| SPI Master Configuration (Applicable to 010, 025, and 050 Devices) | | | | | | |
| sp6m ² | SPI_[0 1]_DO setup time | — | $(\text{SPI_x_CLK_period}/2) - 8.0$ | — | — | ns |
| sp7m ² | SPI_[0 1]_DO hold time | — | $(\text{SPI_x_CLK_period}/2) - 2.5$ | — | — | ns |
| sp8m ² | SPI_[0 1]_DI setup time | — | 12 | — | — | ns |
| sp9m ² | SPI_[0 1]_DI hold time | — | 2.5 | — | — | ns |
| SPI Slave Configuration (Applicable to 010, 025, and 050 Devices) | | | | | | |
| sp6s ² | SPI_[0 1]_DO setup time | — | $(\text{SPI_x_CLK_period}/2) - 17.0$ | — | — | ns |
| sp7s ² | SPI_[0 1]_DO hold time | — | $(\text{SPI_x_CLK_period}/2) + 3.0$ | — | — | ns |
| sp8s ² | SPI_[0 1]_DI setup time | — | 2 | — | — | ns |
| sp9s ² | SPI_[0 1]_DI hold time | — | 7 | — | — | ns |

.....continued

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Unit |
|---|-------------------------|------------|-----------------------------|-----|-----|------|
| | | | Min | Typ | Max | |
| SPI Master Configuration (Applicable to 060, 090, and 150 Devices) | | | | | | |
| sp6m ² | SPI_[0 1]_DO setup time | — | (SPI_x_CLK_period/2) – 7.0 | — | — | ns |
| sp7m ² | SPI_[0 1]_DO hold time | — | (SPI_x_CLK_period/2) – 9.5 | — | — | ns |
| sp8m ² | SPI_[0 1]_DI setup time | — | 15 | — | — | ns |
| sp9m ² | SPI_[0 1]_DI hold time | — | -2.5 | — | — | ns |
| SPI Slave Configuration (Applicable to 060, 090, and 150 Devices) | | | | | | |
| sp6s ² | SPI_[0 1]_DO setup time | — | (SPI_x_CLK_period/2) – 16.0 | — | — | ns |
| sp7s ² | SPI_[0 1]_DO hold time | — | (SPI_x_CLK_period/2) – 3.5 | — | — | ns |
| sp8s ² | SPI_[0 1]_DI setup time | — | 3 | — | — | ns |
| sp9s ² | SPI_[0 1]_DI hold time | — | 2.5 | — | — | ns |

Notes:

- For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website: www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas#ibis.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the [UG0331: SmartFusion 2 Microcontroller Subsystem User Guide](#).

Figure 30-2. SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

31. IGLOO 2 Specifications [\(Ask a Question\)](#)

31.1 HPMS Clock Frequency [\(Ask a Question\)](#)

Table 31-1. Maximum Frequency for HPMS Main Clock—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Symbol | Description | Speed Grade -1 | Units |
|----------|--|----------------|-------|
| HPMS_CLK | Maximum Frequency for the HPMS Main Clock (FCLK) | 133 | MHz |

31.2 Serial Peripheral Interface (SPI) Characteristics [\(Ask a Question\)](#)

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, refer to [Figure 31-1](#).

Table 31-2. SPI Characteristics—Worst-Case Military Conditions: $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{V}$

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Unit |
|------------------|---|--|--------------------------|------|-----|---------------|
| | | | Min | Typ | Max | |
| sp1 | SPI_0_CLK minimum period | | | | | |
| | SPI_0_CLK = PCLK/2 | — | 12 | — | — | ns |
| | SPI_0_CLK = PCLK/4 | — | 24.1 | — | — | ns |
| | SPI_0_CLK = PCLK/8 | — | 48.2 | — | — | ns |
| | SPI_0_CLK = PCLK/16 | — | 0.1 | — | — | μs |
| | SPI_0_CLK = PCLK/32 | — | 0.19 | — | — | μs |
| | SPI_0_CLK = PCLK/64 | — | 0.39 | — | — | μs |
| | SPI_0_CLK = PCLK/128 | — | 0.77 | — | — | μs |
| sp2 | SPI_0_CLK minimum pulse width high | | | | | |
| | SPI_0_CLK = PCLK/2 | — | 6 | — | — | ns |
| | SPI_0_CLK = PCLK/4 | — | 12.05 | — | — | ns |
| | SPI_0_CLK = PCLK/8 | — | 24.1 | — | — | ns |
| | SPI_0_CLK = PCLK/16 | — | 0.05 | — | — | μs |
| | SPI_0_CLK = PCLK/32 | — | 0.095 | — | — | μs |
| | SPI_0_CLK = PCLK/64 | — | 0.195 | — | — | μs |
| | SPI_0_CLK = PCLK/128 | — | 0.385 | — | — | μs |
| sp3 | SPI_0_CLK minimum pulse width low | | | | | |
| | SPI_0_CLK = PCLK/2 | — | 6 | — | — | ns |
| | SPI_0_CLK = PCLK/4 | — | 12.05 | — | — | ns |
| | SPI_0_CLK = PCLK/8 | — | 24.1 | — | — | ns |
| | SPI_0_CLK = PCLK/16 | — | 0.05 | — | — | μs |
| | SPI_0_CLK = PCLK/32 | — | 0.095 | — | — | μs |
| | SPI_0_CLK = PCLK/64 | — | 0.195 | — | — | μs |
| | SPI_0_CLK = PCLK/128 | — | 0.385 | — | — | μs |
| sp4 ¹ | SPI_0_CLK, SPI_0_DO, SPI_0_SS rise time (10%-90%) | I/O Configuration: LVCMOS 2.5V- 8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C | — | 2.77 | — | ns |

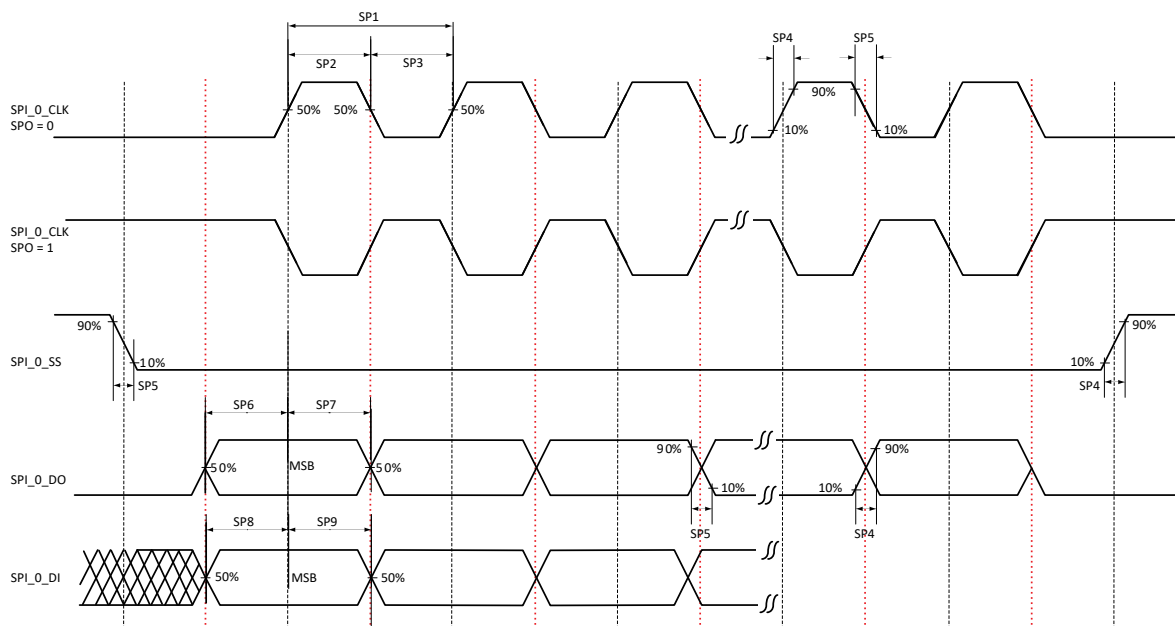
.....continued

| Symbol | Description | Conditions | All Devices/Speed Grades | | | Unit |
|---------------------------------|---|--|-----------------------------|-------|-----|------|
| | | | Min | Typ | Max | |
| sp5 ¹ | SPI_0_CLK, SPI_0_DO, SPI_0_SS fall time (10%-90%) | I/O Configuration: LVCMOS 2.5V- 8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C | — | 2.906 | — | ns |
| SPI Master Configuration | | | | | | |
| sp6m ² | SPI_0_DO setup time | — | (SPI_x_CLK_period/2) - 3.0 | — | — | ns |
| sp7m ² | SPI_0_DO hold time | — | (SPI_x_CLK_period/2) - 2.5 | — | — | ns |
| sp8m ² | SPI_0_DI setup time | — | 8 | — | — | ns |
| sp9m ² | SPI_0_DI hold time | — | 2.5 | — | — | ns |
| SPI Slave Configuration | | | | | | |
| sp6s ² | SPI_0_DO setup time | | (SPI_x_CLK_period/2) - 12.0 | — | — | ns |
| sp7s ² | SPI_0_DO hold time | | (SPI_x_CLK_period/2) + 3.0 | — | — | ns |
| sp8s ² | SPI_0_DI setup time | | 2 | — | — | ns |
| sp9s ² | SPI_0_DI hold time | | 3 | — | — | ns |

Notes:

1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microchip website: www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas#ibis.
2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the [UG0331: SmartFusion 2 Microcontroller Subsystem User Guide](#).

Figure 31-1. SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)



32. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Table 32-1. Revision History

| Revision | Date | Description |
|----------|---------------|--|
| C | December 2024 | In the revision C of this document, updated Table 1-2 by inserting a note to assert that the product is designed and validated for operation within the junction temperature (T _j) range. |
| B | July 2024 | The following information is updated in revision B of this document. <ul style="list-style-type: none"> Added Ordering Information section. Updated Table 14-1 by adding a note to the table on JTAG IOs. Updated Table 15-1, Table 15-2, Table 17-1, and Table 17-2 by adding note that the power-up to Functional time in the tables do not consider SUSPEND_MODE. |
| A | August 2023 | The following information is updated in revision A of this document. <ul style="list-style-type: none"> Migrated this document into Microchip template format and updated the hyperlinks with the recent references. Updated document number from 51700120 to DS60001820A. The Operating Temperature range is updated for Max T_j from 125 °C to 100 °C in Table 1-3. Added Note 3 in the Table 5-3 table. Updated the value of “Access Time with Feed-Through Write Timing” in Table 8-1, Table 8-2, Table 8-3, Table 8-4, and Table 8-5. For more information about this change, see CN SmartFusion 2 IGL00 2 FPGA LSRAM Write-Feed through Timing. Programming Time of JTAG, 2 Step IAP, and MSS/Cortex-M3 ISP table merged with Programming time for Auto Programming, Auto Update, and Programming Recovery table for both Typical Conditions and Worst-case Conditions. See Table 9-1 and Table 9-2. Delay information for SC_SPI_SDO and corresponding Note 2 has been added in Table 18-1. Added a Note information for the XAUI protocol. See Table 27-1. |
| 7.0 | — | The following information was updated in revision 7.0 of this document. <ul style="list-style-type: none"> Information about FPGA Programming Temperature, Operating Temperature, and Retention (Biased/Unbiased) Operating Limits was updated. See Table 1-3. Information about Embedded Flash Programming Temperature and Maximum Operating Temperature Operating Limits was updated. See Table 1-4. Information about Device Storage Temperature and Retention was updated. See Table 1-5. |
| 6.0 | — | The following information was updated in revision 6.0 of this document. <ul style="list-style-type: none"> Information about VOH and VOL were updated. See Table 28, page 23. Information about DEVRSTN ramp time was updated. See Table 149, page 98. Information about System Controller SPI characteristics for sp6 and sp7 were updated. See Table 152, page 100. <p>The following information was added in revision 6.0 of this document.</p> <ul style="list-style-type: none"> A note about VID was added to LVDS differential voltage specification. See Table 84, page 51. |

.....continued

| Revision | Date | Description |
|----------|------|--|
| 5.0 | — | <p>The following information was updated in revision 5.0 of this document.</p> <ul style="list-style-type: none"> • VOH (V) in LVCMOS 2.5 V transmitter drive strength specifications. See Table 31, page 24. • SPI timing. See Table 176, page 111 and Table 178, page 114. • I/O Weak Pull-Up/Down resistances. See Table 20, page 20. • Speed grade -1 was updated for Register Delays, Combinatorial Cell Propagation Delays, Input Data Register Propagation Delays, Output/Enable Data Register Propagation Delays, Input DDR Propagation Delays, and Output DDR Propagation Delays. See Table 109, page 61, Table 110, page 63, Table 111, page 65, Table 112, page 67, Table 113, page 68, and Table 114, page 70. • High temperature data retention. See Table 7, page 7 and Figure 1, page 7. • Absolute maximum temperature (TJ) was changed to 145 °C. See Table 2, page 4. • VTX-DIFF-PP, VTX-CM-AC-P, VTX-RISE-FALL, LTX-SKEW in transmitter parameters table and VRX-IN-PP-CC, RLRX-DIFF, RLRX-CM in Receiver Parameters table. See Table 164, page 106 and Table 165, page 107. • CID limit was corrected. See Table 165, page 107. • Input capacitance and leakage current. See Table 19, page 19. • DEVRESET_N minimum and maximum values. See Table 149, page 98. <p>The following information was added in revision 5.0 of this document.</p> <ul style="list-style-type: none"> • MMUART. See Table 170, page 108. • FMAXPDEVIRST_N was added to DEVIRST_N Characteristics table. See Table 149, page 98. • SerDes Protocol Compliance. See Table 169, page 108. • F*F timing data corresponding to FCLK = 3 MHz for all dies. See Table 158, page 103. • SPI Clock Fmax. See Table 152, page 100. • 060 device was added to VPP (Recommended Operating Conditions). See Table 3, page 5. • SerDes TX-AMP range was added in transmitter parameters table. See Table 164, page 106. • Digest cycle per programming cycle was added to FPGA operating limits table. See Table 4, page 6. • A note was added about CID limit. See Table 165, page 107. • Output duty cycle for 060 device. See Table 144, page 94. • 060 device was added to JTAG table. See Table 146, page 95. • Cryptographic Block Characteristics. See Table 163, page 106. • Non-deterministic Random Bit Generator (NRBG) Characteristics. See Table 162, page 105. • SRAM PUF. See Table 161, page 104. • PLL Acquisition time. See Table 144, page 94. • IIL and IIH was added to input capacitance table. See Table 19, page 19. • Input TRAMPIN specification was added to input capacitance table. See Table 19, page 19. • Power-Up to Functional Time, page 96 and DEVIRST_N to Functional Time, page 98. • Programming Time, page 88 was added. |
| 4.0 | — | Updated Table 10, page 11 , Table 11, page 11 , and Table 145, page 95 . |

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| Revision | Date | Description |
|----------|------|--|
| 3.0 | — | Updated Table 1, page 3 . |
| 2.0 | — | The following is a summary of the changes in revision 2.0 of this document. <ul style="list-style-type: none"> Updated Table 1, page 3, Table 3, page 5, Table 4, page 6, Table 8, page 9, Table 66, page 42, Table 70, page 44, Table 144, page 94, Table 146, page 95, and Table 177, page 114. Added Embedded NVM (eNVM) Characteristics, page 91, DEVRST_N Characteristics, page 98, DDR Memory Interface Characteristics, page 103, SFP Transceiver Characteristics, page 104, CAN Controller Characteristics, page 109, and USB Characteristics, page 109. |
| 1.0 | — | Revision 1.0 was the first publication of this document. |

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